



Data Acquisition Circuits

Data Conversion and DSP Analog Interface

Data Book

1998

Mixed-Signal Products

General Information	1
General Purpose ADCs	2
General Purpose DACs	3
DSP AICs and CODECs	4
Special Functions	5
Video Interface Palettes	6
Digital Imaging Sensor Products	7
Mechanical Information	8

Data Acquisition Circuits Data Book

Data Conversion and DSP Analog Interface

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INTRODUCTION

Texas Instruments offers an extensive line of industry-standard data acquisition integrated circuits. They are designed to provide highly reliable circuits for peripheral support applications of microprocessor-based systems, DSP (digital signal processing) related analog interfaces, video and high-speed converters, digitizing requirements that demand ADC and DAC conversion, and general-purpose functions.

This data book provides information on the following product groups:

- Serial I/O Analog-to-Digital Converters
- General Purpose Parallel Output Analog-to-Digital converters
- Stereo Audio Analog-to-Digital Converters
- Multiplexed BCD-Output, Dual Slope Analog-to-Digital Converters
- Video and High-Speed Analog-to-Digital Converters
- Video and High-Speed Digital-to-Analog Converters
- General Purpose Serial-Input Digital-to-Analog Converters
- General Purpose Parallel-Input Digital-to-Analog Converters
- Stereo Audio Digital-to-Analog Converters
- Analog Interface Circuits (AICs)
- Special Function Circuits (PLL, Clamping, Filter, Amplifier)
- Video Interface Palettes
- CCD Interface Analog-to-Digital Converters

These products cover applications such as audio, graphics, communications, modems and cellular phones, video capture and image processing, industrial control and disk-drive servo-loop control, automotive, electronic instrumentation, digital audio, and any DSP or microprocessor-based system.

Texas Instruments, the world's leading supplier of DSP solutions, is committed to meeting the needs of industry by accelerating the development of new differentiated analog products, while continuing to provide world-class quality, and customer support.

An electronic version of this data book, including all Mixed-Signal & Analog products, is available from TI. The InfoNavigator CD-ROM, which is both a designer's guide and data book may be ordered via the Internet at: <http://www.ti.com/sc/docs/cdrom/ordercd.htm> You may also order by calling Texas Instruments toll-free at: 1-800-477-8924 ext. 5047

To provide full technical support, Texas Instruments has a large fully-staffed product information center available to help you. Simply call our U.S. headquarters at (972) 644-5580. Texas Instruments Sales Offices, listed on the last page of this book, also provide sales and technical support.

General Information	1
General Purpose ADCs	2
General Purpose DACs	3
DSP AICs and CODECs	4
Special Functions	5
Video Interface Palettes	6
Digital Imaging Sensor Products	7
Mechanical Information	8

Contents

	Page
Alphanumeric Index :	1-3
Analog-to-Digital Converter Selection Guide :	1-4
Digital-to-Analog Converter Selection Guide :	1-8
Analog Interface Circuit Selection Guide :	1-11
Special Function Selection Guide :	1-12
Video Interface Palette Selection Guide :	1-13
Digital Imaging Sensor Products Selection Guide :	1-14
Cross Reference :	1-15
Glossary :	1-20

ALPHANUMERIC INDEX

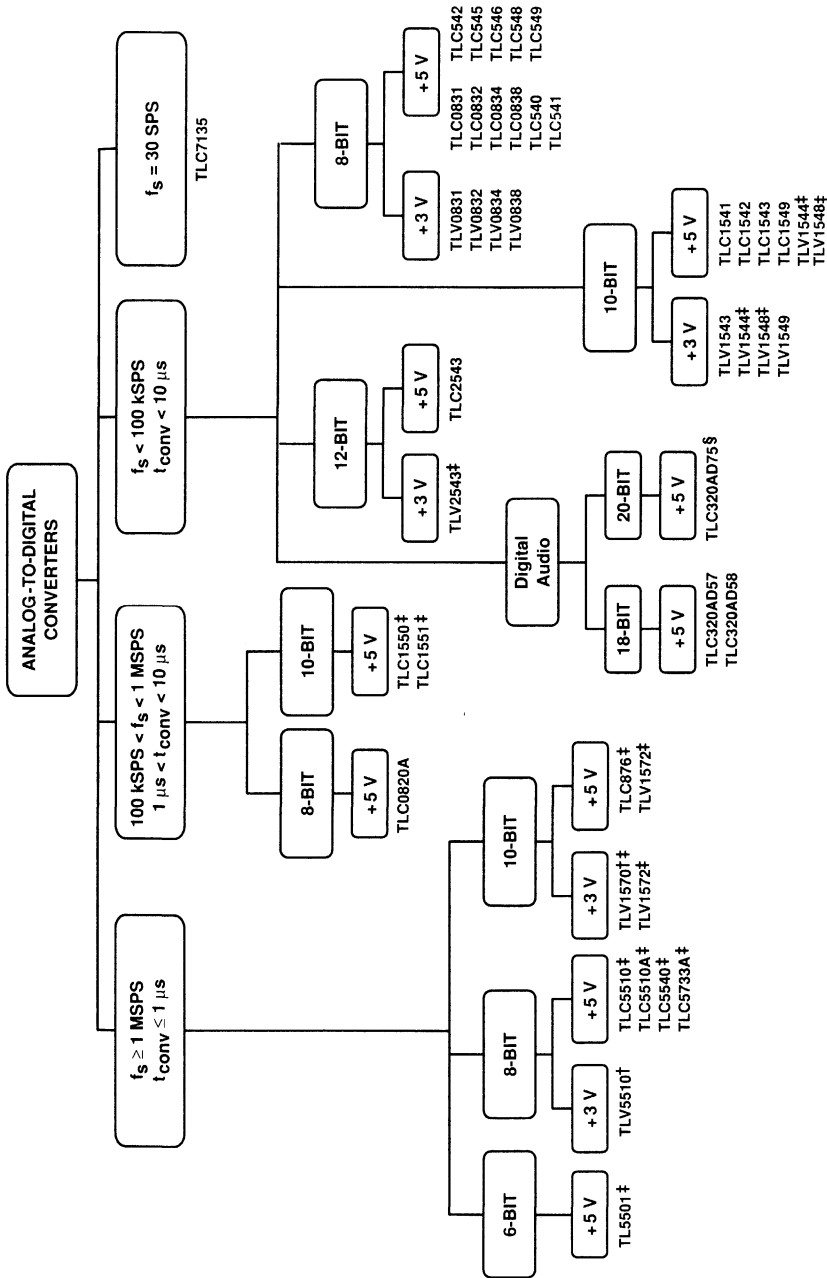
AD7524M	3-3	TLC7226	3-137
ICL7135	2-3	TLC7524	3-153
MF4A-50	5-7	TLC7528	3-163
MF4A-100	5-7	TLC7628	3-177
TL5501	2-13	TLC8044	7-3
TL5632	3-11	TLC8144	7-33
TL7726	5-3	TLC8188	7-61
TL32088	5-61	TLC32040	4-3
TLC04	5-7	TLC32041	4-3
TLC14	5-7	TLC32044	4-35
TLC540	2-19	TLC32045	4-35
TLC541	2-19	TLC32046	4-73
TLC542	2-29	TLC32047	4-129
TLC545	2-39	TLC320AC01	4-187
TLC546	2-39	TLC320AC02	4-273
TLC548	2-51	TLC320AD50	4-361
TLC549	2-51	TLC320AD52	4-361
TLC0820A	2-61	TLC320AD55	4-417
TLC0831	2-71	TLC320AD56	4-455
TLC0832	2-71	TLC320AD57	2-247
TLC0834	2-83	TLC320AD58	2-267
TLC0838	2-83	TLC320AD75	4-495
TLC876	2-97	TLC320AD80	4-535
TLC876M	2-119	TLV0831	2-291
TLC1541	2-123	TLV0832	2-291
TLC1542	2-133	TLV0834	2-303
TLC1543	2-133	TLV0838	2-303
TLC1549	2-153	TLV1543	2-317
TLC1550	2-167	TLV1544	2-335
TLC1551	2-167	TLV1548	2-335
TLC2543	2-175	TLV1548M	2-367
TLC2932	5-19	TLV1549	2-373
TLC2933	5-41	TLV1570	2-387
TLC5510	2-197	TLV1572	2-397
TLC5540	2-209	TLV2543	2-409
TLC5602	3-19	TLV5510	2-429
TLC5604	3-27	TLV5613	3-187
TLC5614	3-29	TLV5619	3-195
TLC5615	3-31	TLV5620	3-203
TLC5616	3-47	TLV5621	3-215
TLC5617	3-55	TLV5628	3-231
TLC5618	3-75	TMS57014A	3-243
TLC5618M	3-95	TVP3026	6-3
TLC5620	3-97	TVP3030	6-7
TLC5628	3-107	TVP3033	6-11
TLC5733	2-225	TVP3409	6-13
TLC7135	2-3	TVP3703	6-15
TLC7225	3-117		

Devices in **bold type** are in the PRODUCT PREVIEW stage of development.



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SELECTION GUIDE ANALOG-TO-DIGITAL CONVERTERS



† This part is in the Product Preview stage of development.

‡ This part is TMS320 compatible.

§ For this part see Section 4, *Analog Interface Circuits*, for more information.

Serial I/O Analog-to-Digital Converters (ADC)

Device	Resolution (bits)	V _{CC} (V)	Power (mW) max	Conversion Time (μs)	Sampling Rate (kSPS) max	Number of Analog Inputs	Internal System Clock	Standby	Linearity Error (LSB)	Page No.
TLC2543	12	5	12	10	66	11	X	X	±1.0	2-175
TLV2543	12	3.3	8	10	66	11	X	X	±1.0	2-409
TLC1541	10	5	12	21	32	11			±1.0	2-123
TLC1542	10	5	12	21	38	11	X		±0.5	2-133
TLC1543	10	5	12	21	38	11	X		±1.0	2-133
TLC1549	10	5	12	21	38	1	X		±1.0	2-153
TLV1543	10	3.3	8	21	38	11	X		±1.0	2-317
TLV1544	10	2.7 - 5.5	4	10	85	4	X	X	±1.0	2-335
TLV1548	10	2.7 - 5.5	4	10	85	8	X	X	±1.0	2-335
TLV1548M	10	2.7 - 5.5	4	10	85	8	X	X	±1.0	2-367
TLV1549	10	3.3	8	21	38	1	X		±1.0	2-373
TLC0831	8	5	12.5	13.3	31	1			±1.0	2-71
TLC0832	8	5	26	13.3	22	2			±1.0	2-71
TLC0834	8	5	12.5	13.3	20	4			±1.0	2-83
TLC0838	8	5	12.5	13.3	20	8			±1.0	2-83
TLC540	8	5	12	9	75	11			±0.5	2-19
TLC541	8	5	12	17	40	11			±0.5	2-19
TLC542	8	5	10	20	25	11	X		±0.5	2-29
TLC545	8	5	12	9	76	19			±0.5	2-39
TLC546	8	5	12	17	40	19			±0.5	2-39
TLC548	8	5	12	17	45.5	1	X		±0.5	2-51
TLC549	8	5	12	17	40	1	X		±0.5	2-51



SELECTION GUIDE ANALOG-TO-DIGITAL CONVERTERS

Serial I/O Analog-to-Digital Converters (ADC) (continued)

Device	Resolution (bits)	V _{CC} (V)	Power (mW) max	Conversion Time (μs)	Sampling Rate (kSPS) max	Number of Analog Inputs	Internal System Clock	Standby	Linearity Error (LSB)	Page No.
TLV0831	8	3.3	4.1	13.3	49	1			±1.0	2-291
TLV0832	8	3.3	15.5	13.3	44.7	2			±1.0	2-291
TLV0834	8	3.3	4.1	13.3	41	4			±1.0	2-303
TLV0838	8	3.3	4.1	13.3	37.9	8			±1.0	2-303

General Purpose Parallel Output Analog-to-Digital Converters (ADC)

Device	Resolution (bits)	V _{CC} (V)	Power (mW) max	Conversion Time (μs)	Sampling Rate (kSPS) max	Number of Analog Inputs	Linearity Error (LSB)	Standby	Internal System Clock	Page No.
TLC1550	10	5	40	6	164	1	±0.5		X	2-167
TLC1551	10	5	40	6	164	1	±1.0		X	2-167
TLC0820A	8	5	7.5	2.5	392	1	±1.0		X	2-61

Stereo Audio Analog-to-Digital Converters (ADC)

Device	Resolution (bits)	V _{CC} (V)	Power (mW) max	Conversion Time (μs)	Sampling Rate (kSPS) max	Number of Analog Inputs	Linearity Error (LSB)	Standby	Internal System Clock	Page No.
TLC320AD57	16/18	5	220		48	2			Serial	2-247
TLC320AD58	16/18	5	220		48	2			Serial	2-267

Multiplexed BCD-Output, Dual Slope Analog-to-Digital Converters (ADC)

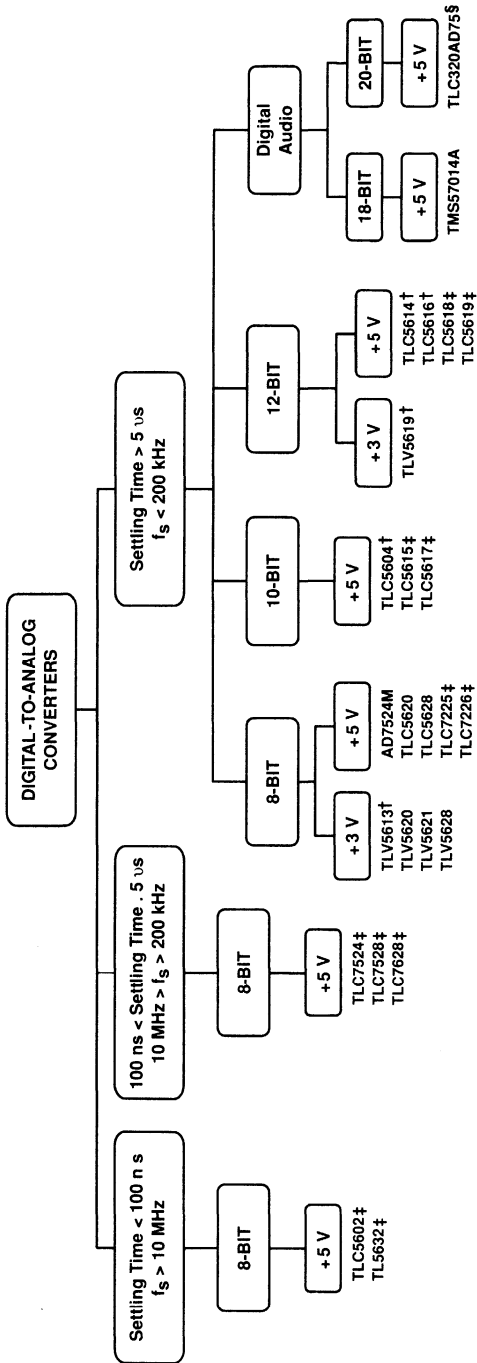
Device	Resolution (bits)	VCC (V)	Power (mW) max	Conversion Time (ms)	Sampling Rate (SPS) max	Number of Analog Inputs	Output Type	Linearity Error (LSB)	Page No.
TLC7135	4.5	±5	30	33.3	30	1	BCD	0.5	2-3

Video and High-Speed Analog-to-Digital Converters (ADC)

Device	Resolution (bits)	Conversion Time (ns)	VCC (V)	Power (mW) max	Sampling Rate (MSPS) max	Number of Analog Inputs	Output Type	Differential Error (DNL) (LSB)	SNR (dB)	Page No.
TL5501	10	50	5	131	20	1	Parallel	±0.5		2-13
TLC876	10	50	5	150	20	1	Parallel	±0.5	55	2-97
TLC876M†	10	50	5	150	20	1	Parallel	±0.5	55	2-119
TLV1570†	10		2.7 ~ 5.5	9		8	Serial	±0.5		2-387
TLV1572	10	800	2.7 ~ 5.5	8	1.25	1	Serial	±0.5		2-397
TLC5510	8	50	5	135	20	1	Parallel	±0.5	46	2-197
TLC5510A	8	50	5	150	20	1	Parallel	±0.5	46	2-197
TLC5733A	8	50	5	300	20	1	Parallel	±0.5	–	2-225
TLC5540	8	25	5	150	40	1	Parallel	±0.75	45	2-209
TLV5510†	8		3.3	50	20	1	Serial	±0.5		2-429

† This part is in the Product Preview stage of development.

SELECTION GUIDE DIGITAL-TO-ANALOG CONVERTERS



† This part is in the Product Preview stage of development.

‡ This part is TMS320 compatible.

§ For this part see Section 4, Analog Interface Circuits, for more information.

Video and High-Speed Digital-to-Analog Converters (DAC)

Device	Resolution (bits)	V _{CC} (V)	Power (mW) max	Bus Interface	Output (I or V)	Number of DACs	Ref.	Settling Time (ns)	Linearity Error (LSB)	Conversion Rate (MHz) min	Page No.
TL5632	8	5	450	Parallel	V	3	Int	10	±0.5	60	3-11
TLC5602	8	5	125	Parallel	V	1	Ext	30	±0.2	20	3-19

General Purpose Serial-Input Digital-to-Analog Converters (DAC)

Device	Resolution (bits)	V _{CC} (V)	Power (mW) max	Bus Interface	Output (I or V)	Number of DACs	Ref.	Settling Time (µs)	Linearity Error (LSB)	Conversion Rate (kHz) min	Multiplying	Page No.
TLC5618	12	5	3.5	Serial	V	2	Ext	2.5	±0.5	121	X	3-75
TLC5618M†	12	5	3.5	Serial	V	2	Ext	2.5	±0.5	121	X	3-95
TLC5614†	12	3 to 5	7.25	Serial	V	4	Ext	—	—	—	—	3-29
TLC5615	10	5	1.75	Serial	V	1	Ext	12.5	±0.5	121	X	3-31
TLC5616†	10	5	3	Serial	V	1	Ext	2.5 – 12.5	±0.5	—	—	3-47
TLC5617	10	5	3.5	Serial	V	2	Ext	2.5	±0.5	121	X	3-55
TLC5604†	10	3 to 5	7.25	Serial	V	4	Ext	—	—	—	—	3-27
TLC5620	8	5	10	Serial	V	4	Ext	10	±1.0	10	—	3-97
TLC5628	8	5	20	Serial	V	8	Ext	10	±1.0	10	—	3-107
TLV5620	8	2.7 to 5.5	6.6	Serial	V	4	Ext	10	±1.0	10	—	3-203
TLV5621	8	2.7 to 5.5	4.5	Serial	V	4	Ext	10	±1.0	10	—	3-215
TLV5628	8	2.7 to 5.5	13.2	Serial	V	8	Ext	10	±1.0	10	—	3-231

† This part is in the Product Preview stage of development.



SELECTION GUIDE DIGITAL-TO-ANALOG CONVERTERS

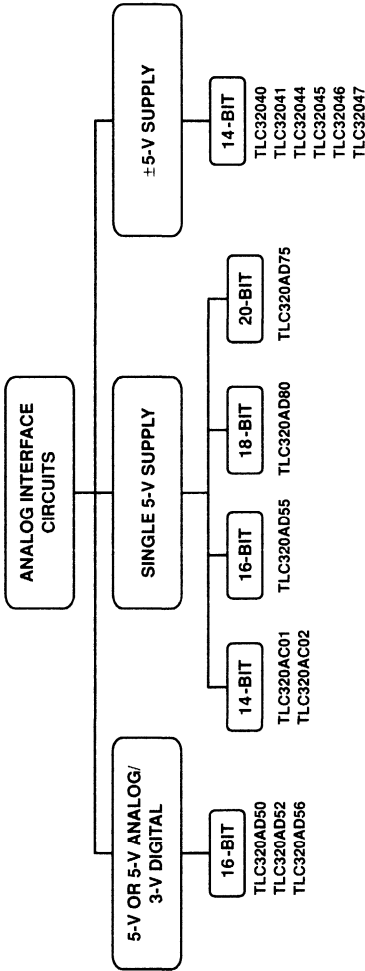
General Purpose Parallel-Input Digital-to-Analog Converters (DAC)

Device	Resolution (bits)	V _{CC} (V)	Power (mW) max	Bus Interface	Output (I or V)	Number of DACs	Ref.	Settling Time (μs)	Linearity Error (LSB)	Multiplying	Page No.
TLV5619†	12	3 to 5	7.25	Parallel	V	1	Ext.	0.8	±0.5		3-195
TLC7225	8	5 to 15	60	Parallel	V	4	Ext.	5	±1.0		3-117
TLC7226	8	15	240	Parallel	V	4	Ext.	5	±1.0		3-137
TLC7524	8	5 to 15	5	Parallel	I	1	Ext. M	0.1	±0.5	X	3-153
TLC7528	8	5 to 15	10	Parallel	I	2	Ext. M	0.1	±0.5	X	3-163
TLC7628	8	11 to 15	20	Parallel	I	2	Ext. M	0.1	±0.5	X	3-177
AD7524M	8	5 to 15	5	Parallel	I	1	Ext. M	0.1	±0.5	X	3-3
TLV5613†	8	3 to 5	7.25	Parallel	V	1	Ext.	0.8	±0.5		3-187

† This part is in the Product Preview stage of development.

Stereo Audio Digital-to-Analog Converters (DAC)

Device	Resolution (bits)	V _{CC} (V)	Power (mW) max	Bus Interface	Output	Number of DACs	Conversion Rate (kHz) max	Page No.
TMS57014A	16/18	5	350	Serial	PWM	2	48	3-243

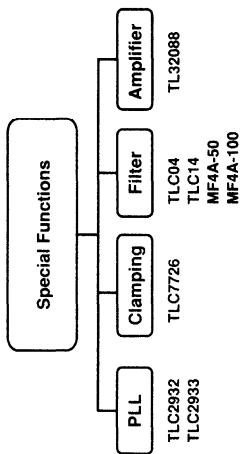


Analog Interface Circuits (AICs)

Device	Resolution (bits)	Sampling Rate (kHz)	Bandwidth (kHz)	Supply Voltage(s) (V)	P _d (mW) typ	SNR (dB) typ	Conversion Method	Description	Page No.
TLC320AD75	20	44.1	0.002 - 20	+5	400	104	Sigma-delta	Stereo ADA circuit (audio)	4-495
TLC320AD80	18	48		+5			Sigma-delta	Audio processor subsystem	4-535
TLC320AD56	16	22.05	8.8	+5 / +3	100	70	Sigma-delta	Sigma-delta AIC	4-455
TLC320AD50	16	22.05	8.8	+5 / +3	175	70	Sigma-delta	Sigma-delta AIC with mstr/slv function	4-361
TLC320AD52	16	22.05	8.8	+5 / +3	175	70	Sigma-delta	Sigma-delta AIC with mstr/slv function	4-361
TLC320AD55	16	10.3	4	+5	150	70	Sigma-delta	Sigma-delta AIC	4-417
TLC320AC02	14	25	10.8	+5	100	70	Successive approx.	Single-supply AIC	4-273
TLC320AC01	14	25	10.8	+5	100	72	Successive approx.	Single-supply AIC	4-187
TLC32047	14	25	0.3 - 11.4	±5	375	70	Successive approx.	Wide-band AIC with (sin x)/x correction	4-129
TLC32046	14	25	0.3 - 7.2	±5	375	85	Successive approx.	AIC with (sin x)/x correction	4-73
TLC32045	14	19.2	0.1 - 3.8	±5	375	80	Successive approx.	Voice-band AIC (relaxed TLC32044)	4-35
TLC32044	14	19.2	0.1 - 3.8	±5	375	80	Successive approx.	Voice-band AIC	4-35
TLC32041	14	19.2	0.3 - 3.6	±5	375	89	Successive approx.	AIC w/o internal reference	4-3
TLC32040	14	19.2	0.3 - 3.6	±5	375	89	Successive approx.	AIC	4-3

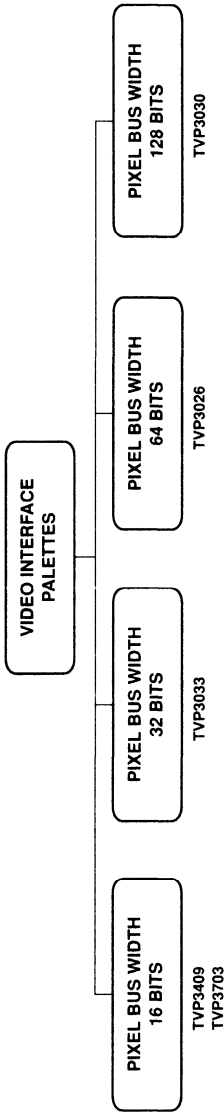


SELECTION GUIDE SPECIAL FUNCTIONS



Special Functions

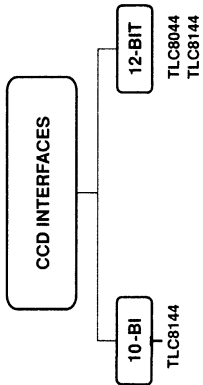
Device	Function	VCC (V)	Description	Page No.
TLC2932	PLL	3.3 to 5	50-MHz high-accuracy phase-locked loop	5-19
TLC2933	PLL	3.3 to 5	100-MHz high-accuracy phase-locked loop	5-41
TLC7726	Clamping	4.5 to 5.5	Provides active clamping at 0.2 V above V _{CC} and 0.2 V below ground	5-3
TLC04/MF4A-50	Filter	3.75	Butterworth fourth-order low-pass switched-capacitor filter	5-7
TLC14/MF4A-100	Filter	3.75	Butterworth fourth-order low-pass switched-capacitor filter	5-7
TL32088	Amplifier	5	Differential analog buffer amplifier	5-61



Video Interface Palettes (RAMDACs)

Device	Pixel Bus Width (bits)	Number of PLLs	Hardware Cursor	Gamma Correction	Packed Pixel	Max Resolution and Refresh Rate	Max Resolution with 24 bits/Pixel	Description	Page No.
TVP3026-135	64	Triple	Yes	Yes	Yes	1280 × 1024 @ 75 Hz	1280 × 1024	Packed-pixel modes VIP	6-3
TVP3026-175	64	Triple	Yes	Yes	Yes	1600 × 1200 @ 60 Hz	1280 × 1024	Packed-pixel modes VIP	6-3
TVP3026-220	64	Triple	Yes	Yes	Yes	1600 × 1200 @ 75 Hz	1280 × 1024	Packed-pixel modes VIP	6-3
TVP3026-250	64	Triple	Yes	Yes	Yes	1600 × 1200 @ 75 Hz	1280 × 1024	Packed-pixel modes VIP	6-3
TVP3030-175	128	Triple	Yes	Yes	Yes	1600 × 1200 @ 60 Hz	1600 × 1200	1600 × 1200, 24-bit true color VIP	6-7
TVP3030-220	128	Triple	Yes	Yes	Yes	1600 × 1200 @ 75 Hz	1600 × 1200	1600 × 1200, 24-bit true color VIP	6-7
TVP3030-250	128	Triple	Yes	Yes	Yes	1600 × 1200 @ 85 Hz	1600 × 1200	1600 × 1200, 24-bit true color VIP	6-7
TVP3033-175	32	Dual	Yes	Yes	Yes	1600 × 1200 @ 86 Hz	1600 × 1280	1600 × 1280, 24-bit true color VIP	6-11
TVP3033-220	32	Dual	Yes	Yes	Yes	1600 × 1200 @ 86 Hz	1600 × 1280	1600 × 1280, 24-bit true color VIP	6-11
TVP3033-250	32	Dual	Yes	Yes	Yes	1600 × 1200 @ 86 Hz	1600 × 1280	1600 × 1280, 24-bit true color VIP	6-11
TVP3409-135	16	Dual	No	No	No	1280 × 1024 @ 75 Hz	1024 × 768	Advanced VIP	6-13
TVP3409-170	16	Dual	No	No	No	1600 × 1200 @ 60 Hz	1024 × 768	Advanced VIP	6-13
TVP3703-135	16	Dual	No	No	No	1280 × 1024 @ 75 Hz	1024 × 768	Advanced VIP	6-15
TVP3703-170	16	Dual	No	No	No	1600 × 1200 @ 60 Hz	1024 × 768	Advanced VIP	6-15

SELECTION GUIDE DIGITAL IMAGING SENSOR PRODUCTS



Digital Imaging Sensor Products

Device	Resolution (bits)	VCC (V)	Power (mW) typ	Conversion Time (μs)	Sampling Rate (kSPS) max	Number of Analog Inputs	Powerdown Mode	Linearity Error (LSB)	Page No.
TLC8044	12	5	400	0.16	6000	6	X	±1.5	7-3
TLC8144	12	5	400	0.16	6000	3	X	±1.0	7-33
TLC8144	10	5	400	0.16	6000	3	X	±1.0	7-61

CROSS REFERENCE GUIDE

Part No	Suggested TI Replacement	Vendor	Replacement Type	Page No
AD573	TLC1549	Analog Devices	SIMILAR FUNCTIONALITY (see Note 4)	2-153
AD573	TLC1550	Analog Devices	SIMILAR FUNCTIONALITY (see Note 4)	2-167
AD775	TLC5540	Analog Devices	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-209
AD875	TLC5510	Analog Devices	SIMILAR FUNCTIONALITY (see Note 4)	2-197
AD876	TLC876	Analog Devices	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-97
AD1878	TLC320AD57	Analog Devices	SIMILAR FUNCTIONALITY (see Note 4)	2-247
AD1878	TLC320AD58	Analog Devices	SIMILAR FUNCTIONALITY (see Note 4)	2-267
AD1887	TLC320AD58	Analog Devices	SIMILAR FUNCTIONALITY (see Note 4)	2-267
AD7524	TLC7524	Analog Devices	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-153
AD7524	TLC7528	Analog Devices	SIMILAR FUNCTIONALITY (see Note 4)	3-163
AD7528	TLC7524	Analog Devices	SIMILAR FUNCTIONALITY (see Note 4)	3-153
AD7528	TLC7528	Analog Devices	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-163
AD7579	TLC1549	Analog Devices	SIMILAR FUNCTIONALITY (see Note 4)	2-153
AD7579	TLV1549	Analog Devices	SIMILAR FUNCTIONALITY (see Note 4)	2-373
AD7628	TLC7628	Analog Devices	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-177
AD7810	TLV1572	Analog Devices	SAME FUNCTIONALITY (see Note 3)	2-397
AD7812	TLV1570	Analog Devices	SAME FUNCTIONALITY (see Note 3)	2-387
AD7820	TLC0820A	Analog Devices	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-61
AD7890	TLC2543	Analog Devices	SIMILAR FUNCTIONALITY (see Note 4)	2-175
AD7890	TLV2543	Analog Devices	SIMILAR FUNCTIONALITY (see Note 4)	2-409
AD9048	TLC5510	Analog Devices	SIMILAR FUNCTIONALITY (see Note 4)	2-197
AD9048	TLC5540	Analog Devices	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-209
ADC0811	TLC540	National Semiconductor	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-19
ADC0811	TLC541	National Semiconductor	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-19
ADC0820	TLC0820A	Phillips	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-61
ADC0820	TLC0820A	Maxim	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-61
ADC0820	TLC0820A	National Semiconductor	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-61
ADC0830	TLC546	National Semiconductor	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-39
ADC0831	TLC0831	National Semiconductor	EXACT EQUIVALENT (see Note 1)	2-71
ADC0831	TLC549	National Semiconductor	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-51
ADC0832	TLC0832	National Semiconductor	EXACT EQUIVALENT (see Note 1)	2-71
ADC0834	TLC0834	National Semiconductor	EXACT EQUIVALENT (see Note 1)	2-83
ADC0838	TLC0838	National Semiconductor	EXACT EQUIVALENT (see Note 1)	2-83
ADC1001	TLC1541	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	2-123
ADC1001	TLC1550	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	2-167
ADC1005	TLC1541	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	2-123
ADC1021	TLC1541	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	2-123
ADC1031	TLC1549	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	2-153
ADC1038	TLC1542	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	2-133

- NOTES:
1. The device is an EXACT EQUIVALENT in functionality and parameters to the competitor's device
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CROSS REFERENCE GUIDE

Part No	Suggested TI Replacement	Vendor	Replacement Type	Page No
ADC1038	TLC1543	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	2-133
ADC1241	TLC2543	National Semiconductor	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-175
ADC1241	TLV2543	National Semiconductor	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-409
ADC12030	TLC2543	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	2-175
ADC12032	TLC2543	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	2-175
ADC12034	TLC2543	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	2-175
ADC12038	TLC2543	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	2-175
ADC12H038	TLC2543	National Semiconductor	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-175
ADC12H038	TLV2543	National Semiconductor	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-409
ADS574	TLC2543	Burr Brown	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-175
ADS7804	TLC2543	Burr Brown	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-175
ATT20C409	TVP3409-135	AT&T	SAME FUNCTIONALITY AND PINOUT (see Note 2)	6-13
ATT20C409	TVP3409-170	AT&T	SAME FUNCTIONALITY AND PINOUT (see Note 2)	6-13
CS4328	TMS57014A	Crystal	SIMILAR FUNCTIONALITY (see Note 4)	3-243
CS5336	TLC320AD57	Crystal	SIMILAR FUNCTIONALITY (see Note 4)	2-247
CS5389	TLC320AD58	Crystal	SIMILAR FUNCTIONALITY (see Note 4)	2-267
CS7820	TLC0820A	Crystal	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-61
CXA1096	TLC5510	Sony	SIMILAR FUNCTIONALITY (see Note 4)	2-197
CXA1175	TLC5510	Sony	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-197
CXA1176	TLC5510	Sony	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-197
CXA1179	TLC5540	Sony	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-209
CXD1175	TLC1550	Sony	SIMILAR FUNCTIONALITY (see Note 4)	2-167
CXD1175	TLC5510	Sony	EXACT EQUIVALENT (see Note 1)	2-197
CXD1179	TLC5540	Sony	SIMILAR FUNCTIONALITY (see Note 4)	2-209
DAC-8800	TLC5628	Analog Devices	SIMILAR FUNCTIONALITY (see Note 4)	3-107
DAC08	TLC7524	Motorola	SIMILAR FUNCTIONALITY (see Note 4)	3-153
DAC08	TLC7524	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	3-153
DAC0800	TLC7524	Phillips	SIMILAR FUNCTIONALITY (see Note 4)	3-153
DAC0800	TLC7524	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	3-153
DAC0801	TLC7524	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	3-153
DAC0802	TLC7524	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	3-153
DAC0808	TLC7524	SGS-Thomson	SIMILAR FUNCTIONALITY (see Note 4)	3-153
DAC0854	TLC5620	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	3-97
DAC0854	TLV5620	National Semiconductor	SIMILAR FUNCTIONALITY (see Note 4)	3-203
DAC7249	TLC5618	Analog Devices	SAME FUNCTIONALITY (see Note 3)	3-75
DAC7528	TLC7528	Burr Brown	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-163
DAC8229	TLC7628	Analog Devices	SAME FUNCTIONALITY (see Note 3)	3-177
LTC1091	TLC1543	Linear Technology	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-133
LTC1091	TLC1549	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-153

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CROSS REFERENCE GUIDE

Part No	Suggested TI Replacement	Vendor	Replacement Type	Page No
LTC1092	TLC1542	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-133
LTC1092	TLC1543	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-133
LTC1092	TLC1549	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-153
LTC1093	TLC1542	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-133
LTC1093	TLC1543	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-133
LTC1094	TLC1542	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-133
LTC1094	TLC1543	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-133
LTC1197	TLV1572	Linear Technology	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-397
LTC1199L	TLV1572	Linear Technology	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-397
LTC1283	TLC1549	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-153
LTC1290	TLC2543	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-175
LTC1291	TLC1543	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-133
LTC1283	TLV1543	Linear Technology	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-317
LTC1283	TLV1549	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-373
LTC1289	TLC2543	Linear Technology	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-175
LTC1289	TLV2543	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-409
LTC1292	TLC1543	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-133
LTC1293	TLC1543	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-133
LTC1293	TLV1543	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-317
LTC1294	TLC1543	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-133
LTC1294	TLC2543	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-175
LTC1296	TLC2543	Linear Technology	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-175
LTC1296	TLV2543	Linear Technology	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-409
LTC1400	TLC5618	Linear Technology	SAME FUNCTIONALITY (see Note 3)	3-75
LTC1446	TLC5618	Linear Technology	SAME FUNCTIONALITY (see Note 3)	3-75
MAX148	TLV1570	Maxim	SAME FUNCTIONALITY (see Note 3)	2-387
MAX149	TLV1570	Maxim	SAME FUNCTIONALITY (see Note 3)	2-387
MAX186	TLC2543	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	2-173
MAX188	TLC2543	Maxim	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-173
MAX192	TLC1543	Maxim	SAME FUNCTIONALITY (see Note 3)	2-133
MAX192	TLC1549	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	2-153
MAX192	TLV1543	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	2-317
MAX192	TLV1544	Maxim	SAME FUNCTIONALITY (see Note 3)	2-335
MAX192	TLV1548	Maxim	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-335
MAX192	TLV1549	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	2-373
MAX500	TLC5620	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	3-97
MAX500	TLV5620	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	3-203
MAX509	TLC5620	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	3-97
MAX509	TLC5628	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	3-107

- NOTES: 1. The device an EXACT EQUIVALENT in functionality and parametrics to the competitors device
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CROSS REFERENCE GUIDE

Part No	Suggested TI Replacement	Vendor	Replacement Type	Page No
MAX509	TLV5620	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	3-203
MAX510	TLC5620	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	3-97
MAX510	TLV5620	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	3-203
MAX528	TLC5628	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	3-107
MAX529	TLC5628	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	3-107
MAX1160	TLC876	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	2-97
MAX1204	TLV1570	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	2-387
MAX5351	TLC5616	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	3-47
MAX5352	TLC5616	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	3-47
MAX5628	TLC5620	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	3-97
MAX5628	TLC5628	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	3-107
MAX5628	TLV5620	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	3-203
MAX7524	TLC7524	Maxim	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-153
MAX7528	TLC7528	Maxim	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-163
MAX7628	TLC7628	Maxim	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-177
MAX7820	TLC0820A	Maxim	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-61
MB4056	TLC548	Fujitsu	SIMILAR FUNCTIONALITY (see Note 4)	2-51
MB4056	TLC549	Fujitsu	SIMILAR FUNCTIONALITY (see Note 4)	2-51
MB4066	TLC540	Fujitsu	SIMILAR FUNCTIONALITY (see Note 4)	2-19
MB4066	TLC541	Fujitsu	SIMILAR FUNCTIONALITY (see Note 4)	2-19
MB40778	TLC5602	Fujitsu	EXACT EQUIVALENT (see Note 1)	3-19
MC10319	TLC5540	Motorola	SIMILAR FUNCTIONALITY (see Note 4)	2-209
MC10321	TLC5540	Motorola	SIMILAR FUNCTIONALITY (see Note 4)	2-209
MC10322	TLC5540	Motorola	SIMILAR FUNCTIONALITY (see Note 4)	2-209
MC14050	TLC1541	Motorola	EXACT EQUIVALENT (see Note 1)	2-123
MC14051	TLC1541	Motorola	SIMILAR FUNCTIONALITY (see Note 4)	2-123
MC14051	TLC1542	Linear Technology	SIMILAR FUNCTIONALITY (see Note 4)	2-133
MC14051	TLC1542	Motorola	SIMILAR FUNCTIONALITY (see Note 4)	2-133
MC14051	TLC1543	Motorola	SIMILAR FUNCTIONALITY (see Note 4)	2-133
MC14051	TLC1549	Motorola	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-153
MC14444P	TLC546	Motorola	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-39
MC145040	TLC541	Motorola	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-19
MC145041	TLC542	Motorola	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-29
MC145051	TLC1543	Motorola	SIMILAR FUNCTIONALITY (see Note 4)	2-133
MC145051	TLV1543	Motorola	SIMILAR FUNCTIONALITY (see Note 4)	2-317
MC1508	TLC7524	Motorola	SIMILAR FUNCTIONALITY (see Note 4)	3-153
MP0820	TLC0820A	MPR	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-61
MP7524	TLC7524	MPR	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-153
MP7528	TLC7528	MPR	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-163

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CROSS REFERENCE GUIDE

Part No	Suggested TI Replacement	Vendor	Replacement Type	Page No
MP7628	TLC7628	MPR	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-177
MX7524	TLC7524	Maxim	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-153
MX7528	TLC7528	Maxim	SIMILAR FUNCTIONALITY (see Note 4)	3-163
MP7628	TLC7628	Maxim	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-177
NE5036	TLC549	Phillips	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-51
NE5037	TLC549	Phillips	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-51
PCM67	TMS57014	Burr Brown	SIMILAR FUNCTIONALITY (see Note 4)	3-243
PCM69	TMS57014	Burr Brown	SIMILAR FUNCTIONALITY (see Note 4)	3-243
PCM1700	TMS57014A	Burr Brown	SIMILAR FUNCTIONALITY (see Note 4)	3-243
PM7524	TLC7524	Analog Devices	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-153
PM7524	TLC7528	Analog Devices	SIMILAR FUNCTIONALITY (see Note 4)	3-163
PM7528	TLC7524	Analog Devices	SIMILAR FUNCTIONALITY (see Note 4)	3-153
PM7528	TLC7528	Analog Devices	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-163
PM7628	TLC7628	MPR	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-177
PM7628	TLC7628	Analog Devices	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-177
SGT1703	TVP3703-135	SGS-Thomson	SAME FUNCTIONALITY AND PINOUT (see Note 2)	6-15
SGT1703	TVP3703-170	SGS-Thomson	SAME FUNCTIONALITY AND PINOUT (see Note 2)	6-15
ST7546	TLC320AD55	SGS-Thomson	SIMILAR FUNCTIONALITY (see Note 4)	4-417
ST7546	TLC320AD56	SGS-Thomson	SIMILAR FUNCTIONALITY (see Note 4)	4-455
TDA8703	TLC5540	Phillips	SAME FUNCTIONALITY AND PINOUT (see Note 2)	2-209
TSC8701	TLC1541	Teledyne (Telcom)	SIMILAR FUNCTIONALITY (see Note 4)	2-123
TSC8701	TLC1550	Teledyne (Telcom)	SIMILAR FUNCTIONALITY (see Note 4)	2-167
TSC8704	TLC1541	Teledyne (Telcom)	SIMILAR FUNCTIONALITY (see Note 4)	2-123
UPD7528	TLC7528	NEC	SAME FUNCTIONALITY AND PINOUT (see Note 2)	3-163

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GLOSSARY TERMS, DEFINITIONS AND LETTER SYMBOLS

TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS

INTRODUCTION

These terms, definitions, and letter symbols are in accordance with those currently approved by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

1. GENERAL TERMS

Analog-to-Digital Converter (ADC)

A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of which exclusively represents a fractional part of the total analog input range (see Figure 1).

NOTE: This quantization procedure introduces inherent errors of one-half LSB (least significant bit) in the representation since, within this fractional range, only one analog value can be represented free of error by a single digital output code.

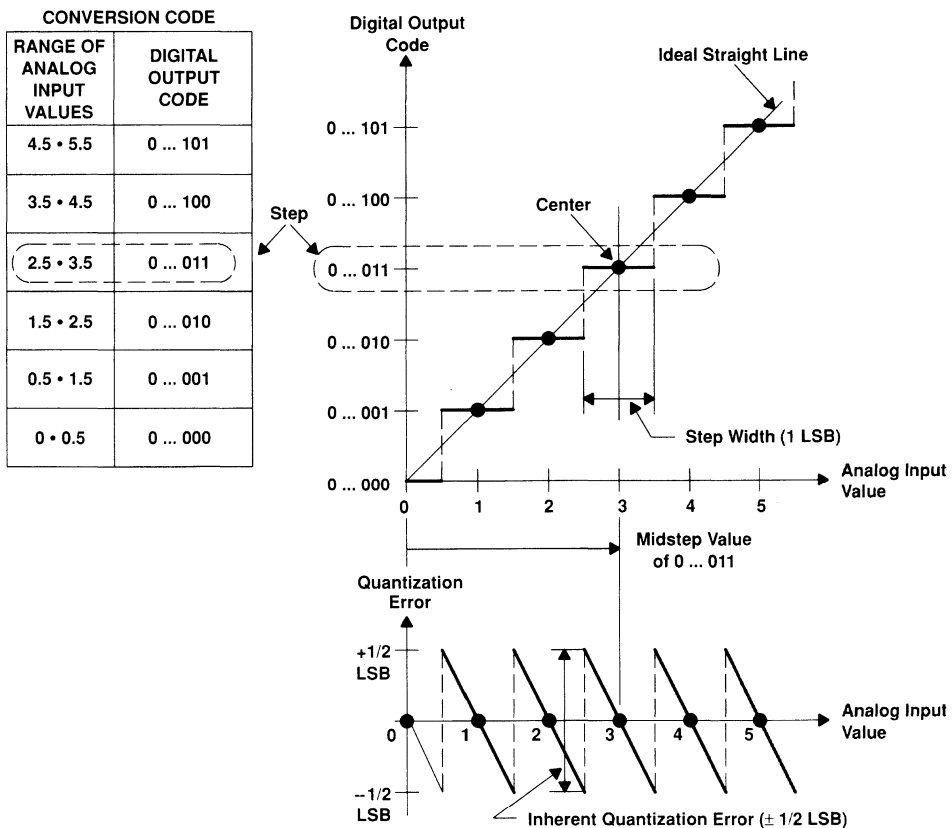


Figure 1. Elements of Transfer Diagram for an Ideal Linear ADC

Analog-to-Digital Processor

An integrated circuit providing the analog part of an ADC; provision of external timing, counting, and arithmetic operations is necessary for implementing a full analog-to-digital converter.

Companding DAC

A DAC whose transfer function complies with a compression or expansion law.

NOTE 1: The corresponding ADC normally consists of such a companding DAC and additional external circuitry.

NOTE 2: The compression or expansion law is usually a logarithmic function, e.g., A-law or μ -law.

Conversion Code (of an ADC or a DAC)

The set of correlations between each of the fractional parts of the total analog input range or each of the digital input codes, respectively, and the corresponding digital output codes or analog output values, respectively (see Figures 1 and 2).

NOTE: Examples of output code formats are straight binary, 2's complement, and binary-coded decimal.

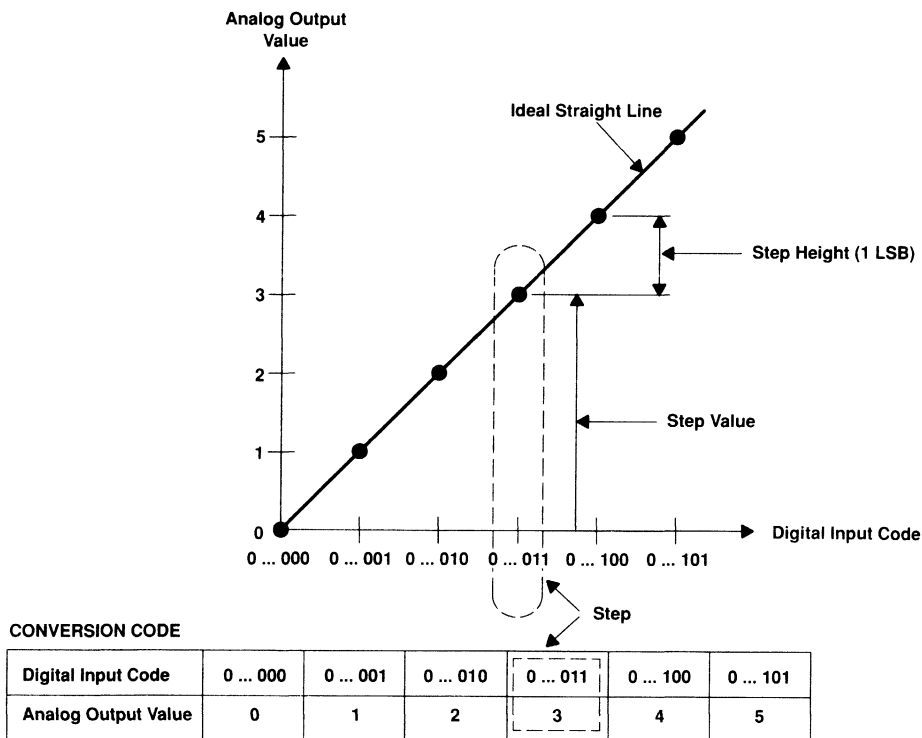


Figure 2. Elements of Transfer Diagram for an Ideal Linear DAC

Digital-to-Analog Converter (DAC)

A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values (see Figure 2)

NOTE: Examples of input code formats are straight binary, 2's complement, and binary-coded decimal.

GLOSSARY TERMS, DEFINITIONS AND LETTER SYMBOLS

Full Scale (of a unipolar ADC or DAC)

A term used to refer a characteristic to that step within the transfer diagram whose nominal midstep value or nominal step value has the highest absolute value [see Figure 3(a) for a linear unipolar ADC].

NOTE 1: The subscript for the letter symbol of a characteristic at full scale is FS.

NOTE 2: In place of a letter symbol, the abbreviation FS is in common use.

Full Scale, Negative (of a bipolar ADC or DAC) [see Figures 3(b) and 3(c)]

A term used to refer a characteristic to the negative end of the transfer diagram, that is, to the step whose nominal midstep value or nominal step value has the most-negative value.

NOTE 1: The subscript for the letter symbol of a characteristic at negative full scale is FS⁻ (V_{FS-} , I_{FS-}).

NOTE 2: In place of a letter symbol, the abbreviation FS⁻ is in common use.

Full Scale, Positive (of a bipolar ADC or DAC) [see Figure 3(b) and 3(c)]

A term used to refer a characteristic to the positive end of the transfer diagram, that is, to the step whose nominal midstep value or nominal step value has the most-positive value.

NOTE 1: The subscript for the letter symbol of a characteristic at positive full scale is FS⁺ (V_{FS+} , I_{FS+}).

NOTE 2: In place of a letter symbol, the abbreviation FS⁺ is in common use.

Full-Scale Range, Nominal (of a linear ADC or DAC) (V_{FSRnom} , I_{FSRnom}) (see Figure 3)

The total range in analog values that can be coded with uniform accuracy by the total number of steps with this number rounded to the next higher power of 2.

NOTE: In place of the letter symbols, the abbreviation FSR(nom) can be used.

Example: Using a straight binary n-bit code format, it follows:

– for an ADC: $FSR(nom) = 2^n \times (\text{nominal value of step width})$

– for a DAC: $FSR(nom) = 2^n \times (\text{nominal value of step height})$

Full-Scale Value, Nominal (V_{FSnom} , I_{FSnom})

A value derived from the nominal full-scale range:

– for a unipolar converter: $V_{FSnom} = V_{FSRnom}$

– for a bipolar converter: $V_{FSnom} = 1/2 V_{FSRnom}$ (see Figure 3)

NOTE 1: In a few data sheets, this analog value is used as a reference value for adjustment procedures or as a rounded value for the full-scale range(s).

NOTE 2: In place of letter symbols, the abbreviation FS(nom) is in common use.

Full-Scale Range, (Practical) (of a linear ADC or DAC) (V_{FSR} , I_{FSR}) (V_{FSRpr} , I_{FSRpr}) (see Figure 3)

The total range of analog values that correspond to the ideal straight line.

NOTE 1: The qualifying adjective practical can usually be deleted from this term provided that, in a very few critical cases, the term nominal full-scale range is not also shortened in the same way. This permits use of the shorter letter symbols or abbreviations (see Note 2).

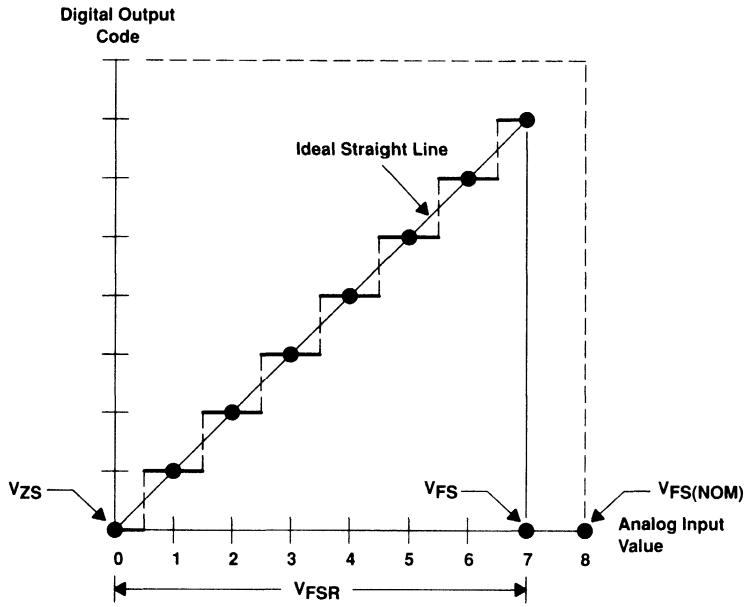
NOTE 2: In place of the letter symbols, the abbreviations FSR and FSR(pr) are in common use.

NOTE 3: The (practical) full-scale range has only a nominal value because it is defined by the end points of the ideal straight line.

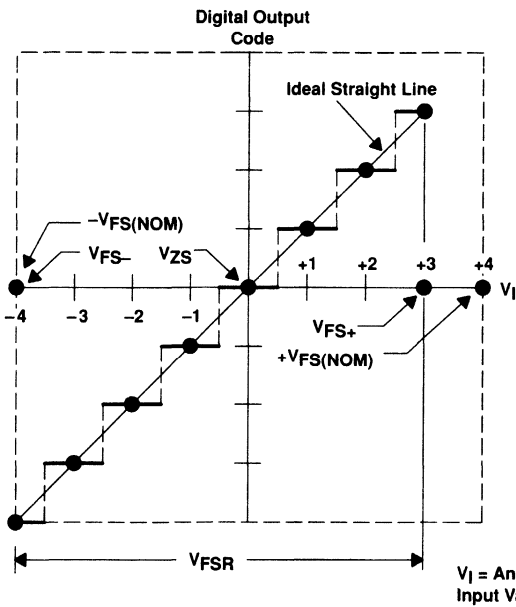
Example: Using a straight binary n-bit code format, it follows:

– for an ADC: $FSR = (2^n - 1) \times (\text{nominal value of step width})$

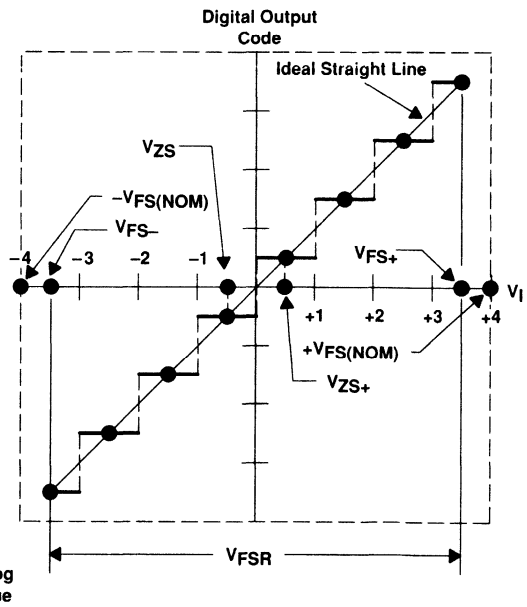
– for a DAC: $FSR = (2^n - 1) \times (\text{nominal value of step height})$



(a) UNIPOLAR ADC



(b) BIPOLAR ADC WITH TRUE ZERO



(c) BIPOLAR ADC WITH NO TRUE ZERO

Figure 3. Ideal Straight Line, Full-Scale Value and Zero-Scale Value
(Shown for Ideal Linear ADCs)

GLOSSARY

TERMS, DEFINITIONS AND LETTER SYMBOLS

Gain Point (of an adjustable ADC or DAC)

The point in the transfer diagram corresponding to the midstep value (for an ADC) or the step value (for a DAC) of the step for which gain error is specified (usually full scale), and in reference to which the gain adjustment is performed (see Figures 4 and 5).

NOTE: Gain adjustment causes only a change of the slope of the transfer diagram, without changing the offset error.

Ideal Straight Line (of a linear ADC or DAC)

In the transfer diagram, a straight line between the specified points for the most-positive (least-negative) and most-negative (least-positive) nominal midstep values or nominal step values, respectively (see Figures 1, 2, and 3).

NOTE: The ideal straight line passes through all the points for nominal midstep values or nominal step values, respectively.

Linear ADC

An ADC having steps ideally of equal width excluding the steps at the two ends of the total range of analog input values.

NOTE: Ideally, the width of each end steps is one half of the width of any other step (see Figure 1).

Linear DAC

A DAC having steps ideally of equal height (see Figure 2).

LSB, Abbreviation

The abbreviation for Least Significant Bit, that is, for the bit that has the lowest positional weight in a natural binary numeral.

Example: In the natural binary numeral 1010, the rightmost bit 0 is the LSB.

LSB, Unit Symbol (for linear converters only)

The unit symbol for the magnitude of the analog resolution of a linear converter, which serves as a reference unit to express the magnitude of other analog quantities of that same converter, especially of analog errors, as multiples or submultiples of the magnitude of the analog resolution.

Example: 1/2 LSB means an analog quantity equal to 0.5 times the analog resolution.

NOTE: The unit symbol LSB refers to the fact that, for a natural binary code, the analog resolution corresponds to the nominal positional weight attributed to the least significant bit of the binary numeral.

In this case, the identity:

$$1 \text{ LSB} = \text{analog resolution}$$

leads, for an n-bit resolution, to:

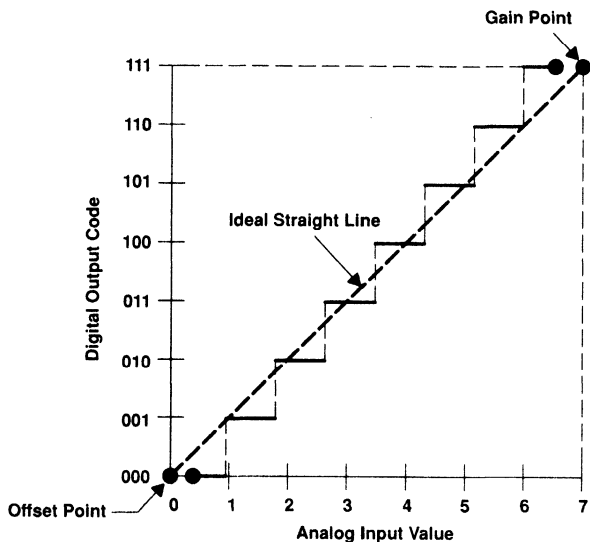
$$1 \text{ LSB} = \frac{\text{FSR}}{2^n - 1} = \frac{\text{FSR}(\text{nom})}{2^n}$$

Midstep Value (of an ADC)

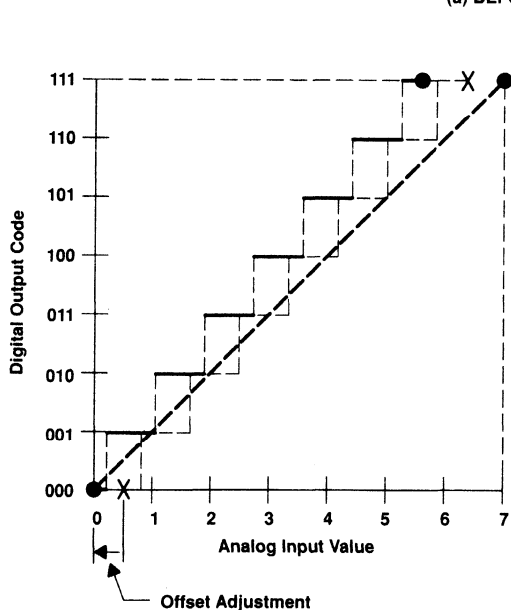
The analog value for the center of the step excluding the steps at the two ends of the total range of analog input values.

NOTE: For the end steps, the midstep value is defined as the analog value that results when the analog value for the transition to the adjacent step is reduced or enlarged, as appropriate, by half the nominal value of the step width (see Figure 1).

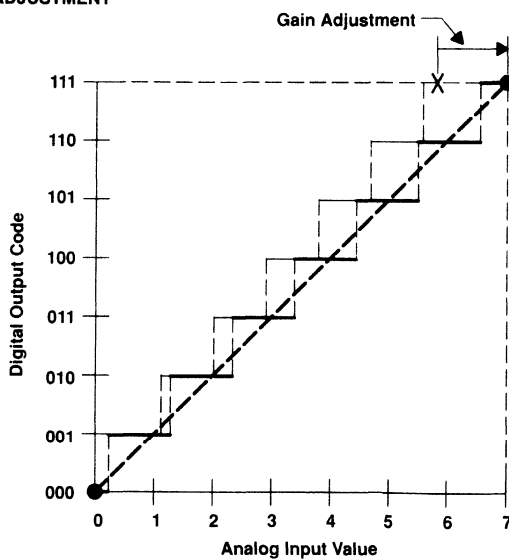




(a) BEFORE ADJUSTMENT



(b) AFTER OFFSET ADJUSTMENT

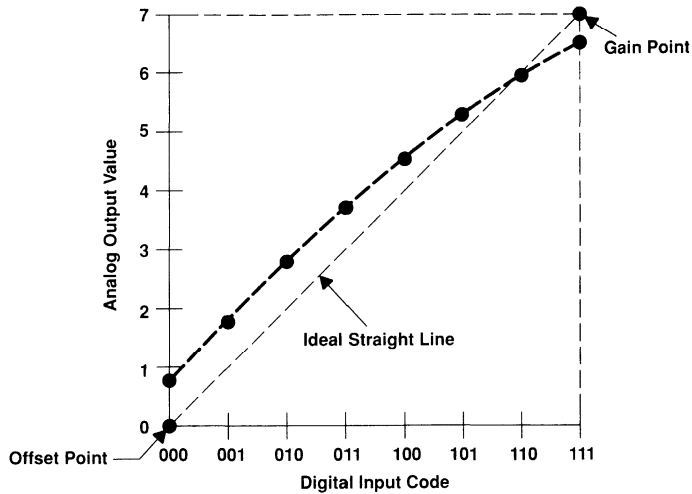


(c) AFTER OFFSET AND GAIN ADJUSTMENTS

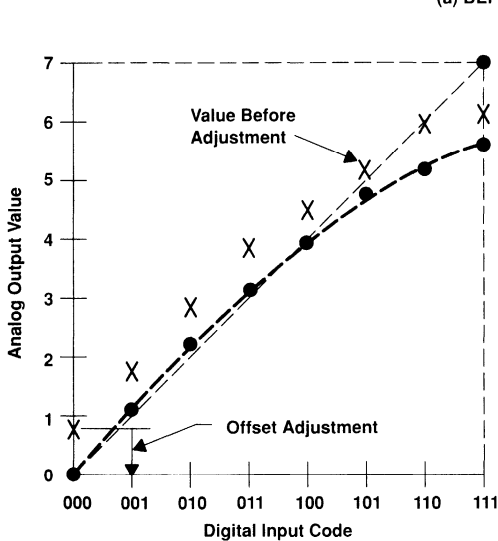
NOTE A: In the above examples, the offset point is referred to the step with the digital code 000, and the gain point is referred to the step with the digital code 111.

Figure 4. Adjustment in Offset Point and Gain Point for an ADC

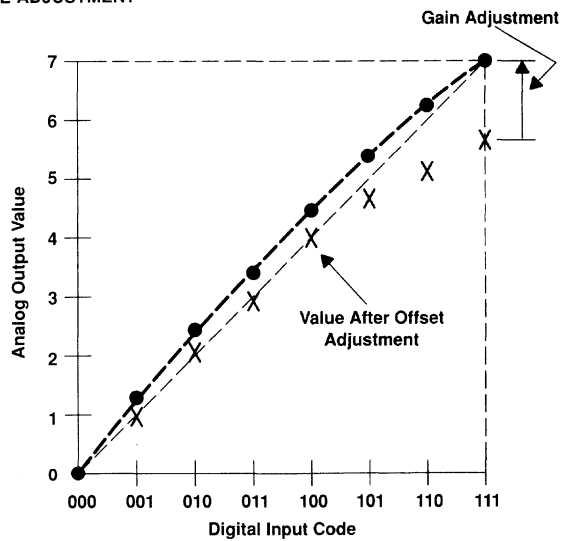
GLOSSARY TERMS, DEFINITIONS AND LETTER SYMBOLS



(a) BEFORE ADJUSTMENT



(b) AFTER OFFSET ADJUSTMENT



(c) AFTER OFFSET AND GAIN ADJUSTMENTS

NOTE A: In the above examples, the offset point is referred to the step with the digital code 000, and the gain point is referred to the step with the digital code 111.

Figure 5. Adjustment in Offset and Gain Point for a DAC

Midstep Value, Nominal (of an ADC)

A specified analog value within a step that is ideally represented free of error by the corresponding digital output code (see Figure 1).

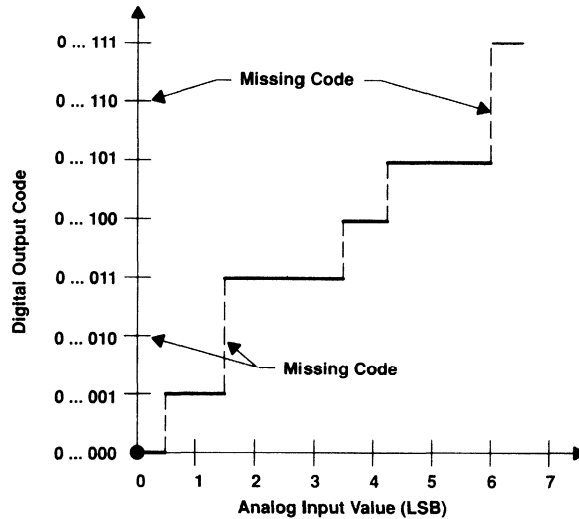


Figure 6. Missing Code for an ADC

Missing Code (of an ADC)

An intermediate code that is absent when the changing analog input to an ADC causes a multiple code change in the digital output (see Figure 6).

Monotonicity (of an ADC or a DAC)

A property of the transfer function that ensures the consistent increase or decrease of the analog output of a DAC or the digital output of an ADC in response to a consistent increase or decrease of the digital or analog input, respectively (Figure 7 illustrates nonmonotonic conversion).

NOTE: An intermediate increment with the value of zero does not invalidate monotonicity.

GLOSSARY TERMS, DEFINITIONS AND LETTER SYMBOLS

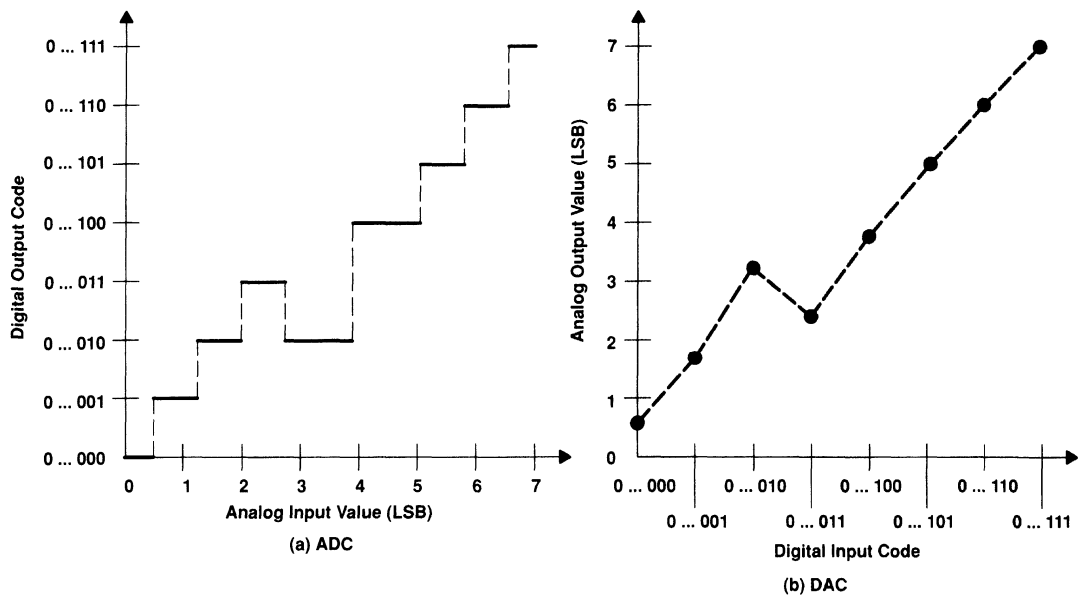


Figure 7. Nonmonotonic Conversion of an ADC or DAC

Multiplying DAC

A DAC having at least two inputs, at least one of which is digital, and whose analog output value is proportional to the product of the inputs.

Nonlinear ADC or DAC

An ADC or a DAC with a specified nonlinear transfer function between the nominal midstep values or nominal step values, respectively, and the corresponding step widths or step heights, respectively.

NOTE: The function may be continuously nonlinear or piece-wise linear.

Offset Point (of an adjustable ADC or DAC)

The point in the transfer diagram corresponding to the midstep value (for an ADC) or the step value (for a DAC) of the step about which the transfer diagram rotates when gain is adjusted (see Figures 4 and 5).

NOTE: Offset adjustment must be performed with respect to this point so that it causes only a parallel displacement of the transfer diagram, without changing its slope.

Resolution (general term)

NOTE 1: Resolution as a capability can be expressed in different forms: (see resolution, analog, resolution, numerical, and resolution, relative).

NOTE 2: Resolution is a design parameter and therefore has only a nominal value.

NOTE 3: The terms for these different forms may all be shortened to resolution if no ambiguity is likely to occur (for example, when the dimension of the term is also given).

Resolution (of an ADC)

The degree to which nearly equal values of the analog input quantity can be discriminated.

Resolution (of a DAC)

The degree to which nearly equal values of the analog output quantity can be produced.

Resolution, Analog (of a linear or nonlinear ADC or DAC)

For an ADC: The nominal value of the step width.

For a DAC: The nominal value of the step height.

NOTE: For a linear ADC or DAC, the constant magnitude of the analog resolution is often used as the reference unit LSB.

Resolution, Numerical

The number (n) of digits in the chosen numbering system necessary to express the total number of steps.

NOTE 1: The numbering system is normally a binary or a decimal system.

NOTE 2: In the binary-coded-decimal numbering system, the term 1/2 digit refers to an additional decimal digit with the highest positional value, but limited to the decimal figures 0 or 1 as it is represented by only a single bit. This additional digit serves to double the range of values covered by the other n digits.

Resolution, Relative (of a Linear ADC or DAC)

The ratio of the analog resolution to the full-scale range (practical or nominal).

NOTE: This ratio is normally expressed as a percentage of the full-scale range [% of FSR, % of FSR(nom)]. For high resolutions (high value of n), it is of little importance whether this ratio refers to the practical or nominal full-scale range.

Step (of an analog-to-digital or digital-to-analog conversion)

In the conversion code: Any of the individual correlations.

In the transfer diagram: Any part of the diagram equating to an individual correlation.

For an ADC, a step represents both a fractional range of analog input values and the corresponding digital output code (see Figure 1).

For a DAC, a step represents both a digital input code and the corresponding discrete analog output value (see Figure 2).

Step Height (Step Size) (of a DAC)

The absolute value of the difference in step value between two adjacent steps in the transfer diagram. (see Figure 2).

NOTE: For companding DACs, the term step size is in general use.

Step Value (of a DAC)

The value of the analog output representing a digital input code (see Figure 2).

Step Value, Nominal (of a DAC)

A specified step value that represents free of error the corresponding digital input code (see Figure 2).

Step Width (of an ADC)

The absolute value of the difference between the two ends of the range of analog values corresponding to one step (see Figure 1).

GLOSSARY TERMS, DEFINITIONS AND LETTER SYMBOLS

Temperature Coefficients of Analog Characteristics (α)

NOTE 1: The letter symbol for the temperature coefficient of an analog characteristic consists of the letter symbol α with a subscript referring to the relevant characteristic.

Example: Temperature coefficient of the gain error: α_{EG}

NOTE 2: Temperature coefficients are usually specified in parts per million (relative to the full-scale value) per degrees Celsius, that is, in ppm/°C.

Zero Scale (of an ADC or a DAC with true zero) [see Figures 3(a) and 3(b)]

A term used to refer a characteristic to the step whose nominal midstep value or nominal step value equals zero.

NOTE 1: The subscript for the letter symbol of a characteristic at zero scale is ZS.

NOTE 2: In place of a letter symbol, the abbreviation ZS is in common use.

Zero Scale, Negative (of an ADC or a DAC with no true zero) [see Figure 3(c)]

A term used to refer a characteristic to the negative step closest to analog zero.

NOTE 1: The subscript for the letter symbol of a characteristic at negative zero scale is ZS⁻ (V_{ZS-} , I_{ZS-}).

NOTE 2: In place of a letter symbol, the abbreviation ZS⁻ is in common use.

Zero Scale, Positive (of an ADC or a DAC with no true zero) [see Figure 3(c)]

A term used to refer a characteristic to the positive step closest to analog zero.

NOTE 1: The subscript for the letter symbol of a characteristic at positive zero scale is ZS⁺ (V_{ZS+} , I_{ZS+}).

NOTE 2: In place of a letter symbol, the abbreviation ZS⁺ is in common use.

2. STATIC PERFORMANCE

Accuracy (see Errors, Part 4)

Asymmetry, Full-Scale (of a DAC with a bipolar analog range) (ΔI_{FSS} , ΔV_{FSS})

The difference between the absolute values of the two full-scale analog values.

Compliance, Current (of a DAC) ($I_{O(op)}$)

The permissible range of output current within which the specifications are valid.

Compliance, Voltage (of a DAC) ($V_{O(op)}$)

The permissible range of output voltage within which the specifications are valid.

Error (see Part 4)

Supply Voltage Sensitivity, (of a DAC) (k_{SVS})

The change in full scale output current (or voltage) caused by a change in supply voltage.

NOTE: This sensitivity is usually expressed as the ratio of the percent change of full-scale current (or voltage) to the percent change of supply voltage.

3. DYNAMIC PERFORMANCE

Conversion Rate (of an externally controlled ADC) (f_c)

The number of conversions per unit time.

NOTE 1: The maximum conversion rate should be specified for full resolution.

NOTE 2: The conversion rate is usually expressed as the number of conversions per second.

NOTE 3: Due to additionally needed settling or recovery times, the maximum specified conversion rate is smaller than the reciprocal of the worst-case conversion time.

Conversion Time (of an ADC) (t_c)

The time elapsed between the command to perform a conversion and the appearance at the converter output of the complete digital representation of the analog input value.

Delay Time, (Digital) (of a linear or a multiplying DAC) (t_d , t_{dd})

The time interval between the instant when the digital input changes and the instant when the analog output passes a specified value that is close to its initial value, ignoring glitches (see Figure 8).

NOTE: For a multiplying DAC, the full term and the additional subscript d must be used to distinguish between the digital and the delay time.

Delay Time, Reference (of a multiplying DAC) (t_{dr})

The time interval between the instant when a step change of the reference voltage occurs and the instant when the analog output passes a specified value that is close to its initial value.

Feedthrough Capacitance (C_F)

The value of the capacitance for a specified value of R in an equivalent circuit for the calculation of the feedthrough error.

NOTE: The equivalent circuit consists of a high-pass R-C filter between the reference input and the analog output.

Feedthrough Error (see Part 4)

Glitch (of a DAC)

A short, undesirable transient in the analog output occurring following a code change at the digital input (see Figure 8).

Glitch Area (of a DAC)

The time integral of the analog value of the glitch transient.

NOTE 1: Usually, the maximum specified glitch area refers to a specified worst-case code change.

NOTE 2: Instead of a letter symbol, the abbreviation GA is in use.

Glitch Energy (of a DAC)

The time integral of the electrical power of the glitch transient.

NOTE 1: Usually, the maximum specified glitch energy refers to a specified worst-case code change.

NOTE 2: Instead of a letter symbol, the abbreviation GE is in use.

GLOSSARY TERMS, DEFINITIONS AND LETTER SYMBOLS

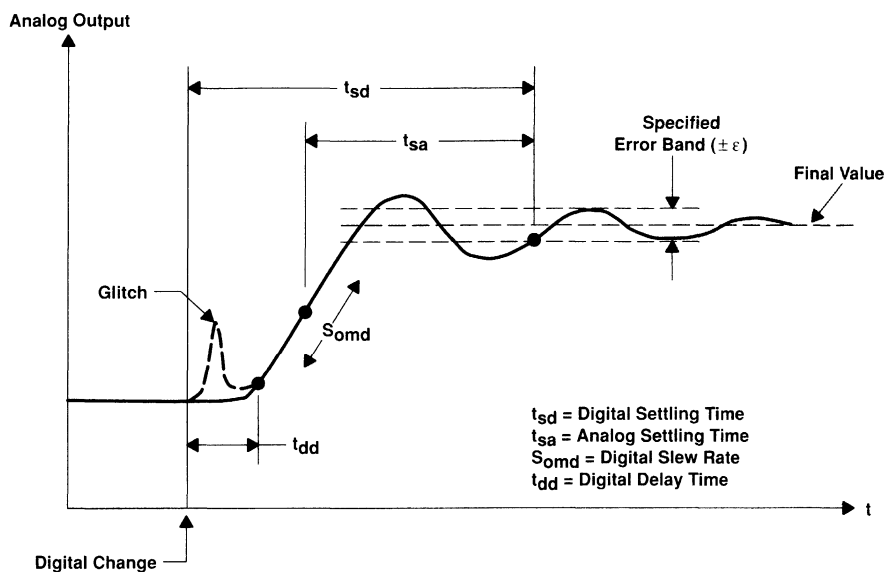


Figure 8. Output Characteristics of a Linear or a Multiplying DAC for a Step Change in the Digital Input Code

Pedestal (Error) (E_p) (see Part 4)

Ramp Delay, Steady-state (of a multiplying DAC) ($t_{d(ramp)}$)

The time separation between the actual curve of the analog output and the theoretical curve (with no delay) for a ramp in reference voltage, after the settling time to steady-state ramp has elapsed (see Figure 9).

Settling Time, Analog (of a DAC) (t_{sa})

The time interval between the instant when the analog output passes a specified value and the instant when the analog output enters for the last time a specified error band about its final value (see Figures 8 and 10).

Settling Time, (Digital) (of a linear or a multiplying DAC) (t_s , t_{sd})

The time interval between the instant when the digital input changes and the instant when the analog output value enters for the last time a specified error band about its final value (see Figure 8).

NOTE: For a multiplying DAC, the full term and the additional subscript d must be used to distinguish between the digital and the settling time.

Settling Time, Reference (of a multiplying DAC) (t_{sr})

The time interval between the instant when a step change of the reference voltage occurs and the instant when the analog output enters for the last time a specified error band about its final value (see Figure 10).

NOTE: Specifications for the reference settling time are usually given for the highest allowed step change in reference voltage.

Settling Time to Steady-State Ramp (of a multiplying DAC) ($t_{s(ramp)}$)

The time interval between the instant a ramp in the reference voltage starts and the instant when the analog output value enters for the last time a specified error band about the final ramp in the output (see Figure 9).

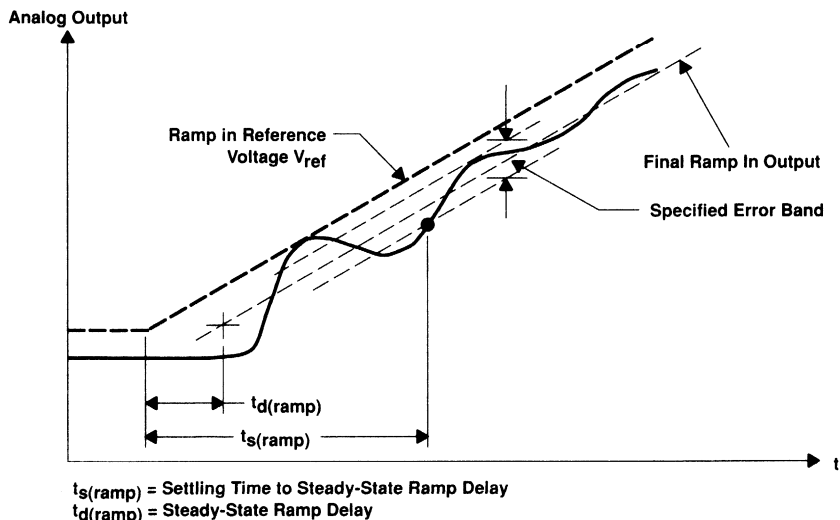


Figure 9. Output Characteristics for a Ramp in Reference Voltage of a Multiplying DAC

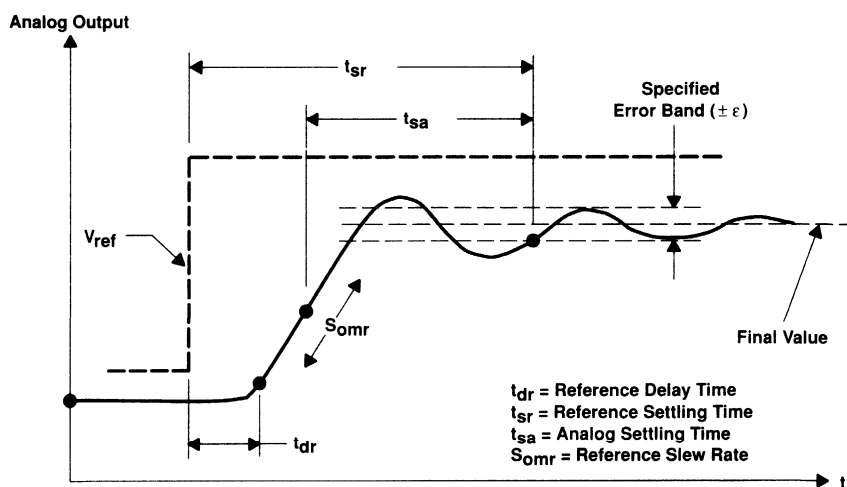


Figure 10. Output Characteristics for a Step Change in Reference Voltage of a Multiplying DAC

Skewing Time, Internal (of a DAC)

The difference in internal delay between the individual output transitions for a given change of digital input.

NOTE: The internal (and external) skew has a major influence on the settling time for critical changes in the digital input, for example, for a 1-LSB change from 011 . . . 111 to 100 . . . 000, and is an important source of commutation noise.

Slew Rate, (Digital) (of a linear or a multiplying DAC) (S_{OM} , S_{OMD})

The maximum rate of change of the analog output value when a change of the digital input code causes a large step change of the analog output value (see Figure 8).

GLOSSARY

TERMS, DEFINITIONS AND LETTER SYMBOLS

NOTE 1: For a multiplying DAC, the full term and the additional subscript D must be used to distinguish between the digital and the slew rate.

NOTE 2: The abbreviations SR and SR(dig) are also used.

Slew Rate, Reference (of a multiplying DAC) (S_{OMR})

The maximum rate of change of the analog output following a large step change of the reference voltage (see Figure 10).

NOTE: The abbreviation SR(ref) is also used.

4. ERRORS, ACCURACY

The definitions in this section describe the errors as the difference between the actual value and the nominal value of the analog quantity. As such they may be expressed in conventional units (for example, millivolts) or as multiples or submultiples of 1 LSB. An error can also be expressed as a relative value, for example, in % of FSR. In this case, it is common practice to use the same term as for the analog value.

Absolute Accuracy Error

Synonym for total error.

Feedthrough Error (of a multiplying DAC) (E_F)

An error in analog output due to variation in the reference voltage that appears as an offset error and is proportional to frequency and amplitude of the reference signal.

NOTE 1: The specification for the feedthrough error is given for the digital input for which the offset error is specified, and for a reference signal of specified frequency and amplitude.

NOTE 2: This error may also be expressed as a peak-to-peak analog value.

Full-Scale Error (of a linear ADC or DAC) (E_{FS})

The difference between the actual midstep value or step value and the nominal midstep value or step value, respectively, at specified full scale.

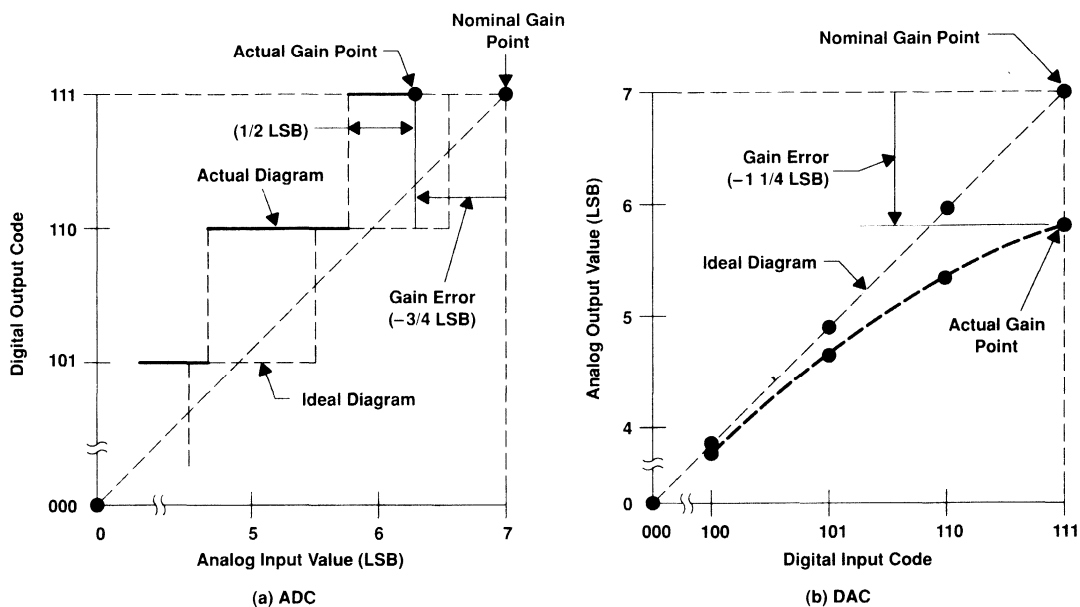
NOTE: Normally, this error specification is applied to converters that have no arrangement for an external adjustment of offset error and gain error.

Gain Error (of a linear ADC or DAC) (E_G)

For an ADC: The difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero [see Figure 11(a)].

For a DAC: The difference between the actual step value and the nominal step value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero [see Figure 11(b)].

NOTE: See Notes 1 and 2 under Offset Error.



**Figure 11. Gain Error of a Linear 3-Bit Natural Binary Code Converter
(Specified at Step 111), After Correction of the Offset Error**

Instability, Long-Term (Accuracy) ($\Delta E_{(\Delta t)}$, $\Delta E_{(t)}$)

The additional error caused by the aging of the components and specified for a longer period in time.

Linearity Error, Best-Straight-Line (of a linear and adjustable ADC) ($E_{L(adj)}$)

The difference between the actual analog value at the transition between any two adjacent steps and its ideal value after offset error and gain error have been adjusted to minimize the magnitude of the extreme values of this difference [see Figure 12(a)].

NOTE 1: The inherent quantization error is not included in the best-straight-line linearity error of an ADC. The ideal value for the transition corresponds to the nominal midstep value $\pm 1/2$ LSB.

NOTE 2: For a uniformly curved transfer diagram, the extreme values will be very close to half of the magnitude of the end-point linearity error [see Figure 12(a)].

Linearity Error, Best-Straight-Line (of a linear and adjustable DAC) ($E_{L(adj)}$)

The difference between the actual step value and the nominal step value after offset error and gain error have been adjusted to minimize the magnitude of the extreme values of this difference [see Figure 12(b)].

NOTE: For a uniformly curved transfer diagram, the extreme values will be very close to half of the magnitude of the end-point linearity error [see Figure 12(b)].

GLOSSARY TERMS, DEFINITIONS AND LETTER SYMBOLS

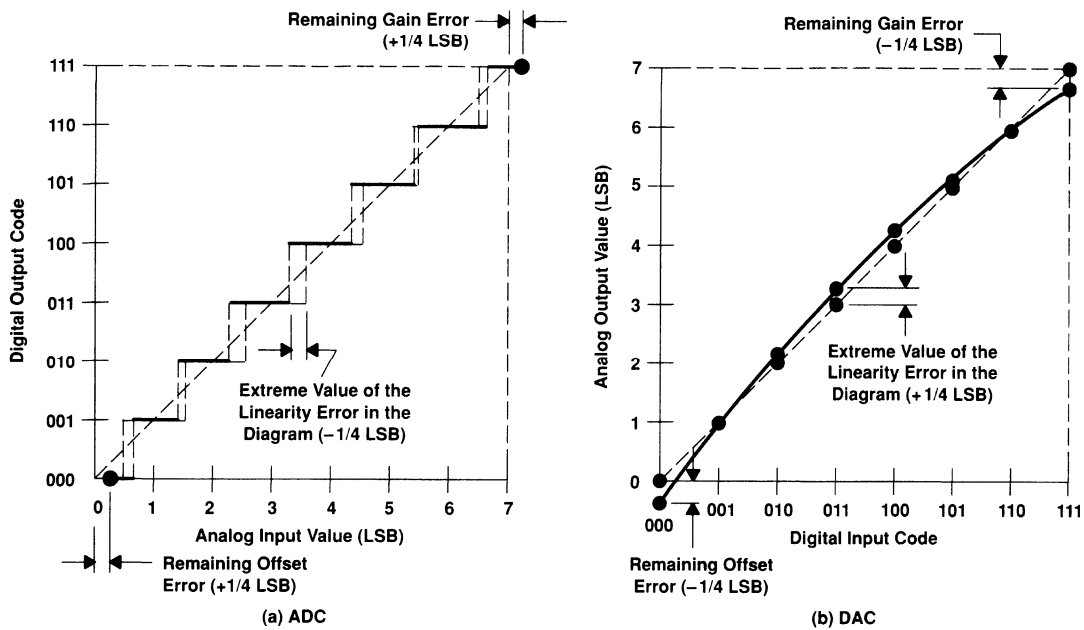


Figure 12. Best-Straight-Line Linearity Error of a Linear 3-Bit Natural Binary-Coded Converter (Values Between $\pm 1/4$ LSB)

Linearity Error, Differential (of a linear ADC or DAC) (E_D)

The difference between the actual step width or step height and the ideal value (1 LSB) (see Figure 13).

NOTE: A differential linearity error greater than 1 LSB can lead to missing codes in an ADC or to nonmonotonicity of an ADC or a DAC (see Figures 6 and 7).

Linearity Error, End-Point (of a linear and adjustable ADC) (E_L)

The difference between the actual analog value at the transition between any two adjacent steps and its ideal value after offset error and gain error have been adjusted to zero [see Figure 14(a)].

NOTE 1: The short term linearity error is in common use and is sufficient if no ambiguity with the best-straight-line linearity error is likely to occur.

NOTE 2: The inherent quantization error is not included in the linearity error of an ADC. The ideal value for the transition corresponds to the nominal midstep value $\pm 1/2$ LSB.

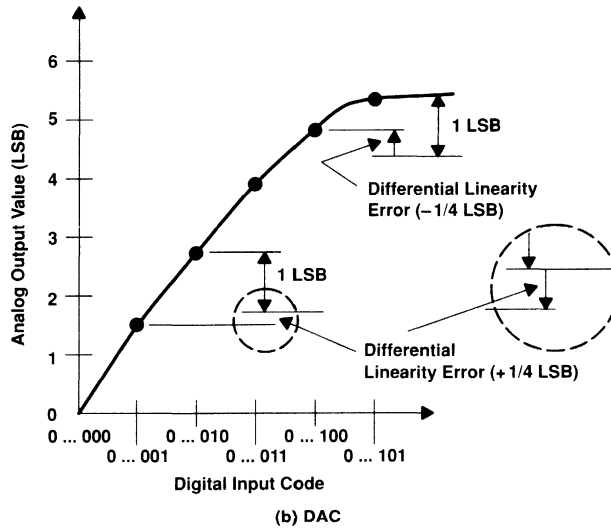
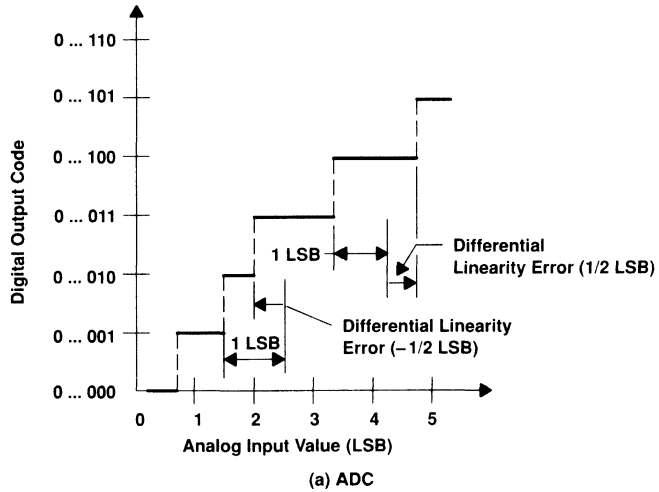


Figure 13. Differential Linearity Error of a Linear ADC or DAC

GLOSSARY TERMS, DEFINITIONS AND LETTER SYMBOLS

Linearity Error, End-Point (of a linear and adjustable DAC) (E_L)

The difference between the actual step value and the nominal step value after offset error and gain error have been adjusted to zero [see Figure 14(b)].

NOTE: The short term linearity error is in common use and is sufficient if no ambiguity with the best-straight-line linearity error is likely to occur.

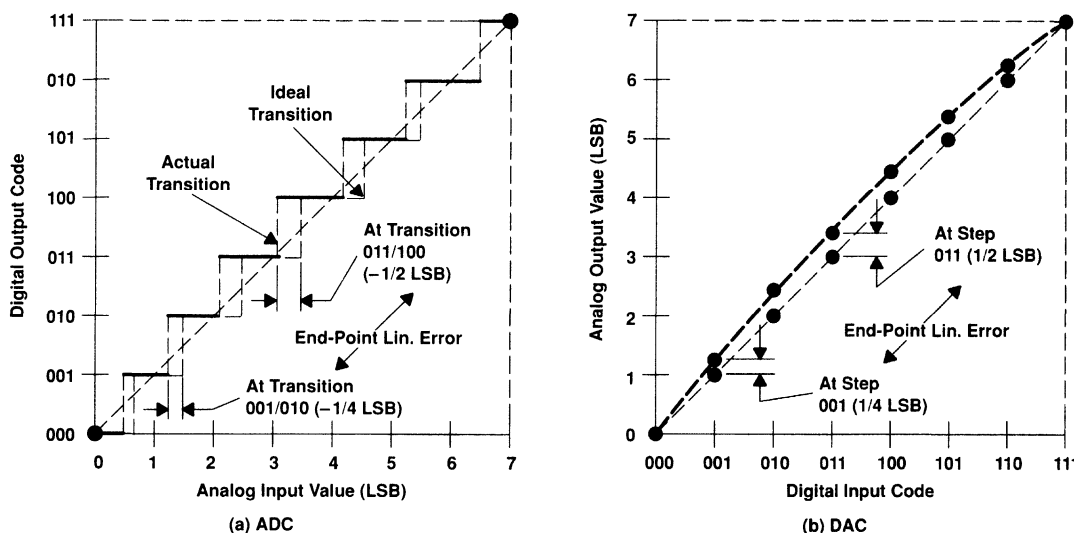


Figure 14. End-Point Linearity Error of a Linear 3-Bit Natural Binary-Coded ADC or DAC (Offset Error and Gain Error are Adjusted to the Value Zero)

Offset Error (of a linear ADC or DAC) (E_O)

For an ADC: The difference between the actual midstep value and the nominal midstep value at the offset point [see Figure 15(a)].

For a DAC: The difference between the actual step value and the nominal step value at the offset point [see Figure 15(b)].

NOTE 1: Usually, the specified steps for the specification of offset error and gain error are the steps at the ends of the practical full-scale range. For an ADC, the midstep value of these steps is defined as the value for a point 1/2 LSB apart from the adjacent transition (see Figures 11 and 15).

NOTE 2: The terms offset error and gain error should be used only for error that can be adjusted to zero. Otherwise, the terms zero-scale error and full-scale error should be used.

Pedestal (Error) (E_P)

A dynamic offset produced in the commutation process.

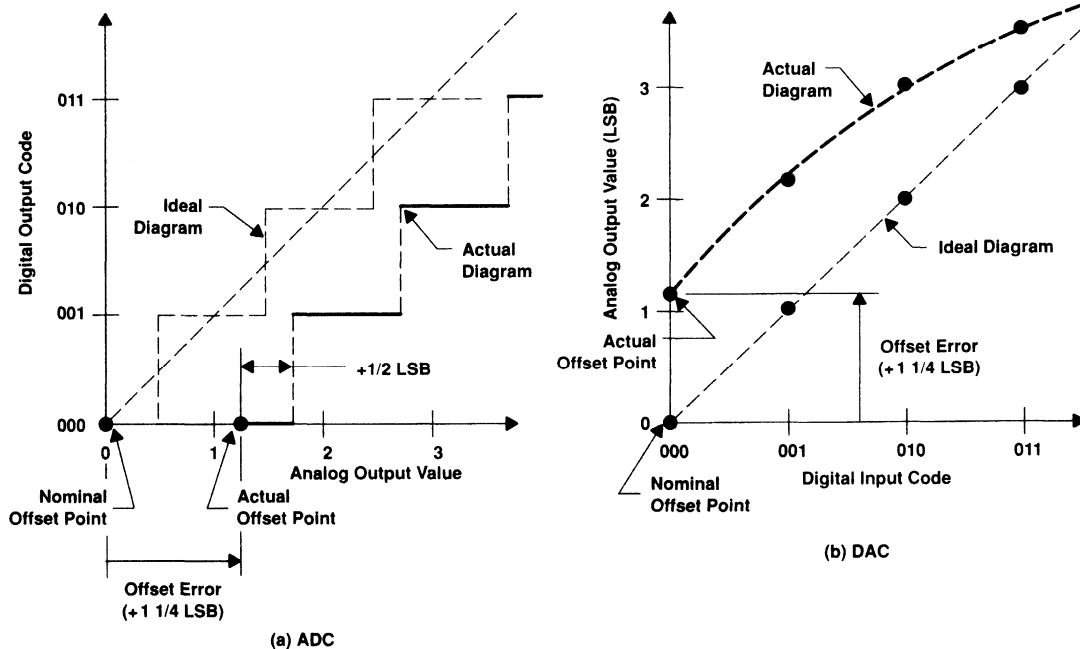


Figure 15. Offset Error of a Linear 3-Bit Natural Binary Code Converter (Specified at Step 000)

Quantization Error, Inherent (of an ideal ADC)

Within a step, the maximum (positive or negative) possible deviation of the actual analog input value from the nominal midstep value.

NOTE 1: This error follows necessarily from the quantization procedure. For a linear ADC, its value equals $\pm 1/2$ LSB (see Figure 1).

NOTE 2: The term resolution error for the inherent quantization error is deprecated, because resolution as a design parameter has only a nominal value.

Rollover Error (of an ADC with decimal output and auto-polarity) (E_{RO})

The difference in output readings with the analog input switched between positive and negative values of the same magnitude (close to full scale).

Total Error (of a linear ADC) (E_T)

The maximum difference (positive or negative) between an analog value and the nominal midstep value within any step [see Figure 16(a)].

NOTE 1: If this error is expressed as a relative value, the term relative accuracy error should be used instead of absolute accuracy error.

NOTE 2: This error includes contributions from offset error, gain error, linearity error, and the inherent quantization error.

GLOSSARY TERMS, DEFINITIONS AND LETTER SYMBOLS

Total Error (of a linear DAC) (E_T)

The difference (positive or negative) between the actual step value and the nominal step value for any step [see Figure 16(b)].

NOTE 1: If this error is expressed as a relative value, the term relative accuracy error should be used instead of absolute accuracy error.

NOTE 2: This error includes contributions from offset error, gain error, and linearity error.

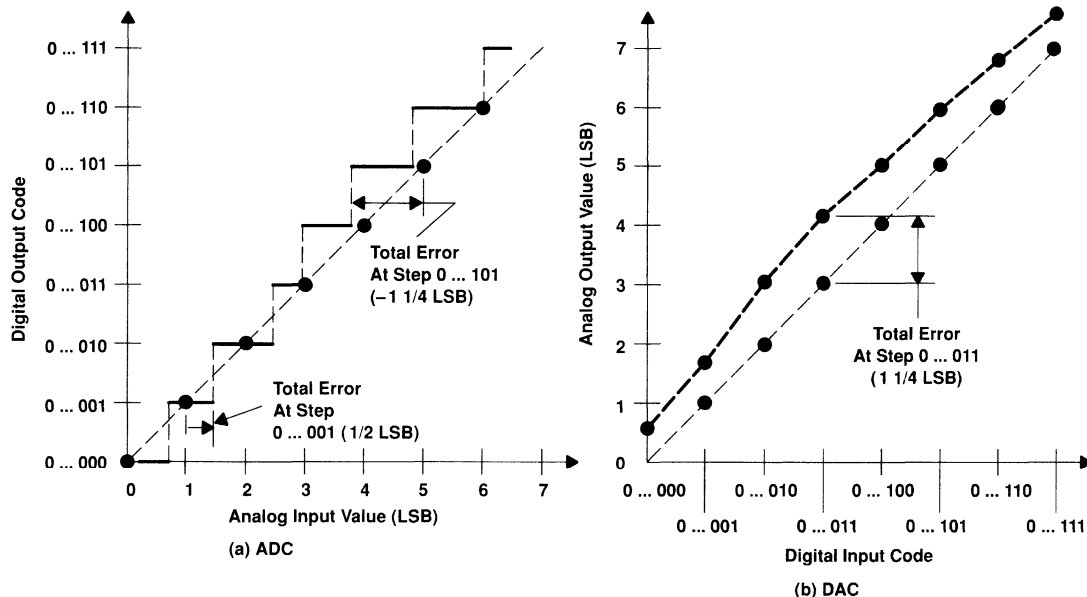


Figure 16. Absolute Accuracy Error, Total Error of a Linear ADC or DAC

Zero-Scale Error (of a linear ADC or DAC) (E_{ZS})

The difference between the actual midstep value or step value and the nominal midstep value or step value, respectively, at specified zero scale.

NOTE: Normally, this error specification is applied to converters that have no arrangement for an external adjustment of offset error and gain error.

5. Dynamic and Sigma-Delta Definitions

Resolution

The number of different output codes possible. Expressed as N , where 2^N is the number of available output codes.

Dynamic Range

The ratio of the largest allowable input signal to the noise floor.

Total Harmonic Distortion

The ratio of the rms sum of all harmonics to the rms value of the largest allowable input signal. Units in dB's.

Signal to Intermodulation Distortion

The ratio of the rms sum of two input signals to the rms sum of all discernible intermodulation and harmonic distortion products.

Linearity Error

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. Zero-scale is a point 1/2 LSB below the first code transition and full-scale is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in %FS.

Differential Nonlinearity

The deviation of a code's width from the ideal width in LSB's.

Positive Full Scale Error

The deviation of the last code transition from the ideal, ($V_{ref} - 1.5 \text{ LSB}$).

Positive Full Scale Drift

The drift in effective, positive, full-scale input voltage with temperature.

Negative Full Scale Error

The deviation of the first code transition from the ideal, ($-V_{ref} + 0.5 \text{ LSB}$).

Negative Full Scale Drift

The drift in effective, negative, full-scale input voltage with temperature.

Bipolar Offset

The deviation of the midscale transition from the ideal. The ideal is defined as the middle transition lying on a straight line between actual positive full-scale and actual negative full-scale.

Bipolar Offset Drift

The drift in the bipolar offset error with temperature.

Absolute Group Delay

The delay through the filter section of the part.

Passband Frequency

The upper -3 dB frequency.

General Information	1
General Purpose ADCs	2
General Purpose DACs	3
DSP AICs and CODECs	4
Special Functions	5
Video Interface Palettes	6
Digital Imaging Sensor Products	7
Mechanical Information	8

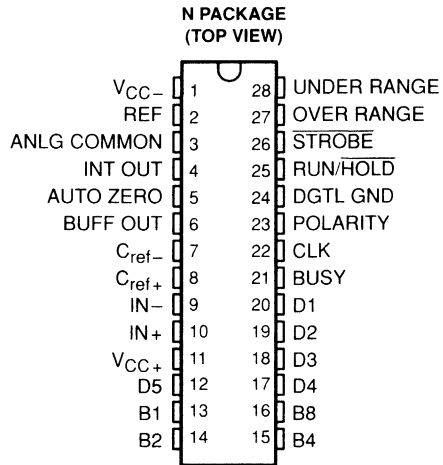
Contents

2 General Purpose ADCs

	Page
TLC7135, ICL7135 :	2-3
TL5501 :	2-13
TLC540, TLC541 :	2-19
TLC542 :	2-29
TLC545, TLC546 :	2-39
TLC548, TLC549 :	2-51
TLC0820A :	2-61
TLC0831, TLC0832 :	2-71
TLC0834, TLC0838 :	2-83
TLC876 :	2-97
TLC876M :	2-119
TLC1541 :	2-123
TLC1542, TLC1543 :	2-133
TLC1549 :	2-153
TLC1550, TLC1551 :	2-167
TLC2543 :	2-175
TLC5510 :	2-197
TLC5540 :	2-209
TLC5733A :	2-225
TLC320AD57 :	2-247
TLC320AD58 :	2-267
TLV0831, TLV0832 :	2-291
TLV0834, TLV0838 :	2-303
TLV1543 :	2-317
TLV1544, TLV1548 :	2-335
TLV1548M :	2-367
TLV1549 :	2-373
TLV1570 :	2-387
TLV1572 :	2-397
TLV2543 :	2-409
TLV5510 :	2-429

ICL7135C, TLC7135C
4 1/2-DIGIT PRECISION
ANALOG-TO-DIGITAL CONVERTERS
SLAS074A – DECEMBER 1986 – REVISED MAY 1995

- Zero Reading for 0-V Input
- Precision Null Detection With True Polarity at Zero
- 1-pA Typical Input Current
- True Differential Input
- Multiplexed Binary-Coded-Decimal (BCD) Output
- Low Rollover Error: ± 1 Count Max
- Control Signals Allow Interfacing With UARTs or Microprocessors
- Autoranging Capability With Over- and Under-Range Signals
- TTL-Compatible Outputs
- Direct Replacement for Teledyne TSC7135, Intersil ICL7135, Maxim ICL7135, and Siliconix Si7135
- CMOS Technology



description

The ICL7135C and TLC7135C converters are manufactured with Texas Instruments highly efficient CMOS technology. This 4 1/2-digit, dual-slope-integrating, analog-to-digital converter (DAC) is designed to provide interfaces to both a microprocessor and a visual display. The digit-drive outputs D1 through D4 and multiplexed binary-coded-decimal outputs B1, B2, B4, and B8 provide an interface for LED or LCD decoder/drivers as well as microprocessors.

The ICL7135C and TLC7135C offer 50-ppm (one part in 20,000) resolution with a maximum linearity error of one count. The zero error is less than 10 μ V and zero drift is less than 0.5 μ V/ $^{\circ}$ C. Source-impedance errors are minimized by low input current (less than 10 pA). Rollover error is limited to ± 1 count.

The BUSY, $\overline{\text{STROBE}}$, $\overline{\text{RUN/HOLD}}$, OVER RANGE, and UNDER RANGE control signals support microprocessor-based measurement systems. The control signals also can support remote data acquisition systems with data transfer through universal asynchronous receiver transmitters (UARTs).

The ICL7135C and TLC7135C are characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.

AVAILABLE OPTIONS

T _A	PACKAGE
	PLASTIC DIP (N)
0 $^{\circ}$ C to 70 $^{\circ}$ C	ICL7135CN
	TLC7135CN



Caution. These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

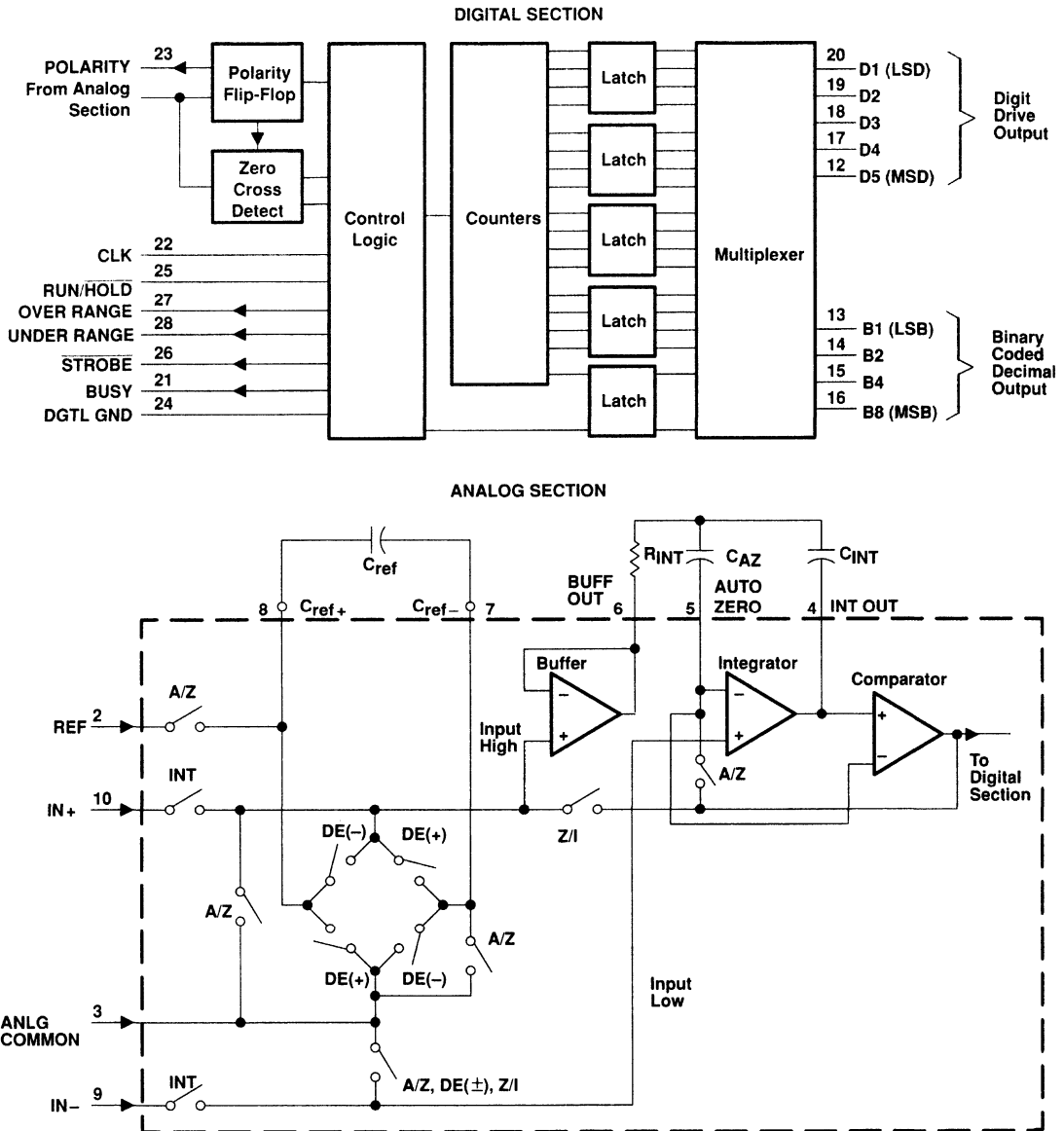
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



ICL7135C, TLC7135C
4 1/2-DIGIT PRECISION
ANALOG-TO-DIGITAL CONVERTERS

SLAS074A - DECEMBER 1986 - REVISED MAY 1995

functional block diagram



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ICL7135C, TLC7135C
4 1/2-DIGIT PRECISION
ANALOG-TO-DIGITAL CONVERTERS
 SLAS074A – DECEMBER 1986 – REVISED MAY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{CC+} with respect to V_{CC-})	15 V
Analog input voltage ($IN-$ or $IN+$)	V_{CC-} to V_{CC+}
Reference voltage range	V_{CC-} to V_{CC+}
Clock input voltage range	0 V to V_{CC+}
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4	5	6	V
Supply voltage, V_{CC-}	-3	-5	-8	V
Reference voltage, V_{ref}		1		V
High-level input voltage, CLK, RUN/HOLD, V_{IH}	2.8			V
Low-level input voltage, CLK, RUN/HOLD, V_{IL}			0.8	V
Differential input voltage, V_{ID}	$V_{CC-} + 1$		$V_{CC+} - 0.5$	V
Maximum operating frequency, f_{clock} (see Note 1)	1.2	2		MHz
Operating free-air temperature range, T_A	0		70	°C

NOTE 1: Clock frequency range extends down to 0 Hz.

electrical characteristics, $V_{CC+} = 5$ V, $V_{CC-} = 5$ V, $V_{ref} = 1$ V, $f_{clock} = 120$ kHz, $T_A = 25^\circ$ C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	D1-D5, B1, B2, B4, B8	$I_O = -1$ mA	2.4	5	V
		Other outputs	$I_O = -10$ μ A	4.9	5	
V_{OL}	Low-level output voltage		$I_O = 1.6$ mA		0.4	V
$V_{ON(PP)}$	Peak-to-peak output noise voltage (see Note 2)	$V_{ID} = 0$, Full scale = 2 V		15		μ V
α_{VO}	Zero-reading temperature coefficient of output voltage	$V_{ID} = 0$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		0.5	2	$\mu\text{V}/^\circ\text{C}$
I_{IH}	High-level input current	$V_I = 5$ V, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		0.1	10	μ A
I_{IL}	Low-level input current	$V_I = 0$ V, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		-0.02	-0.1	mA
I_I	Input leakage current, $IN-$ and $IN+$	$V_{ID} = 0$	$T_A = 25^\circ\text{C}$	1	10	μ A
			$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		250	
I_{CC+}	Positive supply current	$f_{clock} = 0$	$T_A = 25^\circ\text{C}$	1	2	mA
			$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		3	
I_{CC-}	Negative supply current	$f_{clock} = 0$	$T_A = 25^\circ\text{C}$	-0.8	-2	mA
			$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		-3	
C_{pd}	Power dissipation capacitance	See Note 3		40		pF

NOTES: 2. This is the peak-to-peak value that is not exceeded 95% of the time.

3. Factor-relating clock frequency to increase in supply current. At $V_{CC+} = 5$ V, $I_{CC+} = I_{CC+}(f_{clock} = 0) + C_{pd} \times 5$ V $\times f_{clock}$



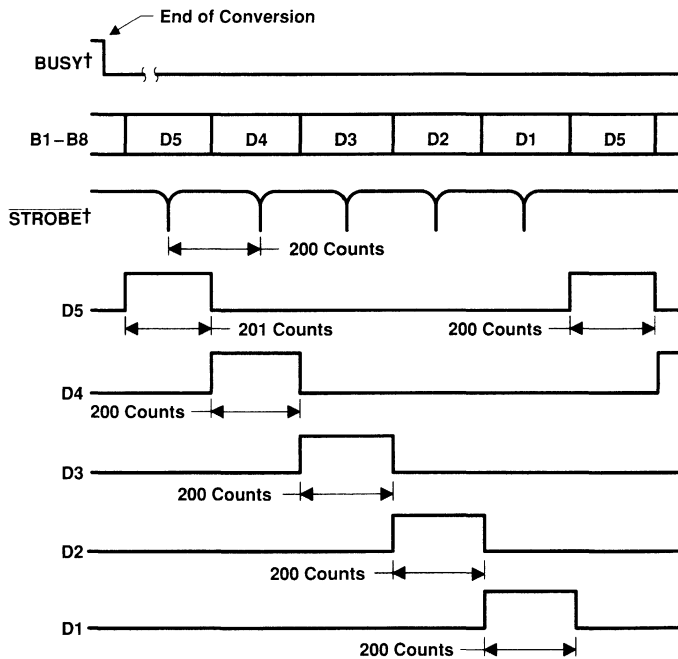
ICL7135C, TLC7135C
4 1/2-DIGIT PRECISION
ANALOG-TO-DIGITAL CONVERTERS
 SLAS074A – DECEMBER 1986 – REVISED MAY 1995

operating characteristics, $V_{CC+} = 5\text{ V}$, $V_{CC-} = 5\text{ V}$, $V_{ref} = 1\text{ V}$, $f_{clock} = 120\text{ kHz}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
α_{FS} Full-scale temperature coefficient (see Note 4)	$V_{ID} = 2\text{ V}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$			5	ppm/ $^\circ\text{C}$
E_L Linearity error	$-2\text{ V} \leq V_{ID} \leq 2\text{ V}$		0.5		count
E_D Differential linearity error (see Note 5)	$-2\text{ V} \leq V_{ID} \leq 2\text{ V}$		0.01		LSB
E_{FS} \pm Full-scale symmetry error (rollover error) (see Note 6)	$V_{ID} = \pm 2\text{ V}$		0.5	1	count
Display reading with 0-V input	$V_{ID} = 0$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	-0.0000	± 0.0000	0.0000	Digital Reading
Display reading in ratiometric operation	$V_{ID} = V_{ref}$, $T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	0.9998	0.9999	1.0000	Digital Reading
		0.9995	0.9999	1.0005	

- NOTES: 4. This parameter is measured with an external reference having a temperature coefficient of less than 0.01 ppm/ $^\circ\text{C}$.
 5. The magnitude of the difference between the worst case step of adjacent counts and the ideal step.
 6. Rollover error is the difference between the absolute values of the conversion for 2 V and -2 V.

timing diagrams



† Delay between **BUSY** going low and the first **STROBE** pulse is dependent upon the analog input.

Figure 1

timing diagrams (continued)

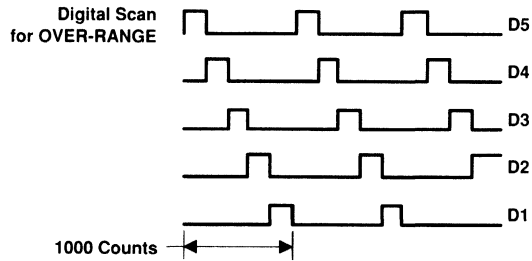


Figure 2

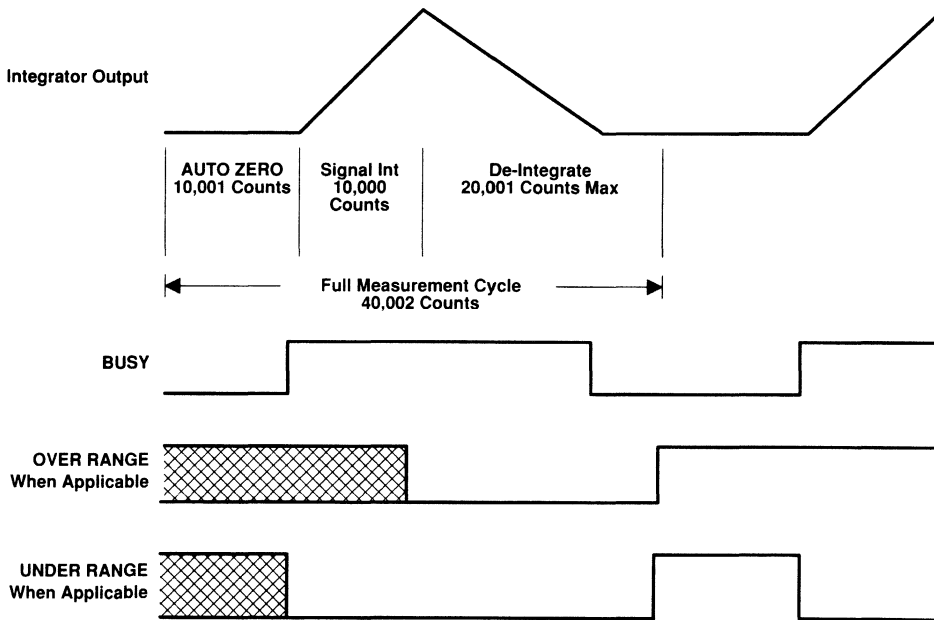
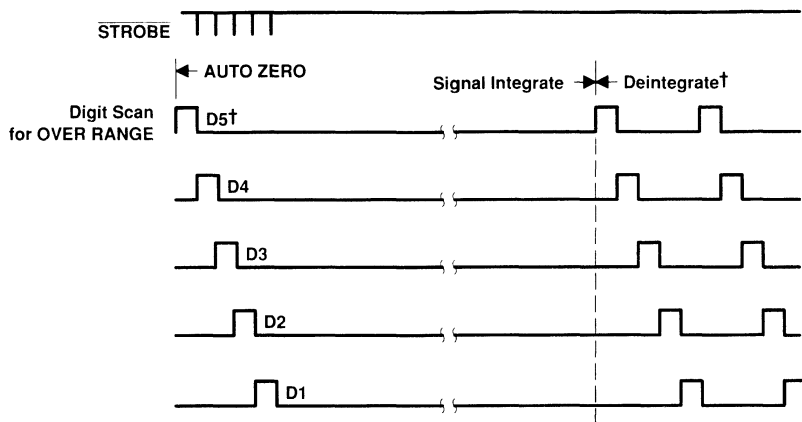


Figure 3

ICL7135C, TLC7135C
4 1/2-DIGIT PRECISION
ANALOG-TO-DIGITAL CONVERTERS

SLAS074A – DECEMBER 1986 – REVISED MAY 1995

timing diagrams (continued)



† First D5 of AUTO ZERO and deintegrate is one count longer.

Figure 4

PRINCIPLES OF OPERATION

A measurement cycle for the ICL7135C and TLC7135C consists of the following four phases.

1. Auto-Zero Phase. The internal IN+ and IN– inputs are disconnected from the terminals and internally connected to ANLG COMMON. The reference capacitor is charged to the reference voltage. The system is configured in a closed loop and the auto-zero capacitor is charged to compensate for offset voltages in the buffer amplifier, integrator, and comparator. The auto-zero accuracy is limited only by the system noise, and the overall offset, as referred to the input, is less than 10 μ V.
2. Signal Integrate Phase. The auto-zero loop is opened and the internal IN+ and IN– inputs are connected to the external terminals. The differential voltage between these inputs is integrated for a fixed period of time. When the input signal has no return with respect to the converter power supply, IN– can be tied to ANLG COMMON to establish the correct common-mode voltage. Upon completion of this phase, the polarity of the input signal is recorded.
3. deintegrate Phase. The reference is used to perform the deintegrate task. The internal IN– is internally connected to ANLG COMMON and IN+ is connected across the previously charged reference capacitor. The recorded polarity of the input signal ensures that the capacitor is connected with the correct polarity so that the integrator output polarity returns to zero. The time required for the output to return to zero is proportional to the amplitude of the input signal. The return time is displayed as a digital reading and is determined by the equation $10,000 \times (V_{ID}/V_{ref})$. The maximum or full-scale conversion occurs when V_{ID} is two times V_{ref} .
4. Zero Integrator Phase. The internal IN– is connected to ANLG COMMON. The system is configured in a closed loop to cause the integrator output to return to zero. Typically, this phase requires 100 to 200 clock pulses. However, after an over-range conversion, 6200 pulses are required.

PRINCIPLES OF OPERATION

description of analog circuits

input signal range

The common mode range of the input amplifier extends from 1 V above the negative supply to 1 V below the positive supply. Within this range, the common-mode rejection ratio (CMRR) is typically 86 dB. Both differential and common-mode voltages cause the integrator output to swing. Therefore, care must be exercised to ensure that the integrator output does not become saturated.

analog common

Analog common (ANLG COMMON) is connected to the internal IN $\bar{}$ during the auto-zero, deintegrate, and zero integrator phases. When IN $\bar{}$ is connected to a voltage that is different than analog common during the signal integrate phase, the resulting common-mode voltage is rejected by the amplifier. However, in most applications, IN $\bar{}$ is set at a known fixed voltage (i.e., power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. Removing the common-mode voltage in this manner slightly increases conversion accuracy.

reference

The reference voltage is positive with respect to analog common. The accuracy of the conversion result is dependent upon the quality of the reference. Therefore, to obtain a high accuracy conversion, a high quality reference should be used.

description of digital circuits

RUN/ $\overline{\text{HOLD}}$ input

When RUN/ $\overline{\text{HOLD}}$ is high or open, the device continuously performs measurement cycles every 40,002 clock pulses. When this input is taken low, the integrated circuit continues to perform the ongoing measurement cycle and then hold the conversion reading for as long as the terminal is held low. When the terminal is held low after completion of a measurement cycle, a short positive pulse (greater than 300 ns) initiates a new measurement cycle. When this positive pulse occurs before the completion of a measurement cycle, it will not be recognized. The first $\overline{\text{STROBE}}$ pulse, which occurs 101 counts after the end of a measurement cycle, is an indication of the completion of a measurement cycle. Thus, the positive pulse could be used to trigger the start of a new measurement after the first $\overline{\text{STROBE}}$ pulse.

$\overline{\text{STROBE}}$ input

Negative going pulses from this input transfer the BCD conversion data to external latches, UARTs, or microprocessors. At the end of the measurement cycle, $\overline{\text{STROBE}}$ goes high and remains high for 201 counts. The most significant digit (MSD) BCD bits are placed on the BCD terminals. After the first 101 counts, halfway through the duration of output D1–D5 going high, the $\overline{\text{STROBE}}$ terminal goes low for 1/2 clock pulse width. The placement of the $\overline{\text{STROBE}}$ pulse at the midpoint of the D5 high pulse allows the information to be latched into an external device on either a low-level or an edge. Such placement of the $\overline{\text{STROBE}}$ pulse also ensures that the BCD bits for the second MSD are not yet competing for the BCD lines and latching of the correct bits is ensured. The above process is repeated for the second MSD and the D4 output. Similarly, the process is repeated through the least significant digit (LSD). Subsequently, inputs D5 through D1 and the BCD lines continue scanning without the inclusion of $\overline{\text{STROBE}}$ pulses. This subsequent continuous scanning causes the conversion results to be continuously displayed. Such subsequent scanning does not occur when an over-range condition occurs.

ICL7135C, TLC7135C

4 1/2-DIGIT PRECISION

ANALOG-TO-DIGITAL CONVERTERS

SLAS074A – DECEMBER 1986 – REVISED MAY 1995

PRINCIPLES OF OPERATION

BUSY output

The BUSY output goes high at the beginning of the signal integrate phase. BUSY remains high until the first clock pulse after zero crossing or at the end of the measurement cycle when an over-range condition occurs. It is possible to use the BUSY terminal to serially transmit the conversion result. Serial transmission can be accomplished by ANDing the BUSY and CLOCK signals and transmitting the ANDed output. The transmitted output consists of 10,001 clock pulses, which occur during the signal integrate phase, and the number of clock pulses that occur during the deintegrate phase. The conversion result can be obtained by subtracting 10,001 from the total number of clock pulses.

OVER-RANGE output

When an over-range condition occurs, this terminal goes high after the BUSY signal goes low at the end of the measurement cycle. As previously noted, the BUSY signal remains high until the end of the measurement cycle when an over-range condition occurs. The OVER RANGE output goes high at the end of BUSY and goes low at the beginning of the deintegrate phase in the next measurement cycle.

UNDER-RANGE output

At the end of the BUSY signal, this terminal goes high when the conversion result is less than or equal to 9% (count of 1800) of the full-scale range. The UNDER RANGE output is brought low at the beginning of the signal integrate phase of the next measurement cycle.

POLARITY output

The POLARITY output is high for a positive input signal and updates at the beginning of each deintegrate phase. The polarity output is valid for all inputs including ± 0 and OVER RANGE signals.

digit-drive (D1, D2, D4 and D5) outputs

Each digit-drive output (D1 through D5) sequentially goes high for 200 clock pulses. This sequential process is continuous unless an over-range occurs. When an over-range occurs, all of the digit-drive outputs are blanked from the end of the strobe sequence until the beginning of the deintegrate phase (when the sequential digit-drive activation begins again). The blanking activity during an over-range condition can cause the display to flash and indicate the over-range condition.

BCD outputs

The BCD bits (B1, B2, B4 and B8) for a given digit are sequentially activated on these outputs. Simultaneously, the appropriate digit-drive line for the given digit is activated.

system aspects

integrating resistor

The value of the integrating resistor (R_{INT}) is determined by the full-scale input voltage and the output current of the integrating amplifier. The integrating amplifier can supply 20 μA of current with negligible nonlinearity. The equation for determining the value of this resistor is:

$$R_{INT} = \frac{\text{Full Scale Voltage}}{I_{INT}}$$

Integrating amplifier current, I_{INT} , from 5 to 40 μA yields good results. However, the nominal and recommended current is 20 μA .

PRINCIPLES OF OPERATION

integrating capacitor

The product of the integrating resistor and capacitor should be selected to give the maximum voltage swing without causing the integrating amplifier output to saturate and get too close to the power supply voltages. When the amplifier output is within 0.3 V of either supply, saturation occurs. With ± 5 -V supplies and ANLG COMMON connected to ground, the designer should design for a ± 3.5 -V to ± 4 -V integrating amplifier swing. A nominal capacitor value is 0.47 μ F. The equation for determining the value of the integrating capacitor (C_{INT}) is:

$$C_{INT} = \frac{10,000 \times \text{Clock Period} \times I_{INT}}{\text{Integrator Output Voltage Swing}}$$

Where:

I_{INT} is nominally 20 μ A.

Capacitors with large tolerances and high dielectric absorption can induce conversion inaccuracies. A capacitor that is too small could cause the integrating amplifier to saturate. High dielectric absorption causes the effective capacitor value to be different during the signal integrate and deintegrate phases. Polypropylene capacitors have very low dielectric absorption. Polystyrene and polycarbonate capacitors have higher dielectric absorption, but also work well.

auto-zero and reference capacitor

Large capacitors tend to reduce noise in the system. Dielectric absorption is unimportant except during power up or overload recovery. Typical values are 1 μ F.

reference voltage

For high-accuracy absolute measurements, a high quality reference should be used.

rollover resistor and diode

The ICL7135C and TLC7135C have a small rollover error; however, it can be corrected. The correction is to connect the cathode of any silicon diode to INT OUT and the anode to a resistor. The other end of the resistor is connected to ANLG COMMON or ground. For the recommended operating conditions, the resistor value is 100 k Ω . This value may be changed to correct any rollover error that has not been corrected. In many noncritical applications the resistor and diode are not needed.

maximum clock frequency

For most dual-slope A/D converters, the maximum conversion rate is limited by the frequency response of the comparator. In this circuit, the comparator follows the integrator ramp with a 3- μ s delay. Therefore, with a 160-kHz clock frequency (6- μ s period), half of the first reference integrate clock period is lost in delay. Hence, the meter reading changes from 0 to 1 with a 50- μ V input, 1 to 2 with a 150- μ V input, 2 to 3 with a 250- μ V input, etc. This transition at midpoint is desirable; however, when the clock frequency is increased appreciably above 160 kHz, the instrument flashes 1 on noise peaks even when the input is shorted. The above transition points assume a 2-V input range is equivalent to 20,000 clock cycles.

When the input signal is always of one polarity, comparator delay need not be a limitation. Clock rates of 1 MHz are possible since nonlinearity and noise do not increase substantially with frequency. For a fixed clock frequency, the extra count or counts caused by comparator delay are a constant and can be subtracted out digitally.

ICL7135C, TLC7135C
4 1/2-DIGIT PRECISION
ANALOG-TO-DIGITAL CONVERTERS
SLAS074A – DECEMBER 1986 – REVISED MAY 1995

PRINCIPLES OF OPERATION

maximum clock frequency (continued)

For signals with both polarities, the clock frequency can be extended above 160 kHz without error by using a low value resistor in series with the integrating capacitor. This resistor causes the integrator to jump slightly towards the zero-crossing level at the beginning of the deintegrate phase, and thus compensates for the comparator delay. This series resistor should be 10 Ω to 50 Ω . This approach allows clock frequencies up to 480 kHz.

minimum clock frequency

The minimum clock frequency limitations result from capacitor leakage from the auto-zero and reference capacitors. Measurement cycles as high as 10 μ s are not influenced by leakage error.

rejection of 50-Hz or 60-Hz pickup

To maximize the rejection of 50-Hz or 60-Hz pickup, the clock frequency should be chosen so that an integral multiple of 50-Hz or 60-Hz periods occur during the signal integrate phase. To achieve rejection of these signals, some clock frequencies that can be used are:

50 Hz: 250, 166.66, 125, 100 kHz, etc.

60 Hz: 300, 200, 150, 120, 100, 40, 33.33 kHz, etc.

zero-crossing flip-flop

This flip-flop interrogates the comparator's zero-crossing status. The interrogation is performed after the previous clock cycle and the positive half of the ongoing clock cycle has occurred, so any comparator transients that result from the clock pulses do not affect the detection of a zero-crossing. This procedure delays the zero-crossing detection by one clock cycle. To eliminate the inaccuracy, which is caused by this delay, the counter is disabled for one clock cycle at the beginning of the deintegrate phase. Therefore, when the zero-crossing is detected one clock cycle later than the zero-crossing actually occurs, the correct number of counts is displayed.

noise

The peak-to-peak noise around zero is approximately 15 μ V (peak-to-peak value not exceeded 95% of the time). Near full scale, this value increases to approximately 30 μ V. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

analog and digital grounds

For high-accuracy applications, ground loops must be avoided. Return currents from digital circuits must not be sent to the analog ground line.

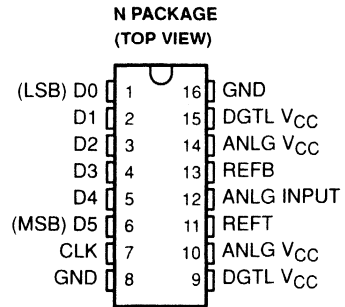
power supplies

The ICL7135C and TLC7135C are designed to work with \pm 5-V power supplies. However, 5-V operation is possible when the input signal does not vary more than \pm 1.5 V from midsupply.

TL5501 6-BIT ANALOG-TO-DIGITAL CONVERTER

SLAS026 – OCTOBER 1989 – REVISED APRIL 1990

- **6-Bit Resolution**
- **Linearity Error . . . $\pm 0.8\%$**
- **Maximum Conversion Rate . . . 30 MHz Typ**
- **Analog Input Voltage Range**
 V_{CC} to $V_{CC} - 2\text{ V}$
- **Analog Input Dynamic Range . . . 1 V**
- **TTL Digital I/O Level**
- **Low Power Consumption**
200 mW Typ
- **5-V Single-Supply Operation**
- **Interchangeable With Fujitsu MB40576**

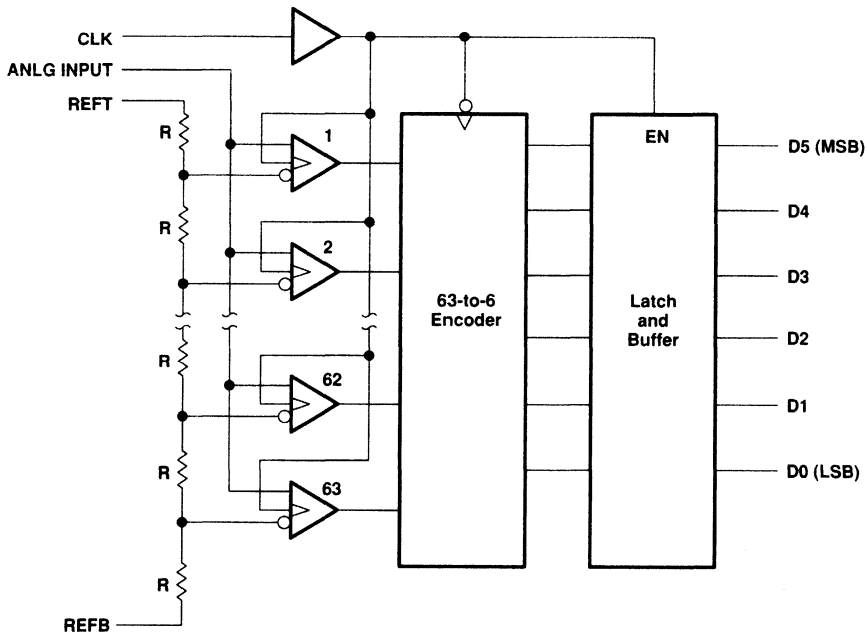


description

The TL5501 is a low-power ultra-high-speed video-band analog-to-digital converter that uses the Advanced Low-Power Schottky (ALS) process. It utilizes the full-parallel comparison (flash method) for high-speed conversion. It converts wide-band analog signals (such as a video signal) to a digital signal at a sampling rate of dc to 30 MHz. Because of this high-speed capability, the TL5501 is suitable for digital video applications such as digital TV, video processing with a computer, or radar signal processing.

The TL5501 is characterized for operation from 0°C to 70°C.

functional block diagram



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

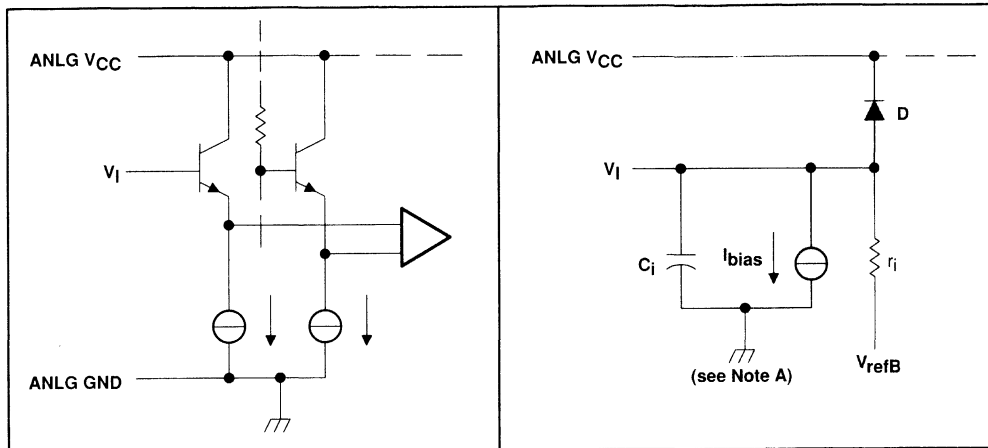

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TL5501 6-BIT ANALOG-TO-DIGITAL CONVERTER

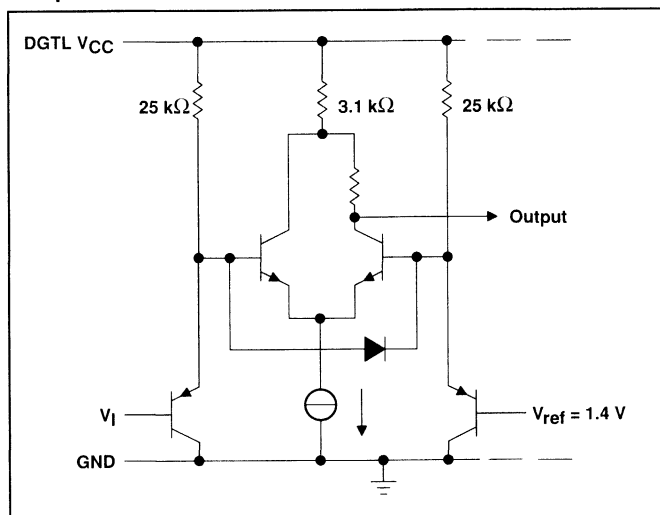
SLAS026 – OCTOBER 1989 – REVISED APRIL 1990

equivalents of analog input circuit



NOTE A: C_i – nonlinear emitter-follower junction capacitance
 r_i – linear resistance model for input current transition caused by comparator switching.
 V_I < V_{refB}: Infinite; CLK high: infinite.
 V_{refB} – voltage at REFB terminal
 I_{bias} – constant input bias current
 D – base-collector junction diode of emitter-follower transistor

equivalent of digital input circuit



TL5501 6-BIT ANALOG-TO-DIGITAL CONVERTER

SLAS026 – OCTOBER 1989 – REVISED APRIL 1990

FUNCTION TABLE

STEP	ANALOG INPUT VOLTAGE	DIGITAL OUTPUT CODE					
0	3.992 V	L	L	L	L	L	L
1	4.008 V	L	L	L	L	L	H
31	4.488 V	L	H	H	H	H	H
32	4.508 V	H	L	L	L	L	L
33	4.520 V	H	L	L	L	L	H
62	4.984 V	H	H	H	H	H	L
63	5.000 V	H	H	H	H	H	H

† These values are based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 4.000 V and the transition to full scale (V_{FT}) is 4.992 V. 1 LSB = 16 mV.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, ANLG V_{CC} (see Note 1)	–0.5 V to 7 V
Supply voltage range, DGTL V_{CC}	–0.5 V to 7 V
Input voltage range at digital input, V_I	–0.5 V to 7 V
Input voltage range at analog input, V_I	–0.5 V to ANLG $V_{CC} + 0.5$ V
Analog reference voltage range, V_{ref}	–0.5 V to ANLG $V_{CC} + 0.5$ V
Storage temperature range	–55°C to 150°C
Operating free-air temperature range	0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, ANLG V_{CC}	4.75	5	5.25	V
Supply voltage, DGTL V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Input voltage at analog input, V_I (see Note 2)	4		5	V
Analog reference voltage (top side), V_{refT} (see Note 2)	4	5	5.1	V
Analog reference voltage (bottom side), V_{refB} (see Note 2)	3	4	4.1	V
High-level output current, I_{OH}	–400			μA
Low-level output current, I_{OL}			4	mA
Clock pulse duration, high-level or low-level, t_w	25			ns
Operating free-air temperature, T_A	0		70	°C

NOTE 2: $V_{refB} < V_I < V_{refT}$. $V_{refT} - V_{refB} = 1 \text{ V} \pm 0.1 \text{ V}$.



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TL5501

6-BIT ANALOG-TO-DIGITAL CONVERTER

SLAS026 – OCTOBER 1989 – REVISED APRIL 1990

electrical characteristics over operating supply voltage range, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

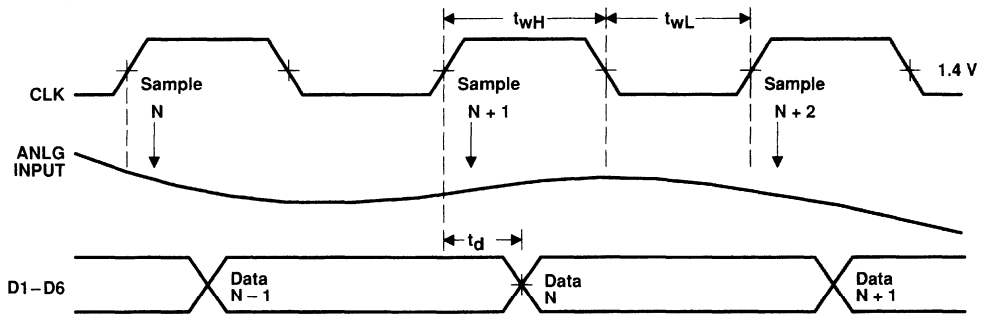
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I Analog input current	$V_I = 5\text{ V}$			75	μA
	$V_I = 4\text{ V}$			73	μA
I_{IH} Digital high-level input current	$V_I = 2.7\text{ V}$		0	20	μA
I_{IL} Digital low-level input current	$V_I = 0.4\text{ V}$	-400	-40		μA
I_I Digital input current	$V_I = 7\text{ V}$			100	μA
I_{refB} Reference current	$V_{\text{refB}} = 4\text{ V}$		-4	-7.2	mA
I_{refT} Reference current	$V_{\text{refB}} = 5\text{ V}$		4	7.2	mA
V_{OH} High-level output voltage	$I_{OH} = -400\ \mu\text{A}$	2.7			V
V_{OL} Low-level output voltage	$I_{OL} = 1.6\ \text{mA}$			0.4	V
r_i Analog input resistance		100			$\text{k}\Omega$
$1C_i$ Analog input capacitance			35	65	pF
I_{CC} Supply current			40	60	mA

operating characteristics over operating supply voltage range, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L Linearity error				± 0.8	%FSR
f_{max} Maximum conversion rate		20	30		MHz
t_d Digital output delay time	See Figure 3		15	30	ns

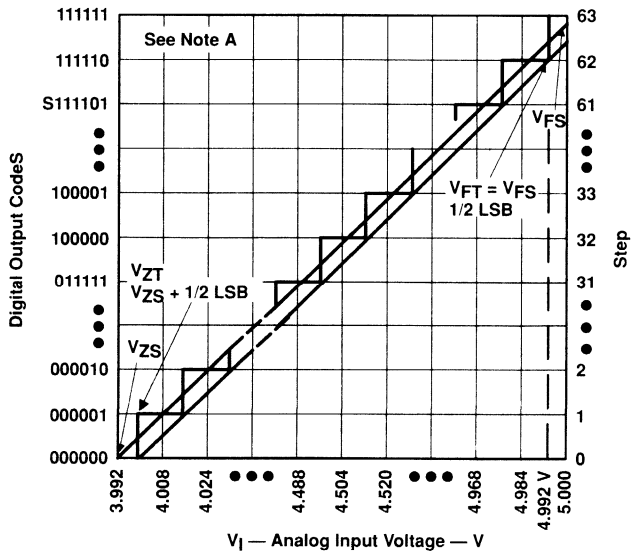
† All typical values are at $V_{CC} = 5\text{ V}$, $V_{\text{ref}} = 4\text{ V}$, $T_A = 25^\circ\text{C}$.

timing diagram



TYPICAL CHARACTERISTICS

IDEAL CONVERSION CHARACTERISTICS



NOTE A: This curve is based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 4.000 V and the transition to full scale (V_{FT}) is 4.992 V. 1 LSB = 16 mV.

Figure 1

END-POINT LINEARITY ERROR

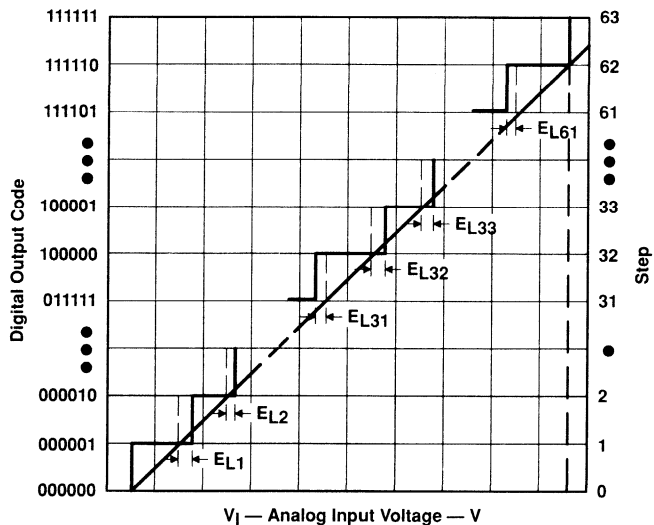


Figure 2

TL5501 6-BIT ANALOG-TO-DIGITAL CONVERTER

SLAS026 – OCTOBER 1989 – REVISED APRIL 1990

PARAMETER MEASUREMENT INFORMATION

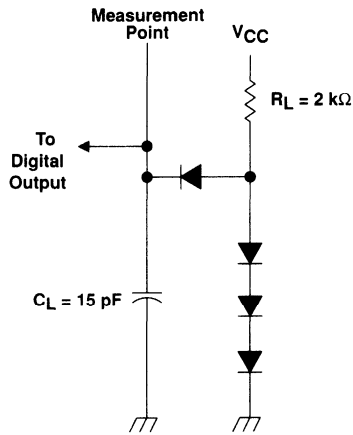


Figure 3. Load Circuit

TLC540I, TLC541I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 INPUTS

SLAS065A – OCTOBER 1983 – REVISED MARCH 1995

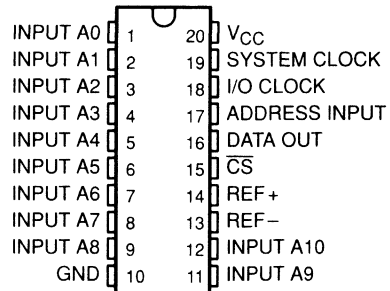
- **8-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **On-Chip 12-Channel Analog Multiplexer**
- **Built-in Self-Test Mode**
- **Software-Controllable Sample and Hold**
- **Total Unadjusted Error . . . ± 0.5 LSB Max**
- **TLC541 is Direct Replacement for Motorola MC145040 and National Semiconductor ADC0811. TLC540 is Capable of Higher Speed**
- **Pinout and Control Signals Compatible with TLC1540 Family of 10-Bit A/D Converters**
- **CMOS Technology**

PARAMETER	TLC540	TLC541
Channel Acquisition Sample Time	2 μ s	3.6 μ s
Conversion Time (Max)	9 μ s	17 μ s
Samples per Second (Max)	75 x 10 ³	40 x 10 ³
Power Dissipation (Max)	12.5 mW	12.5 mW

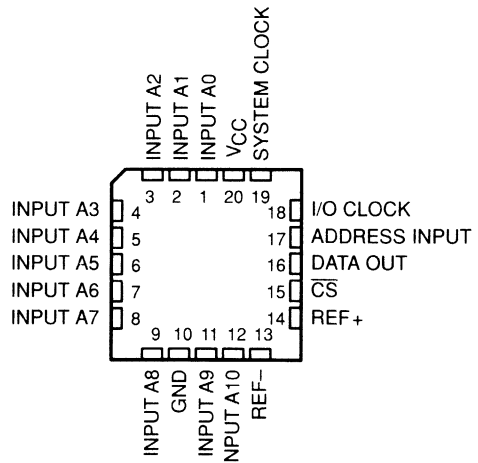
description

The TLC540 and TLC541 are CMOS A/D converters built around an 8-bit switched-capacitor successive-approximation A/D converters. They are designed for serial interface to a microprocessor or peripheral via a 3-state output with up to four control inputs, including independent SYSTEM CLOCK, I/O CLOCK, chip select (\overline{CS}), and ADDRESS INPUT. A 4-MHz system clock for the TLC540 and a 2.1-MHz system clock for the TLC541 with a design that includes simultaneous read/write operation allow high-speed data transfers and sample rates of up to 75,180 samples per second for the TLC540 and 40,000 samples per second for the TLC541. In addition to the high-speed converter and versatile control logic, there is an on-chip 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal self-test voltage, and a sample-and-hold that can operate automatically or under microprocessor control. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T _A	PACKAGE		
	SO PLASTIC DIP (DW)	PLASTIC DIP (N)	CHIP CARRIER (FN)
-40°C to 85°C	— TLC5411DW	TLC540IN TLC541IN	TLC540IFN TLC541IFN
-55°C to 125°C	—	TLC541MN	—

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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TLC540I, TLC541I

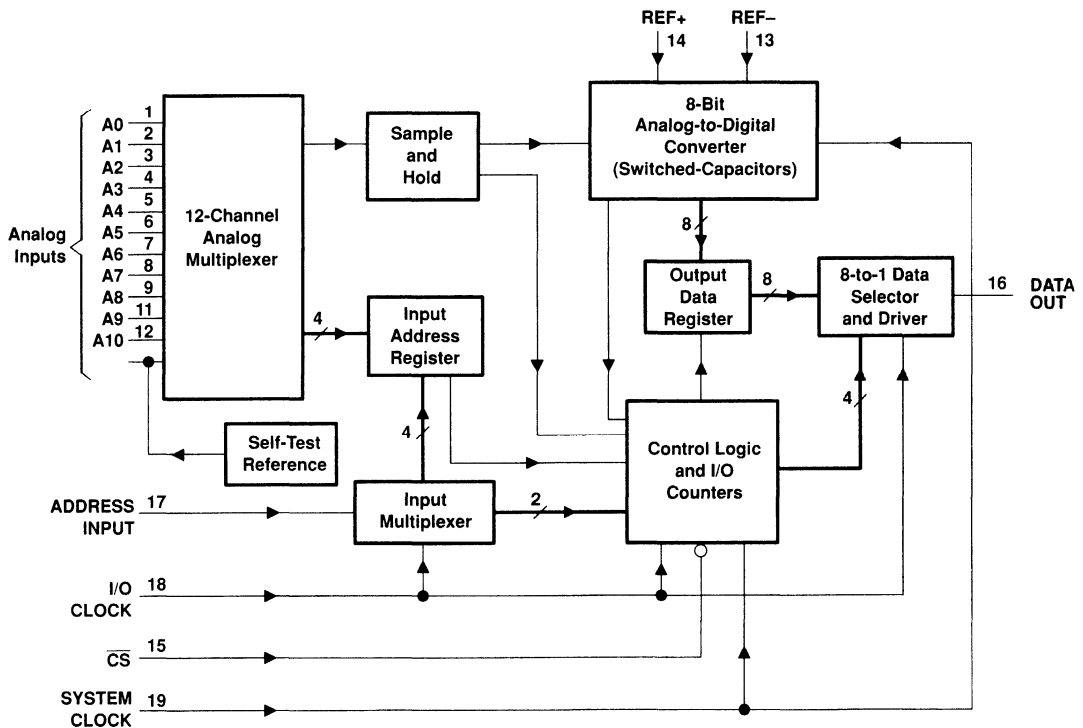
8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 INPUTS

SLAS065A – OCTOBER 1983 – REVISED MARCH 1995

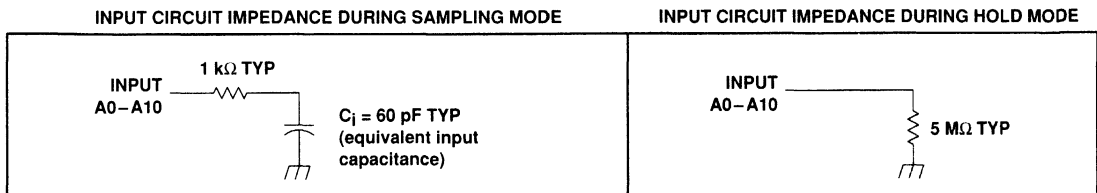
The converters incorporated in the TLC540 and TLC541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A switched-capacitor design allows low-error (± 0.5 LSB) conversion in $9 \mu\text{s}$ for the TLC540 and $17 \mu\text{s}$ for the TLC541 over the full operating temperature range.

The TLC540I and TLC541I are characterized for operation from -40°C to 85°C . The TLC541M is characterized for operation from -55°C to 125°C .

functional block diagram



typical equivalent inputs

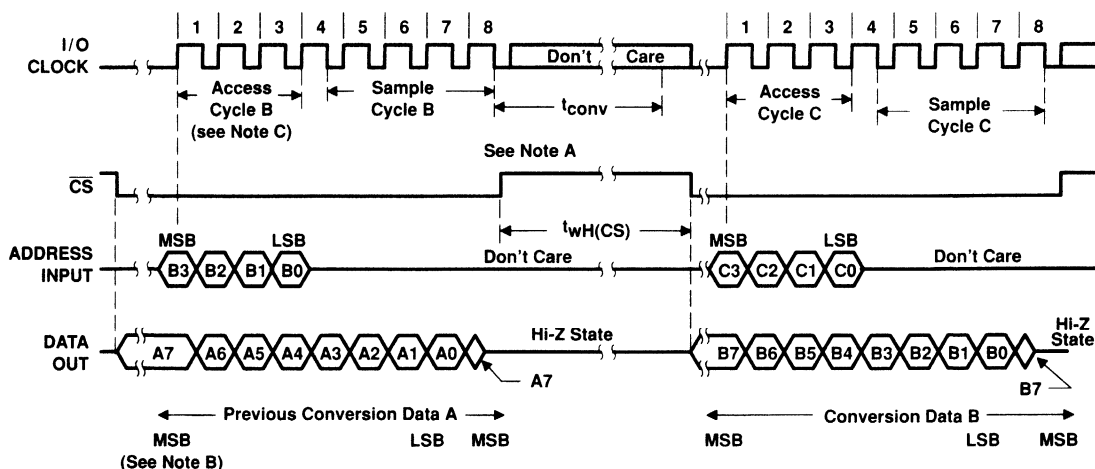


TLC5401, TLC5411

8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 INPUTS

SLAS065A – OCTOBER 1983 – REVISED MARCH 1995

operating sequence



- NOTES: B. The conversion cycle, which requires 36 system clock periods, is initiated on the 8th falling edge of I/O CLOCK after \overline{CS} goes low for the channel whose address exists in memory at that time. If \overline{CS} is kept low during conversion, I/O CLOCK must remain low for at least 36 system clock cycles to allow conversion to be completed.
- C. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after \overline{CS} is brought low. The remaining seven bits (A6–A0) will be clocked out on the first seven I/O CLOCK falling edges.
- D. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range, V_I (any input)	–0.3 V to $V_{CC} + 0.3$ V
Output voltage range, V_O	–0.3 V to $V_{CC} + 0.3$ V
Peak input current range (any input)	± 10 mA
Peak total input current (all inputs)	± 30 mA
Operating free-air temperature range, T_A : TLC5401, TLC5411	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF– and GND wired together (unless otherwise noted).



TLC540I, TLC541I

8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 INPUTS

SLAS065A – OCTOBER 1983 – REVISED MARCH 1995

recommended operating conditions

	TLC540			TLC541			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)	2.5	V_{CC}	$V_{CC}+0.1$	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{ref-} (see Note 2)	-0.1	0	2.5	-0.1	0	2.5	V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)	1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)	0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}	2			2			V
Low-level control input voltage, V_{IL}			0.8			0.8	V
Setup time, address bits at data input before I/O CLOCK \uparrow , $t_{su}(A)$	200			400			ns
Hold time, address bits after I/O CLOCK \uparrow , $t_h(A)$	0			0			ns
Setup time, \overline{CS} low before clocking in first address bit, $t_{su}(CS)$ (see Note 3)	3			3			System clock cycles
\overline{CS} high during conversion, $t_{WH}(CS)$	36			36			System clock cycles
I/O CLOCK frequency, $f_{clock}(I/O)$	0		2,048	0		1.1	MHz
Pulse duration, SYSTEM CLOCK frequency, $f_{clock}(SYS)$	$f_{clock}(I/O)$		4	$f_{clock}(I/O)$		2.1	MHz
Pulse duration, SYSTEM CLOCK high, $t_{WH}(SYS)$	110			210			MHz
Pulse duration, SYSTEM CLOCK low, $t_{WL}(SYS)$	100			190			MHz
Pulse duration, I/O clock high, $t_{WH}(I/O)$	200			404			ns
Pulse duration, I/O clock low, $t_{WL}(I/O)$	200			404			ns
Clock transition time (see Note 4)	System	$f_{clock}(SYS) \leq 1048$ kHz		30		30	ns
		$f_{clock}(SYS) > 1048$ kHz		20		20	
	I/O	$f_{clock}(I/O) \leq 525$ kHz		100		100	
		$f_{clock}(I/O) > 525$ kHz		40		40	
Operating free-air temperature, T_A	TLC540I, TLC541I		-40		85		°C

NOTES: 2. Analog input voltages greater than that applied to REF + convert as all "1"s (11111111), while input voltages less than that applied to REF- convert as all "0"s (00000000). For proper operation, REF+ voltage must be at least 1 V higher than REF- voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

3. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for three SYSTEM CLOCK cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum chip select setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μ s for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.



TLC540I, TLC541I
8-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 INPUTS

SLAS065A – OCTOBER 1983 – REVISED MARCH 1995

electrical characteristics over recommended operating temperature range, $V_{CC} = V_{ref+} = 4.75$ V to 5.5 V, $f_{clock(I/O)} = 2.048$ MHz for TLC540 or $f_{clock(I/O)} = 1.1$ MHz for TLC541 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage, DATA OUT	$V_{CC} = 4.75$ V, $I_{OH} = 360$ μ A	2.4			V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75$ V, $I_{OL} = 1.6$ mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current	$V_O = V_{CC}$, \overline{CS} at V_{CC}			10	μ A
		$V_O = 0$, \overline{CS} at V_{CC}			-10	
I_{IH}	High-level input current	$V_I = V_{CC}$		0.005	2.5	μ A
I_{IL}	Low-level input current	$V_I = 0$		-0.005	-2.5	μ A
I_{CC}	Operating supply current	\overline{CS} at 0 V		1.2	2.5	mA
Selected channel leakage current		Selected channel at V_{CC} , Unselected channel at 0 V		0.4	1	μ A
		Selected channel at 0 V, Unselected channel at V_{CC}		-0.4	-1	
$I_{CC} + I_{ref}$	Supply and reference current	$V_{ref+} = V_{CC}$, \overline{CS} at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs		7	55	pF
		Control inputs		5	15	

† All typical values are at $T_A = 25^\circ\text{C}$.

TLC540I, TLC541I

8-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH SERIAL CONTROL AND 11 INPUTS

SLAS065A – OCTOBER 1983 – REVISED MARCH 1995

operating characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} - 4.75\text{ V to } 5.5\text{ V}$, $f_{clock(I/O)} = 2.048\text{ MHz for TLC540 or } 1.1\text{ MHz for TLC541}$,
 $f_{clock(SYS)} = 4\text{ MHz for TLC540 or } 2.1\text{ MHz for TLC541}$

PARAMETER	TEST CONDITIONS	TLC540		TLC541		UNIT
		MIN	MAX	MIN	MAX	
E_L Linearity error	See Note 5		±0.5		±0.5	LSB
E_{ZS} Zero-scale error	See Notes 2 and 6		±0.5		±0.5	LSB
E_{FS} Full-scale error	See Notes 2 and 6		±0.5		±0.5	LSB
Total unadjusted error	See Note 7		±0.5		±0.5	LSB
Self-test output code	Input A11 address = 1011, (see Note 8)	01111101 (125)	10000011 (131)	01111101 (125)	10000011 (131)	
t_{conv} Conversion time	See Operating Sequence		9		17	μs
Total access and conversion time	See Operating Sequence		13.3		25	μs
t_a Channel acquisition time (sample cycle)	See Operating Sequence		4		4	I/O clock cycles
t_v Time output data remains valid after I/O CLOCK↓		10		10		ns
t_d Delay time, I/O CLOCK↓ to data output valid	See Parameter Measurement Information		300		400	ns
t_{en} Output enable time			150		150	ns
t_{dis} Output disable time			150		150	ns
$t_r(\text{bus})$ Data bus rise time			300		300	ns
$t_f(\text{bus})$ Data bus fall time			300		300	ns

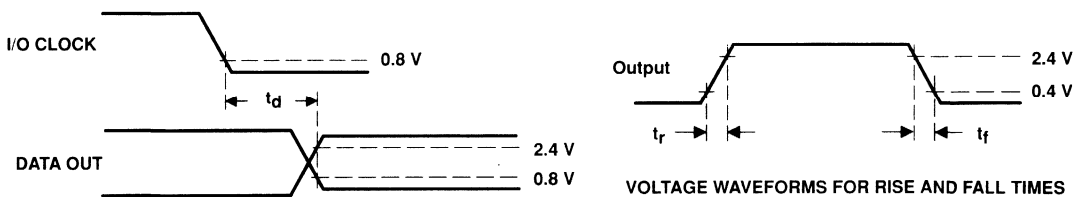
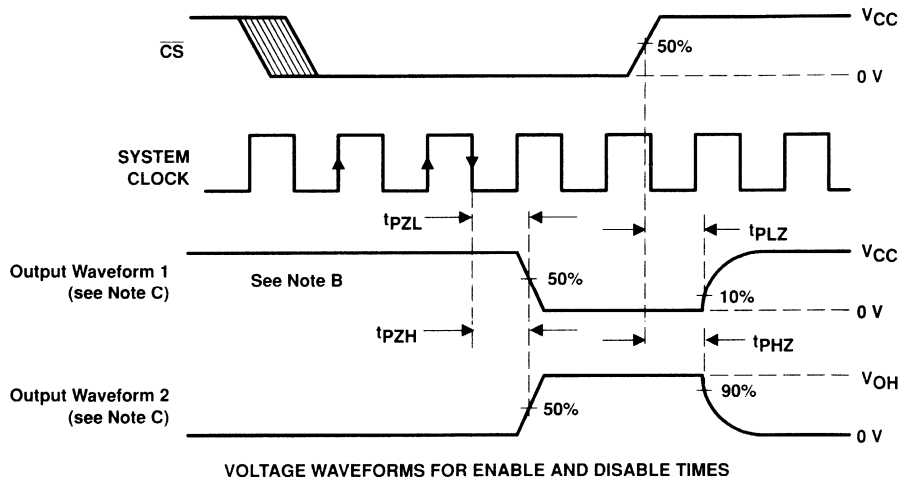
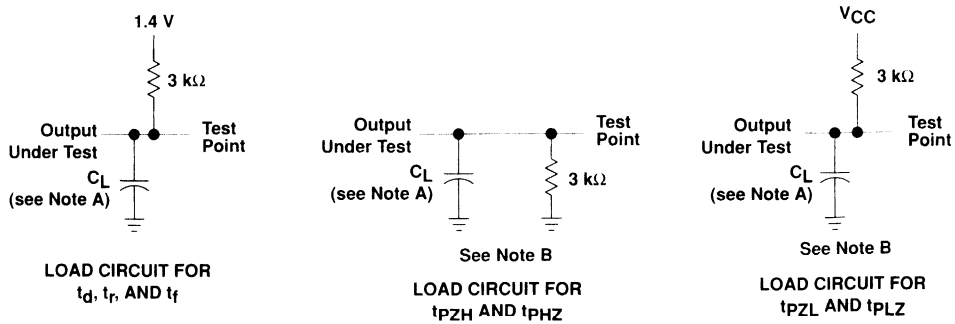
- NOTES:
- Analog input voltages greater than that applied to REF+ convert to all "1"s (11111111) while input voltages less than that applied to REF- convert to all "0"s (00000000). For proper operation, REF+ voltage must be at least 1 V higher than REF- voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.
 - Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
 - Zero-scale error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
 - Total unadjusted error is the sum of linearity, zero-scale, and full-scale errors.
 - Both the input address and the output codes are expressed in positive logic.



TLC540I, TLC541I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 INPUTS

SLAS065A – OCTOBER 1983 – REVISED MARCH 1995

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS FOR DELAY TIME

- NOTES: A. $C_L = 50$ pF for TLC540 and 100 pF for TLC541.
 B. $t_{en} = t_{pZH}$ or t_{pZL} . $t_{dis} = t_{pHZ}$ or t_{pLZ} .
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

TLC540I, TLC541I
8-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 INPUTS

SLAS065A – OCTOBER 1983 – REVISED MARCH 1995

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 1, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c / R_t C_i} \right) \quad (1)$$

where

$$R_t = R_s + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S/512) \quad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S/512) = V_S \left(1 - e^{-t_c / R_t C_i} \right) \quad (3)$$

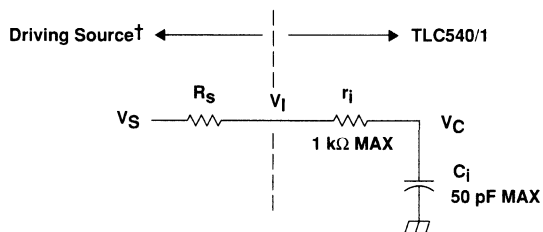
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(512) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_s + 1 \text{ k}\Omega) \times 60 \text{ pF} \times \ln(512) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at INPUT A0–A10
 V_S = External Driving Source Voltage
 R_S = Source Resistance
 r_i = Input Resistance
 C_i = Equivalent Input Capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 1. Equivalent Input Circuit Including the Driving Source

TLC540I, TLC541I

8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 INPUTS

SLAS065A – OCTOBER 1983 – REVISED MARCH 1995

PRINCIPLES OF OPERATION

The TLC540 and TLC541 are each complete data acquisition systems on a single chip. They include such functions as analog multiplexer, sample and hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs [two clocks, chip select (\overline{CS}), and address]. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. With judicious interface timing, with TLC540 a conversion can be completed in 9 μ s, while complete input-conversion-output cycles can be repeated every 13 μ s. With TLC541 a conversion can be completed in 17 μ s, while complete input-conversion-output cycles are repeated every 25 μ s. Furthermore, this fast conversion can be executed on any of 11 inputs or its built-in self-test and in any order desired by the controlling processor.

The system and I/O clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to SYSTEM CLOCK, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using I/O CLOCK. SYSTEM CLOCK will drive the conversion crunching circuitry so that the control hardware and software need not be concerned with this task.

When \overline{CS} is high, DATA OUT is in a 3-state condition and ADDRESS INPUT and I/O CLOCK are disabled. This feature allows each of these terminals, with the exception of \overline{CS} , to share a control logic point with their counterpart terminals on additional A/D devices when additional TLC540/541 devices are used. In this way, the above feature serves to minimize the required control logic terminals when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. \overline{CS} is brought low. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for two rising edges and then a falling edge of SYSTEM CLOCK after a low \overline{CS} transition, before the low transition is recognized. This technique is used to protect the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result automatically appears on DATA OUT.
2. A new positive-logic multiplexer address is shifted in on the first four rising edges of I/O CLOCK. The MSB of the address is shifted in first. The negative edges of these four I/O clock pulses shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample and hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three clock cycles are then applied to I/O CLOCK and the sixth, seventh, and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to I/O CLOCK. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 system clock cycles. After this final I/O clock cycle, \overline{CS} must go high or the I/O CLOCK must remain low for at least 36 system clock cycles to allow for the conversion function.

\overline{CS} can be kept low during periods of multiple conversion. When keeping \overline{CS} low during periods of multiple conversion, special care must be exercised to prevent noise glitches on I/O CLOCK. If glitches occur on I/O CLOCK, the I/O sequence between the microprocessor/controller and the device loses synchronization. Also, if \overline{CS} is taken high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of \overline{CS} causes a reset condition, which aborts the conversion in progress.

A new conversion can be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 system clock cycles occur. Such action yields the conversion result of the previous conversion and not the ongoing conversion.



TLC540I, TLC541I

8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 INPUTS

SLAS065A - OCTOBER 1983 - REVISED MARCH 1995

PRINCIPLES OF OPERATION

It is possible to connect SYSTEM CLOCK and I/O clock together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. The first two clocks are required for this device to recognize \overline{CS} is at a valid low level when the common clock signal is used as an I/O CLOCK. When \overline{CS} is recognized by the device to be at a high level, the common clock signal is used for the conversion clock also.
2. A low \overline{CS} must be recognized before the I/O CLOCK can shift in an analog channel address. The device recognizes a \overline{CS} transition when the SYSTEM CLOCK terminal receives two positive edges and then a negative edge. For this reason, after a \overline{CS} negative edge, the first two clock cycles do not shift in the address. Also, upon shifting in the address, \overline{CS} must be raised after the eighth valid (10 total) I/O CLOCK. Otherwise, additional common clock cycles are recognized as I/O CLOCKS and will shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device accommodates these applications. Although the on-chip sample and hold begins sampling upon the negative edge of the fourth valid I/O clock cycle, the hold function is not initiated until the negative edge of the eighth valid I/O clock cycle. Thus, the control circuitry can leave the I/O clock signal in its high state during the eighth valid I/O clock cycle until the moment at which the analog signal must be converted. The TLC540/TLC541 continues sampling the analog input until the eighth falling edge of the I/O clock. The control circuitry or software then immediately lowers the I/O clock signal and holds the analog signal at the desired point in time and start conversion.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.



TLC542C, TLC542I

8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 INPUTS

SLAS075A – FEBRUARY 1989 – REVISED MARCH 1995

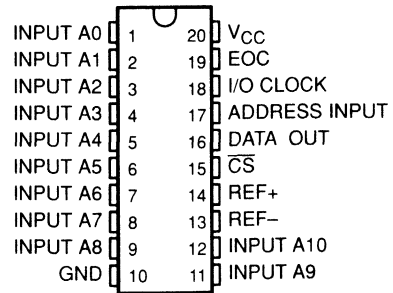
- 8-Bit Resolution A/D Converter
- Microprocessor Peripheral or Stand-Alone Operation
- On-Chip 12-Channel Analog Multiplexer
- Built-in Self-Test Mode
- Software-Controllable Sample and Hold
- Total Unadjusted Error . . . ± 0.5 LSB Max
- Direct Replacement for Motorola MC145041
- On-Board System Clock
- End-of-Conversion (EOC) Output
- Pinout and Control Signals Compatible With the TLC1542/3 10-Bit A/D Converters
- CMOS Technology

PARAMETER	VALUE
Channel Acquisition/Sample Time	16 μ s
Conversion Time (Max)	20 μ s
Samples per Second (Max)	25×10^3
Power Dissipation (Max)	10 mW

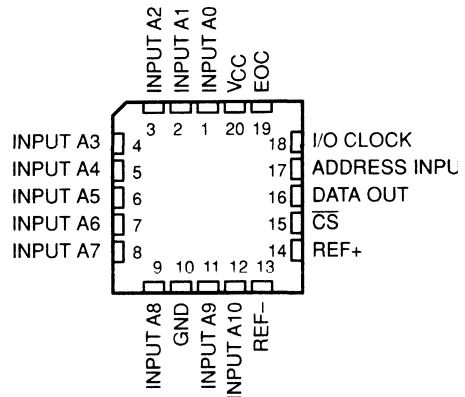
description

The TLC542 is a CMOS converter built around an 8-bit switched-capacitor successive-approximation analog-to-digital converter. The device is designed for serial interface to a microprocessor or peripheral via a 3-state output with three inputs [including I/O CLOCK, \overline{CS} (chip select), and ADDRESS INPUT]. The TLC542 allows high-speed data transfers and sample rates of up to 40,000 samples per second. In addition to the high-speed converter and versatile control logic, an on-chip 12-channel analog multiplexer can sample any one of 11 inputs or an internal "self-test" voltage, and the sample and hold is started under microprocessor control. At the end of conversion, the end-of-conversion (EOC) output pin goes high to indicate that conversion is complete. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T _A	PACKAGE		
	CHIP CARRIER (FN)	PLASTIC DIP (N)	SMALL OUTLINE (DW)
0°C to 70°C	—	TLC542CN	TLC542CDW
-40°C to 85°C	TLC542IFN	TLC542IN	TLC542IDW

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TLC542C, TLC542I

8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 INPUTS

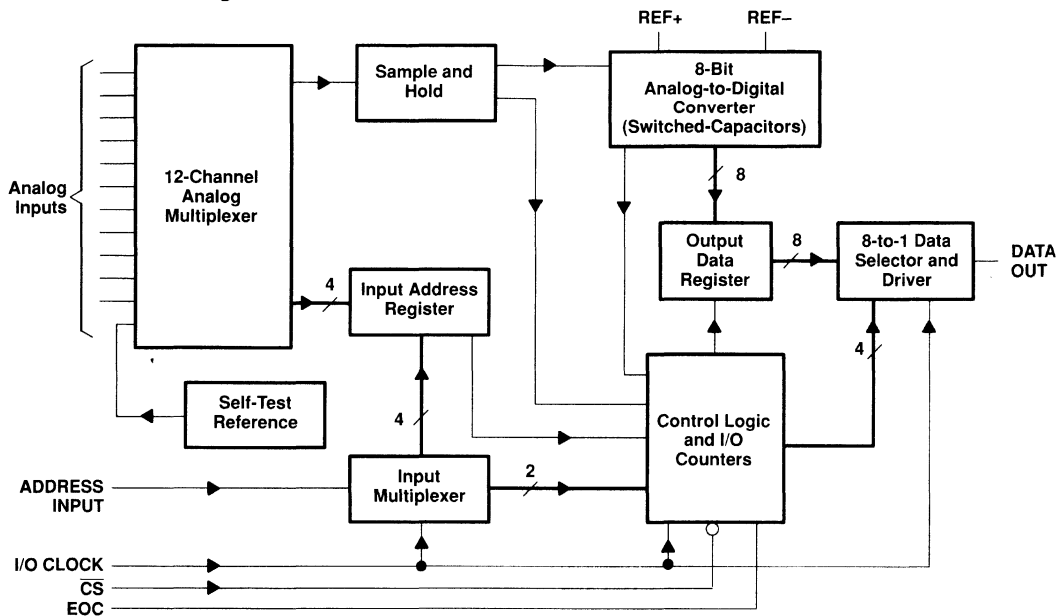
SLAS075A - FEBRUARY 1989 - REVISED MARCH 1995

description (continued)

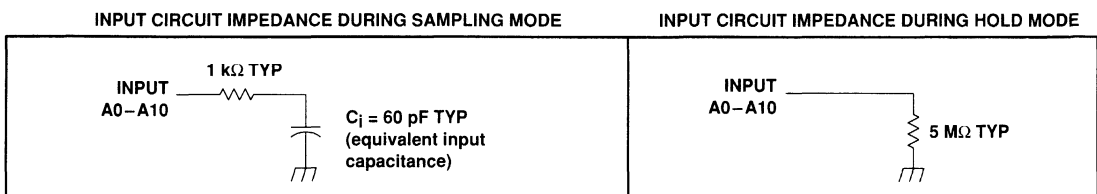
The converter incorporated in the TLC542 features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noises. A switched-capacitor design allows low-error (± 0.5 LSB) conversion in $20 \mu\text{s}$ over the full operating temperature range.

The TLC542C is characterized for operation from 0°C to 70°C and the TLC542I is characterized for operation from -40°C to 85°C .

functional block diagram



typical equivalent inputs

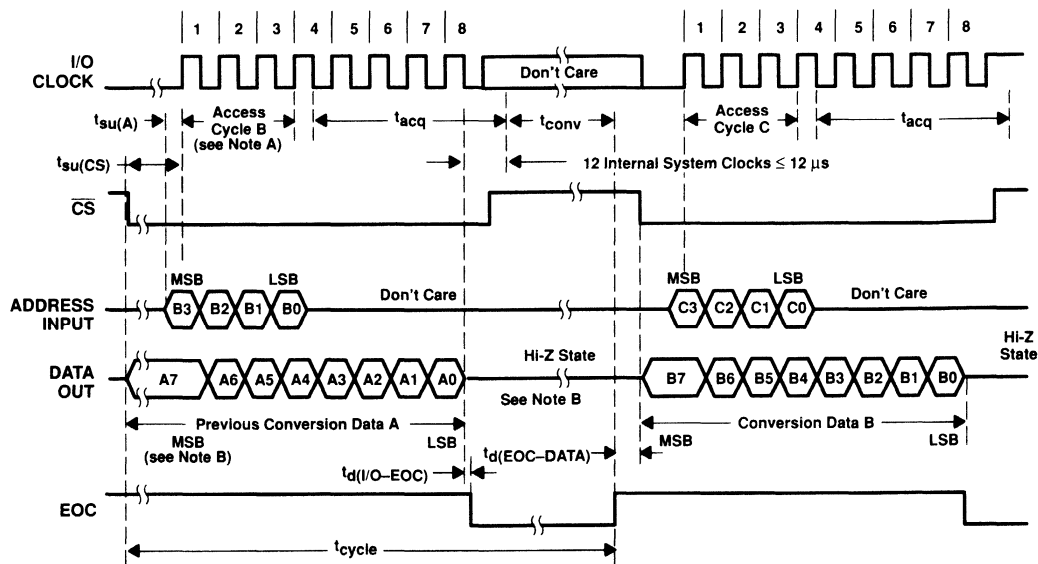


TLC542C, TLC542I

8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 INPUTS

SLAS075A – FEBRUARY 1989 – REVISED MARCH 1995

operating sequence



- NOTES: D. To minimize errors caused by noise at the chip select input, the internal circuitry waits for two rising edges and one falling edge of the internal system clock after \overline{CS} before responding to control input signals. The \overline{CS} setup time is given by the $t_{su}(\overline{CS})$ specifications. Therefore, no attempt should be made to clock-in an address until the minimum chip select setup time has elapsed.
- E. The output is 3-stated on \overline{CS} going high or on the negative edge of the eighth I/O clock.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range (any input)	-0.3 V to $V_{CC} + 0.3$ V
Output voltage range	-0.3 V to $V_{CC} + 0.3$ V
Peak input current range (any input)	± 20 mA
Peak total input current (all inputs)	± 30 mA
Operating free-air temperature range: TLC542C	0°C to 70°C
TLC542I	-40°C to 85°C
Storage temperature range	-65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF- and GND wired together (unless otherwise noted).



TLC542C, TLC542I

8-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH SERIAL CONTROL AND 11 INPUTS

SLAS075A – FEBRUARY 1989 – REVISED MARCH 1995

recommended operating conditions, $V_{CC} = 4.75$ to 5.5 V

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)	V_{ref-}	V_{CC}	$V_{CC} + 0.1$	V
Negative reference voltage, V_{ref-} (see Note 2)	-0.1	0	V_{ref+}	V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)	1	V_{CC}	$V_{CC} + 0.2$	V
Analog input voltage (see Note 3)	0		V_{CC}	V
High-level control input voltage, V_{IH}	2			V
Low-level control input voltage, V_{IL}			0.8	V
Setup time, address bits at data input before I/O CLOCK \uparrow , $t_{su}(A)$	400			ns
Hold time, address bits after I/O CLOCK \uparrow , $t_h(A)$	0			ns
Hold time, \overline{CS} low after 8th I/O CLOCK \uparrow , $t_h(\overline{CS})$	0			ns
Setup time, \overline{CS} low before clocking in first address bit, $t_{su}(\overline{CS})$ (see Note 4)	3.8			μ s
Input/output clock frequency, $f_{clock}(I/O)$	0	1.1		MHz
Input/output clock high, $t_{WH}(I/O)$	404			ns
Input/output clock low, $t_{WL}(I/O)$	404			ns
I/O CLOCK transition time, t_t (see Note 3)	$f_{clock}(I/O) \leq 525$ kHz		100	ns
	$f_{clock}(I/O) > 525$ kHz		40	
Operating free-air temperature, T_A	TLC542C	0	70	$^{\circ}$ C
	TLC542I	-40	85	

- NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (11111111), while input voltages less than that applied to REF- convert as all zeros (00000000). For proper operation, REF+ must be at least 1 V higher than REF-. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.
3. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μ s for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.
4. To minimize errors caused by noise at the chip select input, the internal circuitry waits for two rising edges and one falling edge of the internal system clock after $\overline{CS} \downarrow$ before responding to control input signals. The \overline{CS} setup time is given by the $t_{su}(\overline{CS})$ specifications. Therefore, no attempt should be made to clock-in address data until the minimum chip select setup time has elapsed.

electrical characteristics over recommended operating temperature range, $V_{CC} = V_{ref+} = 4.75$ V to 5.5 V, $f_{clock}(I/O) = 1.1$ MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP \dagger	MAX	UNIT
V_{OH}	High-level output voltage (DATA OUT)	$V_{CC} = 4.75$ V,	$I_{OH} = -360$ μ A	2.4			V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75$ V,	$I_{OL} = 1.6$ mA			0.4	V
	Off-state (high-impedance state) output current	$V_O = V_{CC}$,	\overline{CS} at V_{CC}			10	μ A
		$V_O = 0$,	\overline{CS} at V_{CC}			-10	
I_{IH}	High-level input current	$V_I = V_{CC}$			0.005		μ A
I_{IL}	Low-level input current	$V_I = 0$			-0.005	-2.5	μ A
I_{CC}	Operating supply current	\overline{CS} at 0 V			1.2	2	mA
	Selected channel leakage current	Selected at V_{CC} , Unselected channel at 0 V	0 $^{\circ}$ C to 70 $^{\circ}$ C			0.4	μ A
			-40 $^{\circ}$ C to 85 $^{\circ}$ C			-0.4	
I_{ref}	Maximum static analog reference current into REF+	$V_{ref+} = V_{CC}$,	$V_{ref-} = GND$			10	μ A
C_i	Input capacitance	Analog inputs			7	55	pF
		Control inputs			5	15	

\dagger All typical values are at $T_A = 25^{\circ}$ C.



TLC542C, TLC542I
8-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 INPUTS

SLAS075A – FEBRUARY 1989 – REVISED MARCH 1995

operating characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 4.75$ to 5.5 V, $f_{clock(I/O)} = 1$ MHz

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error (see Note 5)			±0.5	LSB
E_{ZS}	Zero-scale error (see Note 6)	See Note 2		±0.5	LSB
E_{FS}	Full-scale error (see Note 6)	See Note 2		±0.5	LSB
	Total unadjusted error (see Note 7)			±0.5	LSB
	Self-test output code	Input A11 address = 1011, See Note 8	01111101 (126) 128	10000011 (130)	
t_{conv}	Conversion time	See operating sequence		20	μs
t_{cycle}	Total access and conversion cycle time	See operating sequence		40	μs
t_{acq}	Channel acquisition time (sample cycle)	See operating sequence		16	μs
t_v	Time output data remains valid after I/O CLK↓	See Figure 5	10		ns
$t_d(I/O-DATA)$	Delay time, I/O CLK↓ to data output valid	See Figure 5		400	ns
$t_d(I/O-EOC)$	Delay time, 8th I/O CLK↓ to EOC↓	See Figure 6		500	ns
$t_d(EOC-DATA)$	Delay time, EOC↑ to data out (MSB)	See Figure 7		400	ns
t_{PZH}, t_{PLZ}	Delay time, CS↓ to data out (MSB)	See Figure 2		3.4	μs
t_{PHZ}, t_{PLZ}	Delay time, CS↑ to data out (MSB)	See Figure 2		150	ns
$t_r(EOC)$	Rise time	See Figure 7		100	ns
$t_f(EOC)$	Fall time	See Figure 6		100	ns
$t_r(bus)$	Data bus rise time	See Figure 5		300	ns
$t_f(bus)$	Data bus fall time	See Figure 5		300	ns

† All typical values are at $T_A = 25^\circ\text{C}$

- NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all ones (11111111), while input voltages less than that applied to REF- convert to all zeros (00000000). For proper operation, REF+ must be at least 1 V higher than REF-. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.
5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero-scale Error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero-scale, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A11 analog input signal is internally generated and is used for test purposes.



TLC542C, TLC542I
8-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 INPUTS

SLAS075A – FEBRUARY 1989 – REVISED MARCH 1995

PARAMETER MEASUREMENT INFORMATION

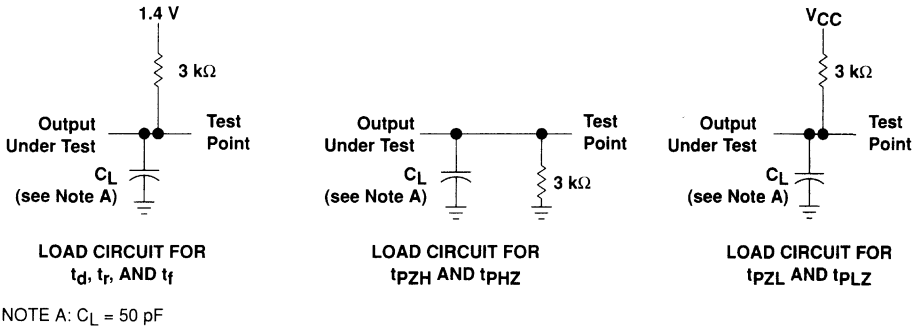


Figure 1. Load Circuits

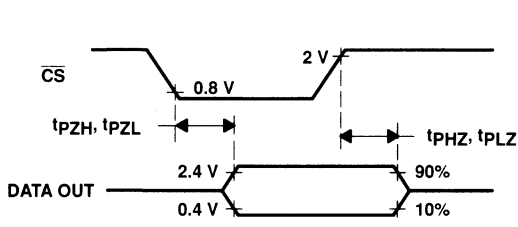


Figure 2. \overline{CS} to Data Output Timing

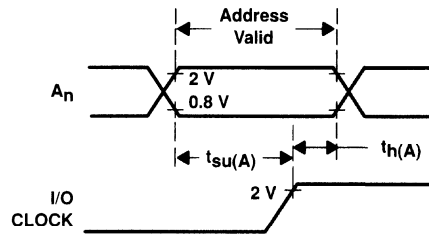


Figure 3. Address Timing

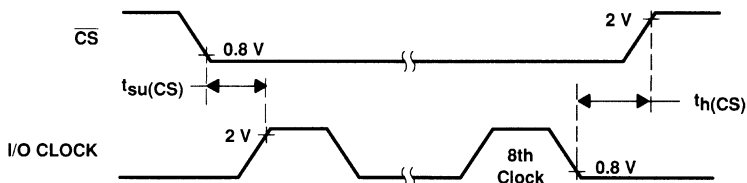


Figure 4. \overline{CS} to I/O CLOCK Timing

PARAMETER MEASUREMENT INFORMATION

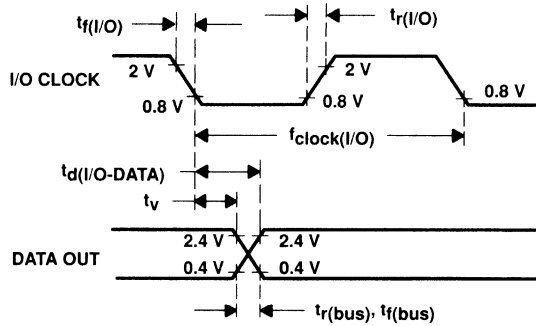


Figure 5. Data Output Timing

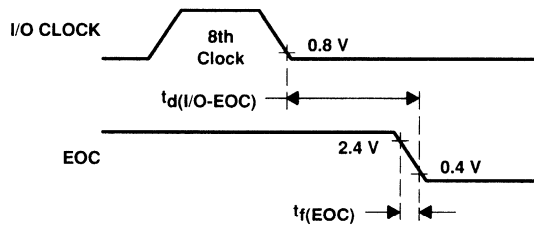


Figure 6. EOC Timing

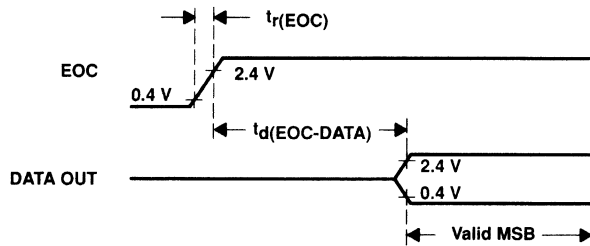


Figure 7. Data Output to EOC Timing

TLC542C, TLC542I
8-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 INPUTS

SLAS075A – FEBRUARY 1989 – REVISED MARCH 1995

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 8, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c/R_t C_i}\right) \quad (1)$$

where

$$R_t = R_s + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S/512) \quad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S/512) = V_S \left(1 - e^{-t_c/R_t C_i}\right) \quad (3)$$

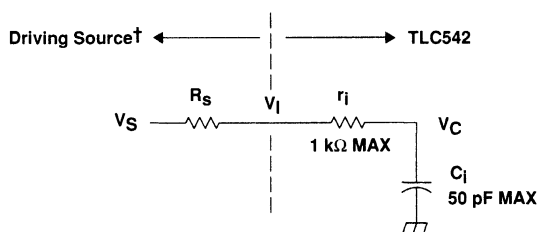
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(512) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_s + 1 \text{ k}\Omega) \times 60 \text{ pF} \times \ln(512) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at INPUT A0–A10
 V_S = External Driving Source Voltage
 R_S = Source Resistance
 r_i = Input Resistance
 C_i = Input Capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 8. Equivalent Input Circuit Including the Driving Source

TLC542C, TLC542I
8-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 INPUTS

SLAS075A – FEBRUARY 1989 – REVISED MARCH 1995

PRINCIPLES OF OPERATION

The TLC542 is a complete data acquisition system on a single chip. The device includes such functions as analog multiplexer, sample and hold, 8-bit A/D converter, data and control registers, and control logic. Three control inputs (I/O CLOCK, \overline{CS} (chip select), and ADDRESS INPUT) are included for flexibility and access speed. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. With judicious interface timing, the TLC542 can complete a conversion in 20 μ s, while complete input-conversion-output cycles can be repeated every 40 μ s. Furthermore, this fast conversion can be executed on any of 11 inputs or its built-in self-test and in any order desired by the controlling processor.

When \overline{CS} is high, the DATA OUT terminal is in a 3-state condition, and the ADDRESS INPUT and I/O CLOCK terminals are disabled. When additional TLC542 devices are used, this feature allows each of these terminals, with the exception of the \overline{CS} terminal, to share a control logic point with their counterpart terminals on additional A/D devices. Thus, this feature minimizes the control logic terminals required when using multiple A/D devices.

The control sequence is designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is as follows:

1. \overline{CS} is brought low. To minimize errors caused by noise at the \overline{CS} input, the internal circuitry waits for two rising edges and then a falling edge of the internal system clock before recognizing the low \overline{CS} transition. The MSB of the result of the previous conversion automatically appears on the DATA OUT terminal.
2. On the first four rising edges of the I/O CLOCK, a new positive-logic multiplexer address is shifted in, with the MSB of this address shifted first. The negative edges of these four I/O CLOCK pulses shift out the second, third, fourth, and fifth most significant bits of the result of the previous conversion. The on-chip sample and hold begins sampling the newly addressed analog input after the fourth falling edge of the I/O CLOCK. The sampling operation basically involves charging the internal capacitors to the level of the analog input voltage.
3. Three clock cycles are applied to the I/O CLOCK terminal and the sixth, seventh, and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to the I/O CLOCK terminal. The falling edge of this clock cycle initiates a 12-system clock ($\approx 12 \mu$ s) additional sampling period while the output is in the high-impedance state. Conversion is then performed during the next 20 μ s. After this final I/O CLOCK cycle, \overline{CS} must go high or the I/O CLOCK must remain low for at least 20 μ s to allow for the conversion function.

\overline{CS} can be kept low during periods of multiple conversion. If \overline{CS} is taken high, it must remain high until the end of conversion. Otherwise, a valid falling edge of \overline{CS} causes a reset condition, which aborts the conversion process.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 20- μ s conversion time has elapsed. Such action yields the conversion result of the previous conversion and not the ongoing conversion.

The end-of-conversion (EOC) output goes low on the negative edge of the eighth I/O CLOCK. The subsequent low-to-high transition of EOC indicates the A/D conversion is complete and the conversion is ready for transfer.



TLC545C, TLC545I, TLC546C, TLC546I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 19 INPUTS

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- 8-Bit Resolution A/D Converter
- Microprocessor Peripheral or Stand-Alone Operation
- On-Chip 20-Channel Analog Multiplexer
- Built-in Self-Test Mode
- Software-Controllable Sample and Hold
- Total Unadjusted Error . . . ± 0.5 LSB Max
- Timing and Control Signals Compatible With 8-Bit TLC540 and 10-Bit TLC1540 A/D Converter Families
- CMOS Technology

PARAMETER	TL545	TL546
Channel Acquisition Time	1.5 μ s	2.7 μ s
Conversion Time (Max)	9 μ s	17 μ s
Sampling Rate (Max)	76 x 10 ³	40 x 10 ³
Power Dissipation (Max)	15 mW	15 mW

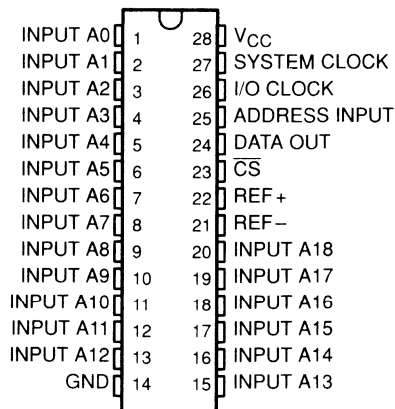
description

The TLC545 and TLC546 are CMOS analog-to-digital converters built around an 8-bit switched capacitor successive-approximation analog-to-digital converter. They are designed for serial interface to a microprocessor or peripheral via a 3-state output with up to four control inputs including independent SYSTEM CLOCK, I/O CLOCK, chip select (\overline{CS}), and ADDRESS INPUT. A 4-MHz system clock for the TLC545 and a 2.1-MHz system clock for the TLC546 with a design that includes simultaneous read/write operation allowing high-speed data transfers and sample rates of up to 76,923 samples per second for the TLC545, and 40,000 samples per second for the TLC546.

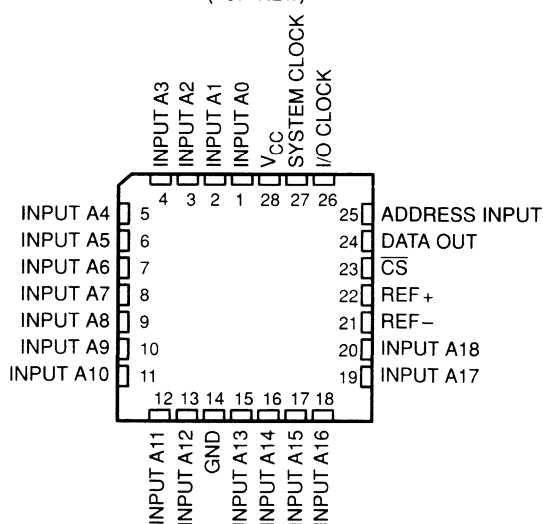
In addition to the high-speed converter and versatile control logic, there is an on-chip 20-channel analog multiplexer that can be used to sample any one of 19 inputs or an internal self-test voltage, and a sample-and-hold that can operate automatically or under microprocessor control.

The converters incorporated in the TLC545 and TLC546 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched capacitor design allows low-error (± 0.5 LSB) conversion in 9 μ s for the TLC545, and 17 μ s for the TLC546, over the full operating temperature range.

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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TLC545C, TLC545I, TLC546C, TLC546I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 19 INPUTS

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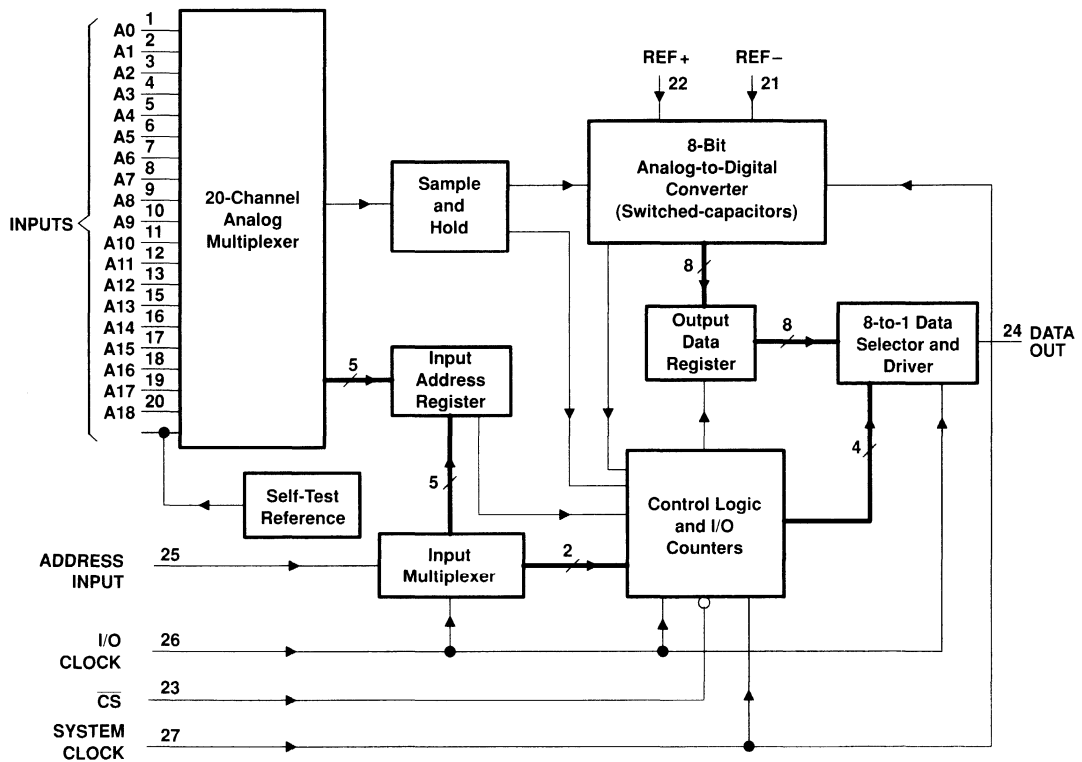
AVAILABLE OPTIONS

T _A	PACKAGE	
	CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC545CFN —	TLC545CN —
-40°C to 85°C	TLC545IFN TLC546IFN	TLC545IN TLC546IN

description (continued)

The TLC545C and the TLC546C are characterized for operation from 0°C to 70°C. The TLC545I and the TLC546I are characterized for operation from -40°C to 85°C.

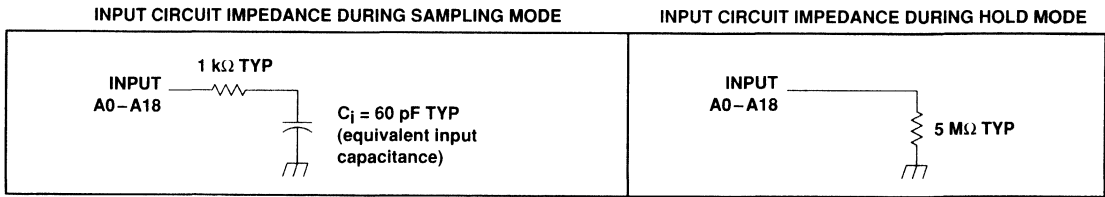
functional block diagram



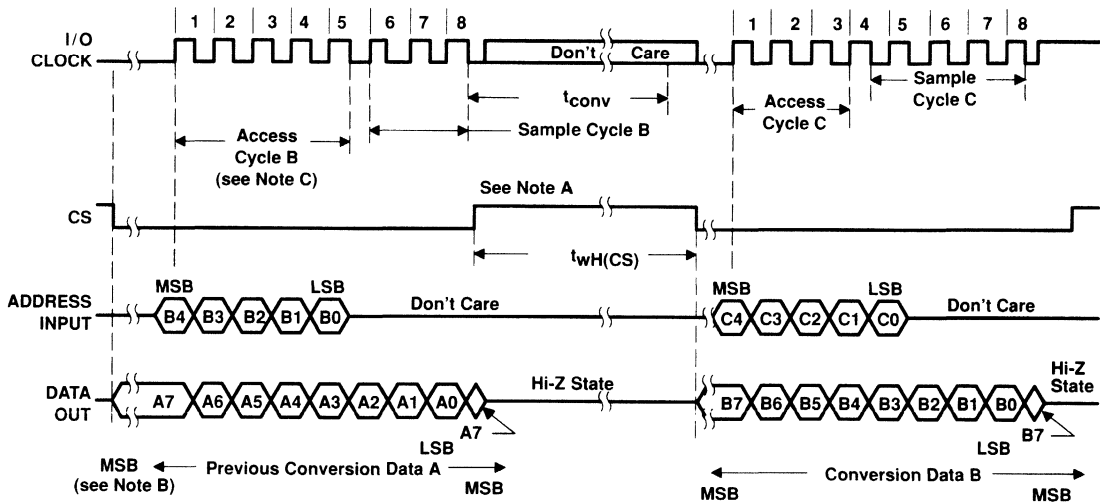
TLC545C, TLC545I, TLC546C, TLC546I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 19 INPUTS

SLAS066B – DECEMBER 1985 – REVISED OCTOBER 1996

typical equivalent inputs



operating sequence



- NOTES:
- The conversion cycle, which requires 36 system clock periods, is initiated with the eighth I/O CLOCK \downarrow after $\overline{CS}\downarrow$ for the channel whose address exists in memory at that time.
 - The most significant bit (MSB) will automatically be placed on the DATA OUT bus after \overline{CS} is brought low. The remaining seven bits (A6–A0) will be clocked out on the first seven I/O CLOCK falling edges.
 - To minimize errors caused by noise at the \overline{CS} input, the internal circuitry waits for three system clock cycles (or less) after a chip select transition before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.



TLC545C, TLC545I, TLC546C, TLC546I
8-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 19 INPUTS

SLAS066B – DECEMBER 1985 – REVISED OCTOBER 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range, V_I (any input)	-0.3 V to $V_{CC} + 0.3$ V
Output voltage range, V_O	-0.3 V to $V_{CC} + 0.3$ V
Peak input current range (any input)	± 10 mA
Peak total input current (all inputs)	± 30 mA
Operating free-air temperature range, T_A : TLC545C, TLC546C	0°C to 70°C
TLC545I, TLC546I	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Case temperature for 10 seconds, T_C : FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.



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TLC545C, TLC545I, TLC546C, TLC546I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 19 INPUTS

SLAS066B – DECEMBER 1985 – REVISED OCTOBER 1996

recommended operating conditions

		TLC545			TLC546			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)		0	V_{CC}	$V_{CC} + 0.1$	0	V_{CC}	$V_{CC} + 0.1$	V
Negative reference voltage, V_{ref-} (see Note 3)		-0.1	0	V_{CC}	-0.1	0	V_{CC}	V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 3)		0	V_{CC}	$V_{CC} + 0.2$	0	V_{CC}	$V_{CC} + 0.2$	V
Analog input voltage (see Note 3)		0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}		2			2			V
Low-level control input voltage, V_{IL}		0.8			0.8			V
Setup time, address bits at data input before I/O CLOCK \uparrow , $t_{su}(A)$		200			400			ns
Address hold time, t_h		0			0			ns
Setup time, \overline{CS} low before clocking in first address bit, $t_{su}(CS)$ (see Note 2)		3			3			System clock cycles
I/O CLOCK frequency, $f_{clock(I/O)}$		0			2.048			MHz
SYSTEM CLOCK frequency, $f_{clock(SYS)}$		$f_{clock(I/O)}$			4			MHz
Pulse duration, \overline{CS} high during conversion, $t_{wH}(CS)$		36			36			System clock cycles
Pulse duration, SYSTEM CLOCK high, $t_{wH}(SYS)$		110			210			ns
Pulse duration, SYSTEM CLOCK low, $t_{wL}(SYS)$		100			190			ns
Pulse duration, I/O CLOCK high, $t_{wH}(I/O)$		200			404			ns
Pulse duration, I/O CLOCK low, $t_{wL}(I/O)$		200			404			ns
Clock transition time (see Note 4)	System	$f_{clock(SYS)} \leq 1048$ kHz		30	30		ns	
		$f_{clock(SYS)} > 1048$ kHz		20	20			
	I/O	$f_{clock(I/O)} \leq 525$ kHz		100	100		ns	
		$f_{clock(I/O)} > 525$ kHz		40	40			
Operating free-air temperature, T_A	TLC545C, TLC546C		0	70	0	70	°C	
	TLC545I, TLC546I		-40	85	-40	85		

- NOTES: 2. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge or rising edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip select setup time has elapsed.
3. Analog input voltages greater than that applied to REF+ convert as all "1"s (11111111), while input voltages less than that applied to REF- convert as all "0"s (00000000). As the differential reference voltage decreases below 4.75 V, the total unadjusted error tends to increase.
4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μ s for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.



TLC545C, TLC545I, TLC546C, TLC546I
8-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 19 INPUTS

SLAS066B – DECEMBER 1985 – REVISED OCTOBER 1996

electrical characteristics over recommended operating temperature range,
 $V_{CC} = V_{ref+} = 4.75\text{ V to }5.5\text{ V}$, $f_{clock(I/O)} = 2.048\text{ MHz for TLC545 or }1.1\text{ MHz for TLC546}$
(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (DATA OUT)	$V_{CC} = 4.75\text{ V}$, $I_{OH} = -360\text{ }\mu\text{A}$	2.4			V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75\text{ V}$, $I_{OL} = 3.2\text{ mA}$			0.4	V
I_{OZ}	Off-state (high-impedance state) output current	$V_O = V_{CC}$, \overline{CS} at V_{CC}			10	μA
		$V_O = 0$, \overline{CS} at V_{CC}			-10	
I_{IH}	High-level input current	$V_I = V_{CC}$		0.005	2.5	μA
I_{IL}	Low-level input current	$V_I = 0$		-0.005	-2.5	μA
I_{CC}	Operating supply current	\overline{CS} at 0 V		1.2	2.5	mA
Selected channel leakage current		Selected channel at V_{CC} , Unselected channel at 0 V		0.4	1	μA
		Selected channel at 0 V, Unselected channel at V_{CC}		-0.4	-1	
$I_{CC} + I_{ref}$	Supply and reference current	$V_{ref+} = V_{CC}$, \overline{CS} at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs		7	55	pF
		Control inputs		5	15	

† All typical values are at $T_A = 25^\circ\text{C}$.



TLC545C, TLC545I, TLC546C, TLC546I
8-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 19 INPUTS

SLAS066B – DECEMBER 1985 – REVISED OCTOBER 1996

operating characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 4.75 \text{ V to } 5.5 \text{ V}$, $f_{clock(I/O)} = 2.048 \text{ MHz for TLC545 or } 1.1 \text{ MHz for TLC546}$,
 $f_{clock(SYS)} = 4 \text{ MHz for TLC545 or } 2.1 \text{ MHz for TLC546}$

PARAMETER	TEST CONDITIONS	TLC545			TLC546			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
E_L	Linearity error	See Note 5			±0.5			LSB	
E_{ZS}	Zero-scale error	See Note 6			±0.5			LSB	
E_{FS}	Full-scale error	See Note 6			±0.5			LSB	
	Total unadjusted error	See Note 7			±0.5			LSB	
	Self-test output code	INPUT A19 address = 10011 (see Note 8)			01111101 (125)	10000011 (131)	01111101 (125)	10000011 (131)	
t_{conv}	Conversion time	See Operating Sequence			9			17	μs
	Total access and conversion time	See Operating Sequence			13			25	μs
t_{acq}	Channel acquisition time (sample cycle)	See Operating Sequence			3			3	I/O clock cycles
t_v	Time output data remains valid after I/O CLOCK↓	10			10				ns
t_d	Delay time, I/O CLOCK to DATA OUT valid	See Parameter Measurement Information			300			400	ns
t_{en}	Output enable time				150			150	ns
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

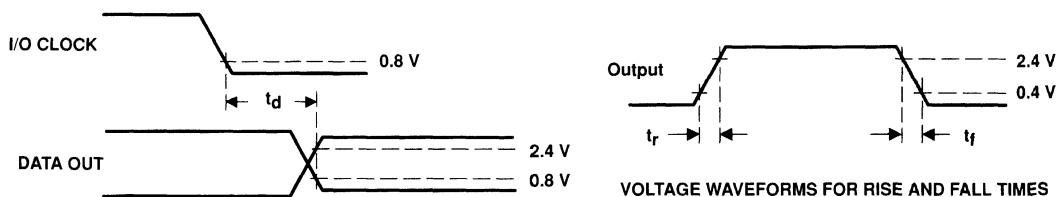
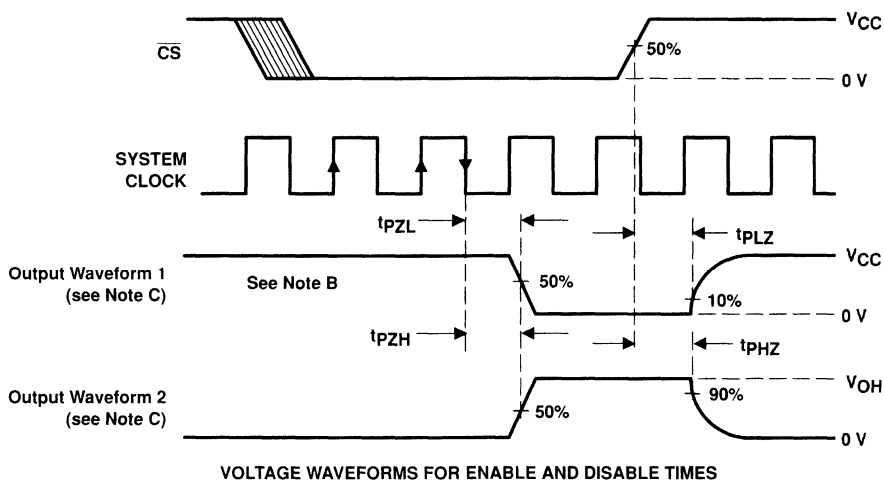
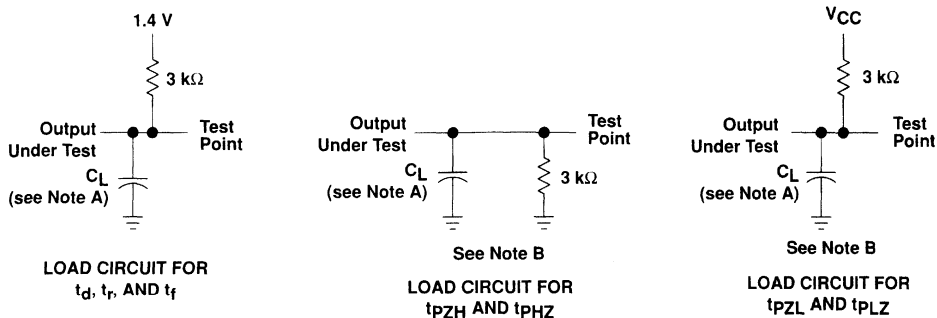
- NOTES:
- Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
 - Zero-scale error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
 - Total unadjusted error is the sum of linearity, zero-scale, and full-scale errors.
 - Both the input address and the output codes are expressed in positive logic. The INPUT A19 analog input signal is internally generated and is used for test purposes.



TLC545C, TLC545I, TLC546C, TLC546I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 19 INPUTS

SLAS066B – DECEMBER 1985 – REVISED OCTOBER 1996

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS FOR DELAY TIME

- NOTES: A. $C_L = 50$ pF for TLC545 and 100 pF for TLC546
 B. $t_{en} = t_{pZH}$ or t_{pZL} . $t_{dis} = t_{pHZ}$ or t_{pLZ}
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.



PARAMETER MEASUREMENT INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 1, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c/R_t C_i}\right) \quad (1)$$

where

$$R_t = R_s + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S/512) \quad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S/512) = V_S \left(1 - e^{-t_c/R_t C_i}\right) \quad (3)$$

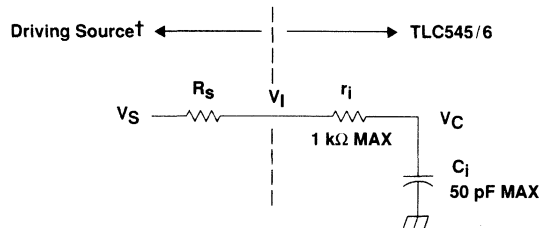
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(512) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_s + 1 \text{ k}\Omega) \times 60 \text{ pF} \times \ln(512) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_i = Input Voltage at INPUT A0–A18
 V_S = External Driving Source Voltage
 R_s = Source Resistance
 r_i = Input Resistance
 C_i = Input Capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

Figure 1. Equivalent Input Circuit Including the Driving Source

TLC545C, TLC545I, TLC546C, TLC546I

8-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH SERIAL CONTROL AND 19 INPUTS

SLAS066B – DECEMBER 1985 – REVISED OCTOBER 1996

PRINCIPLES OF OPERATION

The TLC545 and TLC546 are both complete data acquisition systems on single chips. Each includes such functions as system clock, sample and hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs; \overline{CS} , ADDRESS INPUT, I/O CLOCK, and SYSTEM CLOCK. These control inputs and a TTL-compatible 3-state output facilitate serial communications with a microprocessor or microcomputer. The TLC545 and TLC546 can complete conversions in a maximum of 9 and 17 μs respectively, while complete input-conversion-output cycles can be repeated at a maximum of 13 and 25 μs , respectively.

The system clock and I/O clock are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the SYSTEM CLOCK input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O CLOCK. SYSTEM CLOCK will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When \overline{CS} is high, DATA OUT is in a high-impedance condition, and ADDRESS INPUT and I/O CLOCK are disabled. This feature allows each of these terminals, with the exception of \overline{CS} , to share a control logic point with their counterpart terminals on additional A/D devices when additional TLC545/TLC546 devices are used. Thus, the above feature serves to minimize the required control logic terminals when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. \overline{CS} is brought low. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for two rising edges and then a falling edge of the SYSTEM CLOCK after a \overline{CS} transition before the transition is recognized. The MSB of the previous conversion result automatically appears on DATA OUT.
2. A new positive-logic multiplexer address is shifted in on the first five rising edges of I/O CLOCK. The MSB of the address is shifted in first. The negative edges of these five I/O clocks shift out the second, third, fourth, fifth, and sixth most significant bits of the previous conversion result. The on-chip sample and hold begins sampling the newly addressed analog input after the fifth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Two clock cycles are then applied to I/O CLOCK and the seventh and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to I/O CLOCK. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 system clock cycles. After this final I/O clock cycle, \overline{CS} must go high or the I/O CLOCK must remain low for at least 36 system clock cycles to allow for the conversion function.

\overline{CS} can be kept low during periods of multiple conversion. When keeping \overline{CS} low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O CLOCK line. If glitches occur on the I/O CLOCK line, the I/O sequence between the microprocessor/controller and the device loses synchronization. Also, if \overline{CS} is taken high, it must remain high until the end of conversion. Otherwise, a valid falling edge of \overline{CS} causes a reset condition, which aborts the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 system clock cycles occur. Such action yields the conversion result of the previous conversion and not the ongoing conversion.



TLC545C, TLC545I, TLC546C, TLC546I
8-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 19 INPUTS

SLAS066B – DECEMBER 1985 – REVISED OCTOBER 1996

PRINCIPLES OF OPERATION

It is possible to connect SYSTEM CLOCK and I/O CLOCK together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. The first two clocks are required for this device to recognize \overline{CS} is at a valid low level when the common clock signal is used as an I/O CLOCK. When \overline{CS} is recognized by the device to be at a high level, the common clock signal is used for the conversion clock also.
2. A low \overline{CS} must be recognized before the I/O CLOCK can shift in an analog channel address. The device recognizes a \overline{CS} transition when the SYSTEM CLOCK terminal receives two positive edges and then a negative edge. For this reason, after a \overline{CS} negative edge, the first two clock cycles do not shift in the address. Also, upon shifting in the address, \overline{CS} must be raised after the eighth valid (10 total) I/O CLOCK. Otherwise, additional common clock cycles are recognized as I/O CLOCKS and shift in an erroneous address.

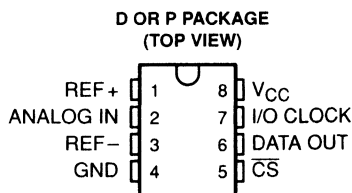
For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device accommodates these applications. Although the on-chip sample and hold begins sampling upon the negative edge of the fourth valid I/O clock cycle, the hold function is not initiated until the negative edge of the eighth valid I/O clock cycle. Thus, the control circuitry can leave the I/O clock signal in its high state during the eighth valid I/O clock cycle, until the moment at which the analog signal must be converted. The TLC545/546 continues sampling the analog input until the eighth valid falling edge of the I/O clock. The control circuitry or software must then immediately lower the I/O clock signal to initiate the hold function at the desired point in time and to start conversion.



TLC548C, TLC548I, TLC549C, TLC549I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS067C – NOVEMBER 1983 – REVISED SEPTEMBER 1996

- Microprocessor Peripheral or Standalone Operation
- 8-Bit Resolution A/D Converter
- Differential Reference Input Voltages
- Conversion Time . . . 17 μ s Max
- Total Access and Conversion Cycles Per Second
 - TLC548 . . . up to 45 500
 - TLC549 . . . up to 40 000
- On-Chip Software-Controllable Sample-and-Hold Function
- Total Unadjusted Error . . . ± 0.5 LSB Max
- 4-MHz Typical Internal System Clock
- Wide Supply Range . . . 3 V to 6 V
- Low Power Consumption . . . 15 mW Max
- Ideal for Cost-Effective, High-Performance Applications including Battery-Operated Portable Instrumentation
- Pinout and Control Signals Compatible With the TLC540 and TLC545 8-Bit A/D Converters and with the TLC1540 10-Bit A/D Converter
- CMOS Technology



description

The TLC548 and TLC549 are CMOS analog-to-digital converter (ADC) integrated circuits built around an 8-bit switched-capacitor successive-approximation ADC. These devices are designed for serial interface with a microprocessor or peripheral through a 3-state data output and an analog input. The TLC548 and TLC549 use only the input/output clock (I/O CLOCK) input along with the chip select (\overline{CS}) input for data control. The maximum I/O CLOCK input frequency of the TLC548 is 2.048 MHz, and the I/O CLOCK input frequency of the TLC549 is specified up to 1.1 MHz.

AVAILABLE OPTIONS

T _A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	TLC548CD TLC549CD	TLC548CP TLC549CP
-40°C to 85°C	TLC548ID TLC549ID	TLC548IP TLC549IP

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.


**TEXAS
INSTRUMENTS**

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TLC548C, TLC548I, TLC549C, TLC549I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS067C – NOVEMBER 1983 – REVISED SEPTEMBER 1996

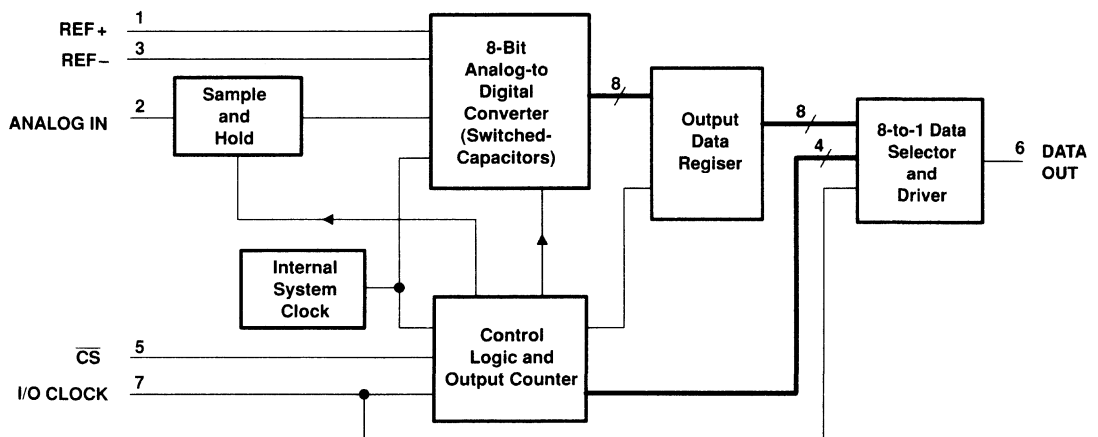
description (continued)

Operation of the TLC548 and the TLC549 is very similar to that of the more complex TLC540 and TLC541 devices; however, the TLC548 and TLC549 provide an on-chip system clock that operates typically at 4 MHz and requires no external components. The on-chip system clock allows internal device operation to proceed independently of serial input/output data timing and permits manipulation of the TLC548 and TLC549 as desired for a wide range of software and hardware requirements. The I/O CLOCK together with the internal system clock allow high-speed data transfer and conversion rates of 45 500 conversions per second for the TLC548, and 40 000 conversions per second for the TLC549.

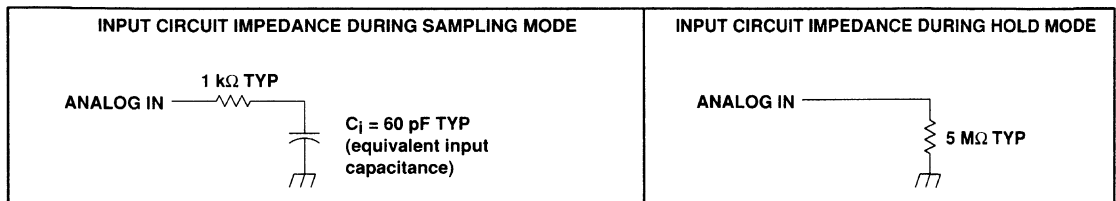
Additional TLC548 and TLC549 features include versatile control logic, an on-chip sample-and-hold circuit that can operate automatically or under microprocessor control, and a high-speed converter with differential high-impedance reference voltage inputs that ease ratiometric conversion, scaling, and circuit isolation from logic and supply noises. Design of the totally switched-capacitor successive-approximation converter circuit allows conversion with a maximum total error of ± 0.5 least significant bit (LSB) in less than 17 μ s.

The TLC548C and TLC549C are characterized for operation from 0°C to 70°C. The TLC548I and TLC549I are characterized for operation from -40°C to 85°C.

functional block diagram



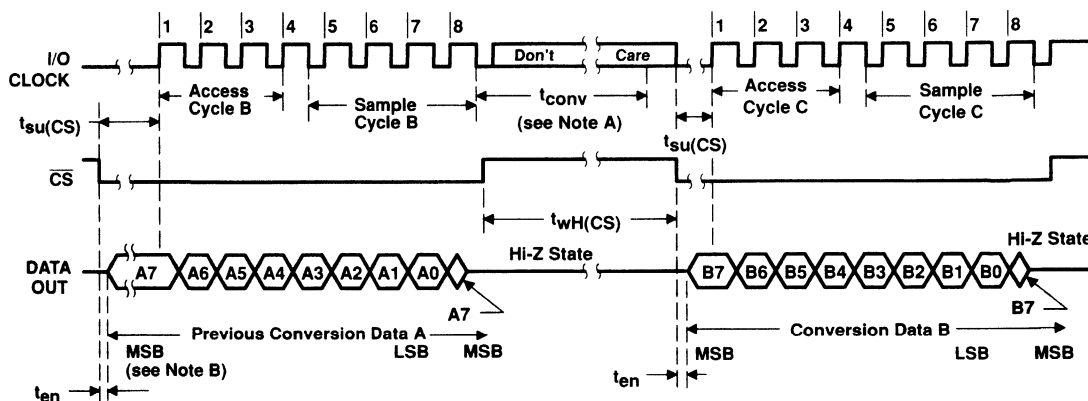
typical equivalent inputs



TLC548C, TLC548I, TLC549C, TLC549I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS067C – NOVEMBER 1983 – REVISED SEPTEMBER 1996

operating sequence



- NOTES: A. The conversion cycle, which requires 36 internal system clock periods (17 μ s maximum), is initiated with the eighth I/O clock pulse trailing edge after \overline{CS} goes low for the channel whose address exists in memory at the time.
- B. The most significant bit (A7) is automatically placed on the DATA OUT bus after \overline{CS} is brought low. The remaining seven bits (A6–A0) are clocked out on the first seven I/O clock falling edges. B7–B0 follows in the same manner.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range at any input	-0.3 V to $V_{CC} + 0.3$ V
Output voltage range	-0.3 V to $V_{CC} + 0.3$ V
Peak input current range (any input)	± 10 mA
Peak total input current range (all inputs)	± 30 mA
Operating free-air temperature range, T_A (see Note 2):	TLC548C, TLC549C 0°C to 70°C
	TLC548I, TLC549I -40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

- NOTES: 1. All voltage values are with respect to the network ground terminal with the REF- and GND terminals connected together, unless otherwise noted.
2. The D package is not recommended below -40°C.



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TLC548C, TLC548I, TLC549C, TLC549I

8-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH SERIAL CONTROL

SLAS067C – NOVEMBER 1983 – REVISED SEPTEMBER 1996

recommended operating conditions

	TLC548			TLC549			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	3	5	6	3	5	6	V
Positive reference voltage, V_{ref+} (see Note 3)	2.5	V_{CC}	$V_{CC}+0.1$	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{ref-} (see Note 3)	-0.1	0	2.5	-0.1	0	2.5	V
Differential reference voltage, V_{ref+} , V_{ref-} (see Note 3)	1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 3)	0	V_{CC}		0	V_{CC}		V
High-level control input voltage, V_{IH} (for $V_{CC} = 4.75$ V to 5.5 V)	2			2			V
Low-level control input voltage, V_{IL} (for $V_{CC} = 4.75$ V to 5.5 V)	0.8			0.8			V
Input/output clock frequency, $f_{clock(I/O)}$ (for $V_{CC} = 4.75$ V to 5.5 V)	0	2.048		0	1.1		MHz
Input/output clock high, $t_{wH(I/O)}$ (for $V_{CC} = 4.75$ V to 5.5 V)	200			404			ns
Input/output clock low, $t_{wL(I/O)}$ (for $V_{CC} = 4.75$ V to 5.5 V)	200			404			ns
Input/output clock transition time, $t_t(I/O)$ (for $V_{CC} = 4.75$ V to 5.5 V) (see Note 4 and Operating Sequence)	100			100			ns
Duration of \overline{CS} input high state during conversion, $t_{wH(CS)}$ (for $V_{CC} = 4.75$ V to 5.5 V) (see Operating Sequence)	17			17			μ s
Setup time, \overline{CS} low before first I/O CLOCK, $t_{su(CS)}$ (for $V_{CC} = 4.75$ V to 5.5 V) (see Note 5)	1.4			1.4			μ s
TLC548C, TLC549C	0		70	0		70	$^{\circ}$ C
TLC548I, TLC549I	-40		85	-40		85	

- NOTES: 3. Analog input voltages greater than that applied to REF+ convert to all ones (11111111), while input voltages less than that applied to REF- convert to all zeros (00000000). For proper operation, the positive reference voltage V_{ref+} , must be at least 1 V greater than the negative reference voltage, V_{ref-} . In addition, unadjusted errors may increase as the differential reference voltage, $V_{ref+} - V_{ref-}$, falls below 4.75 V.
4. This is the time required for the I/O CLOCK input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μ s for remote data acquisition applications in which the sensor and the ADC are placed several feet away from the controlling microprocessor.
5. To minimize errors caused by noise at the \overline{CS} input, the internal circuitry waits for two rising edges and one falling edge of internal system clock after \overline{CS} before responding to control input signals. This \overline{CS} setup time is given by the t_{en} and $t_{su(CS)}$ specifications.



TLC548C, TLC548I, TLC549C, TLC549I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS067C – NOVEMBER 1983 – REVISED SEPTEMBER 1996

**electrical characteristics over recommended operating free-air temperature range,
V_{CC} = V_{ref+} = 4.75 V to 5.5 V, f_{clock(I/O)} = 2.048 MHz for TLC548 or 1.1 MHz for TLC549
(unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage	V _{CC} = 4.75 V, I _{OH} = -360 μA	2.4			V
V _{OL}	Low-level output voltage	V _{CC} = 4.75 V, I _{OL} = 3.2 mA			0.4	V
I _{OZ}	High-impedance off-state output current	V _O = V _{CC} , CS at V _{CC}			10	μA
		V _O = 0, CS at V _{CC}			-10	
I _{IH}	High-level input current, control inputs	V _I = V _{CC}		0.005	2.5	μA
I _{IL}	Low-level input current, control inputs	V _I = 0		-0.005	-2.5	μA
I _{I(on)}	Analog channel on-state input current during sample cycle	Analog input at V _{CC}		0.4	1	μA
		Analog input at 0 V		-0.4	-1	
I _{CC}	Operating supply current	CS at 0 V		1.8	2.5	mA
I _{CC} + I _{ref}	Supply and reference current	V _{ref+} = V _{CC}		1.9	3	mA
C _i	Input capacitance	Analog inputs		7	55	pF
		Control inputs		5	15	

**operating characteristics over recommended operating free-air temperature range,
V_{CC} = V_{ref+} = 4.75 V to 5.5 V, f_{clock(I/O)} = 2.048 MHz for TLC548 or 1.1 MHz for TLC549
(unless otherwise noted)**

PARAMETER	TEST CONDITIONS	TLC548			TLC549			UNIT	
		MIN	TYP†	MAX	MIN	TYP†	MAX		
E _L	Linearity error	See Note 6			±0.5			LSB	
E _{ZS}	Zero-scale error	See Note 7			±0.5			LSB	
E _{FS}	Full-scale error	See Note 7			±0.5			LSB	
	Total unadjusted error	See Note 8			±0.5			LSB	
t _{conv}	Conversion time	See Operating Sequence			8	17	12	17	μs
	Total access and conversion time	See Operating Sequence			12	22	19	25	μs
t _a	Channel acquisition time (sample cycle)	See Operating Sequence			4			I/O clock cycles	
t _v	Time output data remains valid after I/O CLOCK↓				10		10		ns
t _d	Delay time to data output valid	I/O CLOCK↓			200			400	ns
t _{en}	Output enable time				1.4			1.4	μs
t _{dis}	Output disable time				150			150	ns
t _{r(bus)}	Data bus rise time	See Figure 1			300			300	ns
t _{f(bus)}	Data bus fall time				300			300	300

† All typicals are at V_{CC} = 5 V, T_A = 25°C.

- NOTES: 6. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
7. Zero-scale error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
8. Total unadjusted error is the sum of linearity, zero-scale, and full-scale errors.



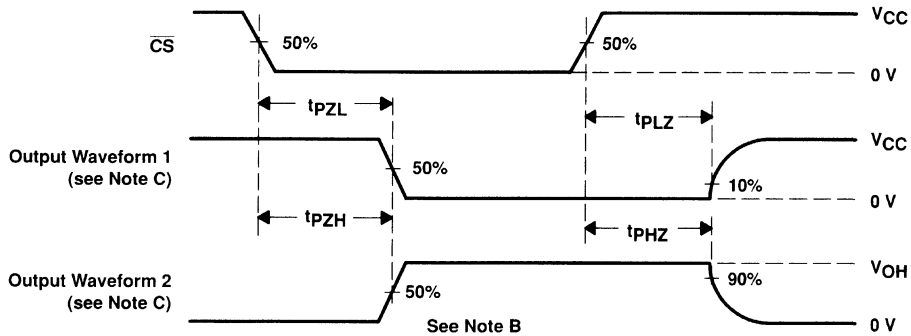
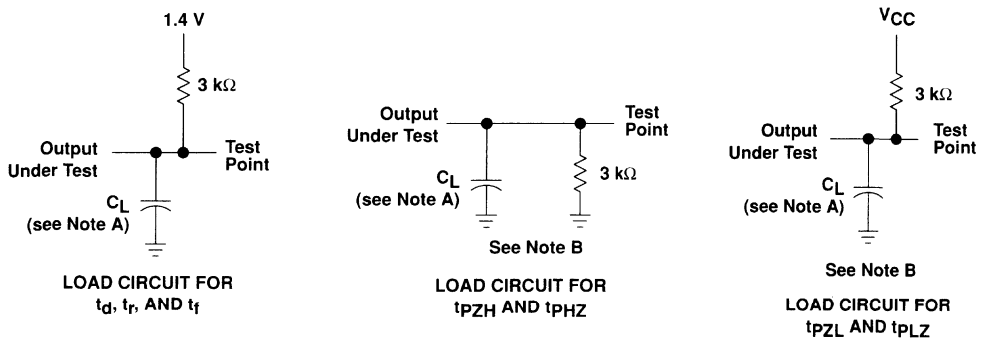
TLC548C, TLC548I, TLC549C, TLC549I

8-BIT ANALOG-TO-DIGITAL CONVERTERS

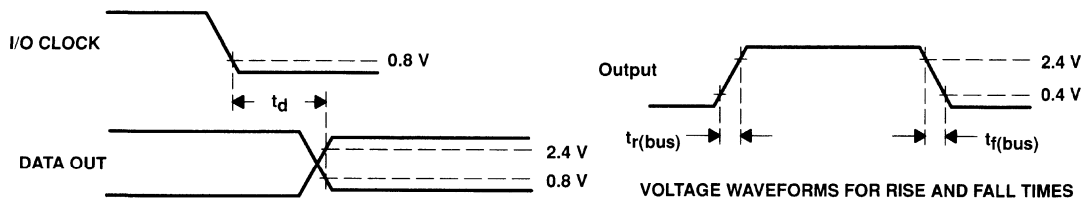
WITH SERIAL CONTROL

SLAS067C – NOVEMBER 1983 – REVISED SEPTEMBER 1996

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS FOR DELAY TIME

VOLTAGE WAVEFORMS FOR RISE AND FALL TIMES

- NOTES: A. $C_L = 50$ pF for TLC548 and 100 pF for TLC549; C_L includes jig capacitance.
 B. $t_{en} = t_{pZH}$ or t_{pZL} , $t_{dis} = t_{pHZ}$ or t_{pLZ} .
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Load Circuits and Voltage Waveforms

APPLICATIONS INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 2, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c/R_t C_i}\right) \quad (1)$$

where

$$R_t = R_S + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S/512) \quad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S/512) = V_S \left(1 - e^{-t_c/R_t C_i}\right) \quad (3)$$

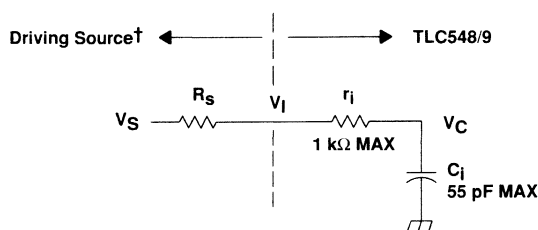
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(512) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_S + 1 \text{ k}\Omega) \times 60 \text{ pF} \times \ln(512) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at ANALOG IN
 V_S = External Driving Source Voltage
 R_S = Source Resistance
 r_i = Input Resistance
 C_i = Input Capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 2. Equivalent Input Circuit Including the Driving Source

TLC548C, TLC548I, TLC549C, TLC549I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS067C – NOVEMBER 1983 – REVISED SEPTEMBER 1996

PRINCIPLES OF OPERATION

The TLC548 and TLC549 are each complete data acquisition systems on a single chip. Each contains an internal system clock, sample-and-hold function, 8-bit A/D converter, data register, and control logic circuitry. For flexibility and access speed, there are two control inputs: I/O CLOCK and chip select (\overline{CS}). These control inputs and a TTL-compatible 3-state output facilitate serial communications with a microprocessor or minicomputer. A conversion can be completed in 17 μs or less, while complete input-conversion-output cycles can be repeated in 22 μs for the TLC548 and in 25 μs for the TLC549.

The internal system clock and I/O CLOCK are used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Due to this independence and the internal generation of the system clock, the control hardware and software need only be concerned with reading the previous conversion result and starting the conversion by using the I/O clock. In this manner, the internal system clock drives the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When \overline{CS} is high, DATA OUT is in a high-impedance condition and I/O CLOCK is disabled. This \overline{CS} control function allows I/O CLOCK to share the same control logic point with its counterpart terminal when additional TLC548 and TLC549 devices are used. This also serves to minimize the required control logic terminals when using multiple TLC548 and TLC549 devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. \overline{CS} is brought low. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for two rising edges and then a falling edge of the internal system clock after a $\overline{CS}\downarrow$ before the transition is recognized. However, upon a \overline{CS} rising edge, DATA OUT goes to a high-impedance state within the specified t_{dis} even though the rest of the integrated circuitry does not recognize the transition until the specified $t_{su}(\overline{CS})$ has elapsed. This technique protects the device against noise when used in a noisy environment. The most significant bit (MSB) of the previous conversion result initially appears on DATA OUT when \overline{CS} goes low.
2. The falling edges of the first four I/O CLOCK cycles shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample-and-hold function begins sampling the analog input after the fourth high-to-low transition of I/O CLOCK. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three more I/O CLOCK cycles are then applied to the I/O CLOCK terminal and the sixth, seventh, and eighth conversion bits are shifted out on the falling edges of these clock cycles.
4. The final (the eighth) clock cycle is applied to I/O CLOCK. The on-chip sample-and-hold function begins the hold operation upon the high-to-low transition of this clock cycle. The hold function continues for the next four internal system clock cycles, after which the holding function terminates and the conversion is performed during the next 32 system clock cycles, giving a total of 36 cycles. After the eighth I/O CLOCK cycle, \overline{CS} must go high or the I/O clock must remain low for at least 36 internal system clock cycles to allow for the completion of the hold and conversion functions. \overline{CS} can be kept low during periods of multiple conversion. When keeping \overline{CS} low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O CLOCK line. If glitches occur on I/O CLOCK, the I/O sequence between the microprocessor/controller and the device loses synchronization. When \overline{CS} is taken high, it must remain high until the end of conversion. Otherwise, a valid high-to-low transition of \overline{CS} causes a reset condition, which aborts the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 internal system clock cycles occur. Such action yields the conversion result of the previous conversion and not the ongoing conversion.



TLC548C, TLC548I, TLC549C, TLC549I
8-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

SLAS067C – NOVEMBER 1983 – REVISED SEPTEMBER 1996

PRINCIPLES OF OPERATION

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device accommodates these applications. Although the on-chip sample-and-hold function begins sampling upon the high-to-low transition of the fourth I/O CLOCK cycle, the hold function does not begin until the high-to-low transition of the eighth I/O CLOCK cycle, which should occur at the moment when the analog signal must be converted. The TLC548 and TLC549 continue sampling the analog input until the high-to-low transition of the eighth I/O CLOCK pulse. The control circuitry or software then immediately lowers I/O CLOCK and starts the holding function to hold the analog signal at the desired point in time and starts the conversion.



TLC0820AC, TLC0820AI

Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL CONVERTERS USING MODIFIED FLASH TECHNIQUES

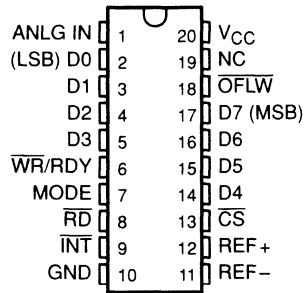
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- **Advanced LinCMOS™ Silicon-Gate Technology**
- **8-Bit Resolution**
- **Differential Reference Inputs**
- **Parallel Microprocessor Interface**
- **Conversion and Access Time Over Temperature Range**
Read Mode . . . 2.5 μ s Max
- **No External Clock or Oscillator Components Required**
- **On-Chip Track and Hold**
- **Single 5-V Supply**
- **TLC0820A Is Direct Replacement for National Semiconductor ADC0820C/CC and Analog Devices AD7820K/B/T**

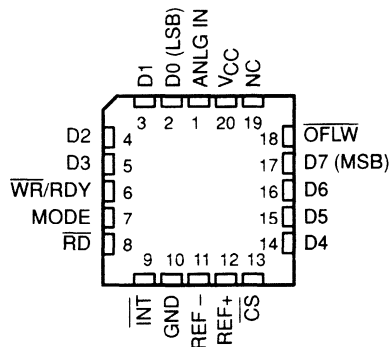
description

The TLC0820AC and the TLC0820AI are Advanced LinCMOS™ 8-bit analog-to-digital converters each consisting of two 4-bit flash converters, a 4-bit digital-to-analog converter, a summing (error) amplifier, control logic, and a result latch circuit. The modified flash technique allows low-power integrated circuitry to complete an 8-bit conversion in 1.18 μ s over temperature. The on-chip track-and-hold circuit has a 100-ns sample window and allows these devices to convert continuous analog signals having slew rates of up to 100 mV/ μ s without external sampling components. TTL-compatible 3-state output drivers and two modes of operation allow interfacing to a variety of microprocessors. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

DB, DW, OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection

AVAILABLE OPTIONS

T _A	TOTAL UNADJUSTED ERROR	PACKAGE			
		SSOP (DB)	PLASTIC SMALL OUTLINE (DW)	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	±1 LSB	TLC0820ACDB	TLC0820ACDW	TLC0820ACFN	TLC0820ACN
-40°C to 85°C	±1 LSB	—	TLC0820AIDW	TLC0820AIFN	TLC0820AIN

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

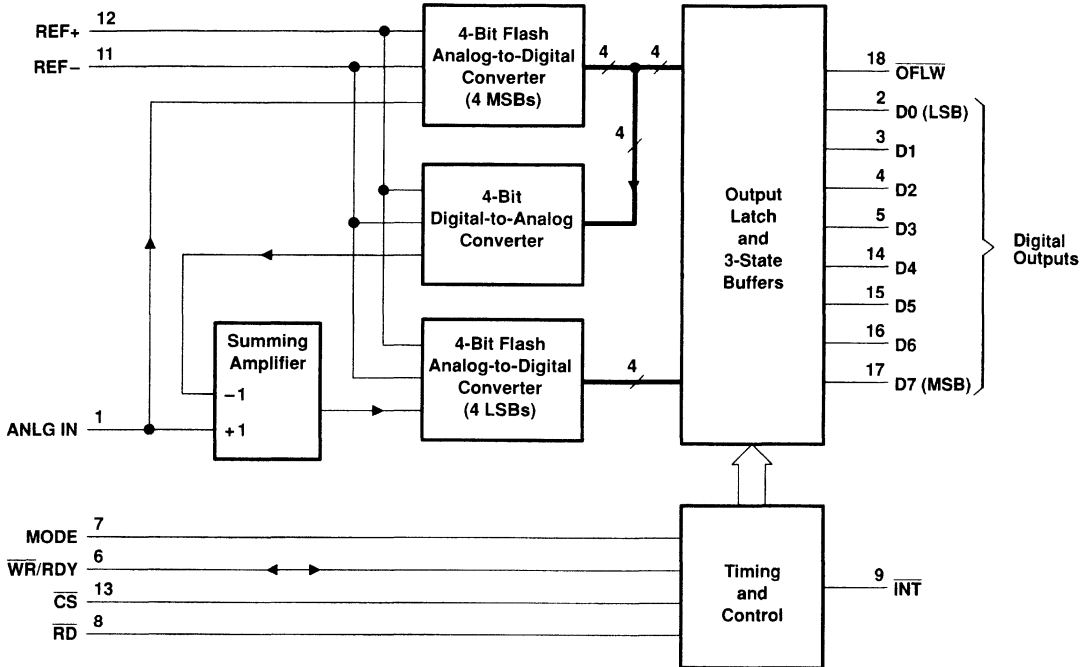


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CONVERTERS USING MODIFIED FLASH TECHNIQUES
 SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

functional block diagram



TLC0820AC, TLC0820AI
Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL
CONVERTERS USING MODIFIED FLASH TECHNIQUES

SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ANLG IN	1	I	Analog input
CS	13	I	Chip select. CS must be low in order for RD or WR to be recognized by the ADC.
D0	2	O	Digital, 3-state output data, bit 1 (LSB)
D1	3	O	Digital, 3-state output data, bit 2
D2	4	O	Digital, 3-state output data, bit 3
D3	5	O	Digital, 3-state output data, bit 4
D4	14	O	Digital, 3-state output data, bit 5
D5	15	O	Digital, 3-state output data, bit 6
D6	16	O	Digital, 3-state output data, bit 7
D7	17	O	Digital, 3-state output data, bit 8 (MSB)
GND	10		Ground
INT	9	O	Interrupt. In the write-read mode, the interrupt output (INT) going low indicates that the internal count-down delay time, $t_{d(int)}$, is complete and the data result is in the output latch. The delay time $t_{d(int)}$ is typically 800 ns starting after the rising edge of WR (see operating characteristics and Figure 3). If RD goes low prior to the end of $t_{d(int)}$, INT goes low at the end of $t_{d(RIL)}$ and the conversion results are available sooner (see Figure 2). INT is reset by the rising edge of either RD or CS.
MODE	7	I	Mode select. MODE is internally tied to GND through a 50- μ A current source, which acts like a pull-down resistor. When MODE is low, the read mode is selected. When MODE is high, the write-read mode is selected.
NC	19		No internal connection
OFLW	18	O	Overflow. Normally OFLW is a logical high. However, if the analog input is higher than V_{ref+} , OFLW will be low at the end of conversion. It can be used to cascade two or more devices to improve resolution (9 or 10 bits).
RD	8	I	Read. In the write-read mode with CS low, the 3-state data outputs D0 through D7 are activated when RD goes low. RD can also be used to increase the conversion speed by reading data prior to the end of the internal count-down delay time. As a result, the data transferred to the output latch is latched after the falling edge of RD. In the read mode with CS low, the conversion starts with RD going low. RD also enables the 3-state data outputs on completion of the conversion. RDY going into the high-impedance state and INT going low indicate completion of the conversion.
REF-	11	I	Reference voltage. REF- is placed on the bottom of the resistor ladder.
REF+	12	I	Reference voltage. REF+ is placed on the top of the resistor ladder.
VCC	20		Power supply voltage
WR/RDY	6	I/O	Write ready. In the write-read mode with CS low, the conversion is started on the falling edge of the WR input signal. The result of the conversion is strobed into the output latch after the internal count-down delay time, $t_{d(int)}$, provided that the RD input does not go low prior to this time. The delay time $t_{d(int)}$ is approximately 800 ns. In the read mode, RDY (an open-drain output) goes low after the falling edge of CS and goes into the high-impedance state when the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system.



TLC0820AC, TLC0820AI

Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL CONVERTERS USING MODIFIED FLASH TECHNIQUES

SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	10 V
Input voltage range, all inputs (see Note 1)	-0.2 V to $V_{CC}+0.2$ V
Output voltage range, all outputs (see Note 1)	-0.2 V to $V_{CC}+0.2$ V
Operating free-air temperature range: TLC0820AC	0°C to 70°C
TLC0820AI	-40°C to 85°C
Storage temperature range	-65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DB, DW or N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to network GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	8	V
Analog input voltage		-0.1		$V_{CC}+0.1$	V
Positive reference voltage, V_{ref+}		V_{ref-}		V_{CC}	V
Negative reference voltage, V_{ref-}		GND		V_{ref+}	V
High-level input voltage, V_{IH}	$V_{CC} = 4.75$ V to 5.25 V	CS, WR/RDY, RD	2		V
		MODE	3.5		
Low-level input voltage, V_{IL}	$V_{CC} = 4.75$ V to 5.25 V	CS, WR/RDY, RD	0.8		V
		MODE	1.5		
Pulse duration, write in write-read mode, $t_w(W)$ (see Figures 2, 3, and 4)		0.5		50	μs
Operating free-air temperature, T_A	TLC0820AC	0		70	°C
	TLC0820AI	-40		85	



TLC0820AC, TLC0820AI
Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL
CONVERTERS USING MODIFIED FLASH TECHNIQUES

SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

electrical characteristics at specified operating free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A †	MIN	TYP	MAX	UNIT			
V_{OH}	High-level output voltage	D0–D7, \overline{INT} , or \overline{OFLW}	Full range	$V_{CC} = 4.75\text{ V}$, $I_{OH} = -360\text{ }\mu\text{A}$	2.4		V			
				$V_{CC} = 4.75\text{ V}$, $I_{OH} = -10\text{ }\mu\text{A}$	4.5					
V_{OL}	Low-level output voltage	D0–D7, \overline{OFLW} , \overline{INT} , or $\overline{WR/RDY}$	Full range	$V_{CC} = 5.25\text{ V}$, $I_{OL} = 1.6\text{ mA}$		0.4	V			
					25°C			0.34		
I_{IH}	High-level input current	\overline{CS} or \overline{RD}	Full range	$V_{IH} = 5\text{ V}$		0.005	1	μA		
					$\overline{WR/RDY}$				3	
					25°C	0.1	0.3			
I_{IL}	Low-level input current	\overline{CS} , $\overline{WR/RDY}$, \overline{RD} , or MODE	Full range	$V_{IL} = 0$			200	μA		
					25°C	50	170			
I_{OZ}	Off-state (high-impedance-state) output current	D0–D7 or $\overline{WR/RDY}$	Full range	$V_O = 5\text{ V}$			3	μA		
					25°C	0.1	0.3			
					Full range	$V_O = 0$				-3
							25°C		-0.1	-0.3
I_I	Analog input current		Full range	CS at 5 V, $V_I = 5\text{ V}$			3	μA		
					25°C		0.3			
					Full range	CS at 5 V, $V_I = 0$				-3
							25°C			-0.3
I_{OS}	Short-circuit output current	D0–D7, \overline{OFLW} , \overline{INT} , or $\overline{WR/RDY}$	Full range	$V_O = 5\text{ V}$		7		mA		
					25°C	8.4	14			
	Full range	D0–D7 or \overline{OFLW}	$V_O = 0$			-6				
				25°C	-7.2	-12				
	Full range	INT	$V_O = 0$			-4.5				
				25°C	-5.3	-9				
R_{ref}	Reference resistance		Full range				6	k Ω		
					25°C	1.4	2.3		5.3	
I_{CC}	Supply current		Full range	\overline{CS} , $\overline{WR/RDY}$, and \overline{RD} at 0 V			15	mA		
					25°C	7.5	13			
C_i	Input capacitance	D0–D7	Full range			5	pF			
		ANLG IN			45					
C_o	Output capacitance	D0–D7	Full range			5	pF			

† Full range is as specified in recommended operating conditions.



TLC0820AC, TLC0820AI
Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL
CONVERTERS USING MODIFIED FLASH TECHNIQUES

SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

operating characteristics, $V_{CC} = 5\text{ V}$, $V_{ref+} = 5\text{ V}$, $V_{ref-} = 0$, $t_r = t_f = 20\text{ ns}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT	
k_{SVS}	Supply-voltage sensitivity	$V_{CC} = 5\text{ V} \pm 5\%$, $T_A = \text{MIN to MAX}$			$\pm 1/16$	$\pm 1/4$	LSB	
	Total unadjusted error‡	MODE at 0 V, $T_A = \text{MIN to MAX}$				1	LSB	
$t_{conv(R)}$	Conversion time, read mode	MODE at 0 V, See Figure 1			1.6	2.5	μs	
$t_a(R)$	Access time, $\overline{RD}\downarrow$ to data valid	MODE at 0 V, See Figure 1			$t_{conv(R)+20}$	$t_{conv(R)+50}$	ns	
$t_a(R1)$	Access time, $\overline{RD}\downarrow$ to data valid	MODE at 5 V, $t_d(WR) < t_d(int)$. See Figure 2		$C_L = 15\text{ pF}$	190	280	ns	
				$C_L = 100\text{ pF}$	210	320		
$t_a(R2)$	Access time, $\overline{RD}\downarrow$ to data valid	MODE at 5 V, $t_d(WR) > t_d(int)$. See Figure 3		$C_L = 15\text{ pF}$	70	120	ns	
				$C_L = 100\text{ pF}$	90	150		
$t_a(INT)$	Access time, $\overline{INT}\downarrow$ to data valid	MODE at 5 V, See Figure 4			20	50	ns	
t_{dis}	Disable time, $\overline{RD}\uparrow$ to data valid	$R_L = 1\text{ k}\Omega$, $C_L = 10\text{ pF}$, See Figures 1, 2, 3, and 5			70	95	ns	
$t_d(int)$	Delay time, $WR/RDY\uparrow$ to $INT\downarrow$	MODE at 5 V, See Figures 2, 3, and 4			800	1300	ns	
$t_d(NC)$	Delay time, to next conversion	See Figures 1, 2, 3, and 4		500			ns	
$t_d(WR)$	Delay time, $WR/RDY\uparrow$ to $RD\downarrow$ in write-read mode	See Figure 2		0.4			μs	
$t_d(RDY)$	Delay time, $CS\downarrow$ to $WR/RDY\downarrow$	MODE at 0 V, See Figure 1			50	100	ns	
$t_d(RIH)$	Delay time, $\overline{RD}\uparrow$ to $\overline{INT}\uparrow$	$C_L = 50\text{ pF}$, See Figures 1, 2, and 3			125	225	ns	
$t_d(RIL)$	Delay time, $RD\downarrow$ to $INT\downarrow$	MODE at 5 V, See Figure 2			$t_d(WR) < t_d(int)$	200	290	ns
$t_d(WIH)$	Delay time, $WR/RDY\uparrow$ to $\overline{INT}\uparrow$	MODE at 5 V, See Figure 4			$C_L = 50\text{ pF}$	175	270	ns
	Slew-rate tracking				0.1		$\text{V}/\mu\text{s}$	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ Total unadjusted error includes offset, full-scale, and linearity errors.

TLC0820AC, TLC0820AI
Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL
CONVERTERS USING MODIFIED FLASH TECHNIQUES
SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

PARAMETER MEASUREMENT INFORMATION

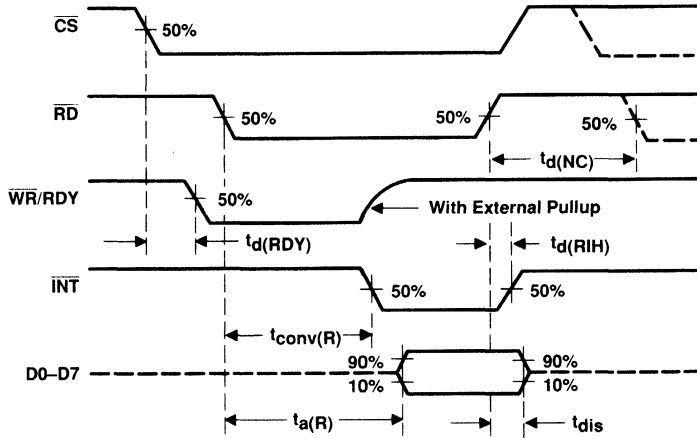


Figure 1. Read-Mode Waveforms (MODE Low)

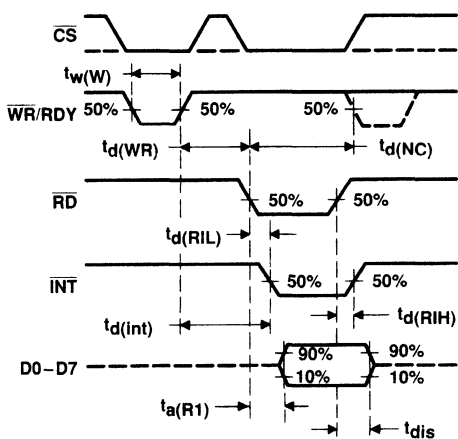


Figure 2. Write-Read-Mode Waveforms
[MODE High and $t_d(WR) < t_d(int)$]

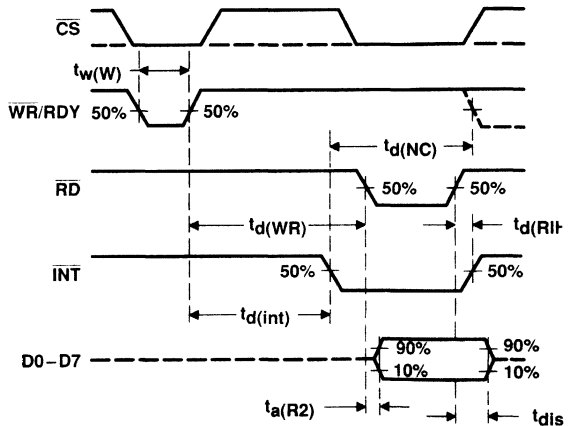


Figure 3. Write-Read-Mode Waveforms
[MODE High and $t_d(WR) > t_d(int)$]

TLC0820AC, TLC0820AI
Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL
CONVERTERS USING MODIFIED FLASH TECHNIQUES

SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

PARAMETER MEASUREMENT INFORMATION

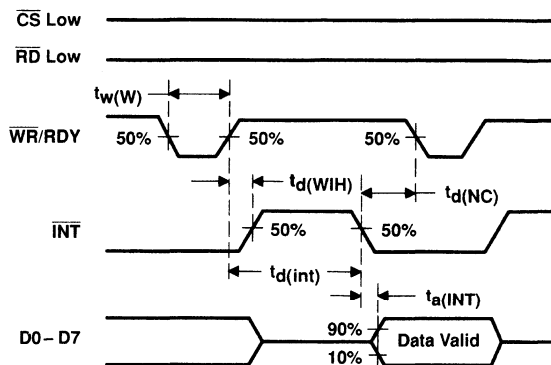


Figure 4. Write-Read-Mode Waveforms
 (Stand-Alone Operation, MODE High, and RD Low)

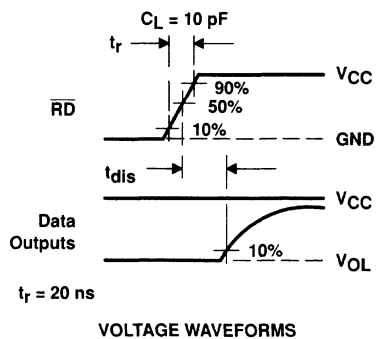
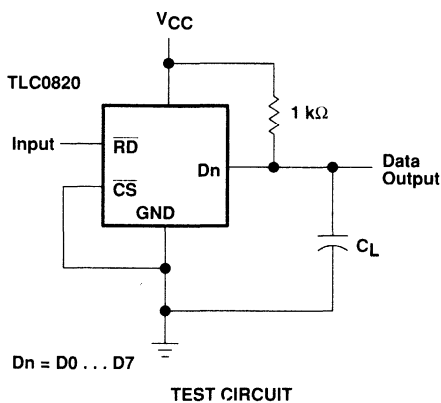
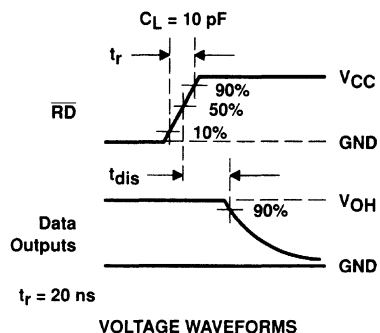
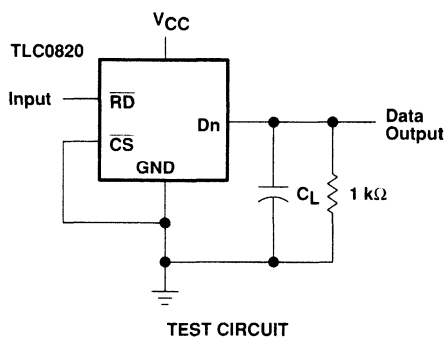


Figure 5. Test Circuit and Voltage Waveforms

TLC0820AC, TLC0820AI
Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL
CONVERTERS USING MODIFIED FLASH TECHNIQUES

SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

PRINCIPLES OF OPERATION

The TLC0820AC and TLC0820AI each employ a combination of sampled-data comparator techniques and flash techniques common to many high-speed converters. Two 4-bit flash analog-to-digital conversions are used to give a full 8-bit output.

The recommended analog input voltage range for conversion is -0.1 V to $V_{CC} + 0.1\text{ V}$. Analog input signals that are less than $V_{ref-} + 1/2\text{ LSB}$ or greater than $V_{ref+} - 1/2\text{ LSB}$ convert to 00000000 or 11111111, respectively. The reference inputs are fully differential with common-mode limits defined by the supply rails. The reference input values define the full-scale range of the analog input. This allows the gain of the ADC to be varied for ratiometric conversion by changing the V_{ref+} and V_{ref-} voltages.

The device operates in two modes, read (only) and write-read, that are selected by MODE. The converter is set to the read (only) mode when MODE is low. In the read mode, \overline{WR}/RDY is used as an output and is referred to as the ready terminal. In this mode, a low on \overline{WR}/RDY while \overline{CS} is low indicates that the device is busy. Conversion starts on the falling edge of \overline{RD} and is completed no more than $2.5\text{ }\mu\text{s}$ later when \overline{INT} falls and \overline{WR}/RDY returns to the high-impedance state. Data outputs also change from high-impedance to active states at this time. After the data is read, \overline{RD} is taken high, \overline{INT} returns high, and the data outputs return to their high-impedance states.

When MODE is high, the converter is set to the write-read mode and \overline{WR}/RDY is referred to as the write terminal. Taking \overline{CS} and \overline{WR}/RDY low selects the converter and initiates measurement of the input signal. Approximately 600 ns after \overline{WR}/RDY returns high, the conversion is completed. Conversion starts on the rising edge of \overline{WR}/RDY in the write-read mode.

The high-order 4-bit flash ADC measures the input by means of 16 comparators operating simultaneously. A high-precision 4-bit DAC then generates a discrete analog voltage from the result of that conversion. After a time delay, a second bank of comparators does a low-order conversion on the analog difference between the input level and the high-order DAC output. The results from each of these conversions enter an 8-bit latch and are output to the 3-state output buffers on the falling edge of \overline{RD} .



TLC0820AC, TLC0820AI
Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL
CONVERTERS USING MODIFIED FLASH TECHNIQUES
 SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

APPLICATION INFORMATION

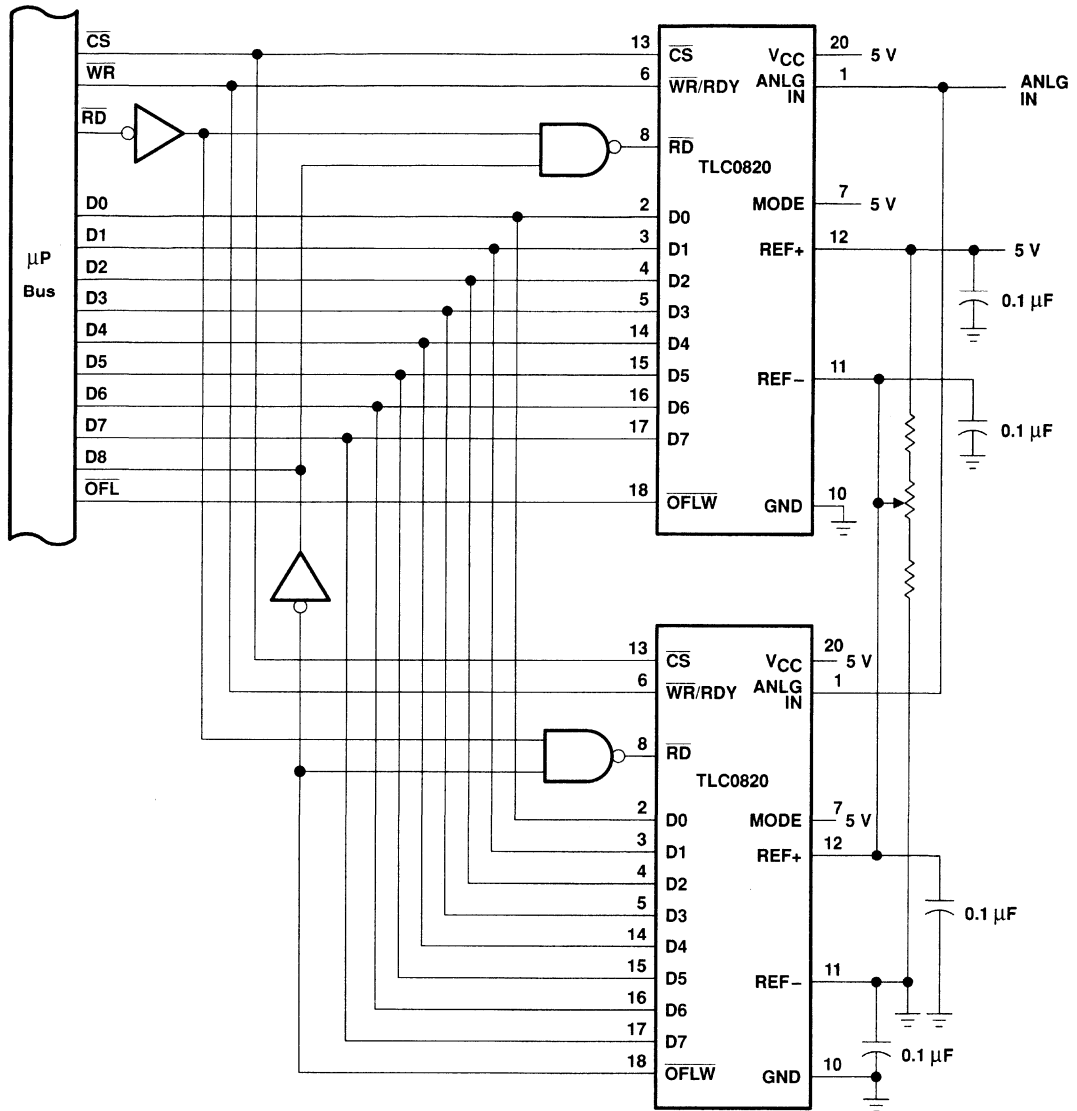


Figure 6. Configuration for 9-Bit Resolution



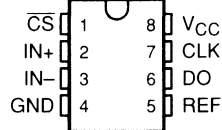
TLC0831C, TLC0831I TLC0832C, TLC0832I

8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

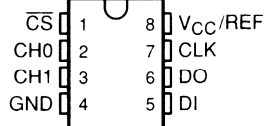
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- **8-Bit Resolution**
- **Easy Microprocessor Interface or Standalone Operation**
- **Operates Ratiometrically or With 5-V Reference**
- **Single Channel or Multiplexed Twin Channels With Single-Ended or Differential Input Options**
- **Input Range 0 to 5 V With Single 5-V Supply**
- **Inputs and Outputs Are Compatible With TTL and MOS**
- **Conversion Time of 32 μ s at $f_{\text{clock}} = 250$ kHz**
- **Designed to Be Interchangeable With National Semiconductor ADC0831 and ADC0832**
- **Total Unadjusted Error . . . ± 1 LSB**

TLC0831 . . . D OR P PACKAGE (TOP VIEW)



TLC0832 . . . D OR P PACKAGE (TOP VIEW)



description

These devices are 8-bit successive-approximation analog-to-digital converters. The TLC0831 has single input channels; the TLC0832 has multiplexed twin input channels. The serial output is configured to interface with standard shift registers or microprocessors.

The TLC0832 multiplexer is software configured for single-ended or differential inputs. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

The operation of the TLC0831 and TLC0832 devices is very similar to the more complex TLC0834 and TLC0838 devices. Ratiometric conversion can be attained by setting the REF input equal to the maximum analog input signal value, which gives the highest possible conversion resolution. Typically, REF is set equal to V_{CC} (done internally on the TLC0832).

The TLC0831C and TLC0832C are characterized for operation from 0°C to 70°C. The TLC0831I and TLC0832I are characterized for operation from -40°C to 85°C.

AVAILABLE OPTIONS

T _A	PACKAGE			
	SMALL OUTLINE (D)		PLASTIC DIP (P)	
0°C to 70°C	TLC0831CD	TLC0832CD	TLC0831CP	TLC0832CP
-40°C to 85°C	TLC0831ID	TLC0832ID	TLC0831IP	TLC0832IP

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

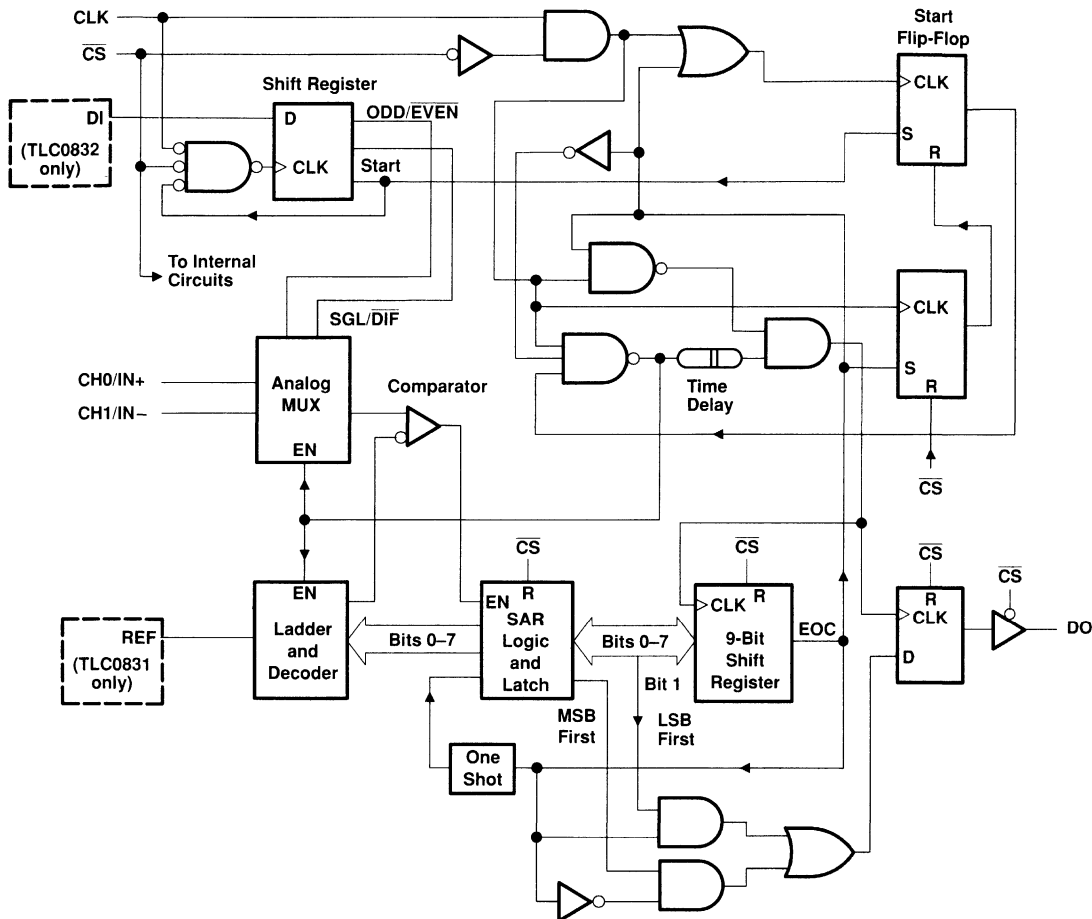
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TLC0831C, TLC0831I
TLC0832C, TLC0832I
8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL
 SLAS107B – JANUARY 1995 – REVISED APRIL 1996

functional block diagram



TLC0831C, TLC0831I
TLC0832C, TLC0832I

8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS107B – JANUARY 1995 – REVISED APRIL 1996

functional description

The TLC0831 and TLC0832 use a sample-data-comparator structure that converts differential analog inputs by a successive-approximation routine. The input voltage to be converted is applied to an input terminal and is compared to ground (single ended), or to an adjacent input (differential). The TLC0832 input terminals can be assigned a positive (+) or negative (–) polarity. The TLC0831 contains only one differential input channel with fixed polarity assignment; therefore it does not require addressing. The signal can be applied differentially, between IN+ and IN–, to the TLC0831 or can be applied to IN+ with IN– grounded as a single ended input. When the signal input applied to the assigned positive terminal is less than the signal on the negative terminal, the converter output is all zeros.

Channel selection and input configuration are under software control using a serial-data link from the controlling processor. A serial-communication format allows more functions to be included in a converter package with no increase in size. In addition, it eliminates the transmission of low-level analog signals by locating the converter at the analog sensor and communicating serially with the controlling processor. This process returns noise-free digital data to the processor.

A conversion is initiated by setting \overline{CS} low, which enables all logic circuits. \overline{CS} must be held low for the complete conversion process. A clock input is then received from the processor. An interval of one clock period is automatically inserted to allow the selected multiplexed channel to settle. DO comes out of the high-impedance state and provides a leading low for one clock period of multiplexer settling time. The SAR comparator compares successive outputs from the resistive ladder with the incoming analog signal. The comparator output indicates whether the analog input is greater than or less than the resistive-ladder output. As the conversion proceeds, conversion data is simultaneously output from DO, with the most significant bit (MSB) first. After eight clock periods, the conversion is complete. When \overline{CS} goes high, all internal registers are cleared. At this time, the output circuits go to the high-impedance state. If another conversion is desired, \overline{CS} must make a high-to-low transition followed by address information.

A TLC0832 input configuration is assigned during the multiplexer-addressing sequence. The multiplexer address shifts into the converter through the data input (DI) line. The multiplexer address selects the analog inputs to be enabled and determines whether the input is single ended or differential. When the input is differential, the polarity of the channel input is assigned. In addition to selecting the differential mode, the polarity may also be selected. Either channel of the channel pair may be designated as the negative or positive input.

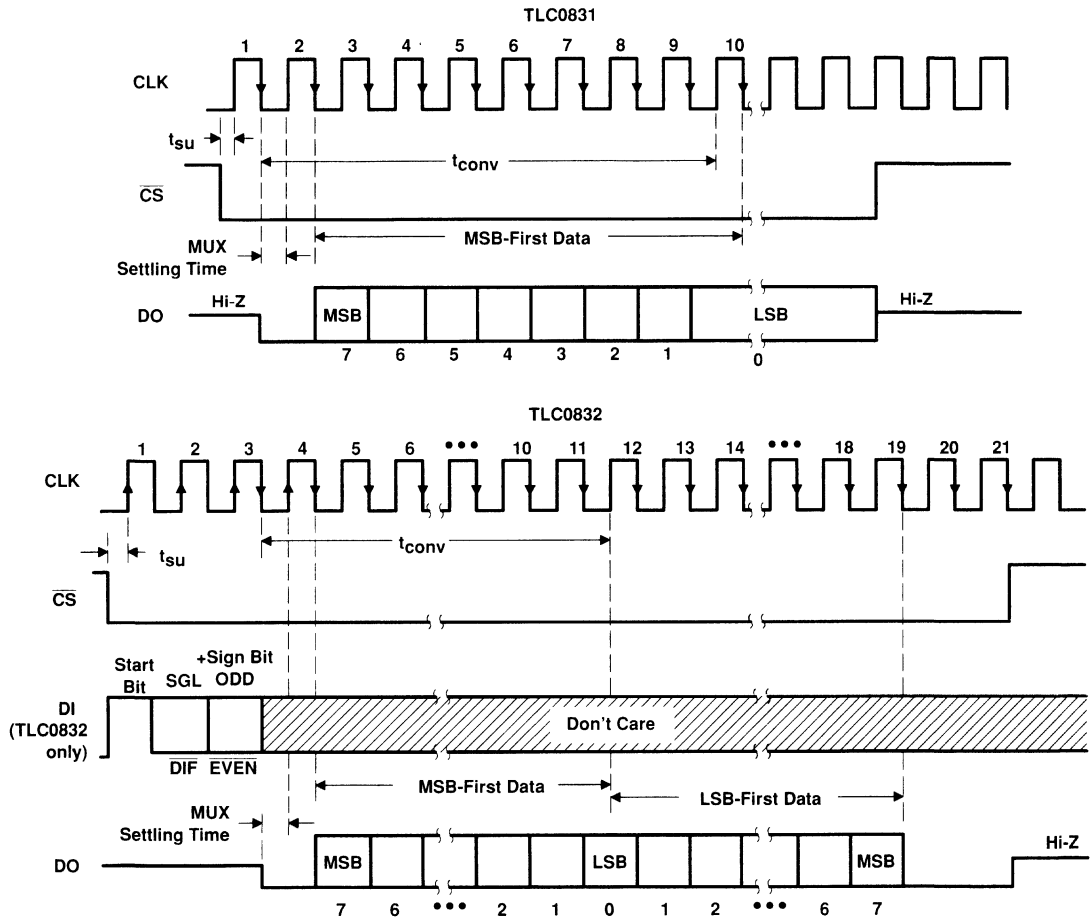
On each low-to-high transition of the clock input, the data on DI is clocked into the multiplexer-address shift register. The first logic high on the input is the start bit. A 2-bit assignment word follows the start bit on the TLC0832. On each successive low-to-high transition of the clock input, the start bit and assignment word are shifted through the shift register. When the start bit is shifted into the start location of the multiplexer register, the input channel is selected and conversion starts. The TLC0832 DI terminal to the multiplexer shift register is disabled for the duration of the conversion.

The TLC0832 outputs the least-significant-bit (LSB) first data after the MSB-first data stream. The DI and DO terminals can be tied together and controlled by a bidirectional processor I/O bit received on a single wire. This is possible because DI is only examined during the multiplexer-addressing interval and DO is still in the high-impedance state.



TLC0831C, TLC0831I
TLC0832C, TLC0832I
8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL
 SLAS107B – JANUARY 1995 – REVISED APRIL 1996

sequence of operation



TLC0832 MUX-ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS		CHANNEL NUMBER	
SGL/DIF	ODD/EVEN	CH0	CH1
L	L	+	-
L	H	-	+
H	L	+	-
H	H	-	+

H = high level, L = low level,
 - or + = terminal polarity for the selected input channel

TLC0831C, TLC0831I
TLC0832C, TLC0832I
8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS107B – JANUARY 1995 – REVISED APRIL 1996

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range, V_I : Logic	–0.3 V to $V_{CC} + 0.3$ V
Analog	–0.3 V to $V_{CC} + 0.3$ V
Input current, I_I	±5 mA
Total input current	±20 mA
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Clock frequency, f_{clock}	10		600	kHz
Clock duty cycle (see Note 2)	40%		60%	
Pulse duration, \overline{CS} high, $t_{wH}(\overline{CS})$	220			ns
Setup time, \overline{CS} low or TLC0832 data valid before $CLK\uparrow$, t_{SU}	350			ns
Hold time, TLC0832 data valid after $CLK\uparrow$, t_H	90			ns
Operating free-air temperature, T_A	C suffix	0	70	°C
	I suffix	–40	85	

NOTE 2: The clock-duty-cycle range ensures proper operation at all clock frequencies. When a clock frequency is used outside the recommended duty-cycle range, the minimum pulse duration (high or low) is 1 μ s.



TLC0831C, TLC0831I
TLC0832C, TLC0832I
8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS107B – JANUARY 1995 – REVISED APRIL 1996

electrical characteristics over recommended range of operating free-air temperature, $V_{CC} = 5\text{ V}$, $f_{\text{clock}} = 250\text{ kHz}$ (unless otherwise noted)

digital section

PARAMETER	TEST CONDITIONS†	C SUFFIX			I SUFFIX			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH} High-level output voltage	$V_{CC} = 4.75\text{ V}$, $I_{OH} = -360\text{ }\mu\text{A}$	2.8			2.4			V
	$V_{CC} = 4.75\text{ V}$, $I_{OH} = -10\text{ }\mu\text{A}$	4.6			4.5			
V_{OL} Low-level output voltage	$V_{CC} = 4.75\text{ V}$, $I_{OL} = 1.6\text{ mA}$	0.34			0.4			V
I_{IH} High-level input current	$V_{IH} = 5\text{ V}$		0.005	1		0.005	1	μA
I_{IL} Low-level input current	$V_{IL} = 0$		-0.005	-1		-0.005	-1	μA
I_{OH} High-level output (source) current	$V_{OH} = V_{OH(A)} - 25^\circ\text{C}$	-6.5	-24		-6.5	-24		mA
I_{OL} Low-level output (sink) current	$V_{OL} = V_{CC}$, $T_A = 25^\circ\text{C}$	8	26		8	26		mA
I_{OZ} High-impedance-state output current (DO)	$V_O = 5\text{ V}$, $T_A = 25^\circ\text{C}$		0.01	3		0.01	3	μA
	$V_O = 0$, $T_A = 25^\circ\text{C}$		-0.01	-3		-0.01	-3	
C_i Input capacitance			5			5		pF
C_o Output capacitance			5			5		pF

† All parameters are measured under open-loop conditions with zero common-mode input voltage.

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

analog and converter section

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IC}	Common-mode input voltage	See Note 3	-0.05	to	$V_{CC} + 0.05$	V
$I_{I(\text{stbdy})}$	Standby input current (see Note 4)	On channel	$V_I = 5\text{ V}$		1	μA
		Off channel	$V_I = 0$		-1	
		On channel	$V_I = 0$		-1	
		Off channel	$V_I = 5\text{ V}$		1	
$r_{I(\text{REF})}$	Input resistance to REF		1.3	2.4	5.9	k Ω

† All parameters are measured under open-loop conditions with zero common-mode input voltage.

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

NOTES: 3. When channel IN^- is more positive than channel IN^+ , the digital output code is 0000 0000. Connected to each analog input are two on-chip diodes that conduct forward current for analog input voltages one diode drop above V_{CC} . Care must be taken during testing at low V_{CC} levels (4.5 V) because high-level analog input voltage (5 V) can, especially at high temperatures, cause the input diode to conduct and cause errors for analog inputs that are near full scale. As long as the analog voltage does not exceed the supply voltage by more than 50 mV, the output code is correct. To achieve an absolute 0- to 5-V input range requires a minimum V_{CC} of 4.95 V for all variations of temperature and load.

4. Standby input currents go in or out of the on or off channels when the A/D converter is not performing conversion and the clock is in a high or low steady-state conditions.

total device

PARAMETER		MIN	TYP‡	MAX	UNIT
I_{CC}	Supply current		0.6	1.25	mA
			2.5	4.7	

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

TLC0831C, TLC0831I
TLC0832C, TLC0832I
8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL
SLAS107B – JANUARY 1995 – REVISED APRIL 1996

operating characteristics $V_{CC} = V_{ref} = 5\text{ V}$, $f_{clock} = 250\text{ kHz}$, $t_r = t_f = 20\text{ ns}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Supply-voltage variation error		$V_{CC} = 4.75\text{ V to }5.25\text{ V}$		$\pm 1/16$	$\pm 1/4$	LSB
Total unadjusted error (see Note 5)		$V_{ref} = 5\text{ V}$, $T_A = \text{MIN to MAX}$			± 1	LSB
Common-mode error		Differential mode		$\pm 1/16$	$\pm 1/4$	LSB
t_{pd}	Propagation delay time, output data after $\text{CLK}\uparrow$ (see Note 6)	MSB-first data	$C_L = 100\text{ pF}$	650	1500	ns
		LSB-first data		250	600	
t_{dis}	Output disable time, DO after $\overline{\text{CS}}\uparrow$	$C_L = 10\text{ pF}$, $R_L = 10\text{ k}\Omega$		125	250	ns
		$C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$			500	
t_{conv}	Conversion time (multiplexer-addressing time not included)				8	clock periods

† All parameters are measured under open-loop conditions with zero common-mode input voltage. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 5. Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

6. The MSB-first data is output directly from the comparator and, therefore, requires additional delay to allow for comparator response time. LSB-first data applies only to TLC0832.



TLC0831C, TLC0831I
TLC0832C, TLC0832I
8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL
SLAS107B – JANUARY 1995 – REVISED APRIL 1996

PARAMETER MEASUREMENT INFORMATION

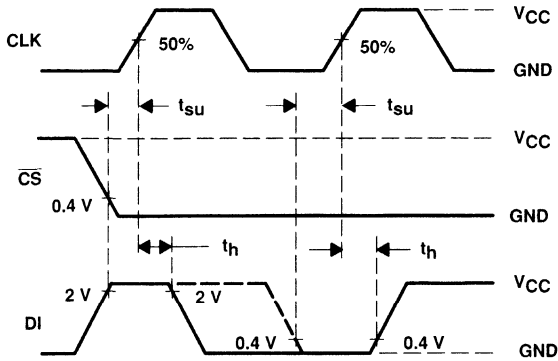


Figure 1. TLC0832 Data-Input Timing

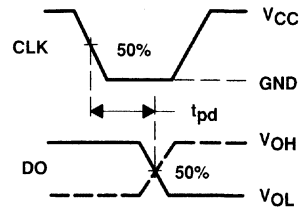
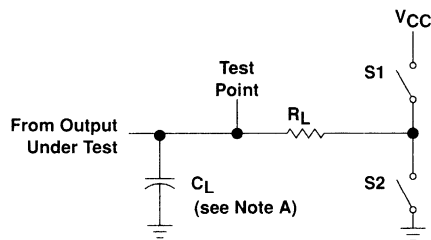
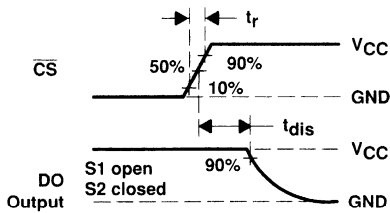


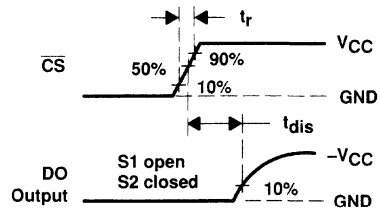
Figure 2. Data-Output Timing



LOAD CIRCUIT



VOLTAGE WAVEFORMS

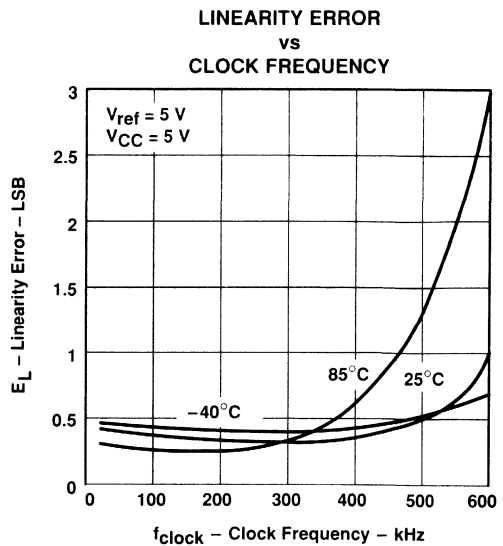
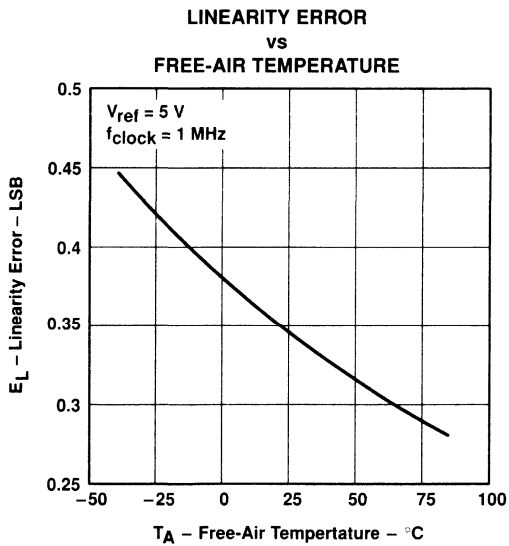
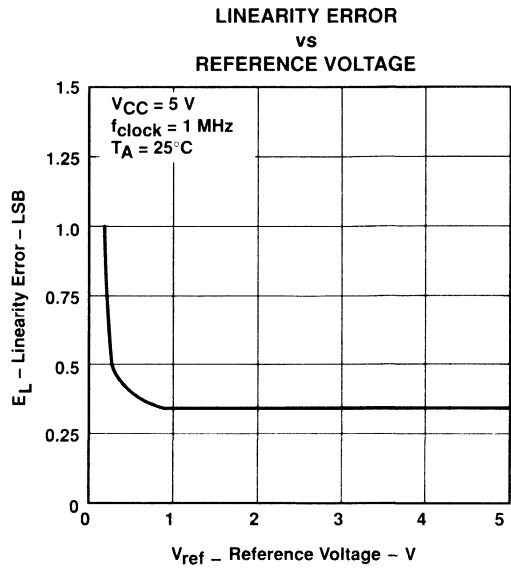
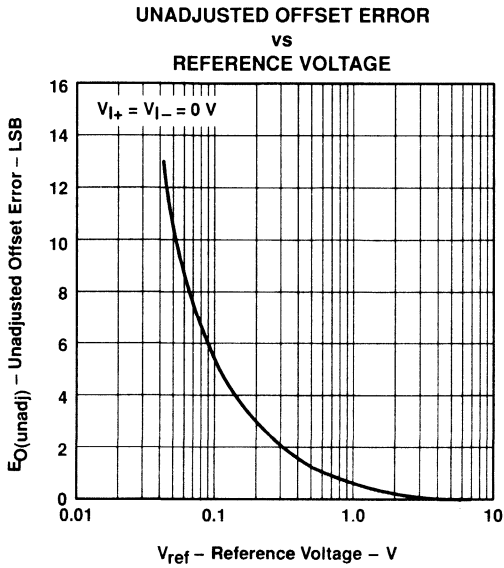


VOLTAGE WAVEFORMS

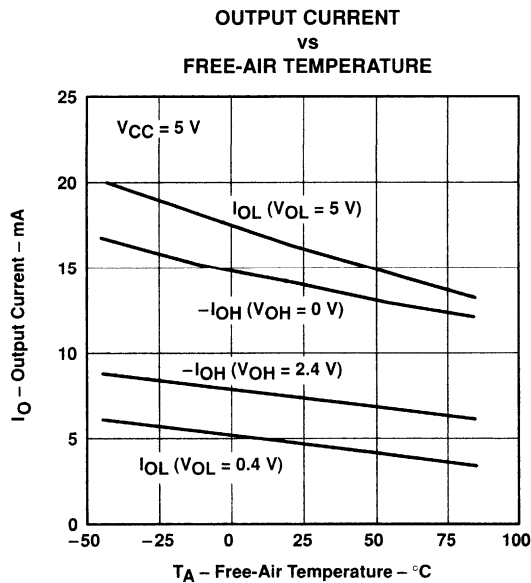
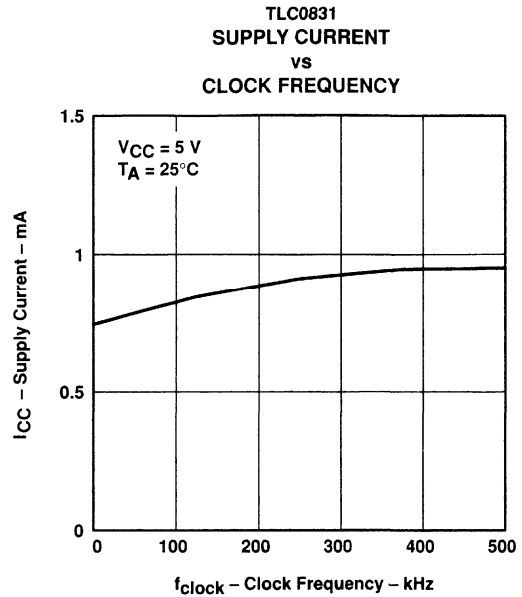
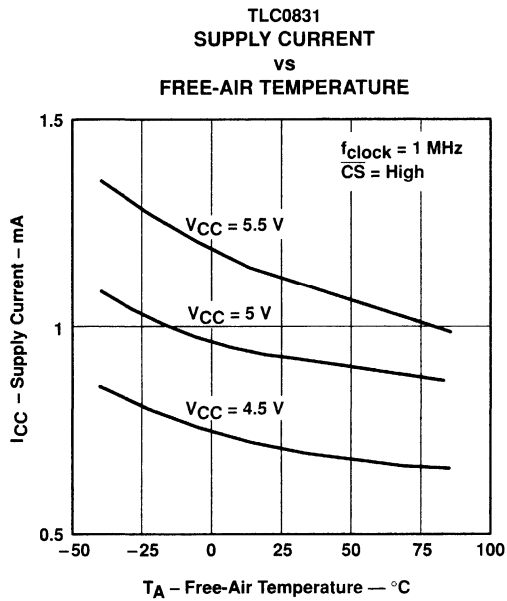
NOTE A: C_L includes probe and jig capacitance.

Figure 3. Output Disable Time Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



TLC0831C, TLC0831I
TLC0832C, TLC0832I
8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL
SLAS107B – JANUARY 1995 – REVISED APRIL 1996

TYPICAL CHARACTERISTICS

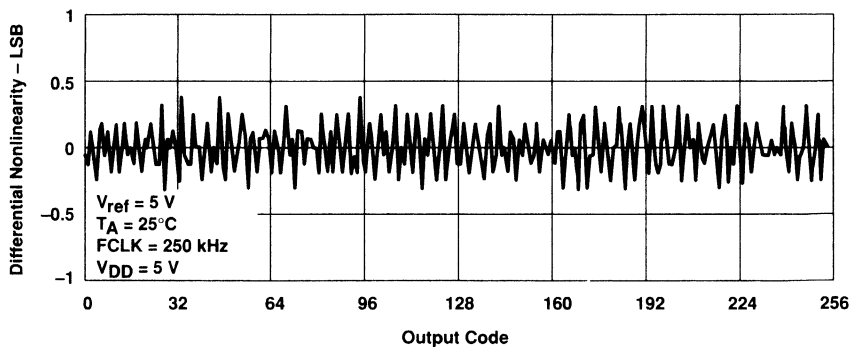


Figure 11. Differential Nonlinearity With Output Code

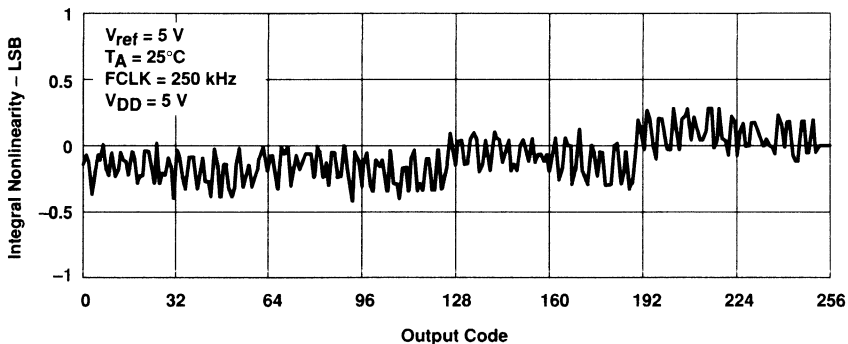


Figure 12. Integral Nonlinearity With Output Code

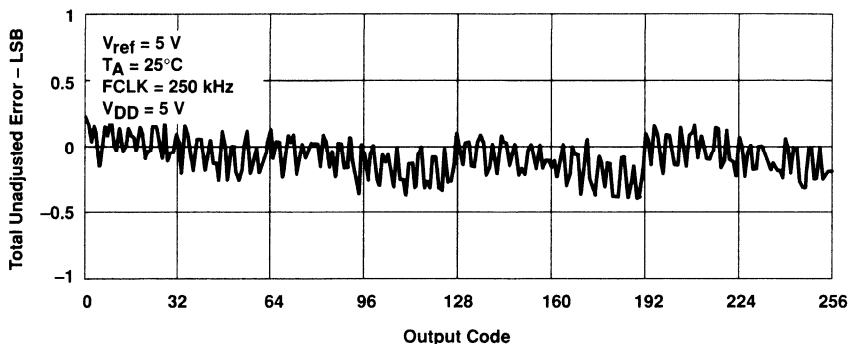


Figure 13. Total Unadjusted Error With Output Code

TLC0834C, TLC0834I, TLC0838C, TLC0838I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS094C – MARCH 1995 – REVISED APRIL 1997

- 8-Bit Resolution
- Easy Microprocessor Interface or Stand-Alone Operation
- Operates Ratiometrically or With 5-V Reference
- 4- or 8-Channel Multiplexer Options With Address Logic
- Input Range 0 to 5 V With Single 5-V Supply
- Remote Operation With Serial Data Link
- Inputs and Outputs Are Compatible With TTL and MOS
- Conversion Time of 32 μ s at $f_{\text{clock}} = 250$ kHz
- Functionally Equivalent to the ADC0834 and ADC0838 Without the Internal Zener Regulator Network
- Total Unadjusted Error . . . ± 1 LSB

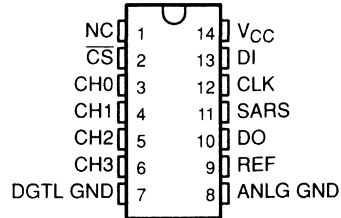
description

These devices are 8-bit successive-approximation analog-to-digital converters, each with an input-configurable multichannel multiplexer and serial input/output. The serial input/output is configured to interface with standard shift registers or microprocessors. Detailed information on interfacing with most popular microprocessors is readily available from the factory.

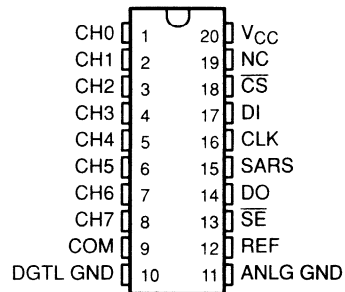
The TLC0834 (4-channel) and TLC0838 (8-channel) multiplexer is software configured for single-ended or differential inputs as well as pseudo-differential input assignments. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding of any smaller analog voltage span to the full 8 bits of resolution.

The TLC0834C and TLC0838C are characterized for operation from 0°C to 70°C. The TLC0834I and TLC0838I are characterized for operation from –40°C to 85°C. The TLC0834Q is characterized for operation from –40°C to 125°C.

TLC0834 . . . D OR N PACKAGE
(TOP VIEW)



TLC0838 . . . DW OR N PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T _A	PACKAGE		
	SMALL OUTLINE (D)	SMALL OUTLINE (DW)	PLASTIC DIP (N)
0°C to 70°C	TLC0834CD	TLC0838CDW	TLC0834CN TLC0838CN
–40°C to 85°C	TLC0834ID	TLC0838IDW	TLC0834IN TLC0838IN
–40°C to 125°C	—	—	TLC0834QN —

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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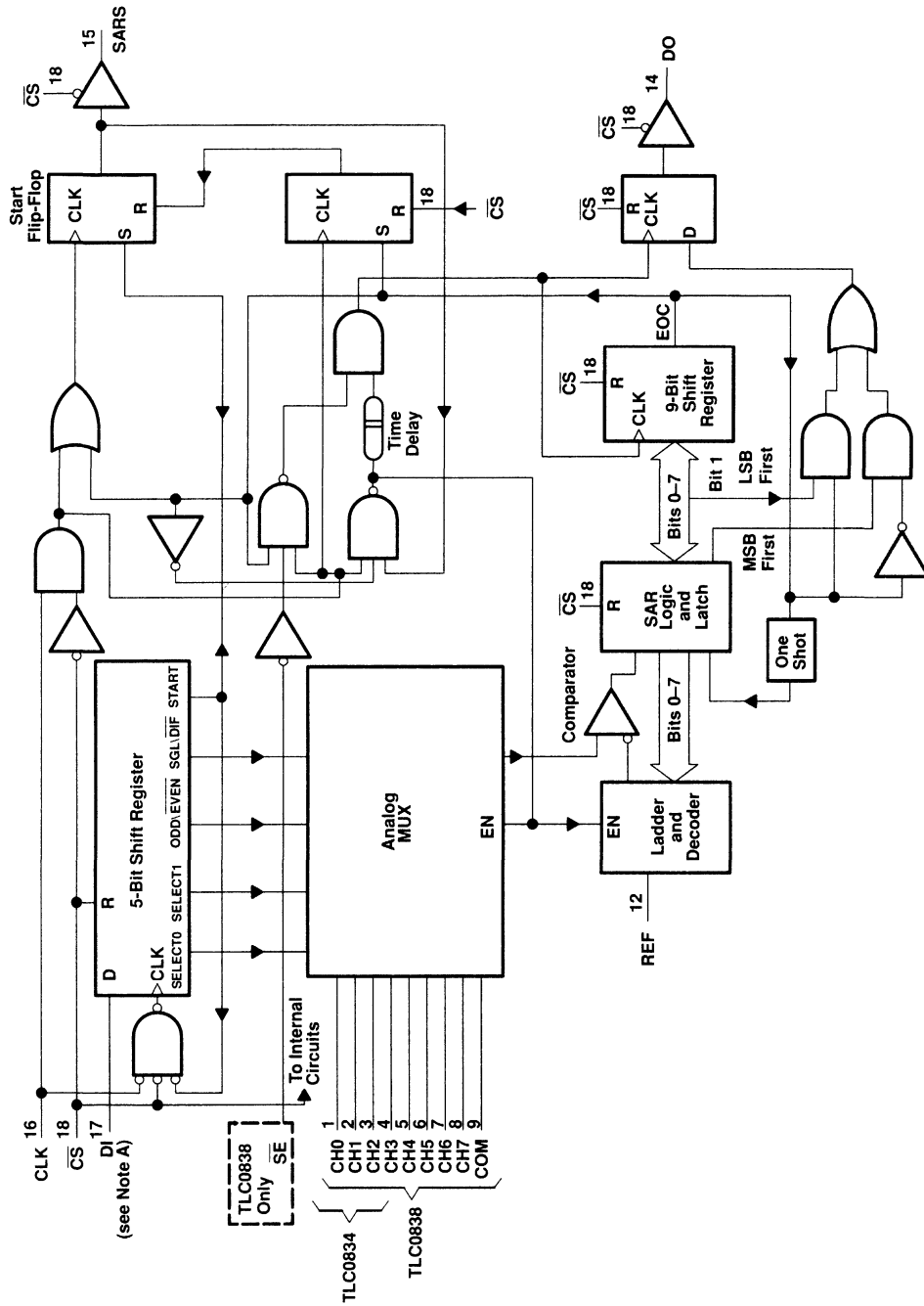
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TLC0834C, TLC0834I, TLC0838C, TLC0838I

8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS094C – MARCH 1995 – REVISED APRIL 1997

functional block diagram



NOTE A: For the TLC0834, DI is input directly to the D input of SELECT1; SELECT0 is forced to a high.
 B: Terminal numbers shown are for the DW or N package.

TLC0834C, TLC0834I, TLC0838C, TLC0838I

8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS094C – MARCH 1995 – REVISED APRIL 1997

functional description

The TLC0834 and TLC0838 use a sample-data-comparator structure that converts differential analog inputs by a successive-approximation routine. Operation of both devices is similar with the exception of \overline{SE} , an analog common input, and multiplexer addressing. The input voltage to be converted is applied to a channel terminal and is compared to ground (single ended), to an adjacent input (differential), or to a common terminal (pseudo differential) that can be an arbitrary voltage. The input terminals are assigned a positive (+) or negative (–) polarity. When the signal input applied to the assigned positive terminal is less than the signal on the negative terminal, the converter output is all zeros.

Channel selection and input configuration are under software control using a serial-data link from the controlling processor. A serial-communication format allows more functions to be included in a converter package with no increase in size. In addition, it eliminates the transmission of low-level analog signals by locating the converter at the analog sensor and communicating serially with the controlling processor. This process returns noise-free digital data to the processor.

A particular input configuration is assigned during the multiplexer-addressing sequence. The multiplexer address shifts into the converter through the data input (DI) line. The multiplexer address selects the analog inputs to be enabled and determines whether the input is single ended or differential. When the input is differential, the polarity of the channel input is assigned. Differential inputs are assigned to adjacent channel pairs. For example, channel 0 and channel 1 may be selected as a differential pair. These channels cannot act differentially with any other channel. In addition to selecting the differential mode, the polarity may also be selected. Either channel of the channel pair may be designated as the negative or positive input.

The common input on the TLC0838 can be used for a pseudo-differential input. In this mode, the voltage on the common input is considered to be the negative differential input for all channel inputs. This voltage can be any reference potential common to all channel inputs. Each channel input can then be selected as the positive differential input. This feature is useful when all analog circuits are biased to a potential other than ground.

A conversion is initiated by setting \overline{CS} low, which enables all logic circuits. \overline{CS} must be held low for the complete conversion process. A clock input is then received from the processor. On each low-to-high transition of the clock input, the data on DI is clocked into the multiplexer-address shift register. The first logic high on the input is the start bit. A 3- to 4-bit assignment word follows the start bit. On each successive low-to-high transition of the clock input, the start bit and assignment word are shifted through the shift register. When the start bit is shifted into the start location of the multiplexer register, the input channel is selected and conversion starts. The SAR status output (SARS) goes high to indicate that a conversion is in progress, and DI to the multiplexer shift register is disabled for the duration of the conversion.

An interval of one clock period is automatically inserted to allow the selected multiplexed channel to settle. DO comes out of the high-impedance state and provides a leading low for one clock period of multiplexer settling time. The SAR comparator compares successive outputs from the resistive ladder with the incoming analog signal. The comparator output indicates whether the analog input is greater than or less than the resistive-ladder output. As the conversion proceeds, conversion data is simultaneously output from DO, with the most significant bit (MSB) first. After eight clock periods, the conversion is complete and SARS goes low.

The TLC0834 outputs the least-significant-bit (LSB) first data after the MSB-first data stream. When \overline{SE} is held high on the TLC0838, the value of the LSB remains on the data line. When \overline{SE} is forced low, the data is then clocked out as LSB-first data. (To output LSB first, \overline{SE} must first go low, then the data stored in the 9-bit shift register outputs LSB first.) When \overline{CS} goes high, all internal registers are cleared. At this time, the output circuits go to the high-impedance state. If another conversion is desired, \overline{CS} must make a high-to-low transition followed by address information.

DI and DO can be tied together and controlled by a bidirectional processor I/O bit received on a single wire. This is possible because DI is only examined during the multiplexer-addressing interval and DO is still in the high-impedance state.

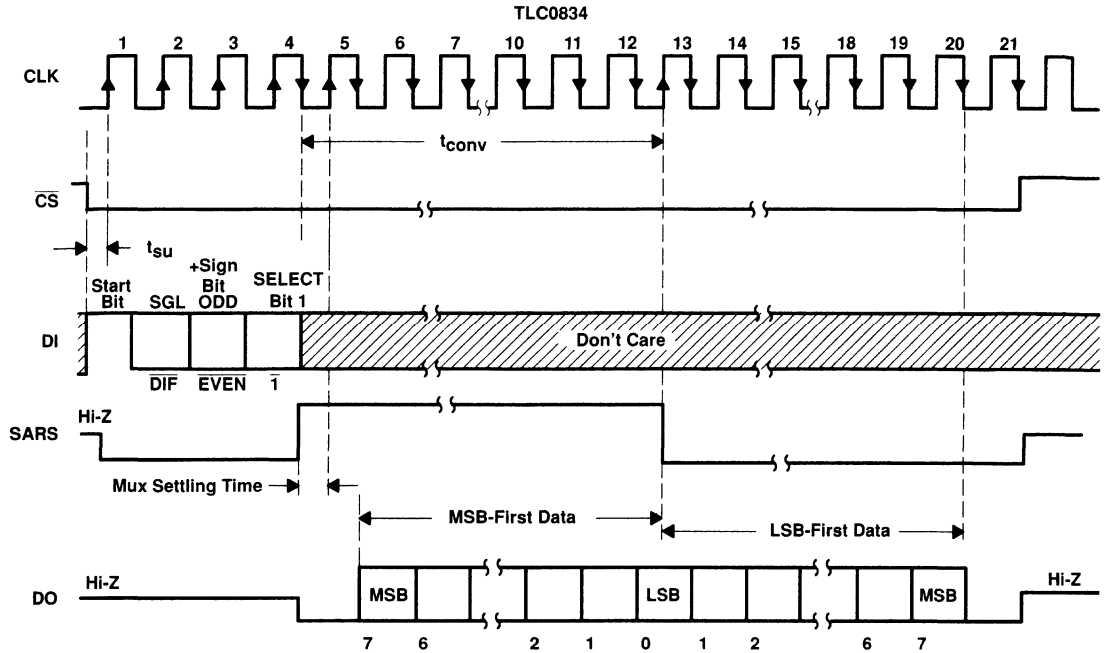


TLC0834C, TLC0834I, TLC0838C, TLC0838I

8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS094C – MARCH 1995 – REVISED APRIL 1997

sequence of operation



TLC0834 MUX-ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS			CHANNEL NUMBER			
SGL/DIF	ODD/EVEN	SELECT BIT 1	CH0	CH1	CH2	CH3
L	L	L	+	-		
L	L	H			+	-
L	H	L	-	+		
L	H	H			-	+
H	L	L	+			
H	L	H			+	
H	H	L		+		
H	H	H				+

H = high level, L = low level, - or + = terminal polarity for the selected input channel

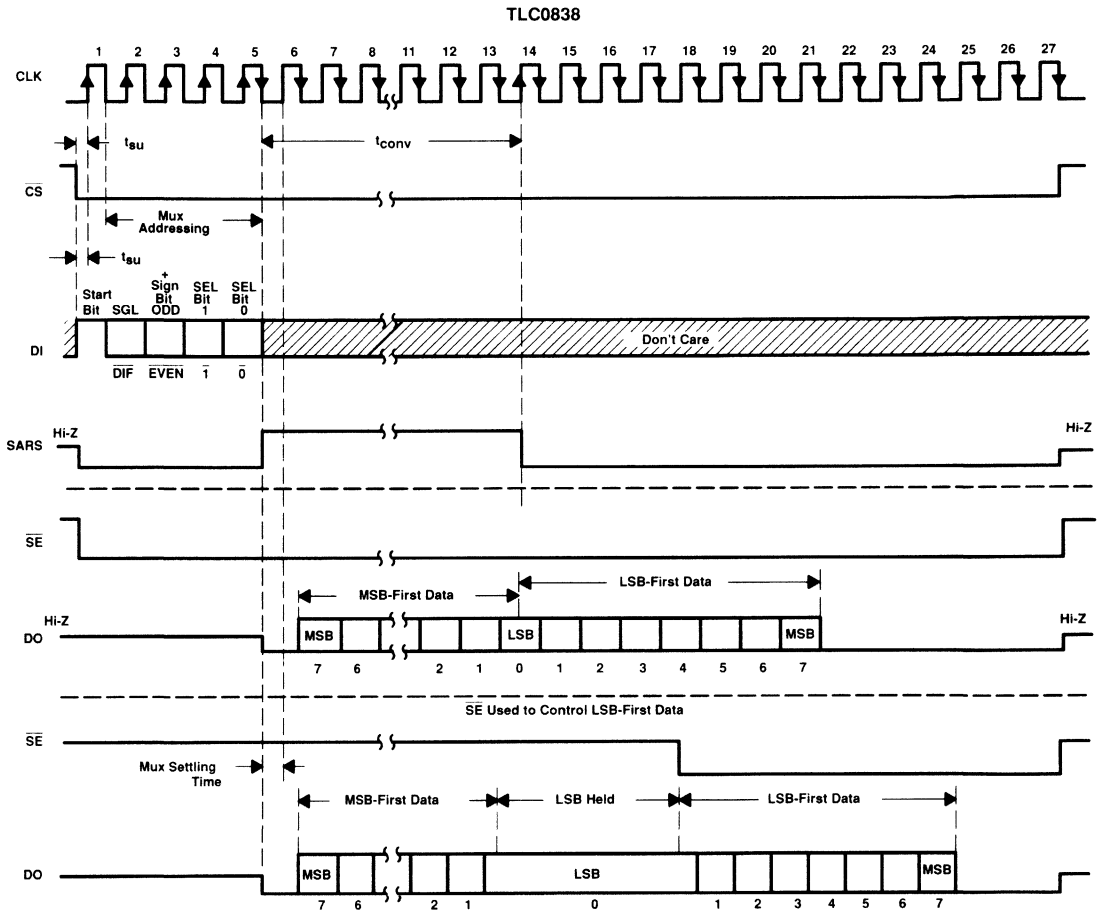


TLC0834C, TLC0834I, TLC0838C, TLC0838I

8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS094C – MARCH 1995 – REVISED APRIL 1997

sequence of operation



TLC0834C, TLC0834I, TLC0838C, TLC0838I

8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS094C – MARCH 1995 – REVISED APRIL 1997

TLC0838 MUX-ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS				SELECTED CHANNEL NUMBER								COM
SGL/DIF	ODD/EVEN	SELECT		0		1		2		3		
		1	0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	
L	L	L	L	+	-							
L	L	L	H			+	-					
L	L	H	L					+	-			
L	L	H	H							+	-	
L	H	L	L	-	+							
L	H	L	H			-	+					
L	H	H	L					-	+			
L	H	H	H							-	+	
H	L	L	L	+								-
H	L	L	H			+						-
H	L	H	L					+				-
H	L	H	H							+		-
H	H	L	L		+							-
H	H	L	H				+					-
H	H	H	L						+			-
H	H	H	H								+	-

H = high level, L = low level, - or + = polarity of external input

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range: Logic	-0.3 V to $V_{CC} + 0.3$ V
Analog	-0.3 V to $V_{CC} + 0.3$ V
Input current, I_I	±5 mA
Total input current	±20 mA
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.



TLC0834C, TLC0834I, TLC0838C, TLC0838I

8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS094C – MARCH 1995 – REVISED APRIL 1997

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Clock frequency, f_{clock}		10		600	kHz
Clock duty cycle (see Note 2)		40%		60%	
Pulse duration, CS high, $t_{wH}(CS)$		220			ns
Setup time, CS low, SE low, or data valid before CLK \uparrow , t_{SU} (see Figures 1 and 2)		350			ns
Hold time, data valid after CLK \uparrow , t_h (see Figure 1)		90			ns
Operating free-air temperature, T_A	C suffix	0		70	°C
	I suffix	-40		85	

NOTE 2: The clock-duty-cycle range ensures proper operation at all clock frequencies. When a clock frequency is used outside the recommended duty-cycle range, the minimum pulse duration (high or low) is 1 μ s.

electrical characteristics over recommended range of operating free-air temperature, $V_{CC} = 5$ V, $f_{clock} = 250$ kHz (unless otherwise noted)

digital section

PARAMETER	TEST CONDITIONS†	C SUFFIX			I SUFFIX			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH} High-level output voltage	$V_{CC} = 4.75$ V, $I_{OH} = -360$ μ A	2.8			2.4			V
	$V_{CC} = 4.75$ V, $I_{OH} = -10$ μ A	4.6			4.5			
V_{OL} Low-level output voltage	$V_{CC} = 5.25$ V, $I_{OL} = 1.6$ mA			0.34			0.4	V
I_{IH} High-level input current	$V_{IH} = 5$ V, $V_{IL} = 5$ V		0.005	1		0.005	1	μ A
I_{IL} Low-level input current	$V_{IL} = 0$, $V_{IH} = 0$		-0.005	-1		-0.005	-1	μ A
I_{OH} High-level output (source) current	$V_{OH} = 0$, $T_A = 25^\circ$ C	-6.5		-24	-6.5		-24	mA
I_{OL} Low-level output (sink) current	$V_{OL} = V_{CC}$, $T_A = 25^\circ$ C	8		26	8		26	mA
I_{OZ} High-impedance-state output current (DO or SARS)	$V_O = 5$ V, $T_A = 25^\circ$ C		0.01	3		0.01	3	μ A
	$V_O = 0$, $T_A = 25^\circ$ C		-0.01	-3		-0.01	-3	
C_i Input capacitance						5		pF
C_o Output capacitance						5		pF

† All parameters are measured under open-loop conditions with zero common-mode input voltage (unless otherwise specified).

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ$ C.



TLC0834C, TLC0834I, TLC0838C, TLC0838I

8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS094C – MARCH 1995 – REVISED APRIL 1997

analog and converter section

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IC}	Common-mode input voltage	See Note 3	-0.05 to $V_{CC}+0.05$			V
$I_{I}(\text{stdby})$	Standby input current (see Note 4)	On channel	$V_I = 5\text{ V}$		1	μA
		Off channel	$V_I = 0$		-1	
		On channel	$V_I = 0$		-1	
		Off channel	$V_I = 5\text{ V}$		1	
$r_{i}(\text{REF})$	Input resistance to REF		1.3	2.4	5.9	$k\Omega$

total device

PARAMETER		MIN	TYP‡	MAX	UNIT
I_{CC}	Supply current		0.6	1.25	mA

† All parameters are measured under open-loop conditions with zero common-mode input voltage.

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

NOTES: 3. When channel IN- is more positive than channel IN+, the digital output code is 0000 0000. Connected to each analog input are two on-chip diodes that conduct forward current for analog input voltages one diode drop above V_{CC} . Care must be taken during testing at low V_{CC} levels (4.5 V) because high-level analog input voltage (5 V) can, especially at high temperatures, cause the input diode to conduct and cause errors for analog inputs that are near full scale. As long as the analog voltage does not exceed the supply voltage by more than 50 mV, the output code is correct. To achieve an absolute 0- to 5-V input range requires a minimum V_{CC} of 4.950 V for all variations of temperature and load.

4. Standby input currents go in or out of the on or off channels when the A/D converter is not performing conversion and the clock is in a high or low steady-state condition.

operating characteristics, $V_{CC} = 5\text{ V}$, $f_{\text{clock}} = 250\text{ kHz}$, $t_r = t_f = 20\text{ ns}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS§	MIN	TYP	MAX	UNIT
Supply-voltage variation error		$V_{CC} = 4.75\text{ V to }5.25\text{ V}$		$\pm 1/16$	$\pm 1/4$	LSB
Total unadjusted error (see Note 5)		$V_{\text{ref}} = 5\text{ V}$, $T_A = \text{MIN to MAX}$			± 1	LSB
Common-mode error		Differential mode		$\pm 1/16$	$\pm 1/4$	LSB
t_{pd}	Propagation delay time, output data after CLK↓ (see Note 6) (see Figure 2)	MSB-first data	$C_L = 100\text{ pF}$		1500	ns
		LSB-first data		600		
t_{dis}	Output disable time, DO or SARS after CS↑ (see Figure 3)	$C_L = 10\text{ pF}$, $R_L = 10\text{ k}\Omega$			250	ns
		$C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$			500	
t_{conv}	Conversion time (multiplexer-addressing time not included)				8	clock periods

§ All parameters are measured under open-loop conditions with zero common-mode input voltage. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 5. Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

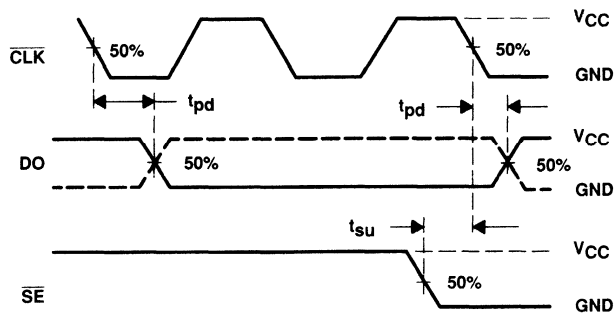
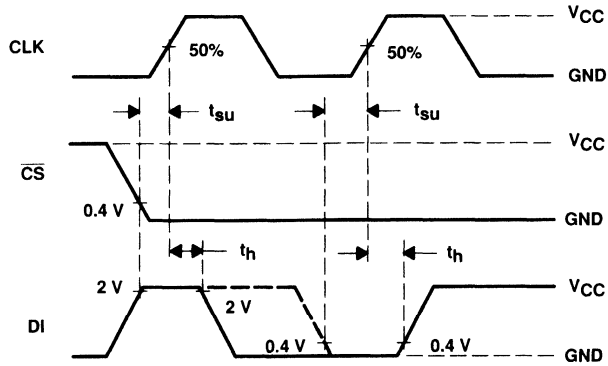
6. The MSB-first data is output directly from the comparator and, therefore, requires additional delay to allow for comparator response time.



TLC0834C, TLC0834I, TLC0838C, TLC0838I
 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS094C – MARCH 1995 – REVISED APRIL 1997

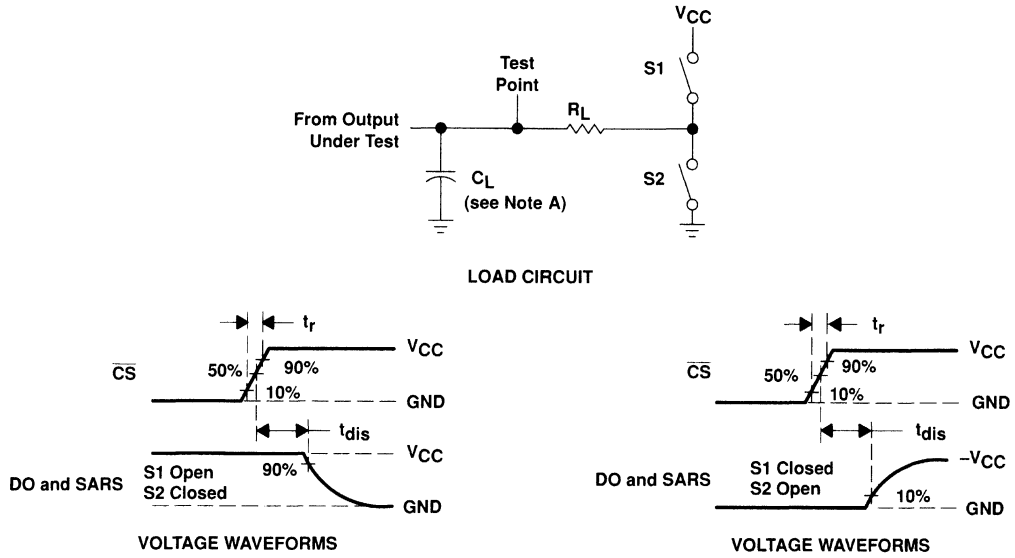
PARAMETER MEASUREMENT INFORMATION



TLC0834C, TLC0834I, TLC0838C, TLC0838I
8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS094C – MARCH 1995 – REVISED APRIL 1997

PARAMETER MEASUREMENT INFORMATION



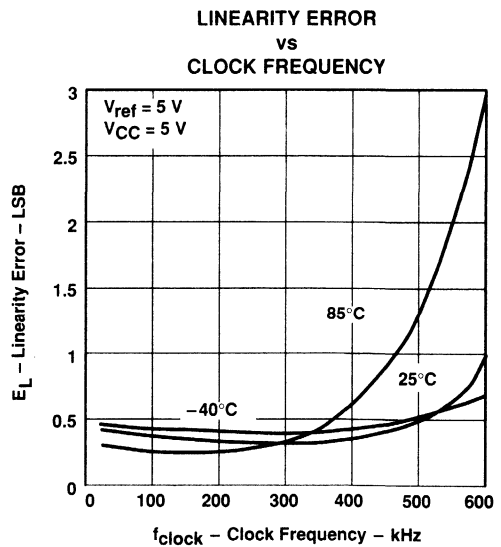
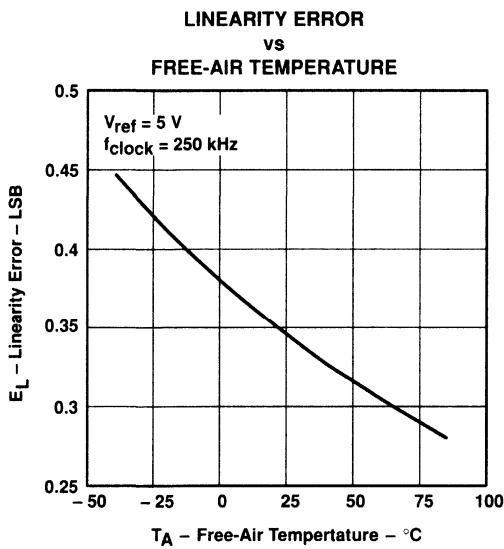
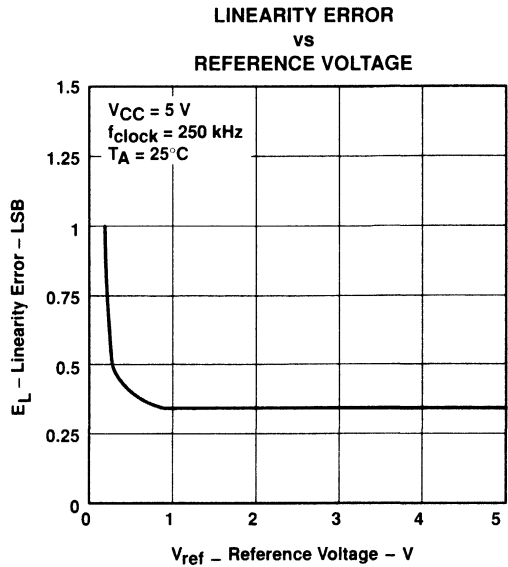
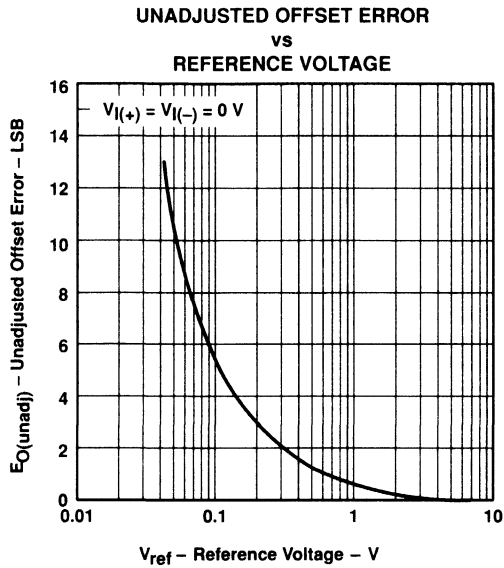
NOTE A: C_L includes probe and jig capacitance.

Figure 3. Output Disable Time Test Circuit and Voltage Waveforms

TLC0834C, TLC0834I, TLC0838C, TLC0838I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS094C – MARCH 1995 – REVISED APRIL 1997

TYPICAL CHARACTERISTICS



TLC0834C, TLC0834I, TLC0838C, TLC0838I
8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS094C – MARCH 1995 – REVISED APRIL 1997

TYPICAL CHARACTERISTICS

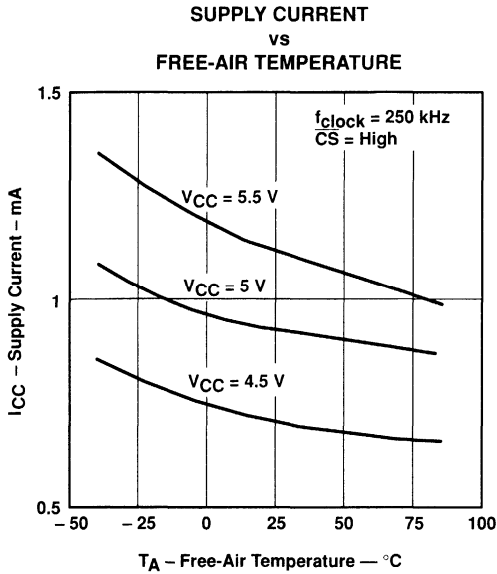


Figure 8

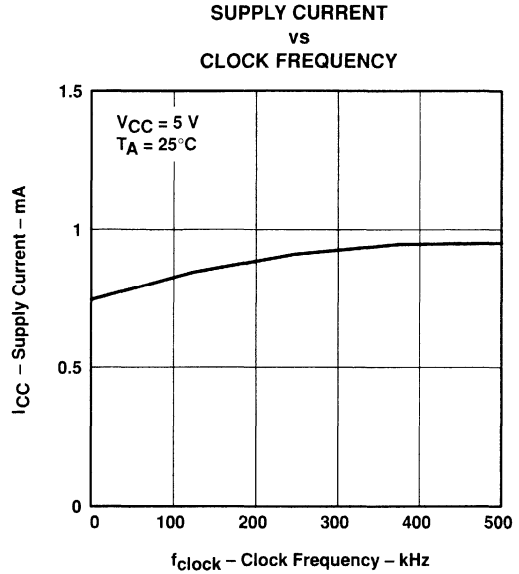


Figure 9

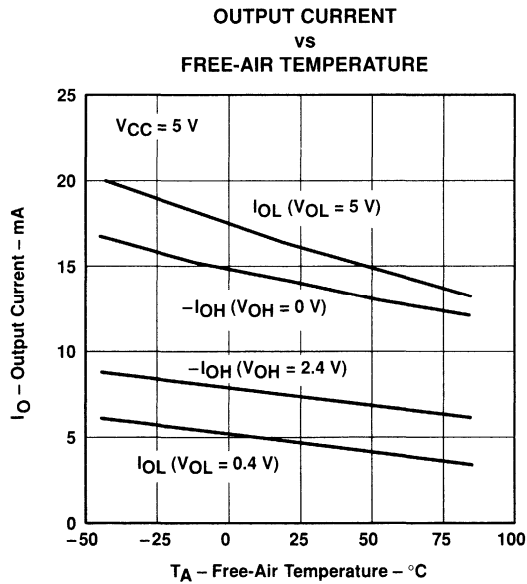


Figure 10

TLC0834C, TLC0834I, TLC0838C, TLC0838I
8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS094C – MARCH 1995 – REVISED APRIL 1997

TYPICAL CHARACTERISTICS

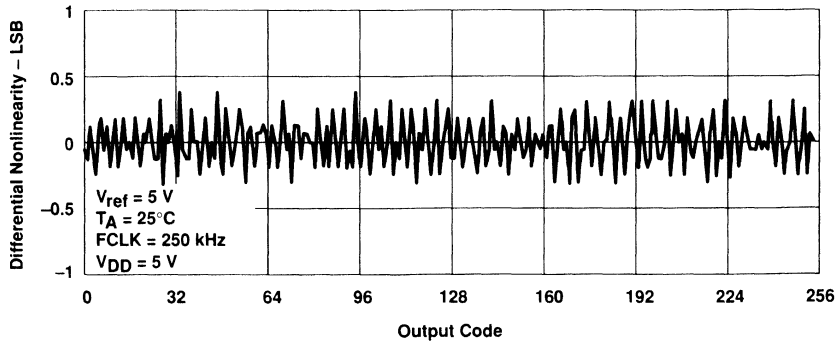


Figure 11. Differential Nonlinearity With Output Code

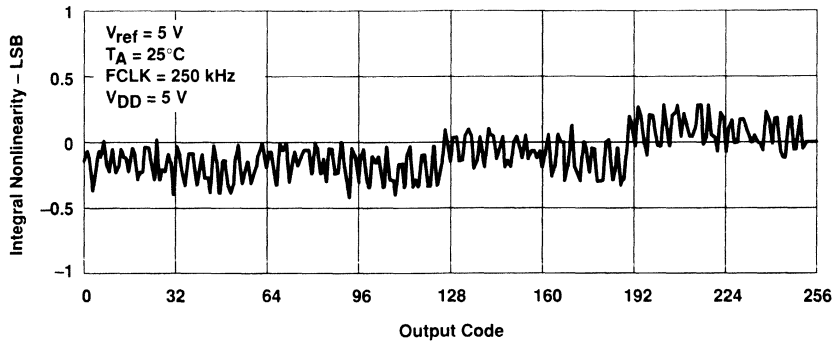


Figure 12. Integral Nonlinearity With Output Code

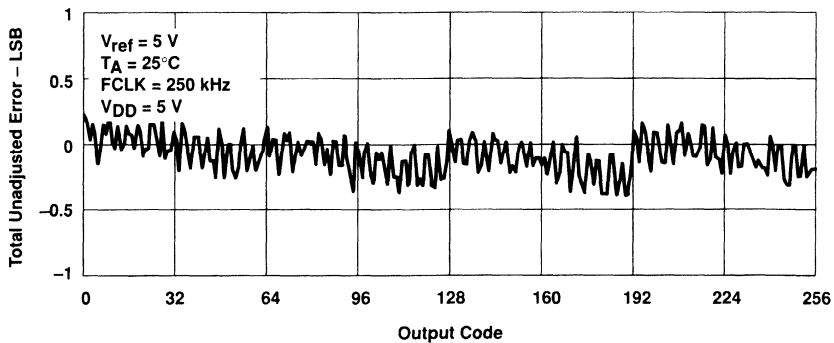
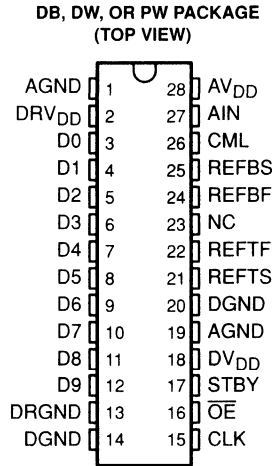


Figure 13. Total Unadjusted Error With Output Code

TLC876I, TLC876C
10-BIT 20 MSPS PARALLEL OUTPUT CMOS
ANALOG-TO-DIGITAL CONVERTERS
 SLAS140B – JULY 1997 – REVISED NOVEMBER 1997

- **10-Bit Resolution 20 MSPS Sampling Analog-to-Digital Converter (ADC)**
- **Power Dissipation . . . 107 mW Typ**
- **5-V Single Supply Operation**
- **Differential Nonlinearity . . . ± 0.5 LSB Typ**
- **No Missing Codes**
- **Power Down (Standby) Mode**
- **Three State Outputs**
- **Digital I/Os Compatible With 5-V or 3.3-V Logic**
- **Adjustable Reference Input**
- **Small Outline Package (SOIC), Super Small Outline Package (SSOP), or Thin Small Outline Package (TSOP)**
- **Pin Compatible With the Analog Devices AD876**



NC – No internal connection

applications

- **Communications**
- **Multimedia**
- **Digital Video Systems**
- **High-Speed DSP Front-End . . . TMS320C6x**

description

The TLC876 is a CMOS, low-power, 10-bit, 20 MSPS analog-to-digital converter (ADC). The speed, resolution, and single-supply operation are suited for applications in video, multimedia, imaging, high-speed acquisition, and communications. The low-power and single-supply operation satisfy requirements for high-speed portable applications. The speed and resolution ideally suit charge-coupled device (CCD) input systems such as color scanners, digital copiers, electronic still cameras, and camcorders. A multistage pipelined architecture with output error correction logic provides for no missing codes over the full operating temperature range. Force and sense connections to the reference inputs provide a more accurate internal reference voltage to the reference resistor string.

A standby mode of operation reduces the power to typically 15 mW. The digital I/O interfaces to either 5-V or 3.3-V logic and the digital output terminals can be placed in a high-impedance state. The format of the output data is straight binary coding.

A pipelined multistaged architecture achieves a high sample rate with low power consumption. The TLC876 distributes the conversion over several smaller ADC sub-blocks, refining the conversion with progressively higher accuracy as the device passes the results from stage to stage. This distributed conversion requires a small fraction of the 1023 comparators used in a traditional flash ADC. A sample-and-hold amplifier (SHA) within each of the stages permits the first stage to operate on a new input sample while the second through the fifth stages operate on the four preceding samples.

The TLC876C is characterized for operation from 0°C to 70°C, and the TLC876I is characterized for operation from –40°C to 85°C.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



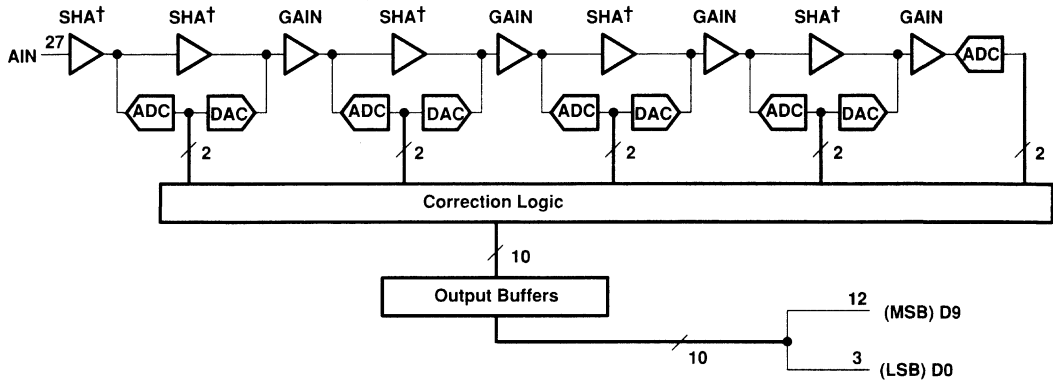
TLC876I, TLC876C
10-BIT 20 MSPS PARALLEL OUTPUT CMOS
ANALOG-TO-DIGITAL CONVERTERS

SLAS140B – JULY 1997 – REVISED NOVEMBER 1997

AVAILABLE OPTIONS

T _A	PACKAGE		
	SUPER SMALL OUTLINE (DB)	SMALL OUTLINE (DW)	TSSOP (PW)
0°C to 70°C	TLC876CDB	TLC876CDW	TLC876CPW
-40°C to 85°C	TLC876IDB	TLC876IDW	TLC876IPW

functional block diagram



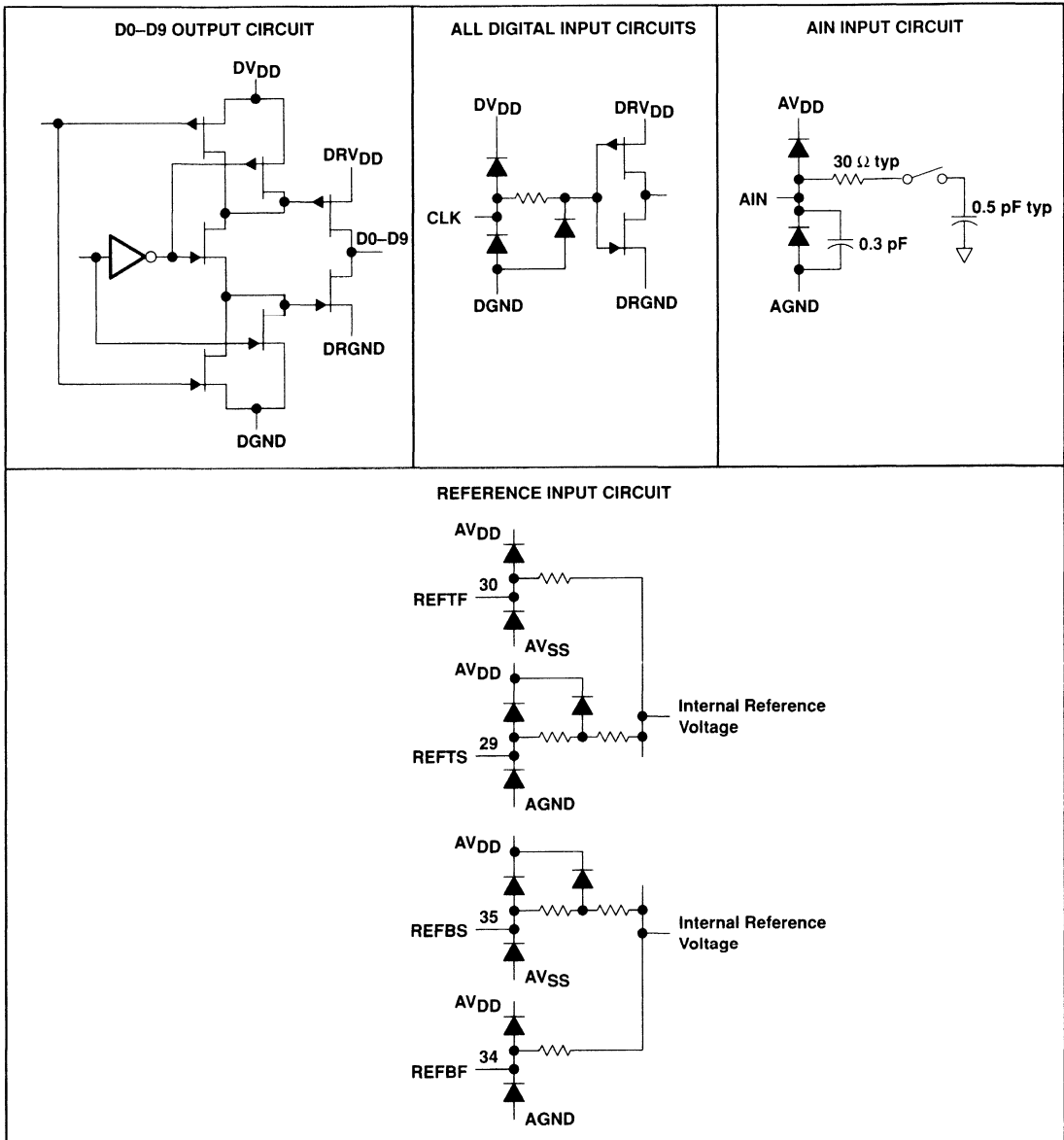
† Sample and hold amplifier



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TLC876I, TLC876C
 10-BIT 20 MSPS PARALLEL OUTPUT CMOS
 ANALOG-TO-DIGITAL CONVERTERS
 SLAS140B – JULY 1997 – REVISED NOVEMBER 1997

equivalent input and output circuits



TLC876I, TLC876C
10-BIT 20 MSPS PARALLEL OUTPUT CMOS
ANALOG-TO-DIGITAL CONVERTERS

SLAS140B – JULY 1997 – REVISED NOVEMBER 1997

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	1, 19		Analog ground
AIN	27	I	Analog input
AVDD	28		5-V analog supply
CLK	15	I	Clock input
CML	26	O	Bypass for an internal bias point. Typically a 0.1 μ F capacitor minimum is connected from this terminal to ground.
DGND	14, 20		Digital ground
DVDD	18		5-V digital supply
DRVDD	2		3.3-V/5-V digital supply. Supply for digital input and output buffers.
DRGND	13		3.3-V/5-V digital ground. Ground for digital input and output buffers.
D0–D9	3–12	O	Digital data out. D0:LSB, D9:MSB
\overline{OE}	16	I	Output enable. When \overline{OE} = low or NC, the device is in normal operating mode. When \overline{OE} = high, D0–D9 are high impedance.
REFBF	24	I	Reference bottom force
REFBS	25	I	Reference bottom sense
REFTF	22	I	Reference top force
REFTS	21	I	Reference top sense
STBY	17	I	Standby enable. When STBY = low or NC, the device is in normal operating mode. When STBY = high, the device is in standby mode.

TLC876I, TLC876C
10-BIT 20 MSPS PARALLEL OUTPUT CMOS
ANALOG-TO-DIGITAL CONVERTERS

SLAS140B – JULY 1997 – REVISED NOVEMBER 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, AV_{DD} to AGND, DV_{DD} to DGND	-0.3 V to 6.5 V
Reference voltage input range to AGND, $V_{I(REFTF)}$, $V_{I(REFBF)}$, $V_{I(REFBS)}$, $V_{I(REFTS)}$	-0.3 V to $AV_{DD} + 0.3$ V
Analog input voltage range to AGND	-0.3 V to $AV_{DD} + 0.3$ V
Digital input voltage range	-0.3 V to $DV_{DD} + 0.3$ V
Digital output voltage range applied from external source	-0.5 V to DV_{DD}
Operating virtual junction temperature range, T_J	-40°C to 150°C
Operating free-air temperature range, T_A : TLC876C	0°C to 70°C
TLC876I	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

analog and reference inputs

	MIN	NOM	MAX	UNIT
Reference input voltage (top), $V_{I(REFT)}$	$V_{I(REFB)} + 1$	3.6	4.5	V
Reference input voltage (bottom), $V_{I(REFB)}$	0	1.6	$V_{I(REFT)} - 1$	V
Analog input voltage, $V_{I(AIN)}$	1	2		V_{pp}

power supply

	MIN	NOM	MAX	UNIT
Supply voltage	$AV_{DD} ‡$	4.5	5.25	V
	$DV_{DD} ‡$	4.5	5.25	
	DRV_{DD}	3	5.25	

‡ The voltage difference between AV_{DD} and DV_{DD} terminals cannot exceed 0.5 V to maintain performance specifications.

digital inputs

	MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	$DRV_{DD} = 3$ V	2.4		V
	$DRV_{DD} = 5$ V	4		
	$DRV_{DD} = 5.25$ V	4.2		
Low-level input voltage, V_{IL}	$DRV_{DD} = 3$ V		0.6	V
	$DRV_{DD} = 5$ V		1	
	$DRV_{DD} = 5.25$ V		1.05	
Clock period, t_C (see Figure 1)		50		ns
Pulse duration, clock high, $t_w(\text{CLKH})$	23	25		ns
Pulse duration, clock low, $t_w(\text{CLKL})$	23	25		ns
Operating free-air temperature, T_A	TLC876C	0	70	°C
	TLC876I	-40	85	°C



TLC876I, TLC876C

10-BIT 20 MSPS PARALLEL OUTPUT CMOS

ANALOG-TO-DIGITAL CONVERTERS

SLAS140B – JULY 1997 – REVISED NOVEMBER 1997

electrical characteristics at $V_{DD} = DV_{DD} = 5\text{ V}$, $DRV_{DD} = 3.3\text{ V}$, $V_{I(REFT)} = 3.6\text{ V}$, $V_{I(REFB)} = 1.6\text{ V}$, $f_{CLK} = 20\text{ MSPS}$ (unless otherwise noted)

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Operating supply current	AV_{DD}^{\dagger}			17	25	mA
		DV_{DD}^{\dagger}			2.7	5	mA
		DRV_{DD}			25	100	μA
P_D	Power dissipation				107	150	mW
$P_{D(STBY)}$	Standby power	STBY = High	CLK running		45	85	mW
			CLK inhibited at V_{DD} or 0 V		15	35	

\dagger The voltage difference between AV_{DD} and DV_{DD} terminals cannot exceed 0.5 V to maintain performance specifications.

digital logic inputs

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	$DV_{DD} = 5\text{ V}$		-10		10	μA
I_{IL}	Low-level input current	$DV_{DD} = 5\text{ V}$		-50		50	
$I_{IL(CLK)}$	Low-level input current, CLK	$DV_{DD} = 5\text{ V}$		-10		10	μA
C_i	Input capacitance				5		pF

logic outputs

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = 50\ \mu\text{A}$	$DRV_{DD} = 3\text{ V}$	2.4			V
			$DRV_{DD} = 5\text{ V}$	3.8			
		$I_{OH} = 0.5\text{ mA}$	$DRV_{DD} = 5\text{ V}$	2.4			
V_{OL}	Low-level output voltage	$I_{OL} = 50\ \mu\text{A}$	$DRV_{DD} = 3.6\text{ V}$			0.7	V
			$DRV_{DD} = 5.25\text{ V}$			1.05	
		$I_{OL} = 0.6\text{ mA}$	$DRV_{DD} = 5.25\text{ V}$			0.4	
C_o	Output capacitance				5		pF
I_{OZ}	High-impedance-state output current			-10		10	μA

dc accuracy

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Integral nonlinearity (INL)					± 1.5		LSB
Differential nonlinearity (DNL) (see Note 1)					± 0.5	$< \pm 1$	
Offset error					-0.4		%FSR
Gain error					0.2		%FSR

NOTE 1: A differential nonlinearity error of less than ± 1 LSB ensures no missing codes.

analog input

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_i	Input capacitance				5		pF

reference input

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R_{ref}	Reference input resistance			350	500	750	Ω
I_{ref}	Reference input current				4		mA
Reference top offset voltage					35		mV
Reference bottom offset voltage					35		mV



TLC876I, TLC876C
10-BIT 20 MSPS PARALLEL OUTPUT CMOS
ANALOG-TO-DIGITAL CONVERTERS

SLAS140B – JULY 1997 – REVISED NOVEMBER 1997

operating characteristics at $V_{DD} = DV_{DD} = 5\text{ V}$, $DRV_{DD} = 3.3\text{ V}$, $V_{I(REFT)} = 3.6\text{ V}$, $V_{I(REFB)} = 1.6\text{ V}$, $f_{CLK} = 20\text{ MSPS}$ (unless otherwise noted)

dynamic performance†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Effective number of bits (ENOB)		$f_I = 1\text{ MHz}$		8.5		Bits
		$f_I = 3.58\text{ MHz}$	8	8.5		
		$f_I = 10\text{ MHz}$		8.1		
Signal-to-total harmonic distortion+noise (S/(THD+N))		$f_I = 1\text{ MHz}$		53		dB
		$f_I = 3.58\text{ MHz}$	50	53		
		$f_I = 10\text{ MHz}$		51		
Total harmonic distortion (THD)		$f_I = 1\text{ MHz}$		-63		dB
		$f_I = 3.58\text{ MHz}$		-62	-56	
		$f_I = 10\text{ MHz}$		-61		
Spurious free dynamic range		$f_I = 3.58\text{ MHz}$		-64		dB
BW	Analog input full-power bandwidth			200		MHz
Differential phase				0.5		degrees
Differential gain				1%		

† The voltage difference between AV_{DD} and DV_{DD} cannot exceed 0.5 V to maintain performance specifications. At input clock rise times less than 20 ns, the offset full-scale error increases approximately by a factor of $(20/t_r)^{0.5}$ where t_r equals the actual rise time in nanoseconds.

timing requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{conv}	Maximum conversion rate (see Note 2)		20			MHz
$t_{d(o)}$	Delay time, output	$C_L = 20\text{ pF}$	5	20		ns
$t_{d(pipe)}$	Delay time, pipeline, latency				3.5	Clock cycles
$t_{d(A)}$	Delay time, aperture			4		ns
	Aperture jitter			22		ps
$t_{dis(DD)}$	Disable time, $\overline{OE}\uparrow$ to Hi-Z	$C_L = 20\text{ pF}$		5	15	ns
$t_{en(HL)}$	Enable time, $\overline{OE}\downarrow$ to valid data			5	15	ns

NOTE 2: The conversion rate can be a minimum of 10 kHz without degradation in specified performance.



TLC876I, TLC876C
10-BIT 20 MSPS PARALLEL OUTPUT CMOS
ANALOG-TO-DIGITAL CONVERTERS

SLAS140B – JULY 1997 – REVISED NOVEMBER 1997

PARAMETER MEASUREMENT INFORMATION

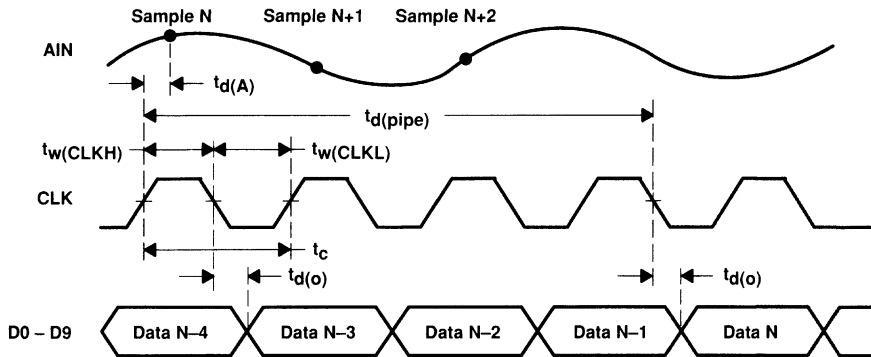


Figure 1. Timing Diagram

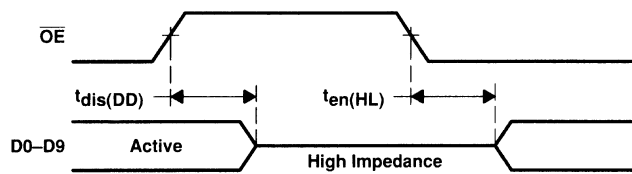


Figure 2. Output Enable to Data Output Timing Diagram

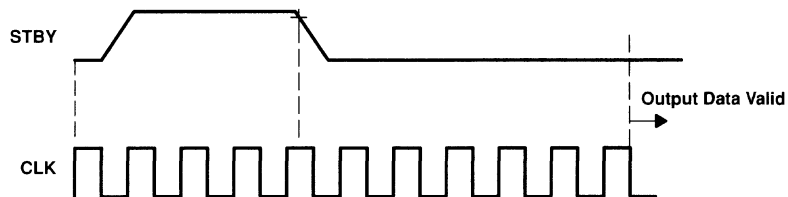


Figure 3. Standby Timing

TYPICAL CHARACTERISTICS

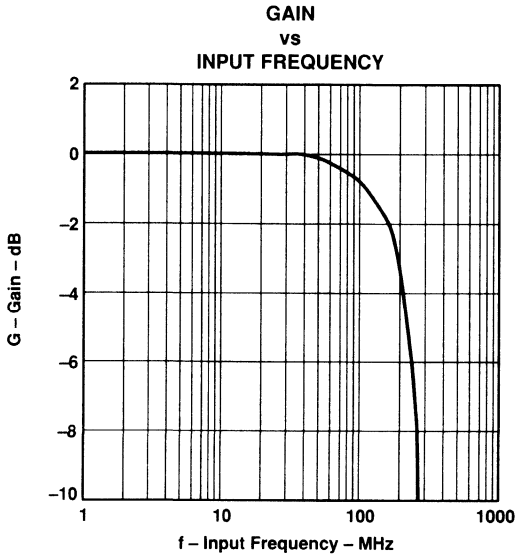


Figure 4

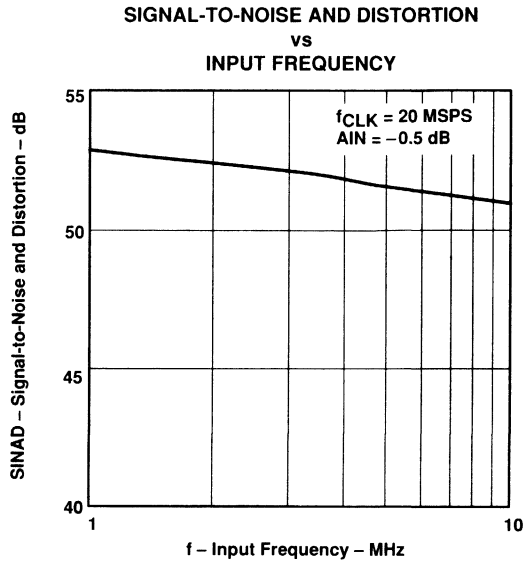


Figure 5

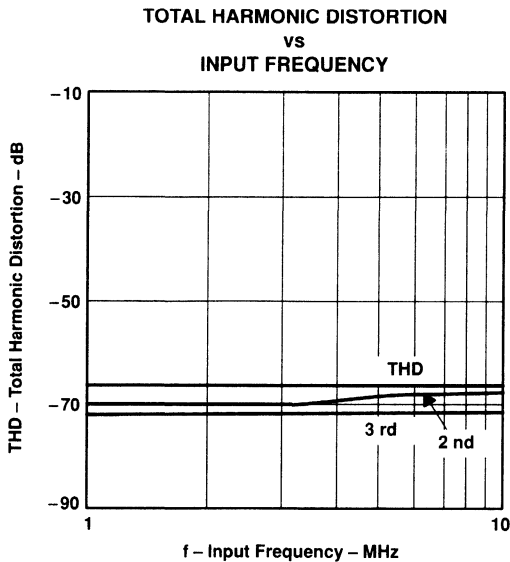


Figure 6

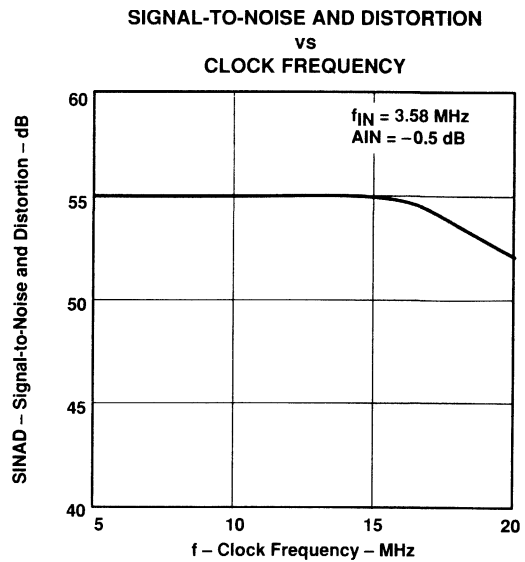


Figure 7

TLC876I, TLC876C
10-BIT 20 MSPS PARALLEL OUTPUT CMOS
ANALOG-TO-DIGITAL CONVERTERS

SLAS140B – JULY 1997 – REVISED NOVEMBER 1997

TYPICAL CHARACTERISTICS

POWER DISSIPATION
vs
CLOCK FREQUENCY

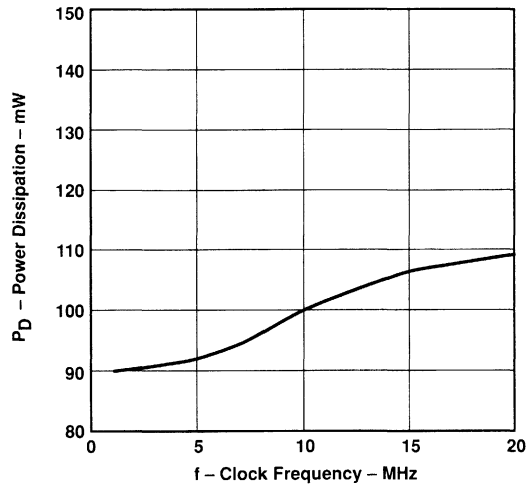


Figure 8

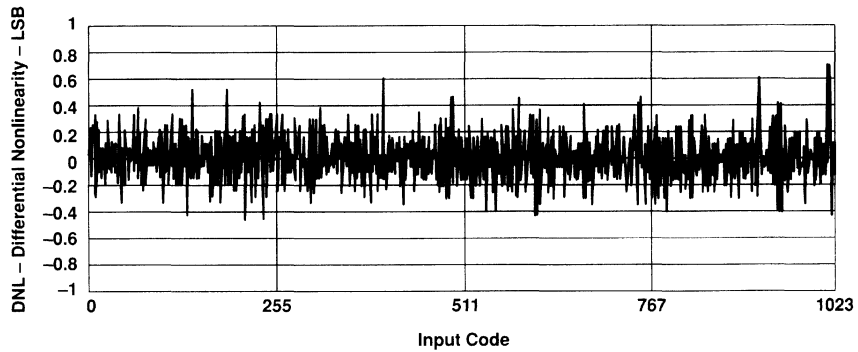


Figure 9. Differential Nonlinearity

TYPICAL CHARACTERISTICS

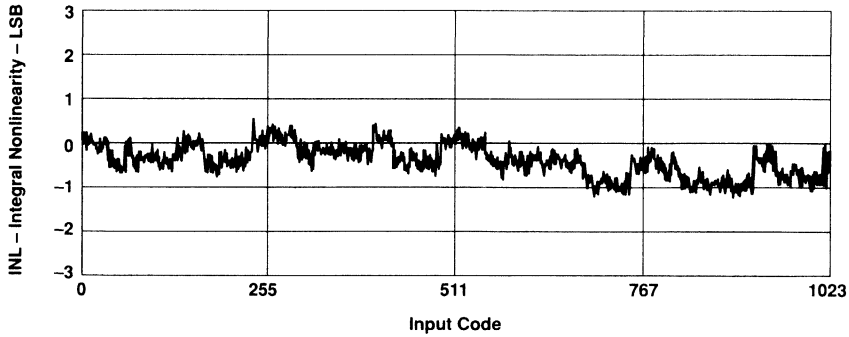


Figure 10. Integral Nonlinearity

SFDR	: -64 dB	4th	: -68 dB
SNRD	: 52 dB	5th	: -71 dB
SNR	: 55 dB	6th	: -71 dB
THD	: -62 dB	7th	: -70 dB
2 nd	: -69 dB	8th	: -70 dB
3 rd	: -72 dB	9th	: -80 dB

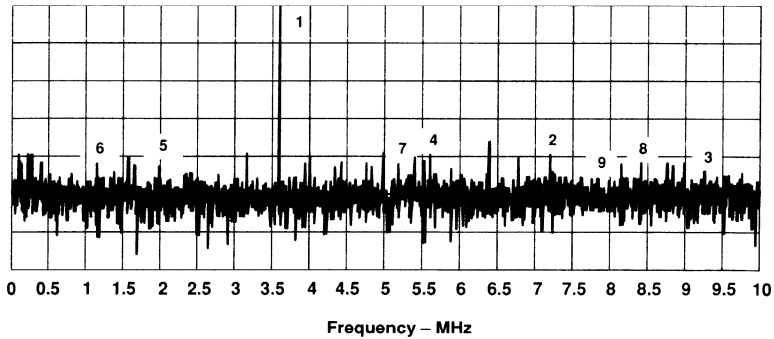


Figure 11. FFT Plot of Dynamic Performance

TLC876I, TLC876C
10-BIT 20 MSPS PARALLEL OUTPUT CMOS
ANALOG-TO-DIGITAL CONVERTERS
SLAS140B – JULY 1997 – REVISED NOVEMBER 1997

PRINCIPLES OF OPERATION

definitions of specifications and terminology

integral nonlinearity (INL)

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points. This parameter is sometimes referred to as linearity error.

differential nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ± 1 LSB ensures no missing codes. This parameter is sometimes referred to as differential error.

offset error

The first transition should occur at a level 1/2 LSB above zero. Offset is defined as the deviation of the actual first code transition from that point.

gain error

The first code transition should occur for an analog value 1/2 LSB above nominal negative full scale (the voltage applied to the REF_{BF} terminal). The last transition should occur for an analog value 1 1/2 LSB below nominal positive full scale (the voltage applied to the REF_{TF} terminal). Gain error is the deviation of the actual difference between the first and last code transitions from the ideal difference between the first and last code transitions.

pipeline delay (latency)

The number of clock cycles between conversion initiation on an input sample and the corresponding output data being made available. Once the data pipeline is full, new valid output data are provided every clock cycle.

reference top/bottom offset

Resistance between the reference input and comparator input tap points causes offset errors. These errors can be nulled out by using the force-sense connection as shown in the driving the reference terminals section.

driving the analog input

Figure 12 shows an equivalent input circuit of the TLC876 sample-and-hold amplifier and it represents an excellent first order approximation.

The total equivalent capacitance, C_E , is typically less than 5 pF and the input source must be able to charge or discharge this capacitance to 10-bit accuracy in the sample period of one half of a clock cycle. When the switch S1 closes, the input source must charge or discharge the capacitor C_E from the voltage already stored on C_E (the previously captured sample) to the new voltage. In the worst case, a full-scale voltage step on the input, the input source must provide the charging current through the switch resistance R_{SW} (50 Ω) of S1 and quickly settle (within 1/2 CLK period), and, therefore, the source is driving a low input impedance. However, when the source voltage equals the value previously stored on C_E , the hold capacitor requires no input current to maintain the charge and the equivalent input impedance is extremely high.

Adding series resistance between the output of the source and the AIN terminal reduces the drive requirements placed on the source, as shown in Figure 13. To maintain the frequency performance outlined in the specifications, the resistor should be limited to 200 Ω minus the source resistance or less. The maximum source resistance, R_S , for 10-bit, 1/2 LSB accuracy is given by equation 1.



PRINCIPLES OF OPERATION

driving the analog input (continued)

$$R_S \leq \frac{1}{2f_{(CLK)} (C_E \ln 2048)} - R_{SW} \tag{1}$$

For $f_{(CLK)} = 20$ MHz, $C_E = 10$ pF, and $R_{SW} = 100 \Omega$, this equation gives 228Ω as a maximum value; hence the 200Ω limit on the total source resistance. For applications with an input clock less than 20 MHz, the size of the series resistor can increase proportionally. Alternatively, adding a shunt capacitor between the AIN terminal and analog ground can lower the ac source impedance. This capacitance value depends on the source resistance and the required signal bandwidth.

The input span is determined by the reference voltages (see driving the reference terminals section).

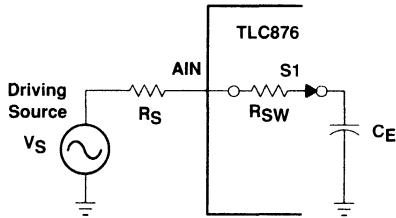


Figure 12. TLC876 Simplified Equivalent Input

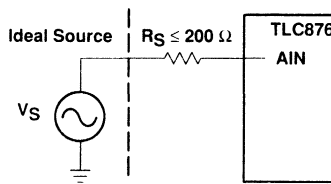


Figure 13. Sample TLC876 Drive Requirements

For many applications, particularly in single supply operation, ac coupling offers a convenient way of biasing the analog input signal at the proper signal range. Figure 14 shows a typical configuration for ac coupling the analog input signal to the TLC876. Maintaining the outlined specifications requires careful selection of the component values. The most important concern is the $f_{-3\text{ dB}}$ high-pass corner that is a function of R_2 , and the parallel combination of C_1 and C_2 . The $f_{-3\text{ dB}}$ point can be approximated by equation 2.

$$f_{-3\text{ dB}} = \frac{1}{2\pi \times (R_2) C_{eq}} \tag{2}$$

where C_{eq} is the parallel combination of C_1 and C_2 . Since C_1 is typically a large electrolytic or tantalum capacitor, the impedance becomes inductive at high frequencies. Adding a small ceramic or polystyrene capacitor, C_2 of approximately $0.01 \mu\text{F}$, which is not inductive within the frequency range of interest, maintains a low impedance. If the minimum expected input signal frequency is 20 kHz, and R_2 equals $1 \text{ k}\Omega$ and R_1 equals 50Ω , the parallel capacitance of C_1 and C_2 must be a minimum of $0.008 \mu\text{F}$ to avoid attenuating signals close to 20 kHz.

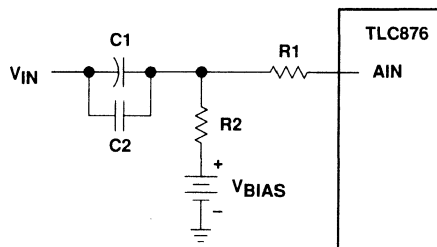


Figure 14. AC-Coupled Inputs

TLC876I, TLC876C
10-BIT 20 MSPS PARALLEL OUTPUT CMOS
ANALOG-TO-DIGITAL CONVERTERS
 SLAS140B – JULY 1997 – REVISED NOVEMBER 1997

PRINCIPLES OF OPERATION

driving the analog input (continued)

The expanded input circuit shown in Figure 15 aids in understanding the voltage offset generation when using the external input circuit in Figure 14.

The ac coupling capacitors, C1 and C2, integrate the switching transients present at the input of the TLC876 causing a net dc bias current, I_B , to flow into the input. The magnitude of this bias current increases with increasing the dc signal level, V_B , and also increases with sample frequency. When the sample clock frequency is 20 MHz, the dc bias current is approximately $30 \mu A^\dagger$ at V_{BIAS} equal to 3 V dc. This bias current causes an offset error of $(R1 + R2) \times I_B$ at the AIN terminal. Making R2 negligibly small or modifying V_{BIAS} to account for the resultant offset can compensate for this error. Note however that R2 loads the signal driving source and the value must be sufficient for the application.

For example, as shown in Figure 15, when V_{BIAS} is 3 V and the resistor values stated above, the bias current causes a $31.5 mV^\ddagger$ offset from the 3 V bias, V_{BIAS} , at the AIN terminal. For the TLC876, V_{BIAS} can be as low as 1 V for a 2 V peak-to-peak input signal swing.

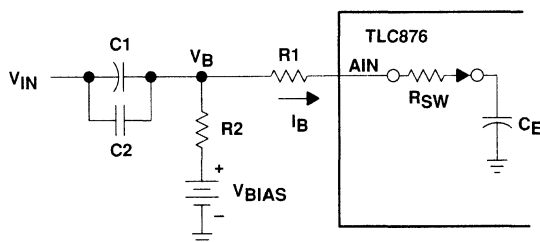


Figure 15. Bias Current and Offset

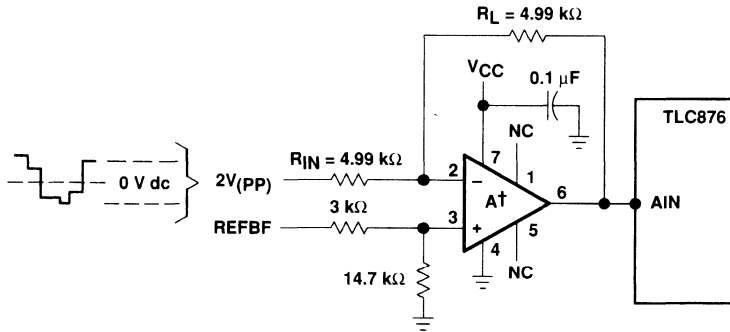
For systems that require dc-coupling, an op-amp can level-shift a ground-referenced signal to comply with the input requirements of the TLC876. Figure 16 shows an amplifier in an inverting mode with ac signal gain of -1 . The dc voltage at the noninverting input of the op-amp controls the amount of dc level shifting. A resistive voltage divider attenuates the REF_{BF} signal and the op-amp then multiplies the attenuated signal by 2. In the case where REF_{BF} = 1.6 V, the dc output level is 2.6 V which is approximately equal to $(V(\text{REF}_{TF}) - V(\text{REF}_{BF}))/2$.

$^\dagger I_{B(AVG)} = C_E (V_B) f_{CLK} = 30 \mu A$, with $R_{SW} = 50 \Omega$, $C_E = 5 pF$, $R1 = 50 \Omega$, and $R2 = 1 k\Omega$

$^\ddagger V_{OFFSET} = I_{B(AVG)} (R1 + R2)$

PRINCIPLES OF OPERATION

driving the analog input (continued)



† Amplifier A can be an AD817 or AD818 with terminal numbers as shown. The AD817 and AD818 are wide bandwidth single supply op-amps.

Figure 16. Bipolar Level Shift

driving the reference terminals

dc considerations

The TLC876 requires an external reference on terminals REFTF and REFBF and a resistor array, nominally 500 Ω, is connected between terminals REFTF and REFBF. A Kelvin connection, using the TLC876 reference sense terminals REFTS and REFBS, minimizes voltage drops caused by external and internal wiring resistance.

Figure 17 shows the equivalent input structure for the reference terminals. There is approximately 5 Ω of resistance between both REFTF and REFBF terminals and the reference ladder. If the force-sense connections are not used, the voltage drop across the 5-Ω resistors results in a reduced voltage appearing across the ladder resistance. This reduces the input span of the converter. Applying a slightly larger span between the REFTF and REFBF terminals compensates for this error. Note that the temperature coefficients of the 5-Ω resistors are 1350 ppm. The effects of temperature should be considered when a force-sense reference configuration is not used.

TLC876I, TLC876C
10-BIT 20 MSPS PARALLEL OUTPUT CMOS
ANALOG-TO-DIGITAL CONVERTERS

SLAS140B – JULY 1997 – REVISED NOVEMBER 1997

PRINCIPLES OF OPERATION

dc considerations (continued)

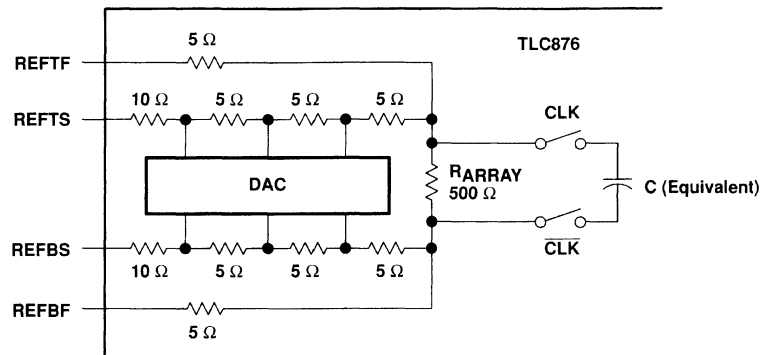


Figure 17. TLC876 Equivalent Reference Structure

The REFTS and REFBS terminals should not be connected in configurations that do not use a force-sense reference. Connecting the force and sense lines together allows current to flow in the sense lines. Any current allowed to flow through these lines must be negligibly small. Current flow causes voltage drops across the resistance in the sense lines. Because the internal DACs tap different points along the sense lines, each DAC would receive a slightly different reference voltage if current were flowing in these lines. To avoid this undesirable condition, leave the sense lines unconnected. Any current allowed to flow through these lines must be negligibly small ($< 100 \mu\text{A}$).

The voltage drop across the internal resistor array (R_{ARRAY}) determines the input span. The nominal differential voltage is $2 V_{\text{pp}}$. The full-scale input span is given by equation 3.

$$\text{Input Voltage Span} = V(\text{REFTS}) - V(\text{REFBS}) \quad (3)$$

Therefore, a full-scale input span is approximately 2 V when $[V(\text{REFTS}) - V(\text{REFBS})] = 2 \text{ V}$. The external reference must provide approximately 4 mA for a 2-V drop across the internal resistor array.

Figure 18 shows the flexibility in determining both the full-scale span of the analog input and where to center this voltage without degrading the typical performance.

PRINCIPLES OF OPERATION

dc considerations (continued)

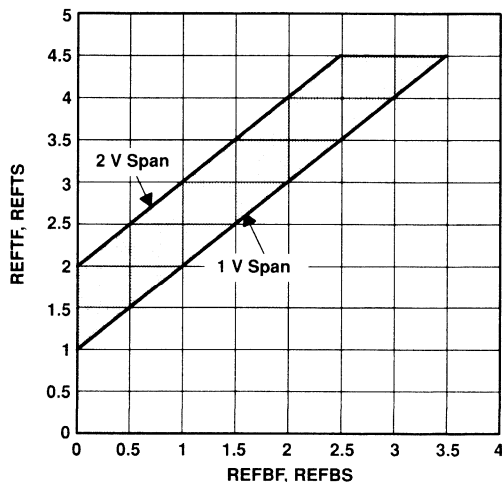


Figure 18. TLC876 Reference Ranges

ac considerations

The simplified diagram of Figure 17 shows that the reference terminals connect to a capacitor for one half of the clock period. The size of the capacitor is a function of the analog input voltage, therefore producing dynamic impedance changes at the reference inputs.

The external reference source must be able to maintain a low impedance over all frequencies of interest to provide the charge required by the capacitance. By supplying the requisite charge, the reference voltages remain relatively constant maintaining specified performance. For some reference configurations, voltage transients are present on the reference lines, especially during the falling edge of CLK. The reference must recover from the transients and settle to the desired level of accuracy prior to the rising edges of CLK.

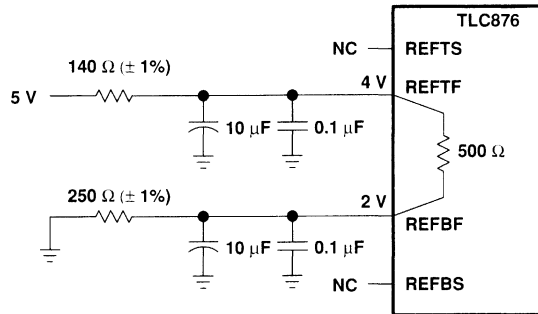
Several useful reference configurations can be used depending on the application, desired level of accuracy, and cost tradeoffs. The simplest configuration, shown in Figure 19, utilizes a resistor divider to generate the reference voltages from the converters analog power supply. The 0.1 μF bypass capacitors reduce high frequency transients. The 10 μF capacitors reduce the impedances at the REFTF and REFBF terminals at lower frequencies; however, as input frequencies approach dc, the capacitors become ineffective, and small voltage deviations appear across the biasing resistors. This reference method maintains 10-bit accuracy for input frequencies above approximately 200 Hz and 8-bit accuracy applications for input frequencies above approximately 50 Hz.

TLC876I, TLC876C
10-BIT 20 MSPS PARALLEL OUTPUT CMOS
ANALOG-TO-DIGITAL CONVERTERS

SLAS140B – JULY 1997 – REVISED NOVEMBER 1997

PRINCIPLES OF OPERATION

ac considerations (continued)



NC – No connect

Figure 19. Low Cost Reference Circuit

The reference configuration in Figure 19 provides the lowest cost, but the disadvantages include reduced dc power supply rejection and reduced accuracy due to the variability of the internal and external resistors.

The force-sense reference connections can eliminate the voltage drops associated with the internal connections to the reference ladder. Figure 20 shows a circuit using a dual, rail-to-rail single-supply operational amplifier. The operational amplifier should provide stable 3.6 V and 1.6 V reference voltages. Each half of the amplifier is compensated to drive 1 μF and 0.1 μF decoupling capacitors at the REFTF and REFBF terminals maintaining stability. The operational amplifiers are connected as voltage followers.

By connecting the operational amplifier feedback through the sense connections of the TLC876, the outputs of the operational amplifiers automatically adjust to compensate for the voltage drops that occur within the converter.

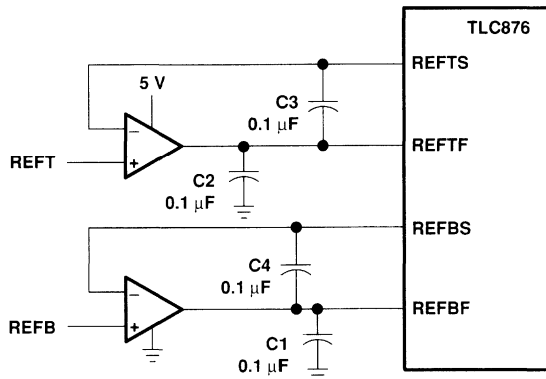
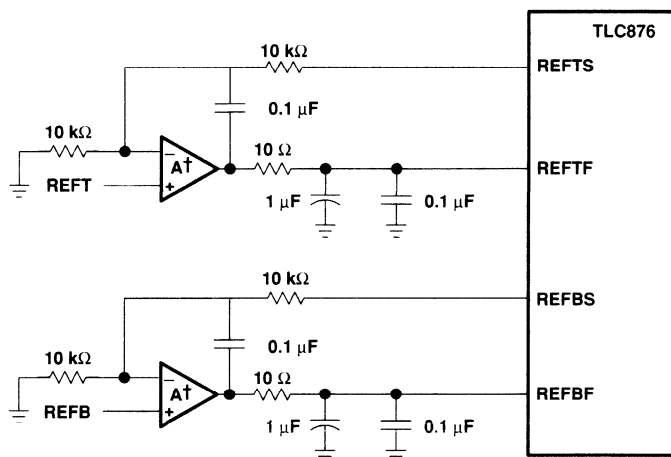


Figure 20. Kelvin Connection Reference Using an Operational Amplifier with Unlimited Capacitive Load Drive Capability

PRINCIPLES OF OPERATION

ac considerations (continued)

Figure 21 shows a circuit using a dual operational amplifier with unlimited capacitive load drive. The operational amplifier should provide stable 3.6 V and 1.6 V reference voltages for REFTF and REFBF, respectively. The amplifier must be able to maintain stability while driving unlimited capacitive loads, so the 0.1 μF capacitors C1 and C2 can connect directly to the outputs of the operational amplifiers, which reduces high frequency transients. Capacitors C3 and C4 shunt across the internal resistors of the force-sense connections and prevent instability. The stability of any operational amplifier used must be examined closely when driving capacitive loads.



† This device is 1/2 of a TLV2442. The TLV2442 is a rail-to-rail output dual operational amplifier.

Figure 21. Kelvin Connection Reference Using an Operational Amplifier with Unlimited Capacitive Load Drive Capability

TLC876I, TLC876C

10-BIT 20 MSPS PARALLEL OUTPUT CMOS

ANALOG-TO-DIGITAL CONVERTERS

SLAS140B – JULY 1997 – REVISED NOVEMBER 1997

PRINCIPLES OF OPERATION

layout and decoupling

With high-frequency high-resolution converters, the layout and decoupling of the reference is critical. The actual voltage digitized by the TLC876 is relative to the reference voltages. In Figure 22, for example, the reference return and the bypass capacitors are connected to the shield of the incoming analog signal. Disturbances in the ground of the analog input, that are common mode to the REFTF, REFBF, and AIN terminals because of the common ground, are effectively removed by the TLC876 high common mode rejection. Also, these capacitors should be connected as close to reference terminals as possible.

High-frequency noise sources, V_{N1} and V_{N2} , are shunted to ground by decoupling capacitors. Any voltage drops between the analog input ground and the reference bypassing points are treated as input signals by the converter using the reference inputs. Consequently, the reference decoupling capacitors should be connected to the same physical analog ground point used by the analog input voltage (see the grounding and layout rules section).

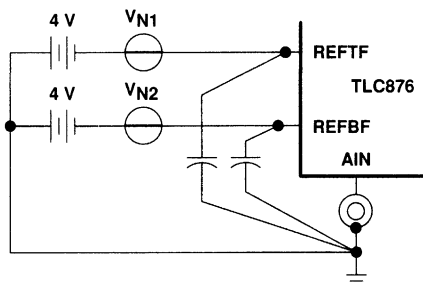


Figure 22. Recommended Bypassing For The Reference

clock input

The clock input is buffered internally with an inverter powered from the DRV_{DD} terminal, which accommodates either 5-V or 3.3-V CMOS logic input signal swings with the input threshold for the CLK terminal nominally at $DRV_{DD}/2$.

The internal pipelined architecture operates on both rising and falling edges of the input clock. To minimize duty cycle variations, the recommended logic family to drive the clock input is high-speed or advanced CMOS (HC/HCT, AC/ACT) logic. CMOS logic provides both symmetrical voltage threshold levels and sufficient rise and fall times to support 20 MSPS operation.

The power dissipated by the correction logic and output buffers is largely proportional to the clock frequency. Figure 8 illustrates this tradeoff between clock rates and a reduction in power consumption.

PRINCIPLES OF OPERATION

digital inputs and outputs

Each of the digital control inputs, \overline{OE} and STBY, has an input buffer powered from the DRV_{DD} supply terminal. With DRV_{DD} set to 5 V, all digital inputs readily interface with 5 V CMOS logic. Using lower voltage CMOS logic, DRV_{DD} can be set to 3.3 V, lowering the nominal input threshold of all digital inputs to $(3.3\text{ V})/2 = 1.65\text{ V}$, typically.

The digital output format is straight binary. For example, Table 1 shows the output format for voltage levels of $V(\text{REFTS}) = 4\text{ V}$ and $V(\text{REFBS}) = 2\text{ V}$.

A low power mode feature is provided such that when STBY is high and the clock is disabled, the static power of the TLC876 drops significantly (see electrical characteristics table).

Table 1. Output Data Format

AIN VOLTAGE (APPROXIMATE)	THREE STATE	DATA									
		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
> 4 V	0	1	1	1	1	1	1	1	1	1	1
4 V	0	1	1	1	1	1	1	1	1	1	1
3 V	0	1	0	0	0	0	0	0	0	0	0
2 V	0	0	0	0	0	0	0	0	0	0	0
< 2 V	0	0	0	0	0	0	0	0	0	0	0
X	1	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

grounding and layout rules

Proper grounding and layout techniques are essential for achieving optimal performance. The analog and digital grounds on the TLC876 have been separated to optimize the management of return currents in a system. A printed circuit board (PCB) of at least 4 layers employing a ground plane and power planes should be used with the TLC876. The use of ground and power planes offers distinct advantages:

- Minimizes the loop area encompassed by a signal and its return path
- Minimizes the impedance associated with ground and power paths
- The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane

These characteristics produce a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

A properly designed layout prevents noise from coupling onto the input signal. Digital signal traces should not run parallel with the input signal traces and should be routed away from the input circuitry. The separate analog and digital grounds should be joined together directly under the TLC876. A solid ground plane under the TLC876 is also acceptable if no significant currents are flowing in that portion of the ground plane under the device. The general rule for mixed signal layouts is that return currents from digital circuitry should not pass through or under critical analog circuitry. The system design should minimize the analog lead-in to reduce potential noise pickup.

TLC876I, TLC876C
10-BIT 20 MSPS PARALLEL OUTPUT CMOS
ANALOG-TO-DIGITAL CONVERTERS

SLAS140B – JULY 1997 – REVISED NOVEMBER 1997

PRINCIPLES OF OPERATION

digital outputs

The DRV_{DD} supply terminal powers each of the on-chip buffers for the output bits (D0–D9) and is a separate lead from AV_{DD} or DV_{DD} . The output drivers are sized to drive a variety of logic families while minimizing the amount of glitch energy generated. A recommended fan-out of one keeps the capacitive load on the output data drivers below the specified 20 pF level.

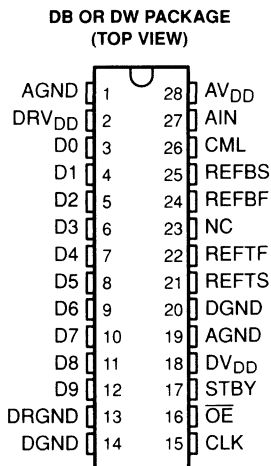
For $DRV_{DD} = 5$ V, the output signal swing can drive both high-speed CMOS and TTL logic families. For TTL, the on-chip output drivers are designed to support several of the high-speed TTL families (F, AS, S). For applications where the clock rate is below 20 MSPS, other TTL families are appropriate. For interfacing with lower voltage CMOS logic, the TLC876 sustains 20 MSPS operation with $DRV_{DD} = 3.3$ V. Refer to logic family data sheets for compatibility with the TLC876 digital specifications.



TLC876M
10-BIT 20 MSPS PARALLEL OUTPUT CMOS
ANALOG-TO-DIGITAL CONVERTER

SGLS105 – DECEMBER 1997

- **10-Bit Resolution 20 MSPS Sampling Analog-to-Digital Converter (ADC)**
- **Power Dissipation . . . 107 mW Typ**
- **5-V Single Supply Operation**
- **Differential Nonlinearity . . . ± 0.5 LSB Typ**
- **No Missing Codes**
- **Power Down (Standby) Mode**
- **Three State Outputs**
- **Digital I/Os Compatible With 5-V or 3.3-V Logic**
- **Adjustable Reference Input**
- **28-Terminal Small Outline Package (SOIC) or 28-Terminal Super Small Outline Package (SSOP)**
- **Pin Compatible With the Analog Devices AD876**



NC – No internal connection

applications

- **Communications**
- **Imaging Systems**
- **High-Speed DSP Front-End . . . SMJ320C6x**

description

The TLC876 is a CMOS, low-power, 10-bit, 20 MSPS analog-to-digital converter (ADC). The speed, resolution, and single-supply operation are suited for military applications in video, imaging, high-speed acquisition, and communications. The low-power and single-supply operation satisfy requirements for high-speed portable applications. The speed and resolution ideally suit charge-coupled device (CCD) input systems such as electronic still cameras. A multistage pipelined architecture with output error correction logic provides for no missing codes over the full operating temperature range. Force and sense connections to the reference inputs provide a more accurate internal reference voltage to the reference resistor string.

A standby mode of operation reduces the power to typically 15 mW. The digital I/O interfaces to either 5-V or 3.3-V logic and the digital output terminals can be placed in a high-impedance state. The format of the output data is straight binary coding.

A pipelined multistaged architecture achieves a high sample rate with low power consumption. The TLC876 distributes the conversion over several smaller ADC sub-blocks, refining the conversion with progressively higher accuracy as the device passes the results from stage to stage. This distributed conversion requires a small fraction of the 1023 comparators used in a traditional flash ADC. A sample-and-hold amplifier (SHA) within each of the stages permits the first stage to operate on a new input sample while the second through the fifth stages operate on the four preceding samples.

The TLC876M is characterized for operation over the full military temperature range of -55°C to 125°C . The target release timeframe for the TLC876M is estimated to be during the second half of 1998.

PRODUCT PREVIEW

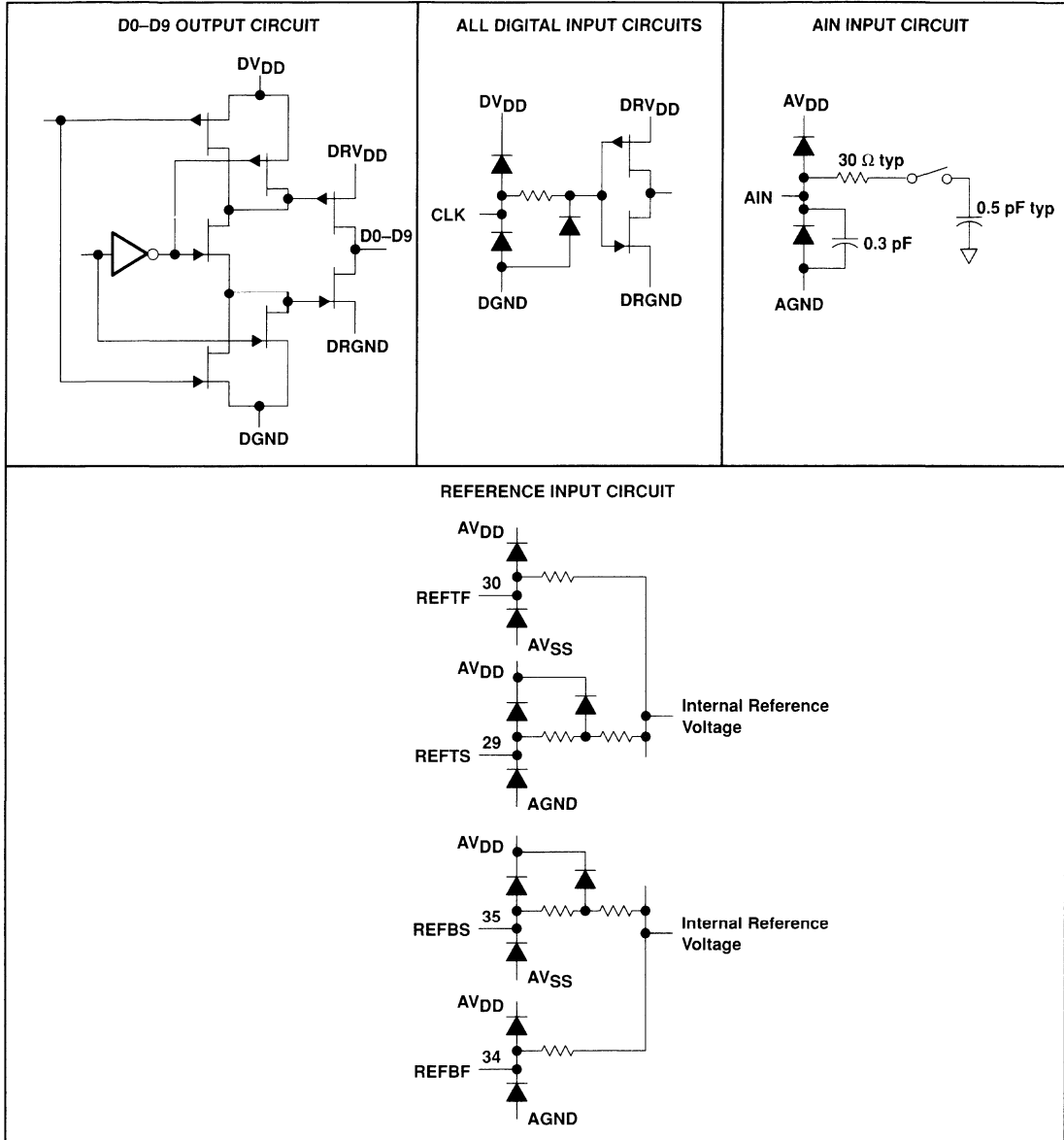
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



TLC876M
10-BIT 20 MSPS PARALLEL OUTPUT CMOS
ANALOG-TO-DIGITAL CONVERTER

SGLS105 - DECEMBER 1997

equivalent input and output circuits



PRODUCT PREVIEW

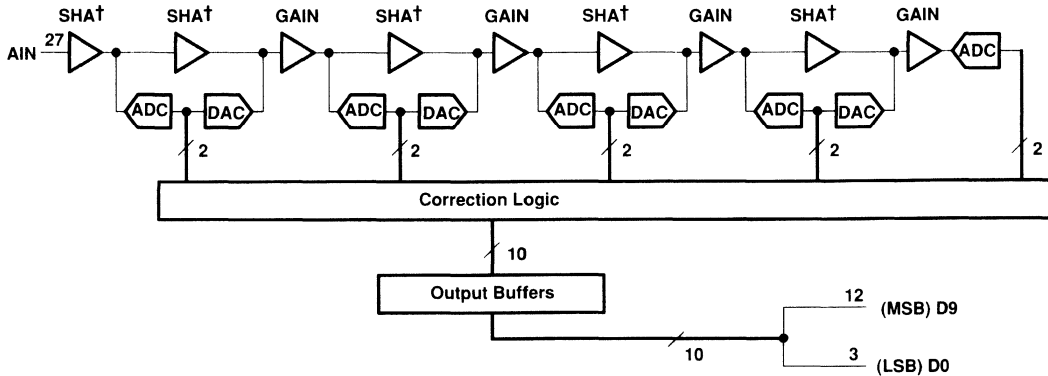
TLC876M
10-BIT 20 MSPS PARALLEL OUTPUT CMOS
ANALOG-TO-DIGITAL CONVERTER

SGLS105 – DECEMBER 1997

AVAILABLE OPTIONS

T _A	PACKAGE	
	SMALL OUTLINE (DW)	SUPER SMALL OUTLINE (DB)
-55°C to 125°C	TLC876MDW	TLC876MDB

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	1, 19		Analog ground
AIN	27	I	Analog input
AV _{DD}	28		5-V analog supply
CLK	15	I	Clock input
CML	26	O	Bypass for an internal bias point. Typically a 0.1 μF capacitor minimum is connected from this terminal to ground.
DGND	14, 20		Digital ground
DV _{DD}	18		5-V digital supply
DRV _{DD}	2		3.3-V/5-V digital supply. Supply for digital input and output buffers.
DRGND	13		3.3-V/5-V digital ground. Ground for digital input and output buffers.
D0–D9	3–12	O	Digital data out. D0:LSB, D9:MSB
OE	16	I	Output enable. When OE = low or NC, the device is in normal operating mode. When OE = high, D0–D9 are high impedance.
REFBF	24	I	Reference bottom force
REFBS	25	I	Reference bottom sense
REFTF	22	I	Reference top force
REFTS	21	I	Reference top sense
STBY	17	I	Standby enable. When STBY = low or NC, the device is in normal operating mode. When STBY = high, the device is in standby mode.

PRODUCT PREVIEW



TLC1541

10-BIT ANALOG-TO-DIGITAL CONVERTER WITH SERIAL CONTROL AND 11 INPUTS

SLAS073C – DECEMBER 1995 – REVISED AUGUST 1996

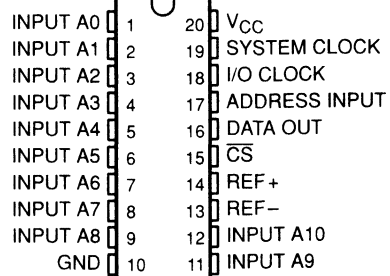
- 10-Bit Resolution A/D Converter
- Microprocessor Peripheral or Standalone Operation
- On-Chip 12-Channel Analog Multiplexer
- Built-In Self-Test Mode
- Software-Controllable Sample-and-Hold Function
- Total Unadjusted Error . . . ± 1 LSB Max
- Pinout and Control Signals Compatible With TLC540 and TLC549 Families of 8-Bit A/D Converters
- CMOS Technology

PARAMETER	VALUE
Channel Acquisition Sample Time	5.5 μ s
Conversion Time (Max)	21 μ s
Samples Per Second (Max)	32×10^3
Power Dissipation (Max)	6 mW

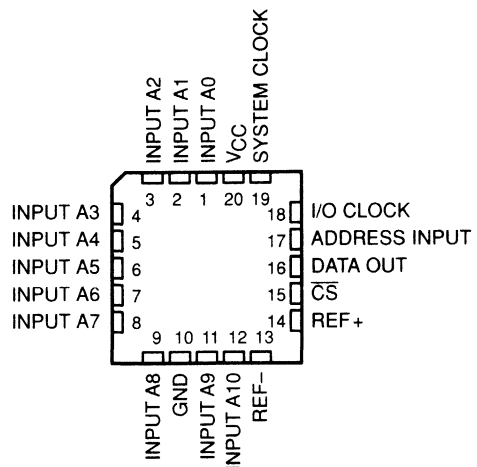
description

The TLC1541 is a CMOS A/D converter built around a 10-bit switched-capacitor successive-approximation A/D converter. The device is designed for serial interface to a microprocessor or peripheral using a 3-state output with up to four control inputs (including independent SYSTEM CLOCK, I/O CLOCK, chip select [\overline{CS}], and ADDRESS INPUT). A 2.1-MHz system clock for the TLC1541, with a design that includes simultaneous read/write operation, allows high-speed data transfers and sample rates up to 32 258 samples per second. In addition to the high-speed converter and versatile control logic, there is an on-chip, 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal self-test voltage and a sample-and-hold function that operates automatically.

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T _A	PACKAGE		
	SMALL OUTLINE (DW)	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC1541CDW	TLC1541CFN	TLC1541CN
-40°C to 85°C	TLC1541IDW	TLC1541IFN	TLC1541IN

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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TLC1541

10-BIT ANALOG-TO-DIGITAL CONVERTER WITH SERIAL CONTROL AND 11 INPUTS

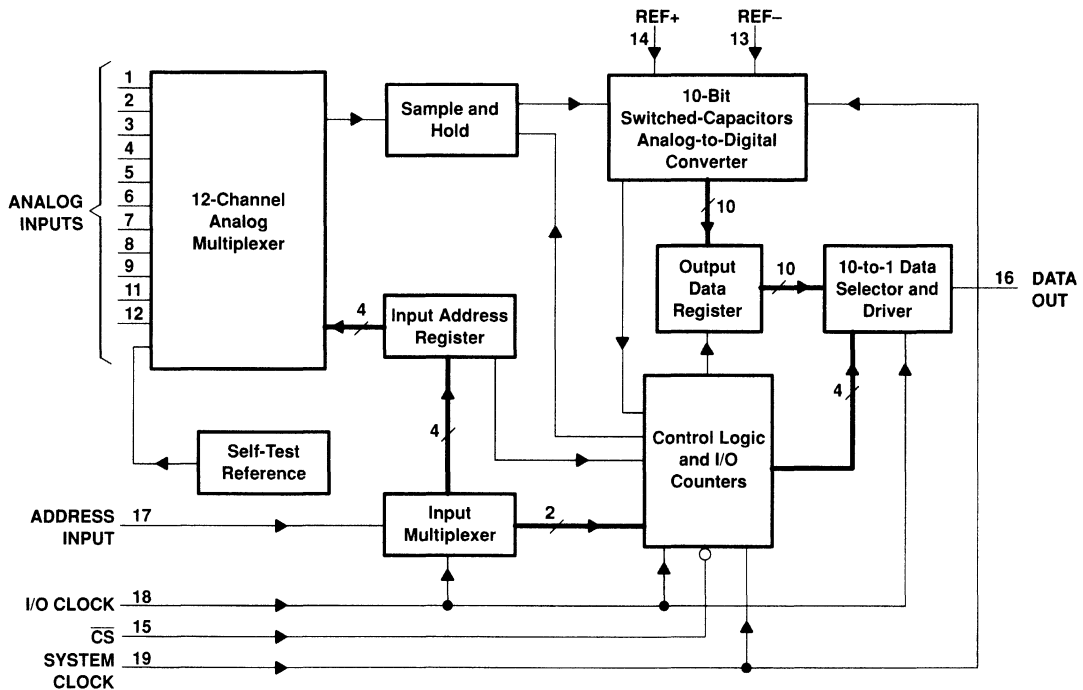
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description (continued)

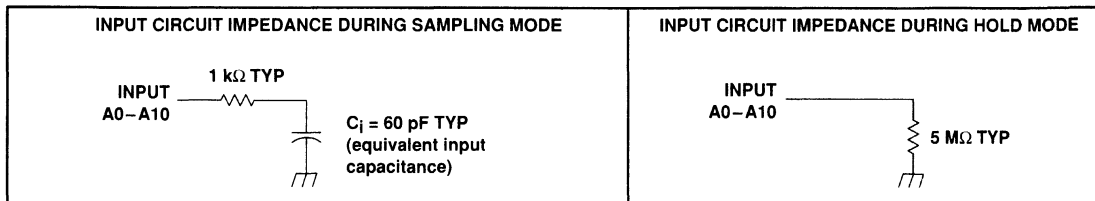
The converters incorporated in the TLC1541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched-capacitor design allows low-error conversion in 21 μ s over the full operating temperature range.

The TLC1541 is available in DW, FN, and N packages. The C-suffix versions are characterized for operation from 0°C to 70°C. The I-suffix versions are characterized for operation from -40°C to 85°C.

functional block diagram

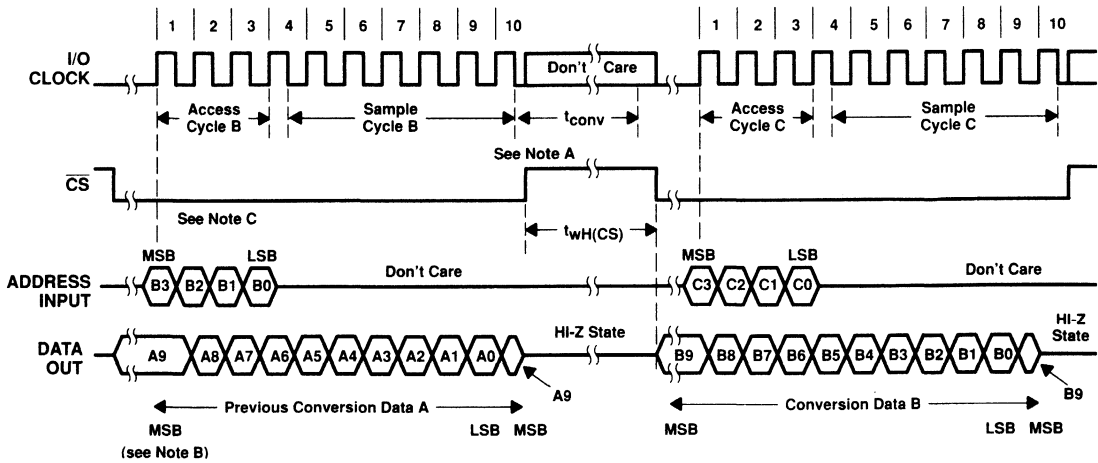


typical equivalent inputs



TLC1541
10-BIT ANALOG-TO-DIGITAL CONVERTER
WITH SERIAL CONTROL AND 11 INPUTS
 SLAS073C – DECEMBER 1995 – REVISED AUGUST 1996

operating sequence



- NOTES: A. The conversion cycle, which requires 44 system clock periods, initiates on the tenth falling edge of the I/O clock after \overline{CS} goes low for the channel whose address exists in memory at that time. When \overline{CS} is kept low during conversion, the I/O clock must remain low for at least 44 system clock cycles to allow the conversion to complete.
- B. The most significant bit (MSB) is automatically placed on the DATA OUT bus after \overline{CS} is brought low. The remaining nine bits (A8–A0) clock out on the first nine I/O clock falling edges.
- C. To minimize errors caused by noise at the \overline{CS} input, the internal circuitry waits for three system clock cycles (or less) after a chip-select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time elapses.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range, V_I (any input)	-0.3 V to $V_{CC} + 0.3$ V
Output voltage range, V_O	-0.3 V to $V_{CC} + 0.3$ V
Peak input current (any input)	± 10 mA
Peak total input current (all inputs)	± 30 mA
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Case temperature for 10 seconds, T_C : FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF- and GND wired together (unless otherwise noted).



TLC1541

10-BIT ANALOG-TO-DIGITAL CONVERTER WITH SERIAL CONTROL AND 11 INPUTS

SLAS073C – DECEMBER 1995 – REVISED AUGUST 1996

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{ref-} (see Note 2)	-0.1	0	2.5	V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)	1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)	0		V_{CC}	V
High-level control input voltage, V_{IH}	2			V
Low-level control input voltage, V_{IL}			0.8	V
Input/output clock frequency, $f_{clock(I/O)}$	0		1.1	MHz
System clock frequency, $f_{clock(SYS)}$	$f_{clock(I/O)}$		2.1	MHz
Setup time, address bits before I/O CLOCK \uparrow , $t_{su(A)}$	400			ns
Hold time, address bits after I/O CLOCK \uparrow , $t_h(A)$	0			ns
Setup time, \overline{CS} low before clocking in first address bit, $t_{su(CS)}$ (see Note 3 and Operating Sequence)	3			System clock cycles
Pulse duration, \overline{CS} high during conversion, $t_{wH(CS)}$ (see Operating Sequence)	44			System clock cycles
Pulse duration, SYSTEM CLOCK high, $t_{wH(SYS)}$	210			ns
Pulse duration, SYSTEM CLOCK low, $t_{wL(SYS)}$	190			ns
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$	404			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$	404			ns
Clock transition time (see Note 4)	System	$f_{clock(SYS)} \leq 1048$ kHz	30	ns
		$f_{clock(SYS)} > 1048$ kHz	20	
	I/O	$f_{clock(I/O)} \leq 525$ kHz	100	ns
		$f_{clock(I/O)} > 525$ kHz	40	
Operating free-air temperature, T_A	C suffix	0	70	°C
	I suffix	-40	85	

- NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000). For proper operation, REF+ voltage must be at least 1 V higher than REF- voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.
3. To minimize errors caused by noise at the chip select input, the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum chip select setup time elapses.
4. The amount of time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μ s for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.



TLC1541
10-BIT ANALOG-TO-DIGITAL CONVERTER
WITH SERIAL CONTROL AND 11 INPUTS

SLAS073C – DECEMBER 1995 – REVISED AUGUST 1996

electrical characteristics over recommended operating temperature range,
 $V_{CC} = V_{ref+} = 4.75\text{ V to }5.5\text{ V}$, $f_{clock(I/O)} = 1.1\text{ MHz}$, $f_{clock(SYS)} = 2.1\text{ MHz}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (terminal 16)	$V_{CC} = 4.75\text{ V}$, $I_{OH} = 360\text{ }\mu\text{A}$	2.4			V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75\text{ V}$, $I_{OL} = 3.2\text{ mA}$			0.4	V
I_{OZ}	High-impedance-state output current	$V_O = V_{CC}$, \overline{CS} at V_{CC}			10	μA
		$V_O = 0$, \overline{CS} at V_{CC}			-10	
I_{IH}	High-level input current	$V_I = V_{CC}$		0.005	2.5	μA
I_{IL}	Low-level input current	$V_I = 0$		-0.005	-2.5	μA
I_{CC}	Operating supply current	\overline{CS} at 0 V		1.2	2.5	mA
	Selected channel leakage current	Selected channel at V_{CC} , Unselected channel at 0 V		0.4	1	μA
		Selected channel at 0 V, Unselected channel at V_{CC}		-0.4	-1	
$I_{CC} + I_{ref}$	Supply and reference current	$V_{ref+} = V_{CC}$, \overline{CS} at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs		7	55	pF
		Control inputs		5	15	

† All typical values are at $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.



TLC1541
10-BIT ANALOG-TO-DIGITAL CONVERTER
WITH SERIAL CONTROL AND 11 INPUTS

SLAS073C – DECEMBER 1995 – REVISED AUGUST 1996

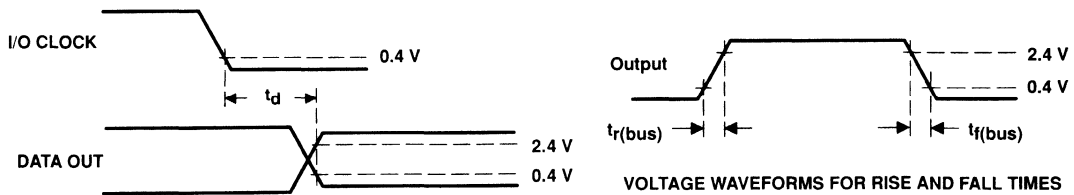
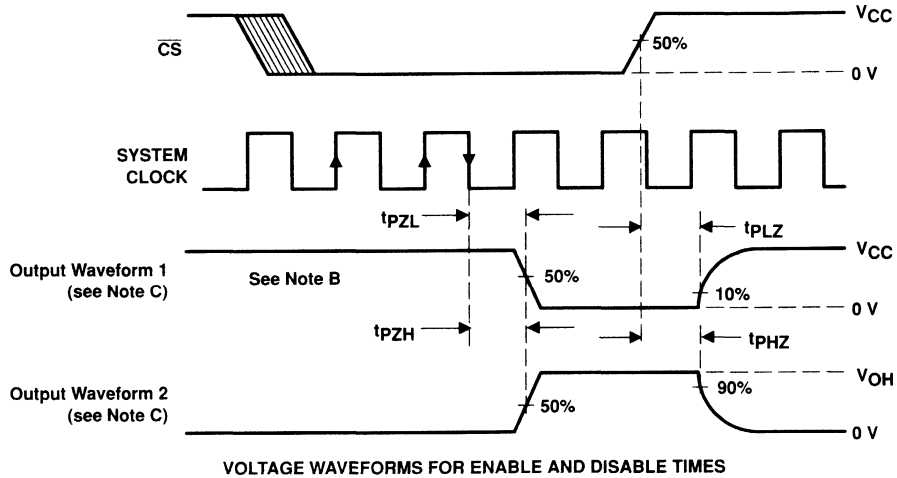
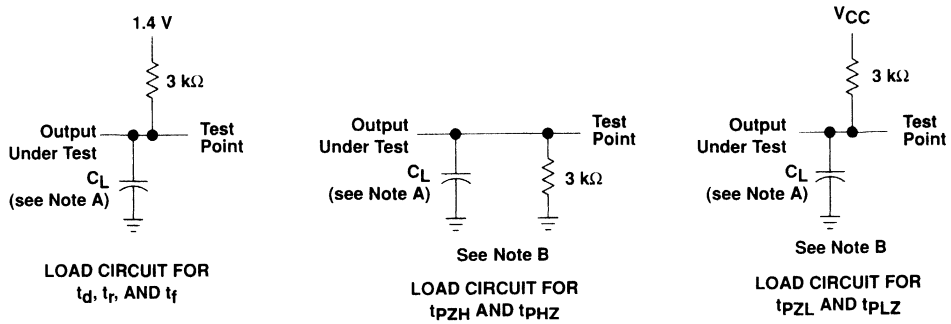
operating characteristics over recommended operating temperature range,
 $V_{CC} = V_{ref+} = 4.75\text{ V to }5.5\text{ V}$, $f_{clock(I/O)} = 1.1\text{ MHz}$, $f_{clock(SYS)} = 2.1\text{ MHz}$

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
E_L	Linearity error	See Note 5		± 1	LSB
E_{ZS}	Zero-scale error	See Notes 2 and 6		± 1	LSB
E_{FS}	Full-scale error	See Notes 2 and 6		± 1	LSB
E_T	Total unadjusted error	See Note 7		± 1	LSB
	Self-test output code	Input A11 address = 1011 (see Note 8)	0111110100 (500)	1000001100 (524)	
t_{conv}	Conversion time			21	μs
	Total access and conversion time			31	μs
	Channel acquisition time (sample cycle)	See Operating Sequence		6	I/O clock cycles
t_v	Time output data remains valid after I/O CLOCK \downarrow		10		ns
t_d	Delay time, I/O CLOCK \downarrow to DATA OUT valid	See Figure 1		400	ns
t_{en}	Output enable time			150	ns
t_{dis}	Output disable time			150	ns
$t_r(\text{bus})$	Data bus rise time			300	ns
$t_f(\text{bus})$	Data bus fall time			300	ns

- NOTES:
- Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000). For proper operation, REF+ voltage must be at least 1 V higher than REF- voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.
 - Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
 - Zero-scale error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
 - Total unadjusted error includes linearity, zero-scale, and full-scale errors.
 - Both the input address and the output codes are expressed in positive logic. The A11 analog input signal is internally generated and used for test purposes.



PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS FOR DELAY TIME

- NOTES: A. $C_L = 50 \text{ pF}$
 B. $t_{en} = t_{pZH}$ or t_{pZL} and $t_{dis} = t_{pHZ}$ or t_{pLZ} .
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Load Circuits and Voltage Waveforms

TLC1541
10-BIT ANALOG-TO-DIGITAL CONVERTER
WITH SERIAL CONTROL AND 11 INPUTS
 SLAS073C – DECEMBER 1995 – REVISED AUGUST 1996

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 2, the time required to charge the analog input capacitance from 0 V to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c/R_t C_i}\right) \quad (1)$$

where

$$R_t = R_S + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S/2048) \quad (2)$$

Equating equation 1 to equation 2 and solving for time (t_c) gives

$$V_S - (V_S/2048) = V_S \left(1 - e^{-t_c/R_t C_i}\right) \quad (3)$$

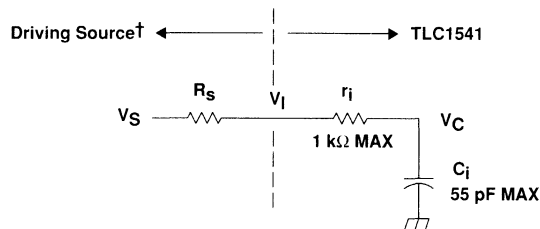
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(2048) \quad (4)$$

Therefore, with the values given, the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_S + 1 \text{ k}\Omega) \times 55 \text{ pF} \times \ln(2048) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at INPUT A0–A10
 V_S = External Driving Source Voltage
 R_S = Source Resistance
 r_i = Input Resistance
 C_i = Input Capacitance

† Driving source requirements:

- Noise and distortion levels for the source must be at least equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 2. Equivalent Input Circuit Including the Driving Source

PRINCIPLES OF OPERATION

The TLC1541 is a complete data acquisition system on a single chip. The device includes such functions as sample and hold, 10-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs: chip select (\overline{CS}), address input, I/O clock, and system clock. These control inputs and a TTL-compatible, 3-state output are intended for serial communications with a microprocessor or microcomputer. The TLC1541 can complete conversions in a maximum of 21 μ s, while complete input-conversion output cycles can be repeated at a maximum of 31 μ s.

The system and I/O clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the SYSTEM CLOCK input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using I/O CLOCK. SYSTEM CLOCK drives the conversion-crunching circuitry so that the control hardware and software need not be concerned with this task.

When \overline{CS} is high, DATA OUT is in a 3-state condition and ADDRESS INPUT and I/O CLOCK are disabled. This feature allows each of these terminals, with the exception of the \overline{CS} terminal, to share a control logic point with its counterpart terminals on additional A/D devices when using additional TLC1541 devices. In this way, the above feature serves to minimize the required control logic terminals when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. \overline{CS} is brought low. To minimize errors caused by noise at the \overline{CS} input, the internal circuitry waits for two rising edges and then a falling edge of SYSTEM CLOCK after a low \overline{CS} transition before recognizing the low transition. This technique protects the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result automatically appears on DATA OUT.
2. A new positive-logic multiplexer address shifts in on the first four rising edges of I/O CLOCK. The MSB of the address shifts in first. The negative edges of these four I/O clock pulses shift out the second, third, fourth, and fifth most-significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Five clock cycles are then applied to the I/O CLOCK, and the sixth, seventh, eighth, ninth, and tenth conversion bits shift out on the negative edges of these clock cycles.
4. The final tenth-clock cycle is applied to the I/O CLOCK. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 44 system clock cycles. After this final I/O clock cycle, \overline{CS} must go high or the I/O CLOCK must remain low for at least 44 system-clock cycles to allow for the conversion function.

\overline{CS} can be kept low during periods of multiple conversion. When keeping \overline{CS} low during periods of multiple conversion, special care must be exercised to prevent noise glitches on I/O CLOCK. When glitches occur on I/O CLOCK, the I/O sequence between the microprocessor/controller and the device loses synchronization. Also, when \overline{CS} goes high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of \overline{CS} causes a reset condition, which aborts the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 44 system-clock cycles occur. Such action yields the conversion result of the previous conversion and not the ongoing conversion.

TLC1541

10-BIT ANALOG-TO-DIGITAL CONVERTER WITH SERIAL CONTROL AND 11 INPUTS

SLAS073C – DECEMBER 1995 – REVISED AUGUST 1996

PRINCIPLES OF OPERATION

It is possible to connect SYSTEM CLOCK and I/O CLOCK together in special situations in which controlling-circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. This device requires the first two clocks to recognize that \overline{CS} is at a valid low level when the common clock signal is used as an I/O CLOCK. When \overline{CS} is recognized by the device to be at a high level, the common clock signal is used for the conversion clock also.
2. A low \overline{CS} must be recognized before the I/O CLOCK can shift in an analog channel address. The device recognizes a \overline{CS} transition when the SYSTEM CLOCK terminal receives two positive edges and then a negative edge. For this reason, after a \overline{CS} negative edge, the first two clock cycles do not shift in the address. Also, upon shifting in the address, \overline{CS} must be raised after the tenth valid (12 total) I/O CLOCK. Otherwise, additional common-clock cycles are recognized as I/O CLOCK cycles and shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device accommodates these applications. Although the on-chip sample-and-hold begins sampling upon the negative edge of the fourth valid I/O CLOCK cycle, the hold function does not initiate until the negative edge of the tenth valid I/O CLOCK cycle. Thus, the control circuitry can leave the I/O CLOCK signal in its high state during the tenth valid I/O CLOCK cycle until the moment at which the analog signal must be converted. The TLC1541 continues sampling the analog input until the eighth valid falling edge of the I/O CLOCK. The control circuitry or software then immediately lowers the I/O CLOCK signal and holds the analog signal at the desired point in time and starts the conversion.



TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D – MARCH 1992 – APRIL 1996

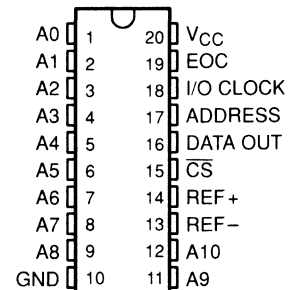
- 10-Bit Resolution A/D Converter
- 11 Analog Input Channels
- Three Built-In Self-Test Modes
- Inherent Sample-and-Hold Function
- Total Unadjusted Error . . . ± 1 LSB Max
- On-Chip System Clock
- End-of-Conversion (EOC) Output
- Terminal Compatible With TLC542
- CMOS Technology

description

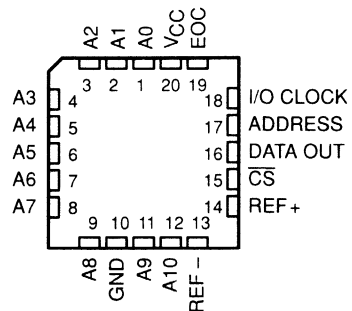
The TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, and TLC1543Q are CMOS 10-bit switched-capacitor successive-approximation analog-to-digital converters. These devices have three inputs and a 3-state output [chip select (\overline{CS}), input-output clock (I/O CLOCK), address input (ADDRESS), and data output (DATA OUT)] that provide a direct 4-wire interface to the serial port of a host processor. These devices allow high-speed data transfers from the host.

In addition to a high-speed A/D converter and versatile control capability, these devices have an on-chip 14-channel multiplexer that can select any one of 11 analog inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of A/D conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the devices features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

DB, J, DW, OR N PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q

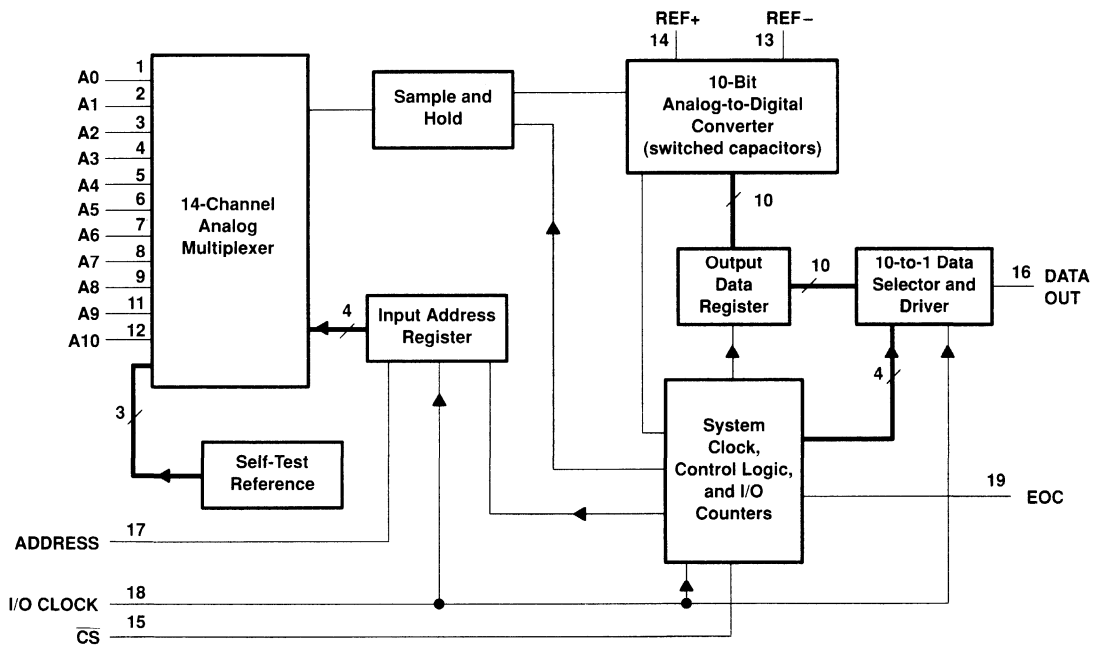
10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D – MARCH 1992 – APRIL 1996

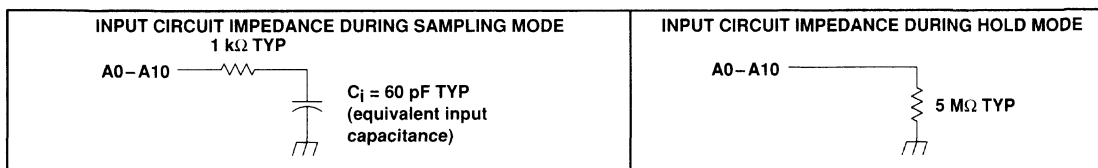
AVAILABLE OPTIONS

T _A	PACKAGE					
	SMALL OUTLINE (DB)	SMALL OUTLINE (DW)	CHIP CARRIER (FN)	PLASTIC DIP (N)	CHIP CARRIER (FK)	CERAMIC DIP (J)
0°C to 70°C		TLC1542CDW	TLC1542CFN	TLC1542CN		
	TLC1543CDB	TLC1543CDW	TLC1543CFN	TLC1543CN		
-40°C to 85°C		TLC1542IDW	TLC1542IFN	TLC1542IN		
	TLC1543IDB	TLC1543IDW	TLC1543IFN	TLC1543IN		
-40°C to 125°C		TLC1542QDW	TLC1542QFN	TLC1542QN		
		TLC1543QDW	TLC1543QFN	TLC1543QN		
-55°C to 125°C					TLC1542MFK	TLC1542MJ

functional block diagram



typical equivalent inputs



TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q
10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH
SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D – MARCH 1992 – APRIL 1996

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ADDRESS	17	I	Serial address input. A 4-bit serial address selects the desired analog input or test voltage that is to be converted next. The address data is presented with the MSB first and shifts in on the first four rising edges of I/O CLOCK. After the four address bits have been read into the address register, this input is ignored for the remainder of the current conversion period.
A0–A10	1–9, 11, 12	I	Analog signal inputs. The 11 analog inputs are applied to these terminals and are internally multiplexed. The driving source impedance should be less than or equal to 1 k Ω .
CS	15	I	Chip select. A high-to-low transition on this input resets the internal counters and controls and enables DATA OUT, ADDRESS, and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables ADDRESS and I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OUT	16	O	The 3-state serial output for the A/D conversion result. This output is in the high-impedance state when CS is high and active when CS is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives this output to the logic level corresponding to the next most significant bit, and the remaining bits shift out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs.
EOC	19	O	End of conversion. This output goes from a high to a low logic level on the trailing edge of the tenth I/O CLOCK and remains low until the conversion is complete and data are ready for transfer.
GND	10	I	The ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to this terminal.
I/O CLOCK	18	I	Input/output clock. This terminal receives the serial I/O CLOCK input and performs the following four functions: 1) It clocks the four input address bits into the address register on the first four rising edges of the I/O CLOCK with the multiplex address available after the fourth rising edge. 2) On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 3) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 4) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF +	14	I	The upper reference voltage value (nominally V_{CC}) is applied to this terminal. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF – terminal.
REF –	13	I	The lower reference voltage value (nominally ground) is applied to this terminal.
VCC	20	I	Positive supply voltage

detailed description

With chip select (\overline{CS}) inactive (high), the ADDRESS and I/O CLOCK inputs are initially disabled and DATA OUT is in the high-impedance state. When the serial interface takes \overline{CS} active (low), the conversion sequence begins with the enabling of I/O CLOCK and ADDRESS and the removal of DATA OUT from the high-impedance state. The serial interface then provides the 4-bit channel address to ADDRESS and the I/O CLOCK sequence to I/O CLOCK. During this transfer, the serial interface also receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host serial interface. The first four I/O clocks load the address register with the 4-bit address on ADDRESS, selecting the desired analog channel, and the next six clocks providing the control timing for sampling the analog input.



TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q

10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D – MARCH 1992 – APRIL 1996

detailed description (continued)

There are six basic serial-interface timing modes that can be used with the device. These modes are determined by the speed of I/O CLOCK and the operation of \overline{CS} as shown in Table 1. These modes are (1) a fast mode with a 10-clock transfer and \overline{CS} inactive (high) between conversion cycles, (2) a fast mode with a 10-clock transfer and \overline{CS} active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and \overline{CS} inactive (high) between conversion cycles. (4) a fast mode with a 16-clock transfer and \overline{CS} active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and \overline{CS} inactive (high) between conversion cycles, and (6) a slow mode with a 16-clock transfer and \overline{CS} active (low) continuously.

The MSB of the previous conversion appears at DATA OUT on the falling edge of \overline{CS} in mode 1, mode 3, and mode 5, on the rising edge of EOC in mode 2 and mode 4, and following the sixteenth clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of I/O CLOCK. Ten bits of data are transmitted to the host-serial interface through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the tenth clock falling edge, the EOC output goes low and returns to the high logic level when conversion is complete and the result can be read by the host. Also, on the tenth clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero when the I/O CLOCK transfer is more than ten clocks long.

Table 1 lists the operational modes with respect to the state of \overline{CS} , the number of I/O serial transfer clocks that can be used, and the timing edge on which the MSB of the previous conversion appears at the output.

Table 1. Mode Operation

MODES		\overline{CS}	NO. OF I/O CLOCKS	MSB AT DATA OUT†	TIMING DIAGRAM
Fast Modes	Mode 1	High between conversion cycles	10	\overline{CS} falling edge	Figure 9
	Mode 2	Low continuously	10	EOC rising edge	Figure 10
	Mode 3	High between conversion cycles	11 to 16‡	\overline{CS} falling edge	Figure 11
	Mode 4	Low continuously	16‡	EOC rising edge	Figure 12
Slow Modes	Mode 5	High between conversion cycles	11 to 16‡	\overline{CS} falling edge	Figure 13
	Mode 6	Low continuously	16‡	16th clock falling edge	Figure 14

† These edges also initiate serial-interface communication.

‡ No more than 16 clocks should be used.

fast modes

The device is in a fast mode when the serial I/O CLOCK data transfer is completed before the conversion is completed. With a 10-clock serial transfer, the device can only run in a fast mode since a conversion does not begin until the falling edge of the tenth I/O CLOCK.

mode 1: fast mode, \overline{CS} inactive (high) between conversion cycles, 10-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O CLOCK transfers and each transfer is ten clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 2: fast mode, \overline{CS} active (low) continuously, 10-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O CLOCK transfers and each transfer is ten clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.



TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D – MARCH 1992 – APRIL 1996

mode 3: fast mode, \overline{CS} inactive (high) between conversion cycles, 11- to 16-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 4: fast mode, \overline{CS} active (low) continuously, 16-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

slow modes

In a slow mode, the conversion is completed before the serial I/O CLOCK data transfer is completed. A slow mode requires a minimum 11-clock transfer into I/O CLOCK, and the rising edge of the eleventh clock must occur before the conversion period is complete; otherwise, the device loses synchronization with the host-serial interface and \overline{CS} has to be toggled to initialize the system. The eleventh rising edge of the I/O CLOCK must occur within 9.5 μ s after the tenth I/O clock falling edge.

mode 5: slow mode, \overline{CS} inactive (high) between conversion cycles, 11- to 16-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 6: slow mode, \overline{CS} active (low) continuously, 16-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions. The falling edge of the sixteenth I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16-clock transfer initiated by the serial interface.

address bits

The 4-bit analog channel-select address for the next conversion cycle is presented to the ADDRESS terminal (MSB first) and is clocked into the address register on the first four leading edges of I/O CLOCK. This address selects one of 14 inputs (11 analog inputs or three internal test inputs).

analog inputs and test modes

The 11 analog inputs and the three internal test inputs are selected by the 14-channel multiplexer according to the input address as shown in Tables 2 and 3. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching.

Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK, and sampling continues for six I/O CLOCK periods. The sample is held on the falling edge of the tenth I/O CLOCK. The three test inputs are applied to the multiplexer, sampled, and converted in the same manner as the external analog inputs.



TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q
10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH
SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D – MARCH 1992 – APRIL 1996

analog inputs and test modes (continued)

Table 2. Analog-Channel-Select Address

ANALOG INPUT SELECTED	VALUE SHIFTED INTO ADDRESS INPUT	
	BINARY	HEX
A0	0000	0
A1	0001	1
A2	0010	2
A3	0011	3
A4	0100	4
A5	0101	5
A6	0110	6
A7	0111	7
A8	1000	8
A9	1001	9
A10	1010	A

Table 3. Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED†	VALUE SHIFTED INTO ADDRESS INPUT		OUTPUT RESULT (HEX)‡
	BINARY	HEX	
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	B	200
V_{ref-}	1100	C	000
V_{ref+}	1101	D	3FF

† V_{ref+} is the voltage applied to the REF+ input, and V_{ref-} is the voltage applied to the REF- input.

‡ The output results shown are the ideal values and vary with the reference stability and with internal offsets.

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF-) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF-. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a 0 bit is placed in the output register and the 512-weight capacitor is switched to REF-. If the voltage at the summing node is less than the trip point of the threshold detector, a 1 bit is placed in the register and the 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are counted.



TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D – MARCH 1992 – APRIL 1996

converter and analog input (continued)

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.

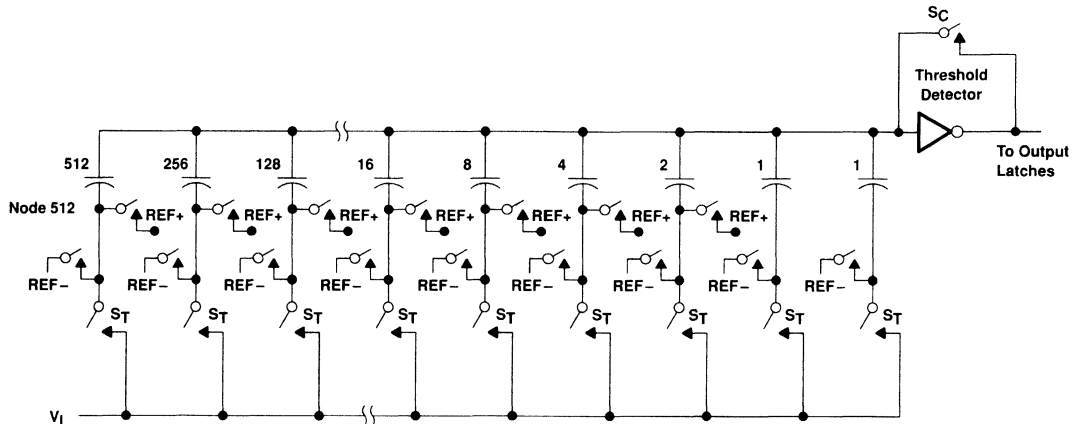


Figure 1. Simplified Model of the Successive-Approximation System

chip-select operation

The trailing edge of \overline{CS} starts all modes of operation, and \overline{CS} can abort a conversion sequence in any mode. A high-to-low transition on \overline{CS} within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Exercise care to prevent \overline{CS} from being taken low close to completion of conversion because the output data can be corrupted.

reference voltage inputs

There are two reference inputs used with the device: REF+ and REF-. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading respectively. The values of REF+, REF-, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF-.

TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q

10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D – MARCH 1992 – APRIL 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	-0.5 V to 6.5 V
Input voltage range, V_I	-0.3 V to $V_{CC} + 0.3$ V
Output voltage range, V_O	-0.3 V to $V_{CC} + 0.3$ V
Positive reference voltage, V_{ref+}	$V_{CC} + 0.1$ V
Negative reference voltage, V_{ref-}	-0.1 V
Peak input current (any input)	± 20 mA
Peak total input current (all inputs)	± 30 mA
Operating free-air temperature range, T_A : TLC1542C, TLC1543C	0°C to 70°C
TLC1542I, TLC1543I	-40°C to 85°C
TLC1542Q, TLC1543Q	-40°C to 125°C
TLC1542M	-55°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF- and GND wired together (unless otherwise noted).

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)	V_{CC}			V
Negative reference voltage, V_{ref-} (see Note 2)	0			V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)	2.5	V_{CC}	$V_{CC} + 0.2$	V
Analog input voltage (see Note 2)	0 to V_{CC}			V
High-level control input voltage, V_{IH}	$V_{CC} = 4.5$ V to 5.5 V			V
Low-level control input voltage, V_{IL}	$V_{CC} = 4.5$ V to 5.5 V			V
Setup time, address bits at data input before I/O CLOCK \uparrow , $t_{su(A)}$ (see Figure 4)	100			ns
Hold time, address bits after I/O CLOCK \uparrow , $t_h(A)$ (see Figure 4)	0			ns
Hold time, \overline{CS} low after last I/O CLOCK \downarrow , $t_h(CS)$ (see Figure 5)	0			ns
Setup time, \overline{CS} low before clocking in first address bit, $t_{su(CS)}$ (see Note 3 and Figure 5)	1.425			μ s
Clock frequency at I/O CLOCK (see Note 4)	0 to 2.1			MHz
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$	190			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$	190			ns
Transition time, I/O CLOCK, $t_t(I/O)$ (see Note 5 and Figure 6)	1			μ s
Transition time, ADDRESS and \overline{CS} , $t_t(CS)$	10			μ s
Operating free-air temperature, T_A	TLC1542C, TLC1543C	0 to 70		°C
	TLC1542I, TLC1543I	-40 to 85		
	TLC1542Q, TLC1543Q	-40 to 125		
	TLC1542M	-55 to 125		

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.

3. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.

4. For 11- to 16-bit transfers, after the tenth I/O CLOCK falling edge (≤ 2 V) at least 1 I/O CLOCK rising edge (≥ 2 V) must occur within 9.5 μ s.

5. This is the time required for the clock input signal to fall from V_{IHmin} to V_{ILmax} or to rise from V_{ILmax} to V_{IHmin} . In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 μ s for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.



TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q
10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH
SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D – MARCH 1992 – APRIL 1996

electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 4.5\text{ V to }5.5\text{ V}$, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage	$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -1.6\text{ mA}$	2.4		$V_{CC} - 0.1$	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$,	$I_{OH} = -20\text{ }\mu\text{A}$				
V _{OL}	Low-level output voltage	$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 1.6\text{ mA}$			0.4	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$,	$I_{OL} = 20\text{ }\mu\text{A}$			0.1	
I _{OZ}	Off-state (high-impedance-state) output current	$V_O = V_{CC}$,	\overline{CS} at V_{CC}			10	μA
		$V_O = 0$,	\overline{CS} at V_{CC}			-10	
I _{IH}	High-level input current	$V_I = V_{CC}$		0.005	2.5		μA
I _{IL}	Low-level input current	$V_I = 0$		-0.005	-2.5		μA
I _{CC}	Operating supply current	\overline{CS} at 0 V		0.8		2.5	mA
Selected channel leakage current TLC1542/TLC1543 C, I, or Q		Selected channel at V_{CC} ,	Unselected channel at 0 V			1	μA
		Selected channel at 0 V,	Unselected channel at V_{CC}			-1	
Selected channel leakage current TLC1542M		Selected channel at V_{CC} ,	Unselected channel at 0 V, $T_A = 25^\circ\text{C}$			1	μA
		Selected channel at 0 V, $T_A = 25^\circ\text{C}$	Unselected channel at V_{CC} .			-1	
		Selected channel at V_{CC} ,	Unselected channel at 0 V			2.5	
		Selected channel at 0 V,	Unselected channel at V_{CC}			-2.5	
Maximum static analog reference current into REF+		$V_{ref+} = V_{CC}$,	$V_{ref-} = \text{GND}$			10	μA
C _i	Input capacitance	Analog inputs		7		pF	
		Control inputs		5			

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.



TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q

10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D – MARCH 1992 – APRIL 1996

**operating characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 4.5\text{ V to }5.5\text{ V}$, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)**

		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E _L	Linearity error (see Note 6)	TLC1542C, I, or Q			±0.5	LSB
		TLC1543C, I, or Q			±1	LSB
		TLC1542M			±1	LSB
E _{ZS}	Zero-scale error (see Note 7)	TLC1542C, I, or Q	See Note 2		±1	LSB
		TLC1543C, I, or Q	See Note 2		±1	LSB
		TLC1542M	See Note 2		±1	LSB
E _{FS}	Full-scale error (see Note 7)	TLC1542C, I, or Q	See Note 2		±1	LSB
		TLC1543C, I, or Q	See Note 2		±1	LSB
		TLC1542M	See Note 2		±1	LSB
	Total unadjusted error (see Note 8)	TLC1542C, I, or Q			±1	LSB
		TLC1543C, I, or Q			±1	LSB
		TLC1542M			±1	LSB
	Self-test output code (see Table 3 and Note 9)	ADDRESS = 1011		512		
		ADDRESS = 1100		0		
		ADDRESS = 1101		1023		
t _{conv}	Conversion time	See timing diagrams			21	μs
t _c	Total cycle time (access, sample, and conversion)	See timing diagrams and Note 10			21 +10 I/O CLOCK periods	μs
t _{acq}	Channel acquisition time (sample)	See timing diagrams and Note 10			6	I/O CLOCK periods
t _v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 6	10			ns
t _{d(I/O-DATA)}	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 6			240	ns
t _{d(I/O-EOC)}	Delay time, tenth I/O CLOCK↓ to EOC↓	See Figure 7		70	240	ns
t _{d(EOC-DATA)}	Delay time, EOC↑ to DATA OUT (MSB)	See Figure 8			100	ns

† All typical values are at T_A = 25°C.

- NOTES:
- Analog input voltages greater than that applied to REF+ convert as all ones (111111111), while input voltages less than that applied to REF- convert as all zeros (000000000). The device is functional with reference voltages down to 1 V (V_{ref+} - V_{ref-}); however, the electrical specifications are no longer applicable.
 - Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
 - Zero-scale error is the difference between 000000000 and the converted output for zero input voltage; full-scale error is the difference between 111111111 and the converted output for full-scale input voltage.
 - Total unadjusted error comprises linearity, zero-scale, and full-scale errors.
 - Both the input address and the output codes are expressed in positive logic.
 - I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 6)



TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q

10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D – MARCH 1992 – APRIL 1996

**operating characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 4.5\text{ V to }5.5\text{ V}$, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted) (continued)**

		TEST CONDITIONS	MIN	TYPT†	MAX	UNIT
t_{PZH}, t_{PZL}	Enable time, $\overline{CS}\downarrow$ to DATA OUT (MSB driven)	See Figure 3		1.3		μs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{CS}\uparrow$ to DATA OUT (high impedance)	See Figure 3			150	ns
$t_r(\text{EOC})$	Rise time, EOC	See Figure 8			300	ns
$t_f(\text{EOC})$	Fall time, EOC	See Figure 7			300	ns
$t_r(\text{DATA})$	Rise time, data bus	See Figure 6			300	ns
$t_f(\text{DATA})$	Fall time, data bus	See Figure 6			300	ns
$t_d(\text{I/O-CS})$	Delay time, tenth I/O CLOCK \downarrow to $\overline{CS}\downarrow$ to abort conversion (see Note 11)				9	μs

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 11. Any transitions of \overline{CS} are recognized as valid only if the level is maintained for a setup time plus two falling edges of the internal clock (1.425 μs) after the transition.

PARAMETER MEASUREMENT INFORMATION

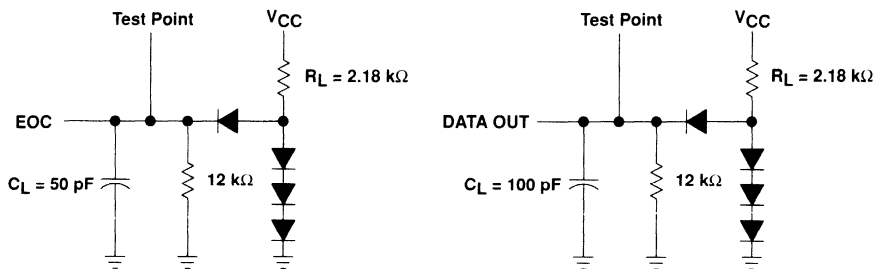


Figure 2. Load Circuits

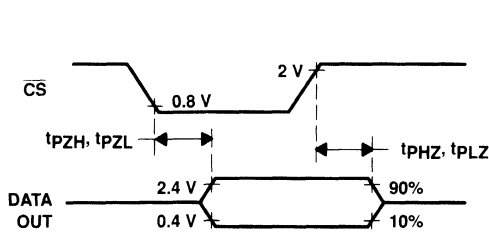


Figure 3. DATA OUT Enable and Disable Voltage Waveforms

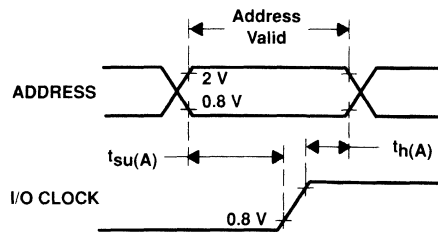


Figure 4. ADDRESS Setup and Hold Time Voltage Waveforms

TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q
10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH
SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D – MARCH 1992 – APRIL 1996

PARAMETER MEASUREMENT INFORMATION

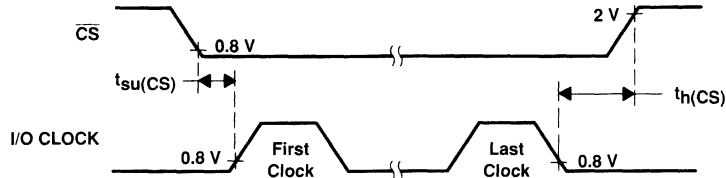


Figure 5. I/O CLOCK Setup and Hold Time Voltage Waveforms

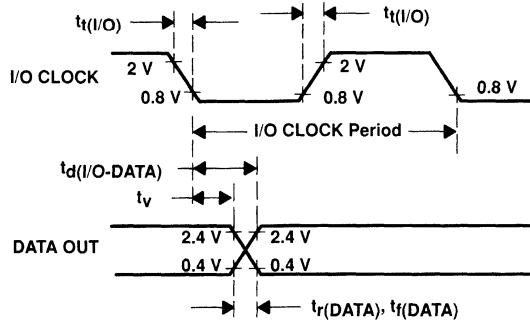


Figure 6. I/O CLOCK and DATA OUT Voltage Waveforms

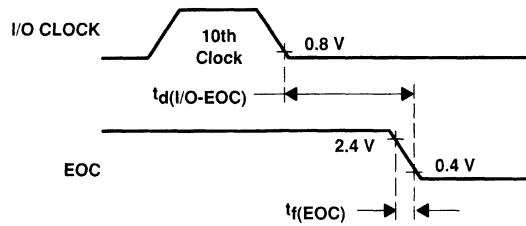


Figure 7. I/O CLOCK and EOC Voltage Waveforms

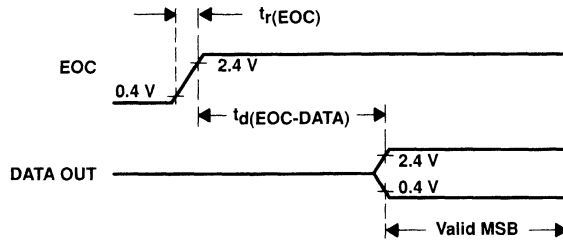


Figure 8. EOC and DATA OUT Voltage Waveforms



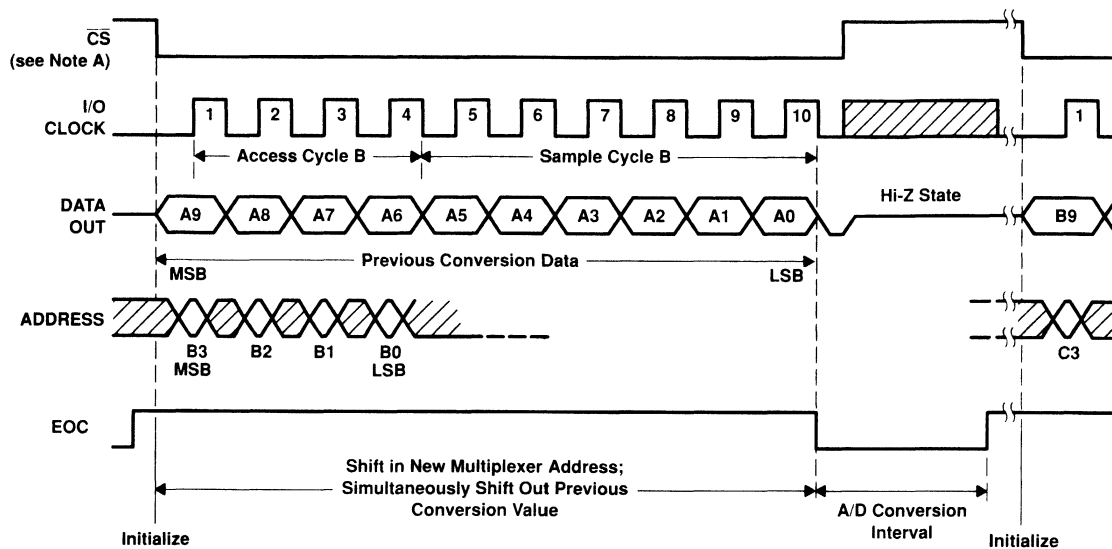
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 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH
 SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D - MARCH 1992 - APRIL 1996

PARAMETER MEASUREMENT INFORMATION

timing diagrams



NOTE A: To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.

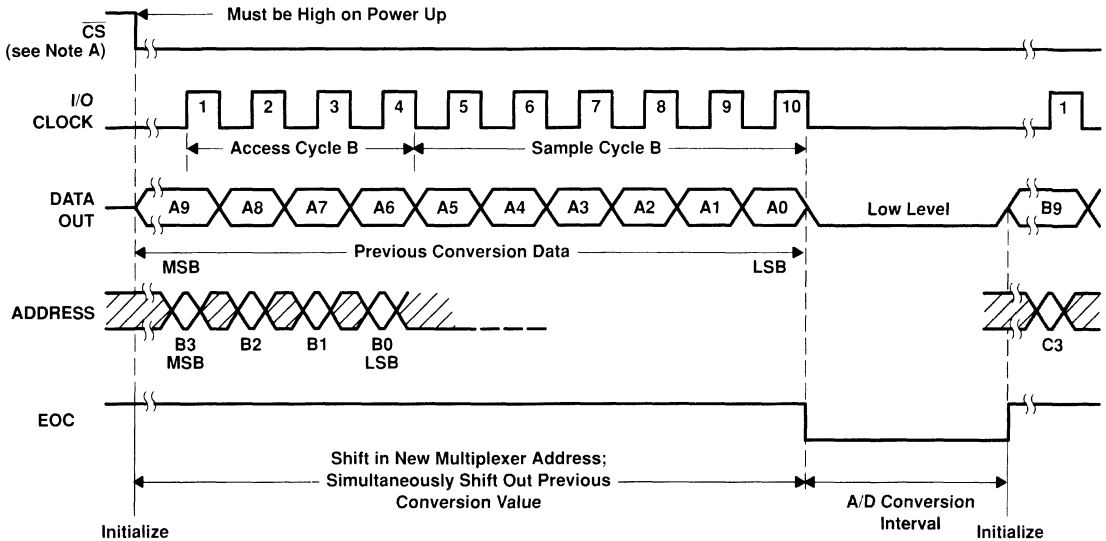
Figure 9. Timing for 10-Clock Transfer Using \overline{CS}

TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q
10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH
SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D – MARCH 1992 – APRIL 1996

PARAMETER MEASUREMENT INFORMATION

timing diagrams (continued)



NOTE A: To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after \overline{CS} before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.

Figure 10. Timing for 10-Clock Transfer Not Using \overline{CS}

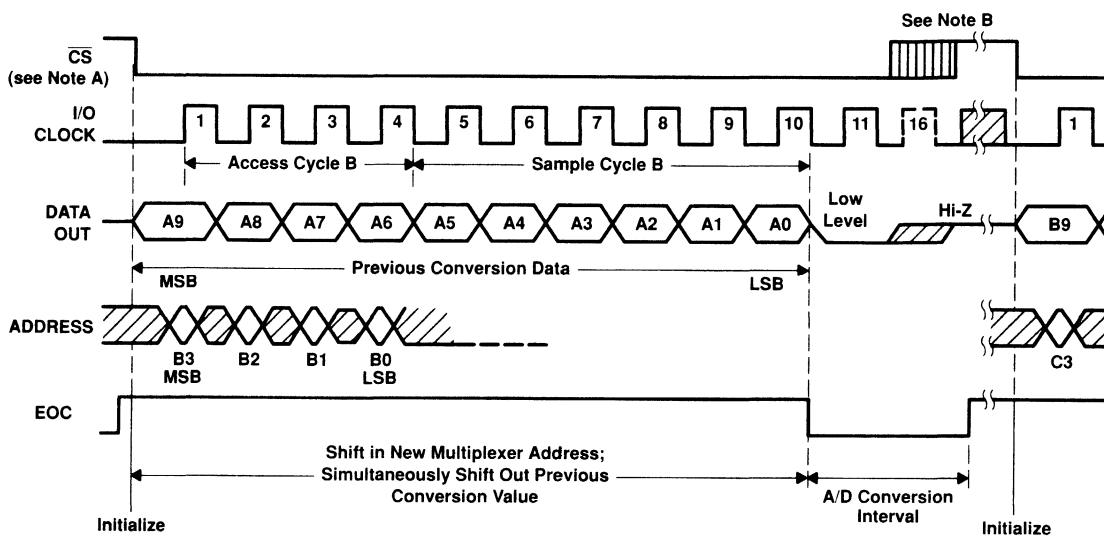


TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q
 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH
 SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D - MARCH 1992 - APRIL 1996

PARAMETER MEASUREMENT INFORMATION

timing diagrams (continued)



- NOTES: A. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.
- B. A low-to-high transition of \overline{CS} disables ADDRESS and the I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

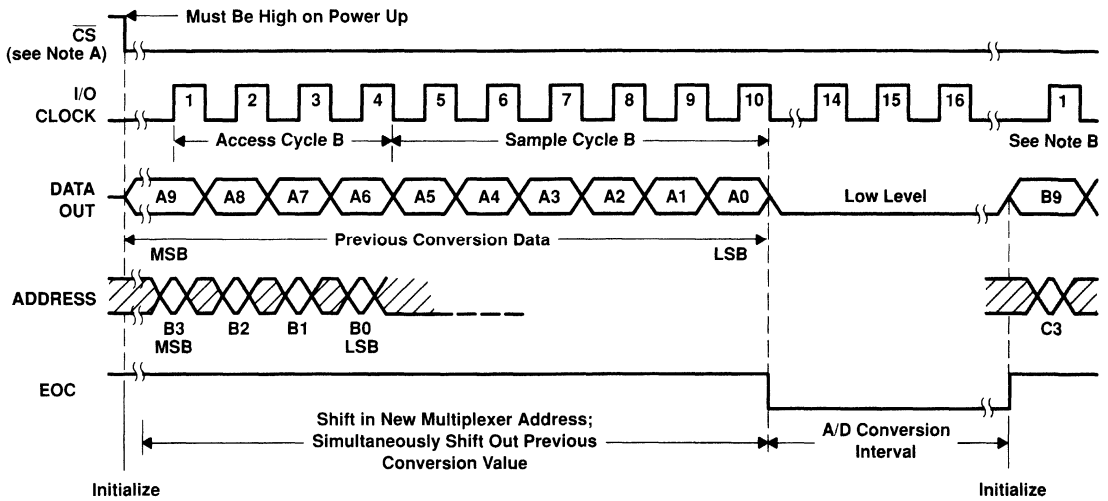
Figure 11. Timing for 11- to 16-Clock Transfer Using \overline{CS} (Serial Transfer Interval Shorter Than Conversion)

TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q
10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH
SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D – MARCH 1992 – APRIL 1996

PARAMETER MEASUREMENT INFORMATION

timing diagrams (continued)



- NOTES: A. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.
- B. The first I/O CLOCK must occur after the rising edge of EOC.

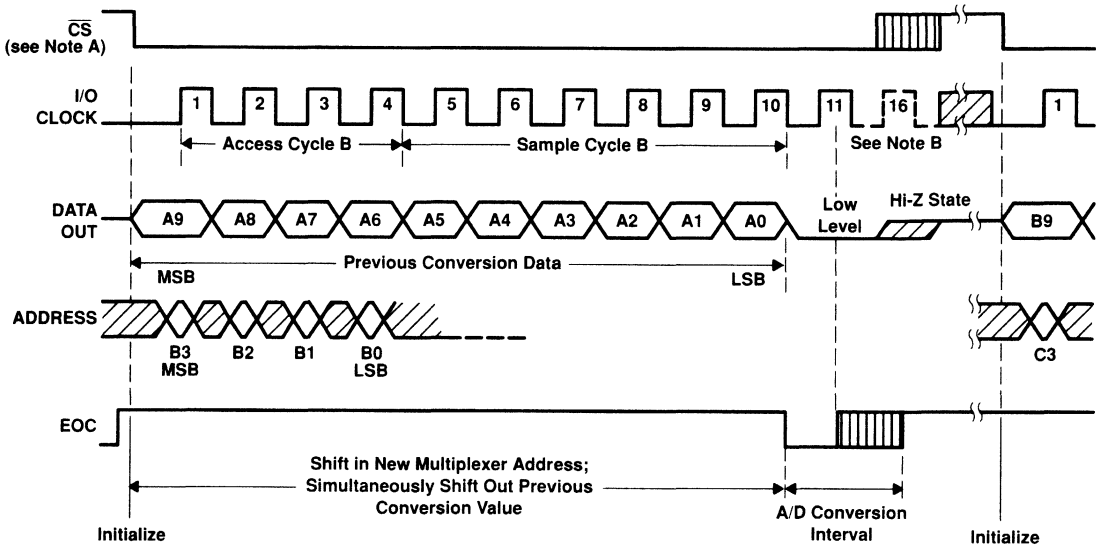
Figure 12. Timing for 16-Clock Transfer Not Using \overline{CS} (Serial Transfer Interval Shorter Than Conversion)

TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q
10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH
SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D - MARCH 1992 - APRIL 1996

PARAMETER MEASUREMENT INFORMATION

timing diagrams (continued)



- NOTES: A. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.
- B. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.

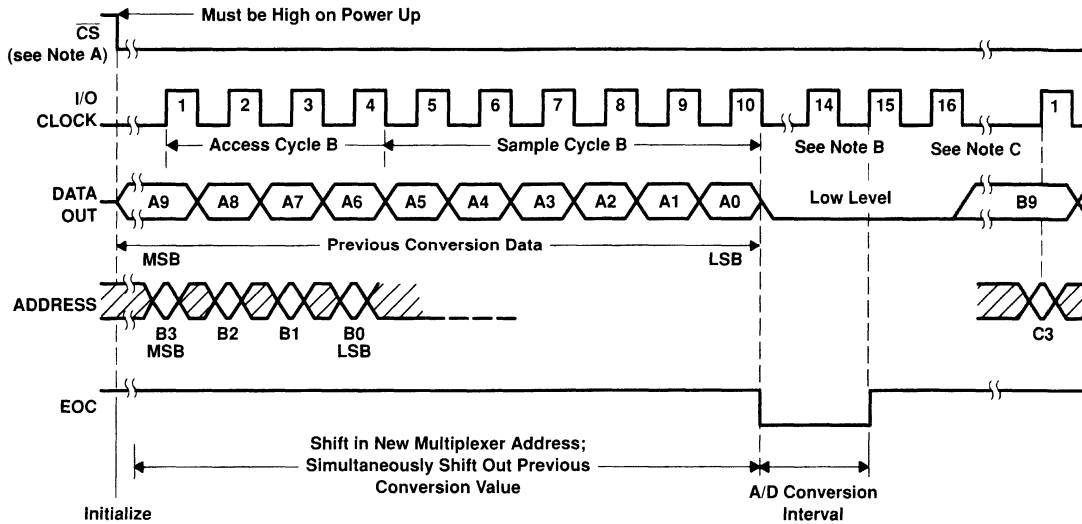
Figure 13. Timing for 11- to 16-Clock Transfer Using \overline{CS} (Serial Transfer Interval Longer Than Conversion)

TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q
10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH
SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D – MARCH 1992 – APRIL 1996

PARAMETER MEASUREMENT INFORMATION

timing diagrams (continued)



- NOTES: A. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.
- B. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.
- C. The I/O CLOCK sequence is exactly 16 clock pulses long.

Figure 14. Timing for 16-Clock Transfer Not Using \overline{CS} (Serial Transfer Interval Longer Than Conversion)

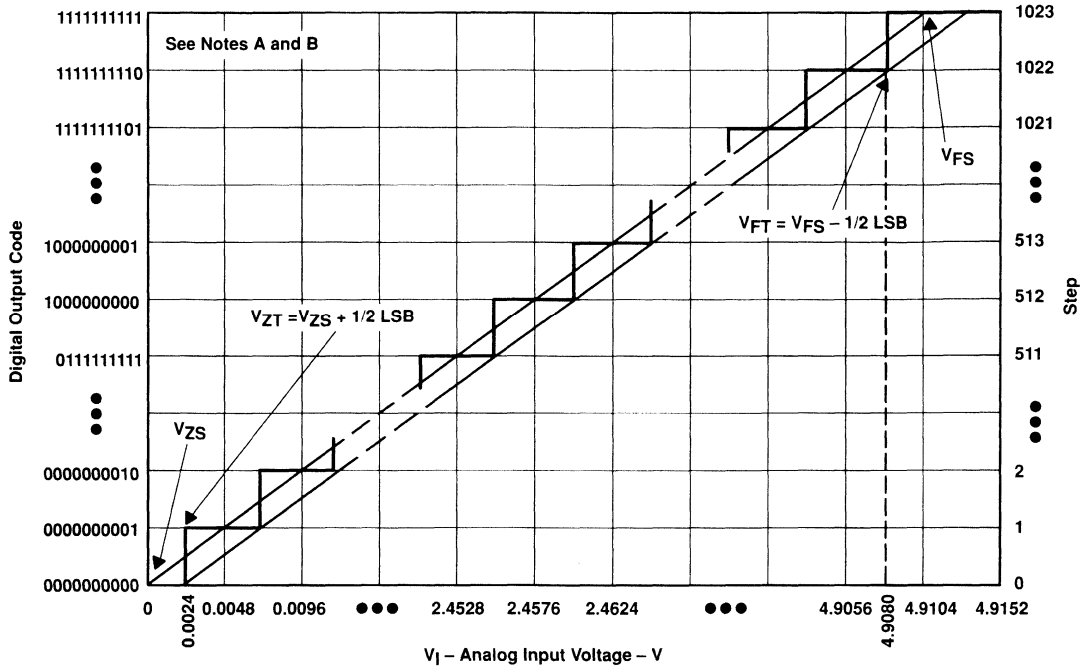


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TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q
 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH
 SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D - MARCH 1992 - APRIL 1996

APPLICATION INFORMATION



- NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0024 V and the transition to full scale (V_{FT}) is 4.908 V. $1 \text{ LSB} = 4.8 \text{ mV}$.
 B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 15. Ideal Conversion Characteristics

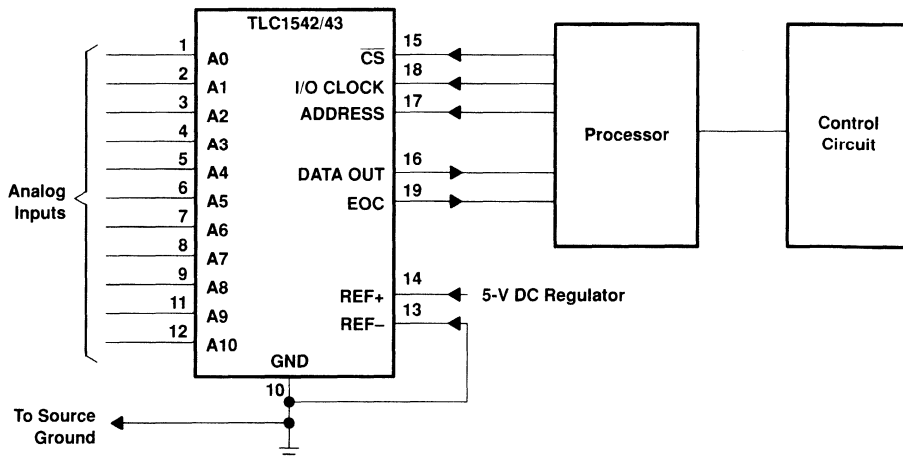


Figure 16. Serial Interface

TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, TLC1543Q
10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH
SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS052D – MARCH 1992 – APRIL 1996

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 17, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c / R_t C_i}\right) \quad (1)$$

where

$$R_t = R_S + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S/2048) \quad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S/2048) = V_S \left(1 - e^{-t_c / R_t C_i}\right) \quad (3)$$

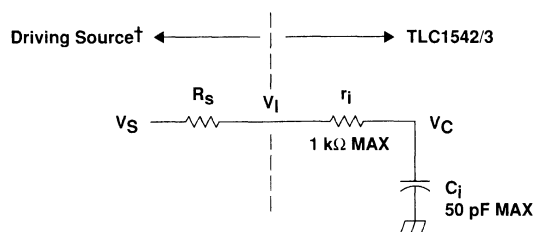
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(2048) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_S + 1 \text{ k}\Omega) \times 60 \text{ pF} \times \ln(2048) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at A0–A10
 V_S = External Driving Source Voltage
 R_S = Source Resistance
 r_i = Input Resistance
 C_i = Equivalent Input Capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 17. Equivalent Input Circuit Including the Driving Source

TLC1549C, TLC1549I, TLC1549M 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

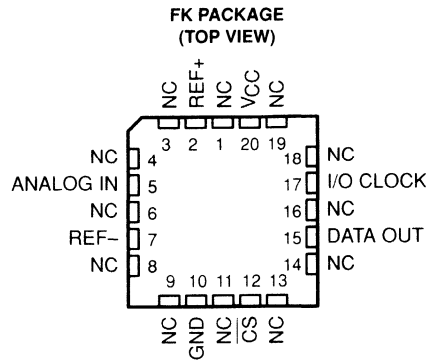
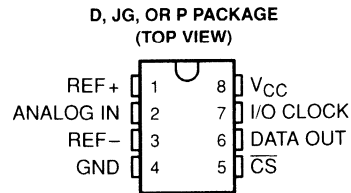
- 10-Bit-Resolution A/D Converter
- Inherent Sample and Hold
- Total Unadjusted Error . . . ± 1 LSB Max
- On-Chip System Clock
- Terminal Compatible With TLC549 and TLV1549
- CMOS Technology

description

The TLC1549C, TLC1549I, and TLC1549M are 10-bit, switched-capacitor, successive-approximation analog-to-digital converters. These devices have two digital inputs and a 3-state output [chip select (\overline{CS}), input-output clock (I/O CLOCK), and data output (DATA OUT)] that provide a three-wire interface to the serial port of a host processor.

The sample-and-hold function is automatic. The converter incorporated in these devices features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

The TLC1549C is characterized for operation from 0°C to 70°C. The TLC1549I is characterized for operation from -40°C to 85°C. The TLC1549M is characterized for operation over the full military temperature range of -55°C to 125°C.



NC – No internal connection

AVAILABLE OPTIONS

T _A	PACKAGE			
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	TLC1549CD	—	—	TLC1549CP
-40°C to 85°C	TLC1549ID	—	—	TLC1549IP
-55°C to 125°C	—	TLC1549MFK	TLC1549MJG	—

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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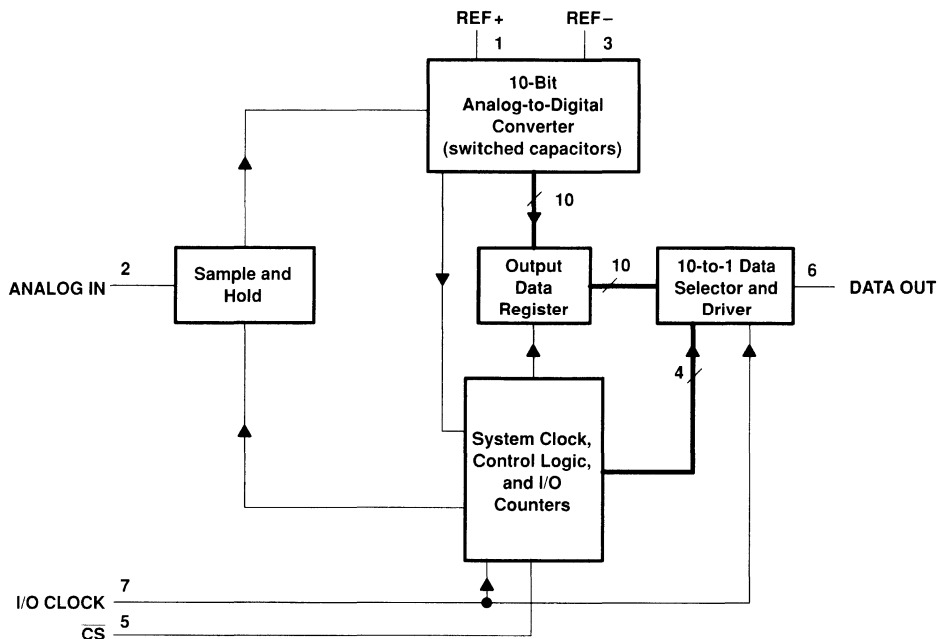
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TLC1549C, TLC1549I, TLC1549M

10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

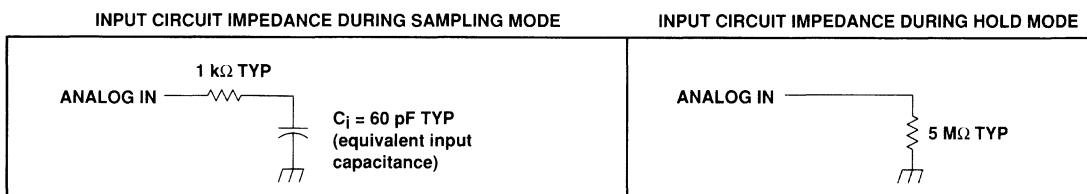
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functional block diagram



Terminal numbers shown are for the D, JG, and P packages only.

typical equivalent inputs



TLC1549C, TLC1549I, TLC1549M

10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ANALOG IN	2	I	Analog signal input. The driving source impedance should be $\leq 1 \text{ k}\Omega$. The external driving source to ANALOG IN should have a current capability $\geq 10 \text{ mA}$.
$\overline{\text{CS}}$	5	I	Chip select. A high-to-low transition on $\overline{\text{CS}}$ resets the internal counters and controls and enables DATA OUT and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OUT	6	O	This 3-state serial output for the A/D conversion result is in the high-impedance state when $\overline{\text{CS}}$ is high and active when $\overline{\text{CS}}$ is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives DATAOUT to the logic level corresponding to the next most significant bit, and the remaining bits are shifted out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs.
GND	4		The ground return for internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	7	I	Input/output clock. I/O CLOCK receives the serial I/O CLOCK input and performs the following three functions: 1) On the third falling edge of I/O CLOCK, the analog input voltage begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 2) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 3) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF +	1	I	The upper reference voltage value (nominally V_{CC}) is applied to REF +. The maximum input voltage range is determined by the difference between the voltage applied to REF + and the voltage applied to REF –.
REF –	3	I	The lower reference voltage value (nominally ground) is applied to REF –.
V_{CC}	8		Positive supply voltage

detailed description

With chip select ($\overline{\text{CS}}$) inactive (high), I/O CLOCK is initially disabled and DATA OUT is in the high impedance state. When the serial interface takes $\overline{\text{CS}}$ active (low), the conversion sequence begins with the enabling of I/O CLOCK and the removal of DATA OUT from the high-impedance state. The serial interface then provides the I/O CLOCK sequence to I/O CLOCK and receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host serial interface. The first ten I/O clocks provide the control timing for sampling the analog input.

There are six basic serial interface timing modes that can be used with the TLC1549. These modes are determined by the speed of I/O CLOCK and the operation of $\overline{\text{CS}}$ as shown in Table 1. These modes are (1) a fast mode with a 10-clock transfer and $\overline{\text{CS}}$ inactive (high) between transfers, (2) a fast mode with a 10-clock transfer and $\overline{\text{CS}}$ active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and $\overline{\text{CS}}$ inactive (high) between transfers, (4) a fast mode with a 16-bit transfer and $\overline{\text{CS}}$ active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and $\overline{\text{CS}}$ inactive (high) between transfers, and (6) a slow mode with a 16-clock transfer and $\overline{\text{CS}}$ active (low) continuously.

The MSB of the previous conversion appears on DATA OUT on the falling edge of $\overline{\text{CS}}$ in mode 1, mode 3, and mode 5, within $21 \mu\text{s}$ from the falling edge of the tenth I/O CLOCK in mode 2 and mode 4, and following the sixteenth clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of I/O CLOCK. Ten bits of data are transmitted to the host serial interface through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the tenth clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLOCK transfer is more than ten clocks long.

Table 1 lists the operational modes with respect to the state of $\overline{\text{CS}}$, the number of I/O serial transfer clocks that can be used, and the timing on which the MSB of the previous conversion appears at the output.



TLC1549C, TLC1549I, TLC1549M

10-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

detailed description

Table 1. Mode Operation

MODES		\overline{CS}	NO. OF I/O CLOCKS	MSB AT Terminal 6†	TIMING DIAGRAM
Fast Modes	Mode 1	High between conversion cycles	10	\overline{CS} falling edge	Figure 6
	Mode 2	Low continuously	10	Within 21 μ s	Figure 7
	Mode 3	High between conversion cycles	11 to 16‡	\overline{CS} falling edge	Figure 8
	Mode 4	Low continuously	16‡	Within 21 μ s	Figure 9
Slow Modes	Mode 5	High between conversion cycles	11 to 16‡	\overline{CS} falling edge	Figure 10
	Mode 6	Low continuously	16‡	16th clock falling edge	Figure 11

† This timing also initiates serial interface communication.

‡ No more than 16 clocks should be used.

All the modes require a minimum period of 21 μ s after the falling edge of the tenth I/O CLOCK before a new transfer sequence can begin. During a serial I/O CLOCK data transfer, \overline{CS} must be active (low) so that I/O CLOCK is enabled. When \overline{CS} is toggled between data transfers (modes 1, 3, and 5), the transitions at \overline{CS} are recognized as valid only if the level is maintained for a minimum period of 1.425 μ s after the transition. If the transfer is more than ten I/O clocks (modes 3, 4, 5, and 6), the rising edge of the eleventh clock must occur within 9.5 μ s after the falling edge of the tenth I/O CLOCK; otherwise, the device could lose synchronization with the host serial interface and \overline{CS} has to be toggled to restore proper operation.

fast modes

The TLC1549 is in a fast mode when the serial I/O CLOCK data transfer is completed within 21 μ s from the falling edge of the tenth I/O CLOCK. With a ten-clock serial transfer, the device can only run in a fast mode.

mode 1: fast mode, \overline{CS} inactive (high) between transfers, 10-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O CLOCK transfers and each transfer is ten clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 2: fast mode, \overline{CS} active (low) continuously, 10-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O CLOCK transfers and each transfer is ten clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions. Within 21 μ s after the falling edge of the tenth I/O CLOCK, the MSB of the previous conversion appears at DATA OUT.

mode 3: fast mode, \overline{CS} inactive (high) between transfers, 11- to 16-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 4: fast mode, \overline{CS} active (low) continuously, 16-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions. Within 21 μ s after the falling edge of the tenth I/O CLOCK, the MSB of the previous conversion appears at DATA OUT.

slow modes

In a slow mode, the serial I/O CLOCK data transfer is completed after 21 μ s from the falling edge of the tenth I/O CLOCK.



TLC1549C, TLC1549I, TLC1549M 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

mode 5: slow mode, \overline{CS} inactive (high) between transfers, 11- to 16-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 6: slow mode, \overline{CS} active (low) continuously, 16-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions. The falling edge of the sixteenth I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16 clock transfer initiated by the serial interface.

analog input sampling

Sampling of the analog input starts on the falling edge of the third I/O CLOCK, and sampling continues for seven I/O CLOCK periods. The sample is held on the falling edge of the tenth I/O CLOCK.

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF-) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF-. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF-. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and this 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are determined.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.



TLC1549C, TLC1549I, TLC1549M
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

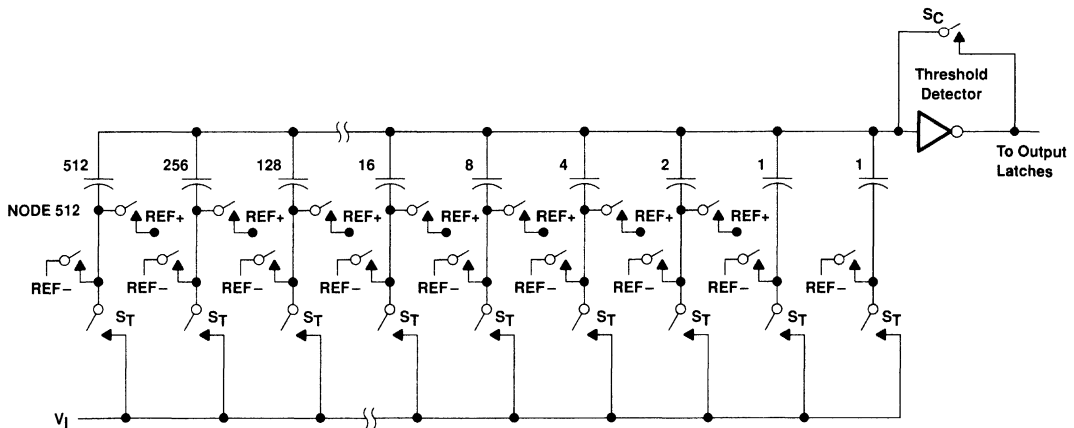


Figure 1. Simplified Model of the Successive-Approximation System

chip-select operation

The trailing edge of \overline{CS} starts all modes of operation, and \overline{CS} can abort a conversion sequence in any mode. A high-to-low transition on \overline{CS} within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Care should be exercised to prevent \overline{CS} from being taken low close to completion of conversion because the output data may be corrupted.

reference voltage inputs

There are two reference inputs used with the TLC1549: REF+ and REF-. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading respectively. The values of REF+, REF-, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF-.

TLC1549C, TLC1549I, TLC1549M 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1):	TLC1549C, TLC1549I	–0.5 V to 6.5 V
	TLC1549M	–0.5 V to 6 V
Input voltage range, V_I (any input)		–0.3 V to $V_{CC} + 0.3$ V
Output voltage range, V_O		–0.3 V to $V_{CC} + 0.3$ V
Positive reference voltage, V_{ref+}		$V_{CC} + 0.1$ V
Negative reference voltage, V_{ref-}		–0.1 V
Peak input current (any input)		± 20 mA
Peak total input current (all inputs)		± 30 mA
Operating free-air temperature range, T_A :	TLC1549C	0°C to 70°C
	TLC1549I	–40°C to 85°C
	TLC1549M	–55°C to 125°C
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from the case for 10 seconds		260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to ground with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)		V_{CC}			V
Negative reference voltage, V_{ref-} (see Note 2)		0			V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)		2.5	V_{CC}	$V_{CC} + 0.2$	V
Analog input voltage (see Note 2)		0			V_{CC}
High-level control input voltage, V_{IH}	$V_{CC} = 4.5$ V to 5.5 V	2			V
Low-level control input voltage, V_{IL}	$V_{CC} = 4.5$ V to 5.5 V	0.8			V
Clock frequency at I/O CLOCK (see Note 3)		0			2.1
Setup time, \overline{CS} low before first I/O CLOCK \downarrow , $t_{su}(CS)$ (see Note 4)		1.425			μ s
Hold time, \overline{CS} low after last I/O CLOCK \downarrow , $t_h(CS)$		0			ns
Pulse duration, I/O CLOCK high, $t_{wH}(I/O)$		190			ns
Pulse duration, I/O CLOCK low, $t_{wL}(I/O)$		190			ns
Transition time, I/O CLOCK, $t_t(I/O)$ (see Note 5 and Figure 5)		1			μ s
Transition time, \overline{CS} , $t_t(CS)$		10			μ s
Operating free-air temperature, T_A	TLC1549C	0			70
	TLC1549I	–40			85
	TLC1549M	–55			125

- NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF– convert as all zeros (0000000000). The TLC1549 is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.
3. For 11- to 16-bit transfers, after the tenth I/O CLOCK falling edge (≤ 2 V) at least 1 I/O CLOCK rising edge (≥ 2 V) must occur within 9.5 μ s.
4. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to the I/O CLOCK. No attempt should be made to clock out the data until the minimum \overline{CS} setup time has elapsed.
5. This is the time required for the clock input signal to fall from V_{IHmin} to V_{ILmax} or to rise from V_{ILmax} to V_{IHmin} . In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 μ s for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.



TLC1549C, TLC1549I, TLC1549M
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 4.5\text{ V to }5.5\text{ V}$, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
V _{OH}	High-level output voltage	V _{CC} = 4.5 V, I _{OH} = -1.6 mA	2.4			V	
		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -20 μA	V _{CC} -0.1				
V _{OL}	Low-level output voltage	V _{CC} = 4.5 V, I _{OL} = 1.6 mA			0.4	V	
		V _{CC} = 4.5 V to 5.5 V, I _{OL} = 20 μA			0.1		
I _{OZ}	Off-state (high-impedance-state) output current	V _O = V _{CC} , \overline{CS} at V _{CC}			10	μA	
		V _O = 0, \overline{CS} at V _{CC}			-10		
I _{IH}	High-level input current	V _I = V _{CC}		0.005	2.5	μA	
I _{IL}	Low-level input current	V _I = 0		-0.005	-2.5	μA	
I _{CC}	Operating supply current	\overline{CS} at 0 V		0.8	2.5	mA	
Analog input leakage current		V _I = V _{CC}			1	μA	
		V _I = 0			-1		
Maximum static analog reference current into REF+		V _{ref+} = V _{CC} , V _{ref-} = GND			10	μA	
C _i	Input capacitance	TLC1549C, I (Analog)	During sample cycle		30	55	pF
		TLC1549M (Analog)	During sample cycle		30		
		TLC1549C, I (Control)			5	15	
		TLC1549M (Control)			5		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.



TLC1549C, TLC1549I, TLC1549M 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

**operating characteristics over recommended operating free-air temperature range,
V_{CC} = V_{ref+} = 4.5 V to 5.5 V, I/O CLOCK frequency = 2.1 MHz**

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
E _L	Linearity error (see Note 6)			±1	LSB
E _{ZS}	Zero-scale error (see Note 7)	See Note 2		±1	LSB
E _{FS}	Full-scale error (see Note 7)	See Note 2		±1	LSB
	Total unadjusted error (see Note 8)			±1	LSB
t _{conv}	Conversion time	See Figures 6–10		21	μs
t _c	Total cycle time (access, sample, and conversion)	See Figures 6–10, See Note 9		21 + 10 I/O CLOCK periods	μs
t _v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 5	10		ns
t _{d(I/O-DATA)}	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 5		240	ns
t _{PZH} , t _{PZL}	Enable time, CS↓ to DATA OUT (MSB driven)	See Figure 3		1.3	μs
t _{PHZ} , t _{PLZ}	Disable time, CS↑ to DATA OUT (high impedance)	See Figure 3		180	ns
t _{r(bus)}	Rise time, data bus	See Figure 5		300	ns
t _{f(bus)}	Fall time, data bus	See Figure 5		300	ns
t _{d(I/O-CS)}	Delay time, tenth I/O CLOCK↓ to CS↓ to abort conversion (see Note 10)			9	μs

- NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000). The TLC1549 is functional with reference voltages down to 1 V (V_{ref+} - V_{ref-}); however, the electrical specifications are no longer applicable.
6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Zero error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
8. Total unadjusted error comprises linearity, zero, and full-scale errors.
9. I/O CLOCK period = 1/(I/O CLOCK frequency). Sampling begins on the falling edge of the third I/O CLOCK, continues for seven I/O CLOCK periods, and ends on the falling edge of the 10th I/O CLOCK (see Figure 5).
10. Any transitions of CS are recognized as valid only if the level is maintained for a minimum of a setup time plus two falling edges of the internal clock (1.425 μs) after the transition.



TLC1549C, TLC1549I, TLC1549M
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

PARAMETER MEASUREMENT INFORMATION

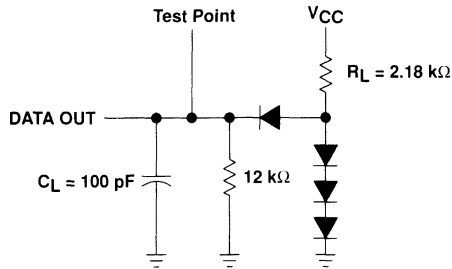


Figure 2. Load Circuit

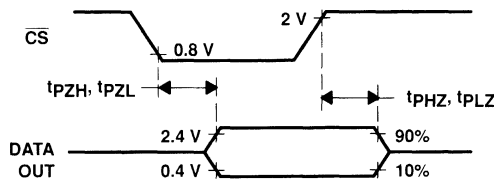


Figure 3. DATA OUT to Hi-Z Voltage Waveforms

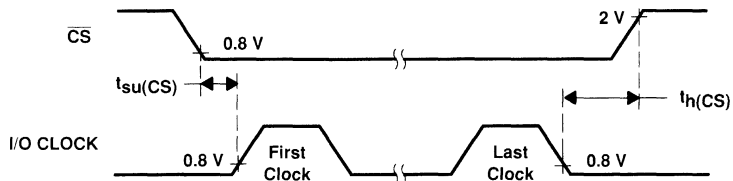


Figure 4. CS to I/O CLOCK Voltage Waveforms

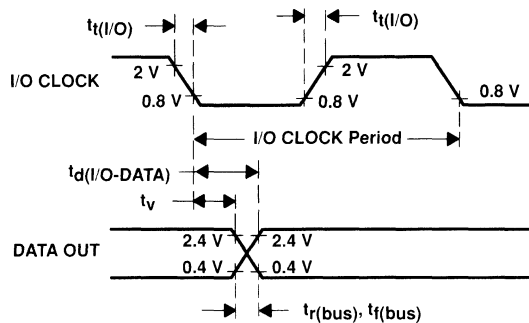


Figure 5. I/O CLOCK and DATA OUT Voltage Waveforms

TLC1549C, TLC1549I, TLC1549M 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS059C - DECEMBER 1992 - REVISED MARCH 1995

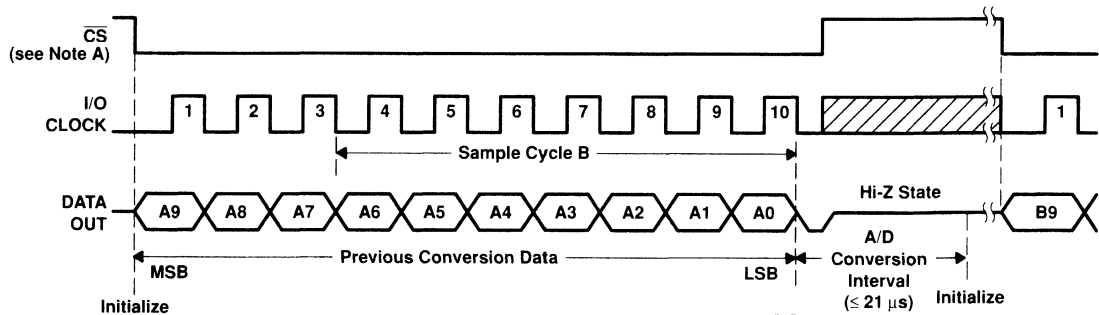


Figure 6. Timing for 10-Clock Transfer Using \overline{CS}

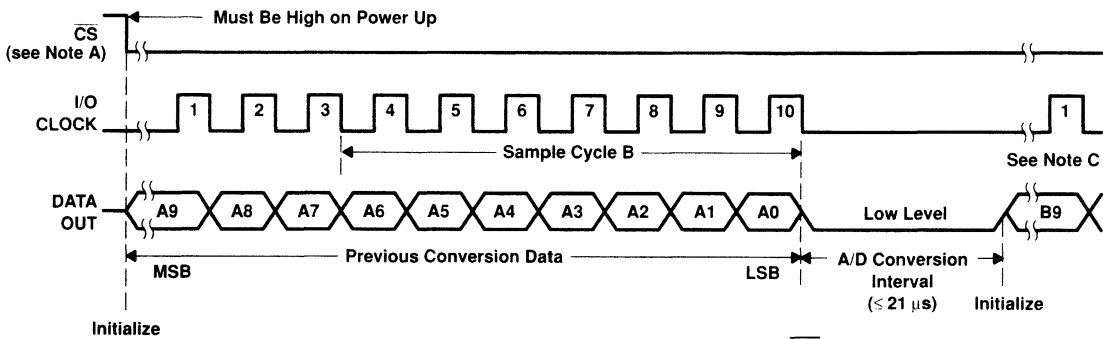


Figure 7. Timing for 10-Clock Transfer Not Using \overline{CS}

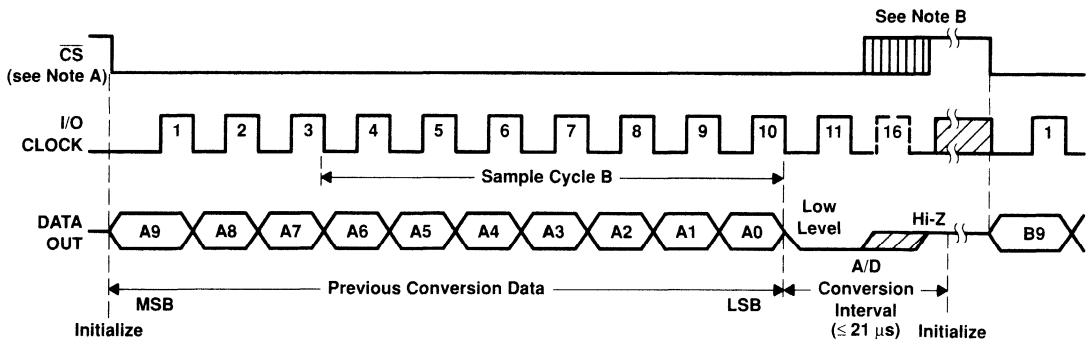


Figure 8. Timing for 11- to 16-Clock Transfer Using \overline{CS} (Serial Transfer Completed Within 21 μs)

- NOTES:
- To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after \overline{CS} before responding to the I/O CLOCK. No attempt should be made to clock out the data until the minimum \overline{CS} setup time has elapsed.
 - A low-to-high transition of \overline{CS} disables I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.
 - The first I/O CLOCK must occur after the end of the previous conversion.

TLC1549C, TLC1549I, TLC1549M 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

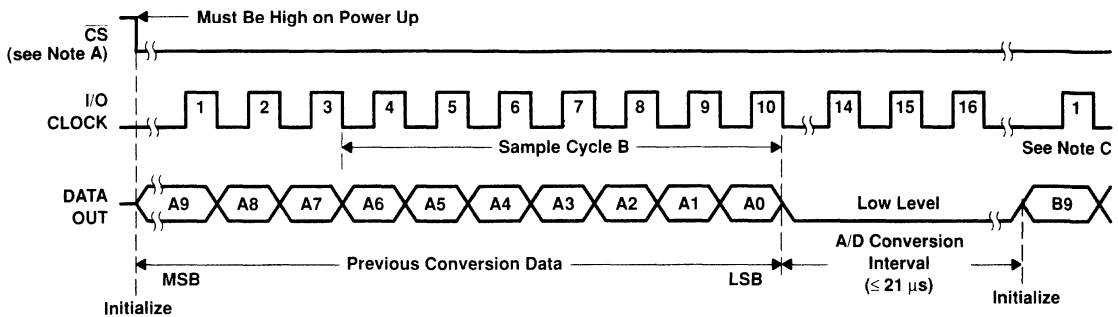


Figure 9. Timing for 16-Clock Transfer Not Using \overline{CS} (Serial Transfer Completed Within 21 μs)

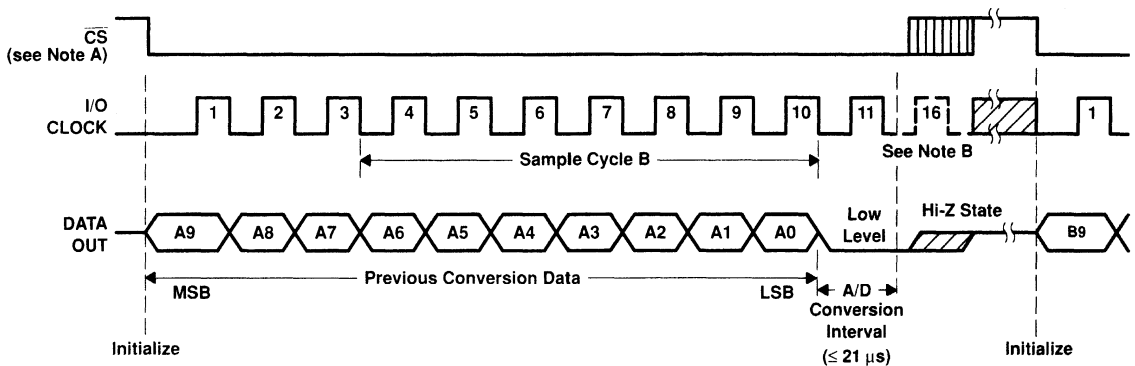


Figure 10. Timing for 11- to 16-Clock Transfer Using \overline{CS} (Serial Transfer Completed After 21 μs)

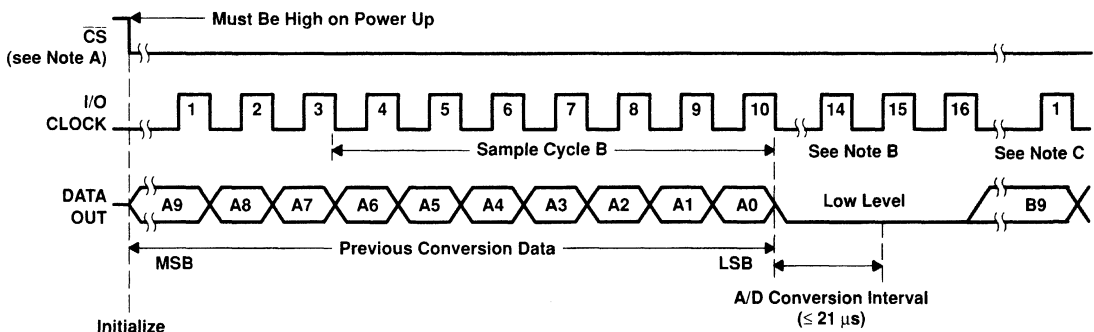


Figure 11. Timing for 16-Clock Transfer Not Using \overline{CS} (Serial Transfer Completed After 21 μs)

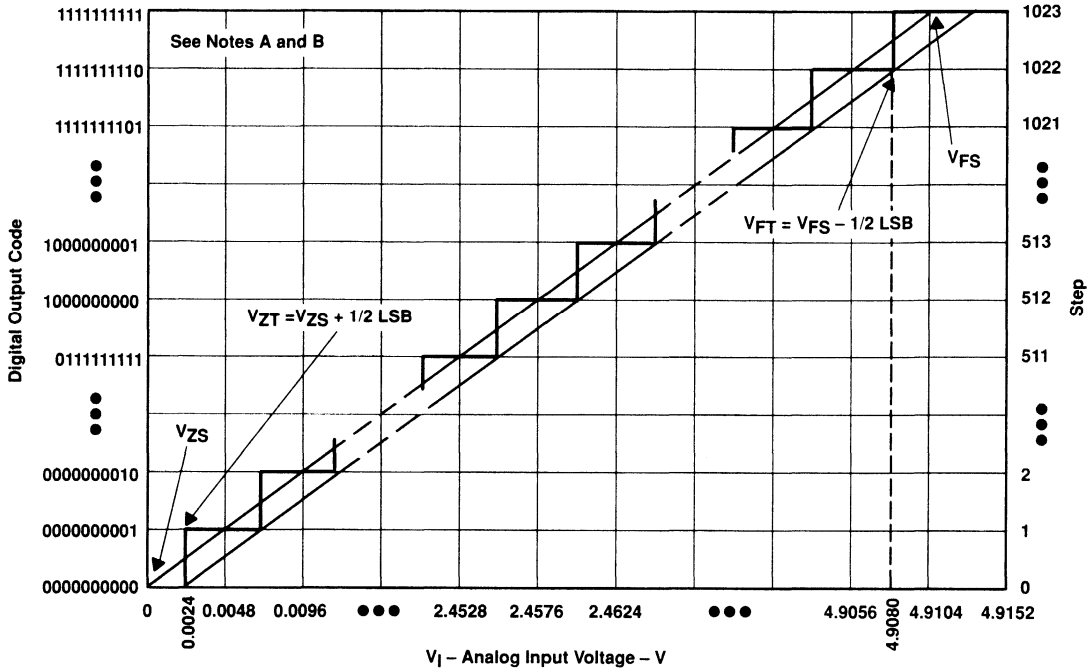
- NOTES:
- To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after \overline{CS} \downarrow before responding to the I/O CLOCK. No attempt should be made to clock out the data until the minimum \overline{CS} setup time has elapsed.
 - A low-to-high transition of \overline{CS} disables I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.
 - The first I/O CLOCK must occur after the end of the previous conversion.



TLC1549C, TLC1549I, TLC1549M
 10-BIT ANALOG-TO-DIGITAL CONVERTERS
 WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

APPLICATION INFORMATION



- NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0024 V and the transition to full scale (V_{FT}) is 4.908 V. 1 LSB = 4.8 mV.
- B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 12. Ideal Conversion Characteristics

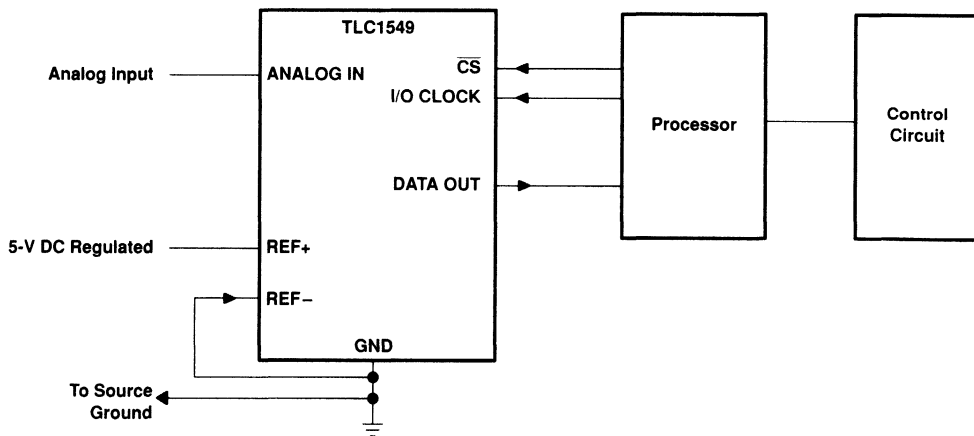


Figure 13. Typical Serial Interface

TLC1549C, TLC1549I, TLC1549M
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 14, the time required to charge the analog input capacitance from 0 V to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c / R_t C_i} \right) \quad (1)$$

where

$$R_t = R_s + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S / 2048) \quad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S / 2048) = V_S \left(1 - e^{-t_c / R_t C_i} \right) \quad (3)$$

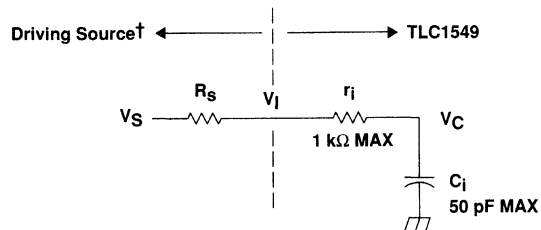
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(2048) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_s + 1 \text{ k}\Omega) \times 60 \text{ pF} \times \ln(2048) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at ANALOG IN
 V_S = External Driving Source Voltage
 R_s = Source Resistance
 r_i = Input Resistance
 C_i = Input Capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

Figure 14. Equivalent Input Circuit Including the Driving Source

TLC1550I, TLC1550M, TLC1551I 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH PARALLEL OUTPUTS

SLAS043C – MAY 1991 – REVISED MARCH 1995

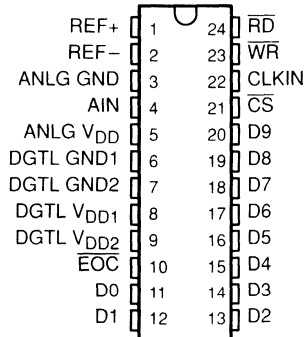
- Power Dissipation . . . 40 mW Max
- Advanced LinEPIC™ Single-Poly Process Provides Close Capacitor Matching for Better Accuracy
- Fast Parallel Processing for DSP and μ P Interface
- Either External or Internal Clock Can Be Used
- Conversion Time . . . 6 μ s
- Total Unadjusted Error . . . ± 1 LSB Max
- CMOS Technology

description

The TLC1550x and TLC1551 are data acquisition analog-to-digital converters (ADCs) using a 10-bit, switched-capacitor, successive-approximation network. A high-speed, 3-state parallel port directly interfaces to a digital signal processor (DSP) or microprocessor (μ P) system data bus. D0 through D9 are the digital output terminals with D0 being the least significant bit (LSB). Separate power terminals for the analog and digital portions minimize noise pickup in the supply leads. Additionally, the digital power is divided into two parts to separate the lower current logic from the higher current bus drivers. An external clock can be applied to CLKIN to override the internal system clock if desired.

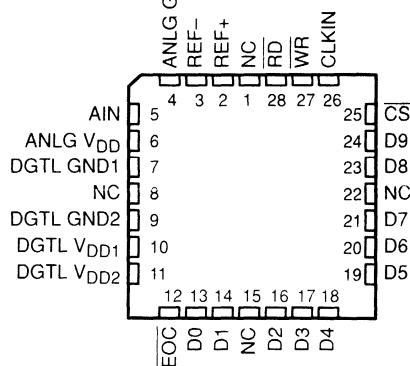
The TLC1550I and TLC1551I are characterized for operation from -40°C to 85°C . The TLC1550M is characterized over the full military range of -55°C to 125°C .

J† OR NW PACKAGE
(TOP VIEW)



† Refer to the mechanical data for the JW package.

FK OR FN PACKAGE
(TOP VIEW)



NC – No internal connection

AVAILABLE OPTIONS

T _A	PACKAGE			
	CERAMIC CHIP CARRIER (FK)	PLASTIC CHIP CARRIER (FN)	CERAMIC DIP (J)	PLASTIC DIP (NW)
-40°C to 85°C	-	TLC1550FN TLC1551FN	-	TLC1550NW
-55°C to 125°C	TLC1550MFK	-	TLC1550MJ	-



This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

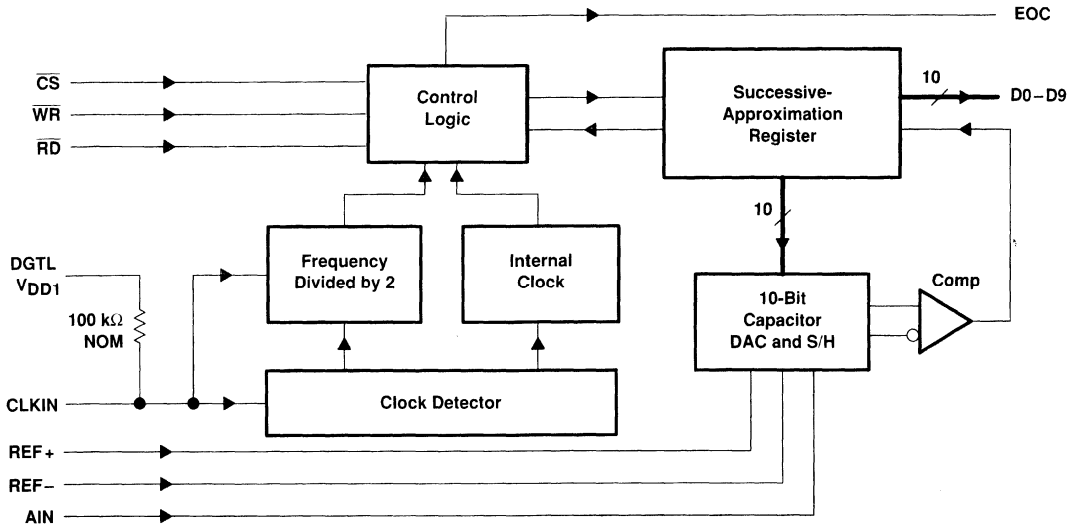
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

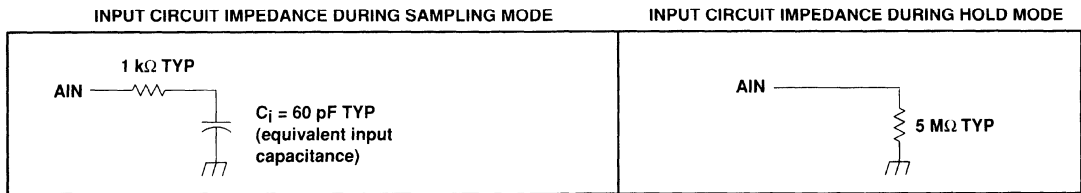
TLC1550I, TLC1550M, TLC1551I
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH PARALLEL OUTPUTS

SLAS043C – MAY 1991 – REVISED MARCH 1995

functional block diagram



typical equivalent inputs



TLC1550I, TLC1550M, TLC1551I
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH PARALLEL OUTPUTS

SLAS043C – MAY 1991 – REVISED MARCH 1995

Terminal Functions

TERMINAL			DESCRIPTION
NAME	NO.†	NO.‡	
ANLG GND	4	3	Analog ground. The reference point for the voltage applied on terminals ANLG V _{DD} , AIN, REF+, and REF-.
AIN	5	4	Analog voltage input. The voltage applied to AIN is converted to the equivalent digital output.
ANLG V _{DD}	6	5	Analog positive power supply voltage. The voltage applied to this terminal is designated V _{DD3} .
CLKIN	26	22	Clock input. CLKIN is used for external clocking instead of using the internal system clock. It usually takes a few microseconds before the internal clock is disabled. To use the internal clock, CLKIN should be tied high or left unconnected.
\overline{CS}	25	21	Chip-select. \overline{CS} must be low for \overline{RD} or \overline{WR} to be recognized by the A/D converter.
D0	13	11	Data bus output. D0 is bit 1 (LSB).
D1	14	12	Data bus output. D1 is bit 2.
D2	16	13	Data bus output. D2 is bit 3.
D3	17	14	Data bus output. D3 is bit 4.
D4	18	15	Data bus output. D4 is bit 5.
D5	19	16	Data bus output. D5 is bit 6.
D6	20	17	Data bus output. D6 is bit 7.
D7	21	18	Data bus output. D7 is bit 8.
D8	23	19	Data bus output. D8 is bit 9.
D9	24	20	Data bus output. D9 is bit 10 (MSB).
DGTL GND1	7	6	Digital ground 1. The ground for power supply DGTL V _{DD1} and is the substrate connection.
DGTL GND2	9	7	Digital ground 2. The ground for power supply DGTL V _{DD2} .
DGTL V _{DD1}	10	8	Digital positive power-supply voltage 1. DGTL V _{DD1} supplies the logic. The voltage applied to DGTL V _{DD1} is designated V _{DD1} .
DGTL V _{DD2}	11	9	Digital positive power-supply voltage 2. DGTL V _{DD2} supplies only the higher-current output buffers. The voltage applied to DGTL V _{DD2} is designated V _{DD2} .
\overline{EOC}	12	10	End-of-conversion. \overline{EOC} goes low indicating that conversion is complete and the results have been transferred to the output latch. \overline{EOC} can be connected to the μ P- or DSP-interrupt terminal or can be continuously polled.
\overline{RD}	28	24	Read input. When \overline{CS} is low and \overline{RD} is taken low, the data is placed on the data bus from the output latch. The output latch stores the conversion results at the most recent negative edge of \overline{EOC} . The falling edge of \overline{RD} resets \overline{EOC} to a high within the $t_{d}(\overline{EOC})$ specifications.
REF+	2	1	Positive voltage-reference input. Any analog input that is greater than or equal to the voltage on REF+ converts to 11111111. Analog input voltages between REF+ and REF- convert to the appropriate result in a ratiometric manner.
REF-	3	2	Negative voltage reference input. Any analog input that is less than or equal to the voltage on REF- converts to 0000000000.
\overline{WR}	27	23	Write input. When \overline{CS} is low, conversion is started on the rising edge of \overline{WR} . On this rising edge, the ADC holds the analog input until conversion is completed. Before and after the conversion period, which is given by t_{conv} , the ADC remains in the sampling mode.

† Terminal numbers for FK and FN packages.

‡ Terminal numbers for J and NW packages.



TLC1550I, TLC1550M, TLC1551I

10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH PARALLEL OUTPUTS

SLAS043C – MAY 1991 – REVISED MARCH 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD1} , V_{DD2} , and V_{DD3} (see Note 1)	6.5 V
Input voltage range, V_I (any input)	-0.3 V to $V_{DD} + 0.3$ V
Output voltage range, V_O	-0.3 V to $V_{DD} + 0.3$ V
Peak input current (any digital input)	± 10 mA
Peak total input current (all inputs)	± 30 mA
Operating free-air temperature range, T_A : TLC1550I, TLC1551I	-40°C to 85°C
TLC1550M	-55°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Case temperature for 10 seconds: FK or FN package	260°C
Lead temperature 1.6 mm (1/16 inch) from the case for 10 seconds: J or NW package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: V_{DD1} is the voltage measured at DGTL V_{DD1} with respect to DGND1. V_{DD2} is the voltage measured at DGTL V_{DD2} with respect to the DGND2. V_{DD3} is the voltage measured at ANLG V_{DD} with respect to AGND. For these specifications, all ground terminals are tied together (and represent 0 V). When V_{DD1} , V_{DD2} , and V_{DD3} are equal, they are referred to simply as V_{DD} .

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD1} , V_{DD2} , V_{DD3}	4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)	V_{DD3}			V
Negative reference voltage, V_{ref-} (see Note 2)	0			V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)	0.3			V
Analog input voltage range	0	V_{DD3}		V
High-level control input voltage, V_{IH}	2			V
Low-level control input voltage, V_{IL}				0.8 V
Input clock frequency, $f_{(CLKIN)}$	0.5	7.8		MHz
Setup time, \overline{CS} low before \overline{WR} or \overline{RD} goes low, $t_{su}(CS)$	0			ns
Hold time, \overline{CS} low after \overline{WR} or \overline{RD} goes high, $t_h(CS)$	0			ns
\overline{WR} or \overline{RD} pulse duration, $t_w(WR)$	50			ns
Input clock low pulse duration, $t_{wL}(CLKIN)$	40% of period		80% of period	
Operating free-air temperature, T_A	TLC155xI		85	°C
	TLC1550M		125	

NOTE 2: Analog input voltages greater than that applied to REF+ convert to all 1s (1111111111), while input voltages less than that applied to REF- convert to all 0s (0000000000). The total unadjusted error may increase as this differential voltage falls below 4.75 V.



TLC1550I, TLC1550M, TLC1551I
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH PARALLEL OUTPUTS

SLAS043C – MAY 1991 – REVISED MARCH 1995

electrical characteristics over recommended operating free-air temperature range,
 $V_{DD} = V_{ref+} = 4.75$ to 5.5 V and $V_{ref-} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
V_{OH}	High-level output voltage	$V_{DD} = 4.75$ V, $I_{OH} = -360$ μ A	2.4			V	
V_{OL}	Low-level output voltage	$V_{DD} = 4.75$ V, $I_{OL} = 2.4$ mA	$T_A = 25^\circ\text{C}$		0.4	V	
			$T_A = -55^\circ\text{C}$ to 125°C		0.5		
I_{OZ}	Off-state (high-impedance-state) output current	$V_O = V_{DD}$, \overline{CS} and \overline{RD} at V_{DD}			10	μ A	
		$V_O = 0$, \overline{CS} and \overline{RD} at V_{DD}			-10		
I_{IH}	High-level input current	$V_I = V_{DD}$	0.005		2.5	μ A	
I_{IL}	Low-level input current (except CLKIN)	$V_I = 0$	-2.5	-0.005		μ A	
I_{IL}	Low-level input current (CLKIN)		-150	-50		μ A	
I_{OS}	Short-circuit output current	$V_O = 5$ V, $T_A = 25^\circ\text{C}$	7	14		mA	
		$V_O = 0$, $T_A = 25^\circ\text{C}$		-12	-6		
I_{DD}	Operating supply current	\overline{CS} low and \overline{RD} high	2		8	mA	
C_i	Input capacitance	Analog inputs			60	90*	pF
		Digital inputs	See typical equivalent inputs TLC1550/11		5	15*	

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† All typical values are at $V_{DD} = 5$ V, $T_A = 25^\circ\text{C}$.



TLC1550I, TLC1550M, TLC1551I

10-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH PARALLEL OUTPUTS

SLAS043C – MAY 1991 – REVISED MARCH 1995

operating characteristics over recommended operating free-air temperature range with internal clock and minimum sampling time of 4 μ s, $V_{DD} = V_{ref+} = 5$ V and $V_{ref-} = 0$ (unless otherwise noted)

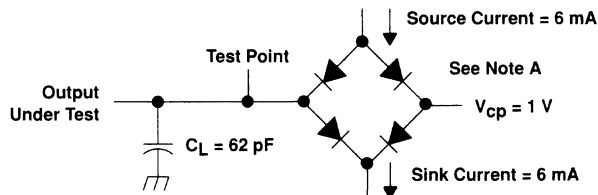
PARAMETER		TEST CONDITIONS	T_A †	MIN	TYP‡	MAX	UNIT
E _L	Linearity error	See Note 3	Full range			±0.5	LSB
						±1	
						±0.5	
						±1	
E _{ZS}	Zero-scale error	See Notes 2 and 4	Full range			±0.5	LSB
						±1	
						±0.5	
						±1	
E _{FS}	Full-scale error	See Notes 2 and 4	Full range			±0.5	LSB
						±1	
						±0.5	
						±1	
Total unadjusted error		See Note 5	Full range			±0.5	LSB
						±1	
						±1	
t _{conv}	Conversion time	f _{clock(external)} = 4.2 MHz or internal clock				6	μ s
t _{a(D)}	Data access time after \overline{RD} goes low	See Figure 3				35	ns
t _{v(D)}	Data valid time after \overline{RD} goes high					5	
t _{dis(D)}	Disable time, delay time from \overline{RD} high to high impedance					30	
t _{d(EOC)}	Delay time, \overline{RD} low to \overline{EOC} high					0	

† Full range is -40°C to 85°C for the TL155xI devices and -55°C to 125°C for the TLC1550M.

‡ All typical values are at $V_{DD} = 5$ V, $T_A = 25^{\circ}\text{C}$.

- NOTES:
- Analog input voltages greater than that applied to REF+ convert to all 1s (1111111111), while input voltages less than that applied to REF- convert to all 0s (0000000000). The total unadjusted error may increase as this differential voltage falls below 4.75 V.
 - Linearity error is the difference between the actual analog value at the transition between any two adjacent steps and its ideal value after zero-scale error and full-scale error have been removed.
 - Zero-scale error is the difference between the actual mid-step value and the nominal mid-step value at specified zero scale. Full-scale error is the difference between the actual mid-step value and the nominal mid-step value at specified full scale.
 - Total unadjusted error is the difference between the actual analog value at the transition between any two adjacent steps and its ideal value. It includes contributions from zero-scale error, full-scale error, and linearity error.

PARAMETER MEASUREMENT INFORMATION



V_{cp} = voltage commutation point for switching between source and sink currents

NOTE A: Equivalent load circuit of the Teradyne A500 tester for timing parameter measurement

Figure 1. Test Load Circuit



APPLICATION INFORMATION

simplified analog input analysis

Using the circuit in Figure 2, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c / R_t C_i} \right) \quad (1)$$

where

$$R_t = R_s + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S / 1024) \quad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S / 512) = V_S \left(1 - e^{-t_c / R_t C_i} \right) \quad (3)$$

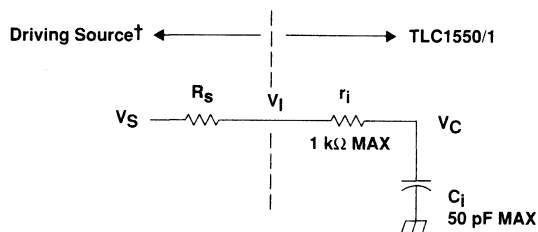
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(1024) \quad (4)$$

Therefore, with the values given, the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_s + 1 \text{ k}\Omega) \times 60 \text{ pF} \times \ln(1024) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input voltage at AIN
 V_S = External driving source voltage
 R_s = Source resistance
 r_i = Input resistance
 C_i = Input capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

Figure 2. Input Circuit Including the Driving Source

TLC1550I, TLC1550M, TLC1551I 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH PARALLEL OUTPUTS

SLAS043C – MAY 1991 – REVISED MARCH 1995

PRINCIPLES OF OPERATION

The operating sequence for complete data acquisition is shown in Figure 3. Processors can address the TLC1550 and TLC1551 as an external memory device by simply connecting the address lines to a decoder and the decoder output to \overline{CS} . Like other peripheral devices, the write (\overline{WR}) and read (\overline{RD}) input signals are valid only when \overline{CS} is low. Once \overline{CS} is low, the on-board system clock permits the conversion to begin with a simple write command and the converted data to be presented to the data bus with a simple read command. The device remains in a sampling (track) mode from the rising edge of \overline{EOC} until conversion begins with the rising edge of \overline{WR} , which initiates the hold mode. After the hold mode begins, the clock controls the conversion automatically. When the conversion is complete, the end-of-conversion (\overline{EOC}) signal goes low indicating that the digital data has been transferred to the output latch. Lowering \overline{CS} and \overline{RD} then resets \overline{EOC} and transfers the data to the data bus for the processor read cycle.

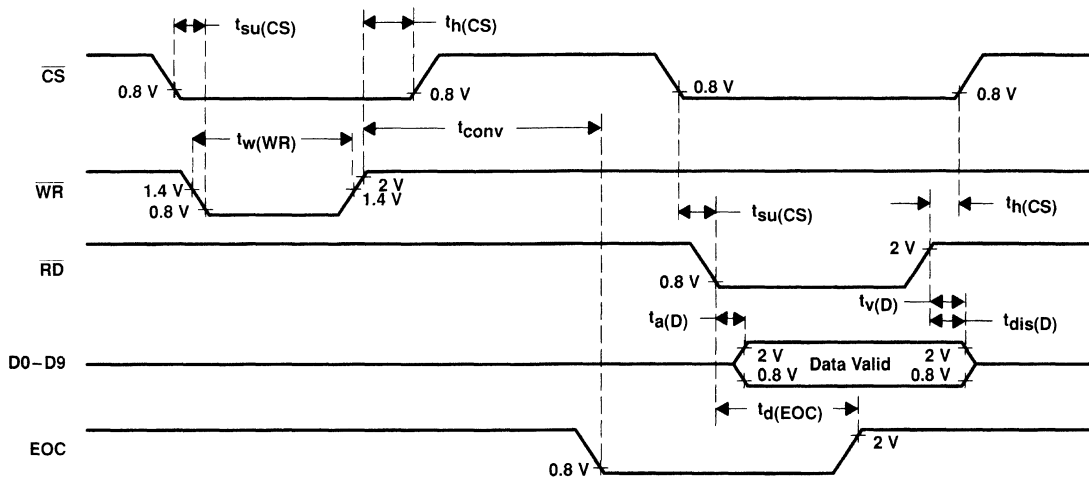


Figure 3. TLC1550 or TLC1551 Operating Sequence

TLC2543C, TLC2543I, TLC2543M 12-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS079D – DECEMBER 1993 – REVISED MAY 1997

- 12-Bit-Resolution A/D Converter
- 10- μ s Conversion Time Over Operating Temperature
- 11 Analog Input Channels
- 3 Built-In Self-Test Modes
- Inherent Sample-and-Hold Function
- Linearity Error . . . ± 1 LSB Max
- On-Chip System Clock
- End-of-Conversion Output
- Unipolar or Bipolar Output Operation (Signed Binary With Respect to 1/2 the Applied Voltage Reference)
- Programmable MSB or LSB First
- Programmable Power Down
- Programmable Output Data Length
- CMOS Technology
- Application Report Available†

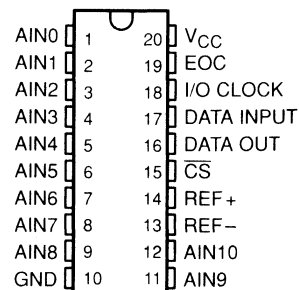
description

The TLC2543C and TLC2543I are 12-bit, switched-capacitor, successive-approximation, analog-to-digital converters. Each device has three control inputs [chip select (\overline{CS}), the input-output clock (I/O CLOCK), and the address input (DATA INPUT)] and is designed for communication with the serial port of a host processor or peripheral through a serial 3-state output. The device allows high-speed data transfers from the host.

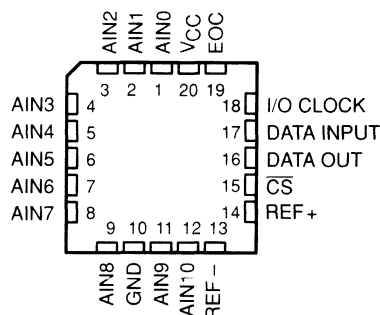
In addition to the high-speed converter and versatile control capability, the device has an on-chip 14-channel multiplexer that can select any one of 11 inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the device features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating temperature range.

The TLC2543C is characterized for operation from $T_A = 0^\circ\text{C}$ to 70°C . The TLC2543I is characterized for operation from $T_A = -40^\circ\text{C}$ to 85°C . The TLC2543M is characterized for operation from $T_A = -55^\circ\text{C}$ to 125°C .

DB, DW, J, OR N PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



† Microcontroller Based Data Acquisition Using the TLC2543 12-bit Serial-Out ADC (SLAA012)

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



TLC2543C, TLC2543I, TLC2543M

12-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH SERIAL CONTROL AND 11 ANALOG INPUTS

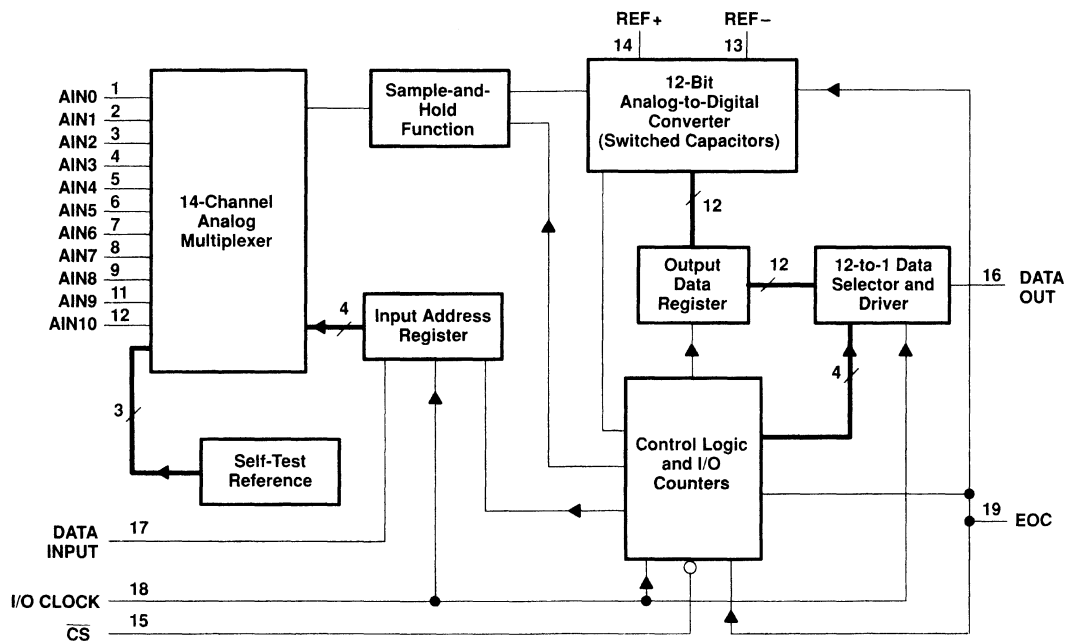
SLAS079D – DECEMBER 1993 – REVISED MAY 1997

AVAILABLE OPTIONS

T _A	PACKAGE					
	SMALL OUTLINE		PLASTIC CHIP CARRIER	PLASTIC CHIP CARRIER	PLASTIC DIP	PLASTIC DIP
	(DB)†	(DW)†	(FK)	(FN)†	(J)	(N)
0°C to 70°C	TLC2543CDB	TLC2543CDW	—	TLC2543CFN	—	TLC2543CN
-40°C to 85°C	—	TLC2543IDW	—	TLC2543IFN	—	TLC2543IN
-55°C to 125°C	—	—	TLC2543MFK	—	TLC2543MJ	—

† Available in tape and reel and ordered as the TLC2543CDBLE, TLC2543CDWR, TLC2543IDWR, TLC2543CFNR, or TLC2543IFNR.

functional block diagram



TLC2543C, TLC2543I, TLC2543M
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS079D – DECEMBER 1993 – REVISED MAY 1997

Terminal Functions

TERMINAL NAME NO.		I/O	DESCRIPTION
AIN0 – AIN10	1–9, 11, 12	I	Analog input. These 11 analog-signal inputs are internally multiplexed. The driving source impedance should be less than or equal to 50 Ω for 4.1-MHz I/O CLOCK operation and be capable of slewing the analog input voltage into a capacitance of 60 pF.
\overline{CS}	15	I	Chip select. A high-to-low transition on \overline{CS} resets the internal counters and controls and enables DATA OUT, DATA INPUT, and I/O CLOCK. A low-to-high transition disables DATA INPUT and I/O CLOCK within a setup time.
DATA INPUT	17	I	Serial-data input. A 4-bit serial address selects the desired analog input or test voltage to be converted next. The serial data is presented with the MSB first and is shifted in on the first four rising edges of I/O CLOCK. After the four address bits are read into the address register, I/O CLOCK clocks the remaining bits in order.
DATA OUT	16	O	The 3-state serial output for the A/D conversion result. DATA OUT is in the high-impedance state when \overline{CS} is high and active when \overline{CS} is low. With a valid \overline{CS} , DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB/LSB [†] value of the previous conversion result. The next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next MSB/LSB, and the remaining bits are shifted out in order.
EOC	19	O	End of conversion. EOC goes from a high to a low logic level after the falling edge of the last I/O CLOCK and remains low until the conversion is complete and the data is ready for transfer.
GND	10		Ground. GND is the ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	18	I	Input/output clock. I/O CLOCK receives the serial input and performs the following four functions: 1. It clocks the eight input data bits into the input data register on the first eight rising edges of I/O CLOCK with the multiplexer address available after the fourth rising edge. 2. On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplexer input begins charging the capacitor array and continues to do so until the last falling edge of the I/O CLOCK. 3. It shifts the 11 remaining bits of the previous conversion data out on DATA OUT. Data changes on the falling edge of I/O CLOCK. 4. It transfers control of the conversion to the internal state controller on the falling edge of the last I/O CLOCK.
REF+	14	I	Positive reference voltage. The upper reference voltage value (nominally V_{CC}) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF– terminal.
REF–	13	I	Negative reference voltage. The lower reference voltage value (nominally ground) is applied to REF–.
VCC	20		Positive supply voltage

[†] MSB/LSB = Most significant bit /least significant bit



TLC2543C, TLC2543I, TLC2543M

12-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS079D – DECEMBER 1993 – REVISED MAY 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 6.5 V
Input voltage range, V_I (any input)	–0.3 V to $V_{CC} + 0.3$ V
Output voltage range, V_O	–0.3 V to $V_{CC} + 0.3$ V
Positive reference voltage, V_{ref+}	$V_{CC} + 0.1$ V
Negative reference voltage, V_{ref-}	–0.1 V
Peak input current, I_I (any input)	±20 mA
Peak total input current, I_I (all inputs)	±30 mA
Operating free-air temperature range, T_A :	
TLC2543C	0°C to 70°C
TLC2543I	–40°C to 85°C
TLC2543M	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminal with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)	V_{CC}			V
Negative reference voltage, V_{ref-} (see Note 2)	0			V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)	2.5	V_{CC}	$V_{CC} + 0.1$	V
Analog input voltage (see Note 2)	0			V_{CC}
High-level control input voltage, V_{IH}	$V_{CC} = 4.5$ V to 5.5 V			2
Low-level control input voltage, V_{IL}	$V_{CC} = 4.5$ V to 5.5 V			0.8
Clock frequency at I/O CLOCK	0			4.1
Setup time, address bits at DATA INPUT before I/O CLOCK↑, $t_{su(A)}$ (see Figure 4)	100			ns
Hold time, address bits after I/O CLOCK↑, $t_h(A)$ (see Figure 4)	0			ns
Hold time, \overline{CS} low after last I/O CLOCK↓, $t_h(\overline{CS})$ (see Figure 5)	0			ns
Setup time, \overline{CS} low before clocking in first address bit, $t_{su}(\overline{CS})$ (see Note 3 and Figure 5)	1.425			µs
Pulse duration, I/O CLOCK high, $t_{wH}(I/O)$	120			ns
Pulse duration, I/O CLOCK low, $t_{wL}(I/O)$	120			ns
Transition time, I/O CLOCK high to low, $t_t(I/O)$ (see Note 4 and Figure 6)	1			µs
Transition time, DATA INPUT and \overline{CS} , $t_t(\overline{CS})$	10			µs
Operating free-air temperature, T_A	TLC2543C	0		70
	TLC2543I	–40		85
	TLC2543M	–55		125

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (111111111111), while input voltages less than that applied to REF– convert as all zeros (000000000000).

3. To minimize errors caused by noise at the \overline{CS} input, the internal circuitry waits for a setup time after \overline{CS} ↓ before responding to control input signals. No attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IHmin} to V_{ILmax} or to rise from V_{ILmax} to V_{IHmin} . In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.



TLC2543C, TLC2543I, TLC2543M
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS079D – DECEMBER 1993 – REVISED MAY 1997

electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 4.5\text{ V to }5.5\text{ V}$, $f_{(I/O\ CLOCK)} = 4.1\text{ MHz}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLC2543C, TLC2543I			UNIT
			MIN	TYP†	MAX	
V _{OH}	High-level output voltage	V _{CC} = 4.5 V, I _{OH} = -1.6 mA	2.4			V
		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -20 μA	V _{CC} - 0.1			
V _{OL}	Low-level output voltage	V _{CC} = 4.5 V, I _{OL} = 1.6 mA	0.4			V
		V _{CC} = 4.5 V to 5.5 V, I _{OL} = 20 μA	0.1			
I _{OZ}	High-impedance off-state output current	V _O = V _{CC} , \overline{CS} at V _{CC}	1 2.5			μA
		V _O = 0, \overline{CS} at V _{CC}	1 -2.5			
I _{IH}	High-level input current	V _I = V _{CC}	1 2.5			μA
I _{IL}	Low-level input current	V _I = 0	1 -2.5			μA
I _{CC}	Operating supply current	\overline{CS} at 0 V	1 2.5			mA
I _{CC(PD)}	Power-down current	For all digital inputs, 0 ≤ V _I ≤ 0.5 V or V _I ≥ V _{CC} - 0.5 V	4 25			μA
	Selected channel leakage current	Selected channel at V _{CC} , Unselected channel at 0 V	1			μA
		Selected channel at 0 V, Unselected channel at V _{CC}	-1			
	Maximum static analog reference current into REF+	V _{ref+} = V _{CC} , V _{ref-} = GND	1 2.5			μA
C _i	Input capacitance	Analog inputs	30 60			pF
		Control inputs	5 15			

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 4.5\text{ V to }5.5\text{ V}$, $f_{(I/O\ CLOCK)} = 4.1\text{ MHz}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLC2543M			UNIT
			MIN	TYP†	MAX	
V _{OH}	High-level output voltage	V _{CC} = 4.5 V, I _{OH} = -1.6 mA	2.4			V
		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -20 μA	V _{CC} - 0.1			
V _{OL}	Low-level output voltage	V _{CC} = 4.5 V, I _{OL} = 1.6 mA	0.4			V
		V _{CC} = 4.5 V to 5.5 V, I _{OL} = 20 μA	0.1			
I _{OZ}	High-impedance off-state output current	V _O = V _{CC} , \overline{CS} at V _{CC}	1 2.5			μA
		V _O = 0, \overline{CS} at V _{CC}	1 -2.5			
I _{IH}	High-level input current	V _I = V _{CC}	1 10			μA
I _{IL}	Low-level input current	V _I = 0	1 -10			μA
I _{CC}	Operating supply current	\overline{CS} at 0 V	1 10			mA
I _{CC(PD)}	Power-down current	For all digital inputs, 0 ≤ V _I ≤ 0.5 V or V _I ≥ V _{CC} - 0.5 V	4 25			μA
	Selected channel leakage current	Selected channel at V _{CC} , Unselected channel at 0 V	10			μA
		Selected channel at 0 V, Unselected channel at V _{CC}	-10			
	Maximum static analog reference current into REF+	V _{ref+} = V _{CC} , V _{ref-} = GND	1 2.5			μA
C _i	Input capacitance	Analog inputs	30 60			pF
		Control inputs	5 15			

† All typical values are at V_{CC} = 5 V, T_A = 25°C.



TLC2543C, TLC2543I, TLC2543M
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS079D – DECEMBER 1993 – REVISED MAY 1997

operating characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 4.5\text{ V to }5.5\text{ V}$, $f_{(I/O\ CLOCK)} = 4.1\text{ MHz}$

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error (see Note 5)			±1	LSB
E_D	Differential linearity error			±1	LSB
E_O	Offset error (see Note 6)			±1.5	LSB
E_G	Gain error (see Note 6)			±1	LSB
E_T	Total unadjusted error (see Note 7)			±1.75	LSB
Self-test output code (see Table 3 and Note 8)	DATA INPUT = 1011		2048		
	DATA INPUT = 1100		0		
	DATA INPUT = 1101		4095		
t_{conv}	Conversion time		8	10	μs
t_c	Total cycle time (access, sample, and conversion)			10 + total I/O CLOCK periods + $t_d(I/O\ EOC)$	μs
t_{acq}	Channel acquisition time (sample)		4	12	I/O CLOCK periods
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓		10		ns
$t_d(I/O\ DATA)$	Delay time, I/O CLOCK↓ to DATA OUT valid			150	ns
$t_d(I/O\ EOC)$	Delay time, last I/O CLOCK↓ to EOC↓		1.5	2.2	μs
$t_d(EOC\ DATA)$	Delay time, EOC↑ to DATA OUT (MSB/LSB)			100	ns
t_{PZH}, t_{PZL}	Enable time, \overline{CS} ↓ to DATA OUT (MSB/LSB driven)		0.7	1.3	μs
t_{PHZ}, t_{PLZ}	Disable time, \overline{CS} ↑ to DATA OUT (high impedance)		70	150	ns
$t_r(EOC)$	Rise time, EOC		15	50	ns
$t_f(EOC)$	Fall time, EOC		15	50	ns
$t_r(bus)$	Rise time, data bus		15	50	ns
$t_f(bus)$	Fall time, data bus		15	50	ns
$t_d(I/O\ CS)$	Delay time, last I/O CLOCK↓ to \overline{CS} ↓ to abort conversion (see Note 10)			5	μs

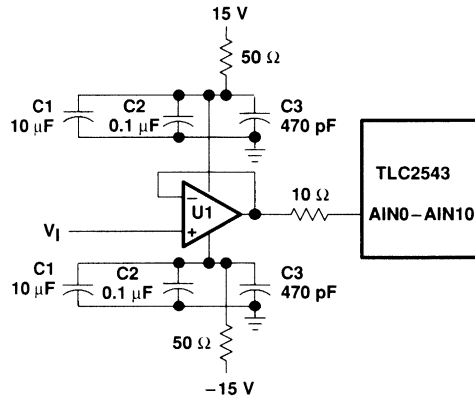
† All typical values are at $T_A = 25^\circ\text{C}$.

- NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (111111111111), while input voltages less than that applied to REF- convert as all zeros (000000000000).
5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Gain error is the difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. Offset error is the difference between the actual midstep value and the nominal midstep value at the offset point.
7. Total unadjusted error comprises linearity, zero-scale, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic.
9. I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 7).
10. Any transitions of \overline{CS} are recognized as valid only when the level is maintained for a setup time. \overline{CS} must be taken low at $\leq 5\ \mu\text{s}$ of the tenth I/O CLOCK falling edge to ensure a conversion is aborted. Between 5 μs and 10 μs, the result is uncertain as to whether the conversion is aborted or the conversion results are valid.



TLC2543C, TLC2543I, TLC2543M
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS
SLAS079D – DECEMBER 1993 – REVISED MAY 1997

PARAMETER MEASUREMENT INFORMATION



LOCATION	DESCRIPTION	PART NUMBER
U1	OP27	—
C1	10- μ F 35-V tantalum capacitor	—
C2	0.1- μ F ceramic NPO SMD capacitor	AVX 12105C104KA105 or equivalent
C3	470-pF porcelain Hi-Q SMD capacitor	Johanson 201S420471JG4L or equivalent

Figure 1. Analog Input Buffer to Analog Inputs AIN0–AIN10

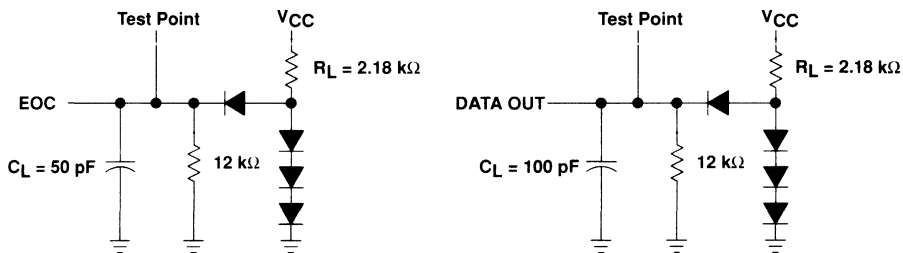


Figure 2. Load Circuits

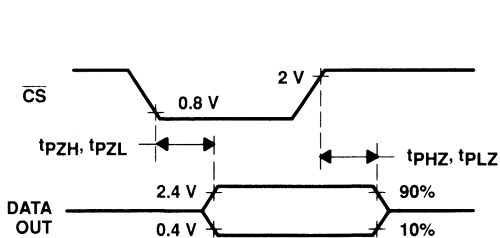


Figure 3. DATA OUT to Hi-Z Voltage Waveforms

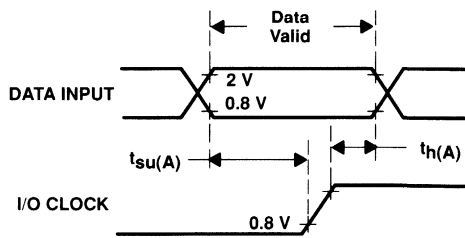
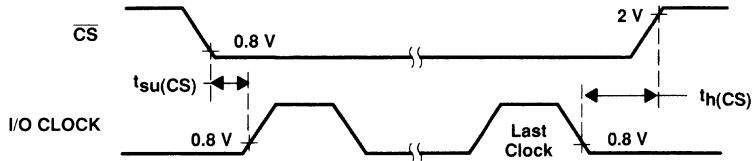


Figure 4. DATA INPUT and I/O CLOCK Voltage Waveforms

TLC2543C, TLC2543I, TLC2543M
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS079D – DECEMBER 1993 – REVISED MAY 1997

PARAMETER MEASUREMENT INFORMATION



NOTE A: To ensure full conversion accuracy, it is recommended that no input signal change occurs while a conversion is ongoing.

Figure 5. CS and I/O CLOCK Voltage Waveforms

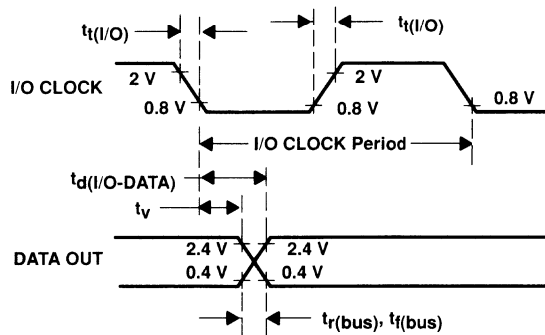


Figure 6. I/O CLOCK and DATA OUT Voltage Waveforms

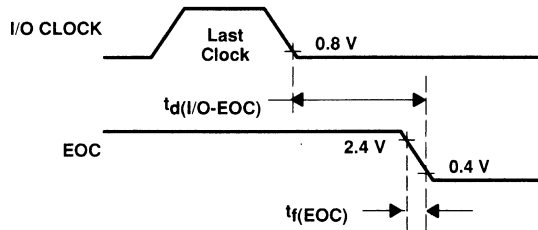


Figure 7. I/O CLOCK and EOC Voltage Waveforms

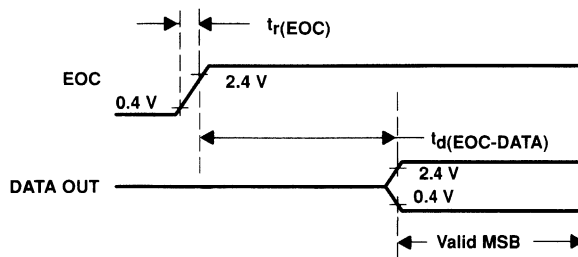
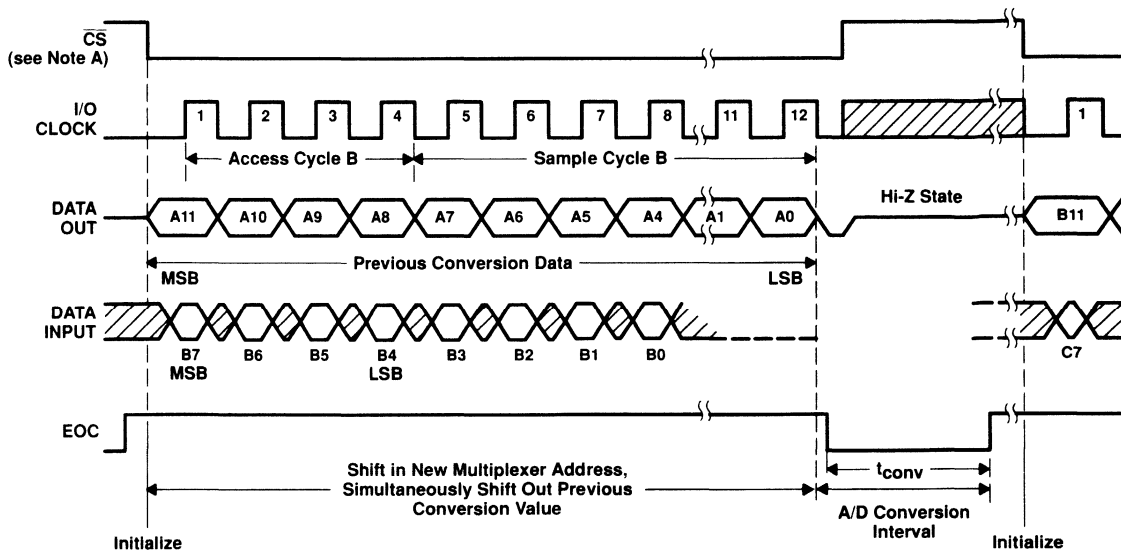


Figure 8. EOC and DATA OUT Voltage Waveforms

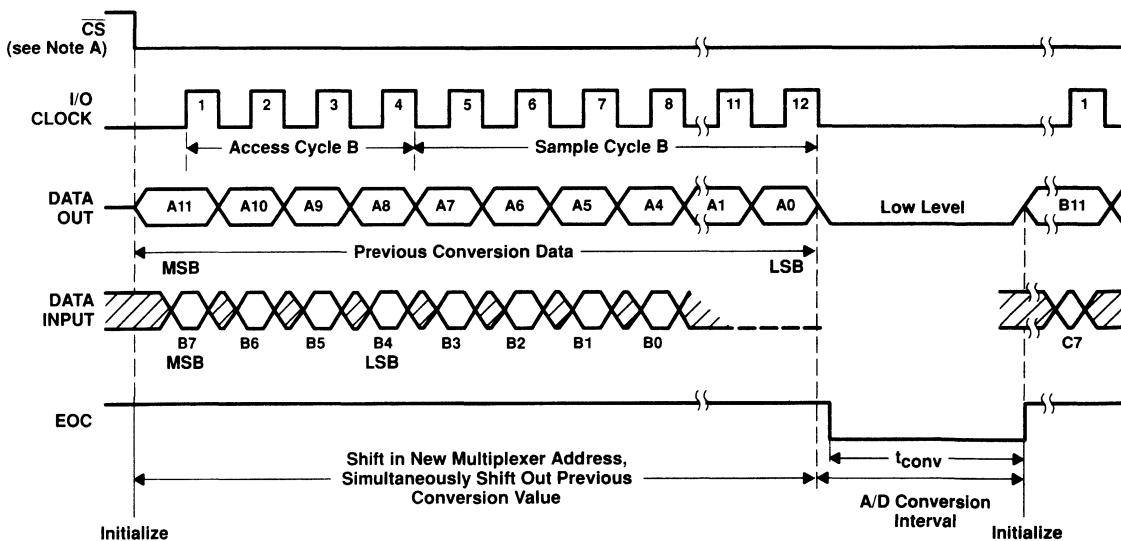
TLC2543C, TLC2543I, TLC2543M
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS
SLAS079D – DECEMBER 1993 – REVISED MAY 1997

PARAMETER MEASUREMENT INFORMATION



NOTE A: To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.

Figure 9. Timing for 12-Clock Transfer Using \overline{CS} With MSB First

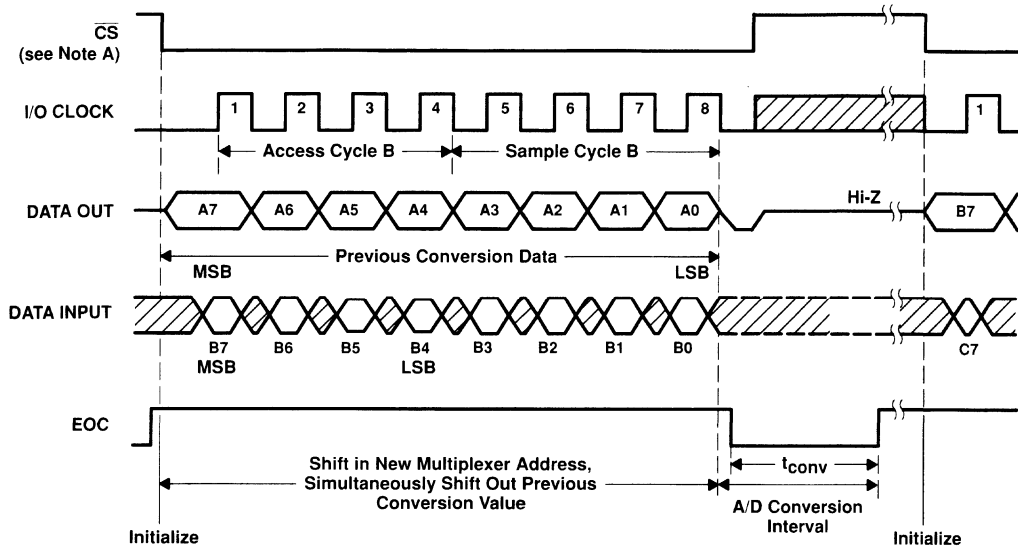


NOTE A: To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.

Figure 10. Timing for 12-Clock Transfer Not Using \overline{CS} With MSB First

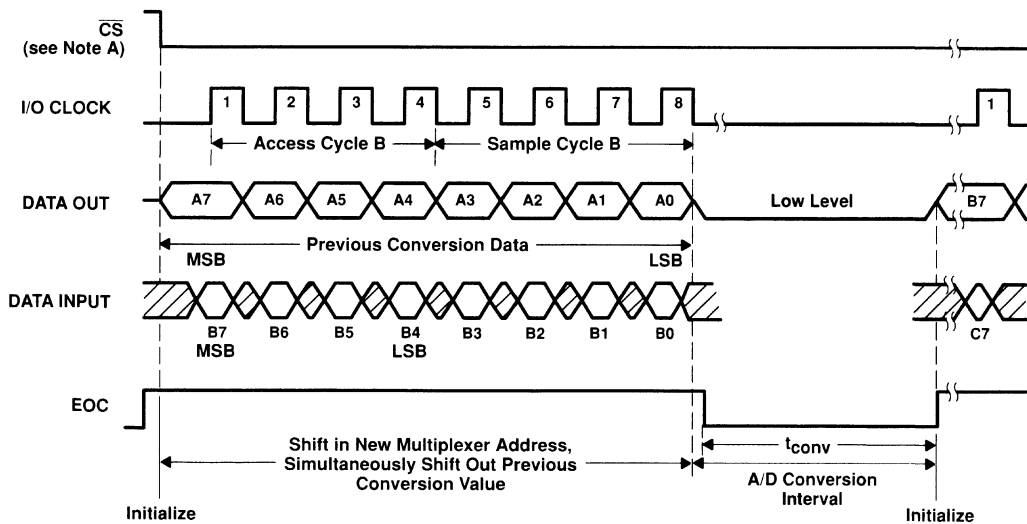
TLC2543C, TLC2543I, TLC2543M
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS
 SLAS079D – DECEMBER 1993 – REVISED MAY 1997

PARAMETER MEASUREMENT INFORMATION



NOTE A: To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.

Figure 11. Timing for 8-Clock Transfer Using \overline{CS} With MSB First

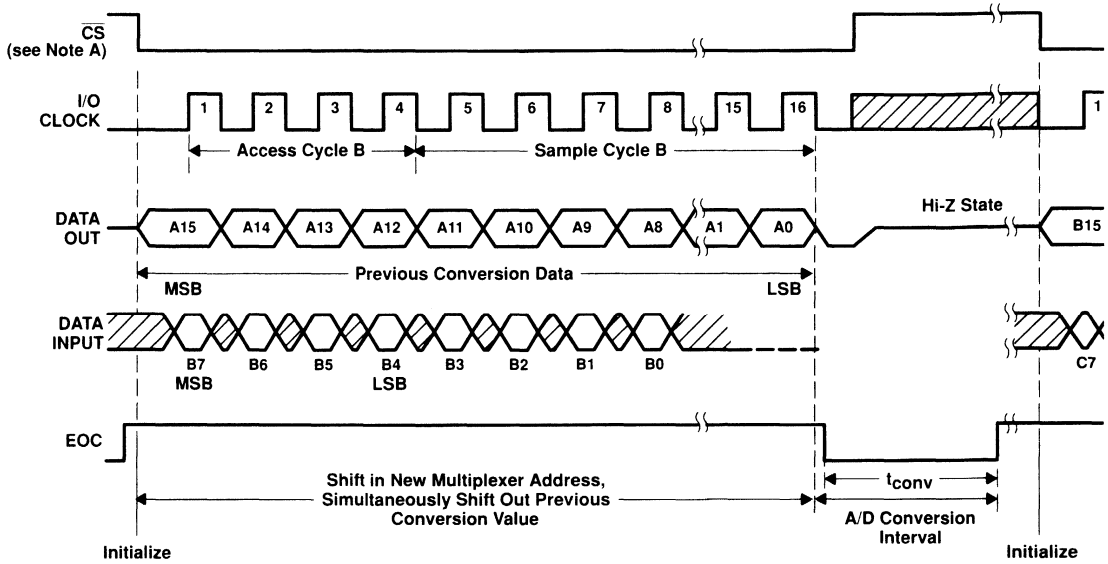


NOTE A: To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.

Figure 12. Timing for 8-Clock Transfer Not Using \overline{CS} With MSB First

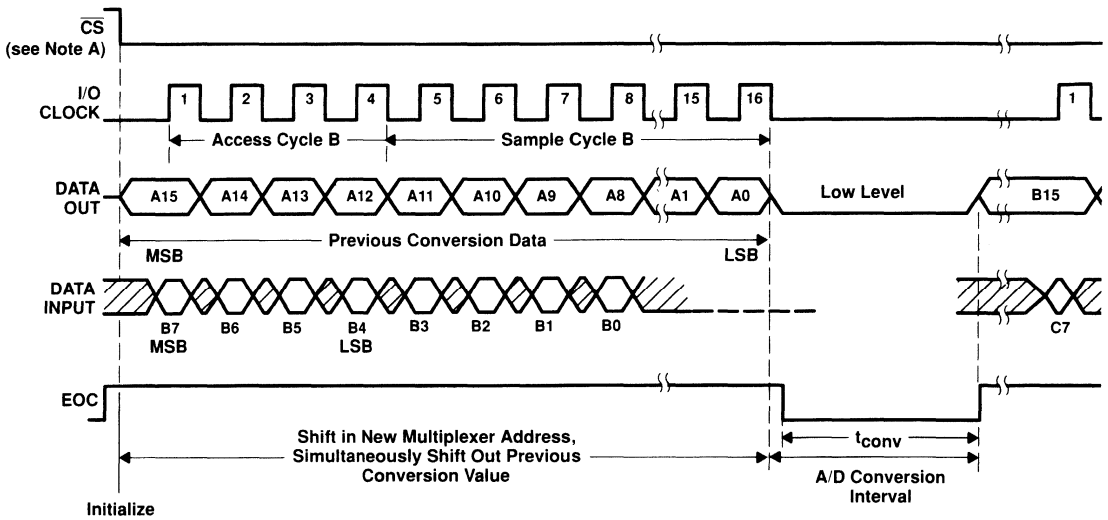
TLC2543C, TLC2543I, TLC2543M
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS
SLAS079D – DECEMBER 1993 – REVISED MAY 1997

PARAMETER MEASUREMENT INFORMATION



NOTE A: To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.

Figure 13. Timing for 16-Clock Transfer Using \overline{CS} With MSB First



NOTE A: To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.

Figure 14. Timing for 16-Clock Transfer Not Using \overline{CS} With MSB First

TLC2543C, TLC2543I, TLC2543M

12-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS079D – DECEMBER 1993 – REVISED MAY 1997

PRINCIPLES OF OPERATION

Initially, with chip select (\overline{CS}) high, I/O CLOCK and DATA INPUT are disabled and DATA OUT is in the high-impedance state. \overline{CS} going low begins the conversion sequence by enabling I/O CLOCK and DATA INPUT and removes DATA OUT from the high-impedance state.

The input data is an 8-bit data stream consisting of a 4-bit analog channel address (D7–D4), a 2-bit data length select (D3–D2), an output MSB or LSB first bit (D1), and a unipolar or bipolar output select bit (D0) that are applied to DATA INPUT. The I/O CLOCK sequence applied to the I/O CLOCK terminal transfers this data to the input data register.

During this transfer, the I/O CLOCK sequence also shifts the previous conversion result from the output data register to DATA OUT. I/O CLOCK receives the input sequence of 8, 12, or 16 clock cycles long depending on the data-length selection in the input data register. Sampling of the analog input begins on the fourth falling edge of the input I/O CLOCK sequence and is held after the last falling edge of the I/O CLOCK sequence. The last falling edge of the I/O CLOCK sequence also takes EOC low and begins the conversion.

converter operation

The operation of the converter is organized as a succession of two distinct cycles: 1) the I/O cycle and 2) the actual conversion cycle.

I/O cycle

The I/O cycle is defined by the externally provided I/O CLOCK and lasts 8, 12, or 16 clock periods, depending on the selected output data length.

During the I/O cycle, the following two operations take place simultaneously.

An 8-bit data stream consisting of address and control information is provided to DATA INPUT. This data is shifted into the device on the rising edge of the first eight I/O CLOCKS. DATA INPUT is ignored after the first eight clocks during 12- or 16-clock I/O transfers.

The data output, with a length of 8, 12, or 16 bits, is provided serially on DATA OUT. When \overline{CS} is held low, the first output data bit occurs on the rising edge of EOC. When \overline{CS} is negated between conversions, the first output data bit occurs on the falling edge of \overline{CS} . This data is the result of the previous conversion period, and after the first output data bit, each succeeding bit is clocked out on the falling edge of each succeeding I/O CLOCK.

conversion cycle

The conversion cycle is transparent to the user, and it is controlled by an internal clock synchronized to I/O CLOCK. During the conversion period, the device performs a successive-approximation conversion on the analog input voltage. The EOC output goes low at the start of the conversion cycle and goes high when conversion is complete and the output data register is latched. A conversion cycle is started only after the I/O cycle is completed, which minimizes the influence of external digital noise on the accuracy of the conversion.

TLC2543C, TLC2543I, TLC2543M
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS079D – DECEMBER 1993 – REVISED MAY 1997

PRINCIPLES OF OPERATION

power up and initialization

After power up, \overline{CS} must be taken from high to low to begin an I/O cycle. EOC is initially high, and the input data register is set to all zeroes. The contents of the output data register are random, and the first conversion result should be ignored. To initialize during operation, \overline{CS} is taken high and is then returned low to begin the next I/O cycle. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

Table 1. Operational Terminology

Current (N) I/O cycle	The entire I/O CLOCK sequence that transfers address and control data into the data register and clocks the digital result from the previous conversion from DATA OUT
Current (N) conversion cycle	The conversion cycle starts immediately after the current I/O cycle. The end of the current I/O cycle is the last clock falling edge in the I/O CLOCK sequence. The current conversion result is loaded into the output register when conversion is complete.
Current (N) conversion result	The current conversion result is serially shifted out on the next I/O cycle.
Previous (N-1) conversion cycle	The conversion cycle just prior to the current I/O cycle
Next (N+1) I/O cycle	The I/O period that follows the current conversion cycle

Example: In the 12-bit mode, the result of the current conversion cycle is a 12-bit serial-data stream clocked out during the next I/O cycle. The current I/O cycle must be exactly 12 bits long to maintain synchronization, even when this corrupts the output data from the previous conversion. The current conversion is begun immediately after the twelfth falling edge of the current I/O cycle.



TLC2543C, TLC2543I, TLC2543M
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS079D – DECEMBER 1993 – REVISED MAY 1997

PRINCIPLES OF OPERATION

data input

The data input is internally connected to an 8-bit serial-input address and control register. The register defines the operation of the converter and the output data length. The host provides the data word with the MSB first. Each data bit is clocked in on the rising edge of the I/O CLOCK sequence (see Table 2 for the data input-register format).

Table 2. Input-Register Format

FUNCTION SELECT	INPUT DATA BYTE							
	ADDRESS BITS				L1	L0	LSBF	BIP
	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
Select input channel								
AIN0 _____	0	0	0	0				
AIN1 _____	0	0	0	1				
AIN2 _____	0	0	1	0				
AIN3 _____	0	0	1	1				
AIN4 _____	0	1	0	0				
AIN5 _____	0	1	0	1				
AIN6 _____	0	1	1	0				
AIN7 _____	0	1	1	1				
AIN8 _____	1	0	0	0				
AIN9 _____	1	0	0	1				
AIN10 _____	1	0	1	0				
Select test voltage								
$(V_{ref+} - V_{ref-})/2$ _____	1	0	1	1				
V_{ref-} _____	1	1	0	0				
V_{ref+} _____	1	1	0	1				
Software power down _____	1	1	1	0				
Output data length								
8 bits _____					0	1		
12 bits _____					X†	0		
16 bits _____					1	1		
Output data format								
MSB first _____							0	
LSB first (LSBF) _____							1	
Unipolar (binary) _____								0
Bipolar (BIP) 2s complement _____								1

† X represents a do not care condition.

data input address bits

The four MSBs (D7 – D4) of the data register address one of the 11 input channels, a reference-test voltage, or the power-down mode. The address bits affect the current conversion, which is the conversion that immediately follows the current I/O cycle. The reference voltage is nominally equal to $V_{ref+} - V_{ref-}$.



PRINCIPLES OF OPERATION

data output length

The next two bits (D3 and D2) of the data register select the output data length. The data-length selection is valid for the current I/O cycle (the cycle in which the data is read). The data-length selection, being valid for the current I/O cycle, allows device startup without losing I/O synchronization. A data length of 8, 12, or 16 bits can be selected. Since the converter has 12-bit resolution, a data length of 12 bits is suggested.

With D3 and D2 set to 00 or 10, the device is in the 12-bit data-length mode and the result of the current conversion is output as a 12-bit serial data stream during the next I/O cycle. The current I/O cycle must be exactly 12 bits long for proper synchronization, even when this means corrupting the output data from a previous conversion. The current conversion is started immediately after the twelfth falling edge of the current I/O cycle.

With bits D3 and D2 set to 11, the 16-bit data-length mode is selected, which allows convenient communication with 16-bit serial interfaces. In the 16-bit mode, the result of the current conversion is output as a 16-bit serial data stream during the next I/O cycle with the four LSBs always reset to 0 (pad bits). The current I/O cycle must be exactly 16 bits long to maintain synchronization even when this means corrupting the output data from the previous conversion. The current conversion is started immediately after the sixteenth falling edge of the current I/O cycle.

With bits D3 and D2 set to 01, the 8-bit data-length mode is selected, which allows fast communication with 8-bit serial interfaces. In the 8-bit mode, the result of the current conversion is output as an 8-bit serial data stream during the next I/O cycle. The current I/O cycle must be exactly eight bits long to maintain synchronization, even when this means corrupting the output data from the previous conversion. The four LSBs of the conversion result are truncated and discarded. The current conversion is started immediately after the eighth falling edge of the current I/O cycle.

Since D3 and D2 take effect on the current I/O cycle when the data length is programmed, there can be a conflict with the previous cycle when the data-word length is changed from one cycle to the next. This may occur when the data format is selected to be least significant bit first, since at the time the data length change becomes effective (six rising edges of I/O CLOCK), the previous conversion result has already started shifting out.

In actual operation, when different data lengths are required within an application and the data length is changed between two conversions, no more than one conversion result can be corrupted and only when it is shifted out in LSB-first format.

sampling period

During the sampling period, one of the analog inputs is internally connected to the capacitor array of the converter to store the analog input signal. The converter starts sampling the selected input immediately after the four address bits have been clocked into the input data register. Sampling starts on the fourth falling edge of I/O CLOCK. The converter remains in the sampling mode until the eighth, twelfth, or sixteenth falling edge of the I/O CLOCK depending on the data-length selection. After the EOC delay time from the last I/O CLOCK falling edge, the EOC output goes low indicating that the sampling period is over and the conversion period has begun. After EOC goes low, the analog input can be changed without affecting the conversion result. Since the delay from the falling edge of the last I/O CLOCK to EOC low is fixed, time-varying analog input signals can be digitized at a fixed rate without introducing systematic harmonic distortion or noise due to timing uncertainty.

After the 8-bit data stream has been clocked in, DATA INPUT should be held at a fixed digital level until EOC goes high (indicating that the conversion is complete) to maximize the sampling accuracy and minimize the influence of external digital noise.

TLC2543C, TLC2543I, TLC2543M
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS
SLAS079D – DECEMBER 1993 – REVISED MAY 1997

PRINCIPLES OF OPERATION

data register, LSB first

D1 in the input data register (LSB first) controls the direction of the output binary data transfer. When D1 is reset to 0, the conversion result is shifted out MSB first. When set to 1, the data is shifted out LSB first. Selection of MSB first or LSB first always affects the next I/O cycle and not the current I/O cycle. When changing from one data direction to another, the current I/O cycle is never disrupted.

data register, bipolar format

D0 (BIP) in the input data register controls the binary data format used to represent the conversion result. When D0 is cleared to 0, the conversion result is represented as unipolar (unsigned binary) data. Nominally, the conversion result of an input voltage equal to V_{ref-} is a code of all zeros (000 . . . 0), the conversion result of an input voltage equal to V_{ref+} is a code of all ones (111 . . . 1), and the conversion result of $(V_{ref+} + V_{ref-})/2$ is a code of a one followed by zeros (100 . . . 0).

When D0 is set to 1, the conversion result is represented as bipolar (signed binary) data. Nominally, conversion of an input voltage equal to V_{ref-} is a code of a one followed by zeros (100 . . . 0), conversion of an input voltage equal to V_{ref+} is a code of a zero followed by all ones (011 . . . 1), and the conversion of $(V_{ref+} + V_{ref-})/2$ is a code of all zeros (000 . . . 0). The MSB is interpreted as the sign bit. The bipolar data format is related to the unipolar format in that the MSBs are always each other's complement.

Selection of the unipolar or bipolar format always affects the current conversion cycle, and the result is output during the next I/O cycle. When changing between unipolar and bipolar formats, the data output during the current I/O cycle is not affected.

EOC output

The EOC signal indicates the beginning and the end of conversion. In the reset state, EOC is always high. During the sampling period (beginning after the fourth falling edge of the I/O CLOCK sequence), EOC remains high until the internal sampling switch of the converter is safely opened. The opening of the sampling switch occurs after the eighth, twelfth, or sixteenth I/O CLOCK falling edge, depending on the data-length selection in the input data register. After the EOC signal goes low, the analog input signal can be changed without affecting the conversion result.

The EOC signal goes high again after the conversion is completed and the conversion result is latched into the output data register. The rising edge of EOC returns the converter to a reset state and a new I/O cycle begins. On the rising edge of EOC, the first bit of the current conversion result is on DATA OUT when \overline{CS} is low. When \overline{CS} is negated between conversions, the first bit of the current conversion result occurs at DATA OUT on the falling edge of \overline{CS} .

data format and pad bits

D3 and D2 of the input data register determine the number of significant bits in the digital output that represent the conversion result. The LSB-first bit determines the direction of the data transfer while the BIP bit determines the arithmetic conversion. The numerical data is always justified toward the MSB in any output format.

The internal conversion result is always 12 bits long. When an 8-bit data transfer is selected, the four LSBs of the internal result are discarded to provide a faster one-byte transfer. When a 12-bit transfer is used, all bits are transferred. When a 16-bit transfer is used, four LSB pad bits are always appended to the internal conversion result. In the LSB-first mode, four leading zeros are output. In the MSB-first mode, the last four bits output are zeros.

TLC2543C, TLC2543I, TLC2543M
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS
SLAS079D – DECEMBER 1993 – REVISED MAY 1997

PRINCIPLES OF OPERATION

data format and pad bits (continued)

When \overline{CS} is held low continuously, the first data bit of the newly completed conversion occurs on DATA OUT on the rising edge of EOC. When a new conversion is started after the last falling edge of I/O CLOCK, EOC goes low and the serial output is forced to a setting of 0 until EOC goes high again.

When \overline{CS} is negated between conversions, the first data bit occurs on DATA OUT on the falling edge of \overline{CS} . On each subsequent falling edge of I/O CLOCK after the first data bit appears, the data is changed to the next bit in the serial conversion result until the required number of bits has been output.

chip-select input (\overline{CS})

\overline{CS} enables and disables the device. During normal operation, \overline{CS} should be low. Although the use of \overline{CS} is not necessary to synchronize a data transfer, it can be brought high between conversions to coordinate the data transfer of several devices sharing the same bus.

When \overline{CS} is brought high, the serial-data output is immediately brought to the high-impedance state, releasing its output data line to other devices that may share it. After an internally generated debounce time, I/O CLOCK is inhibited, thus preventing any further change in the internal state.

When \overline{CS} is subsequently brought low again, the device is reset. \overline{CS} must be held low for an internal debounce time before the reset operation takes effect. After \overline{CS} is debounced low, I/O CLOCK must remain inactive (low) for a minimum time before a new I/O cycle can start.

\overline{CS} can interrupt any ongoing data transfer or any ongoing conversion. When \overline{CS} is debounced low long enough before the end of the current conversion cycle, the previous conversion result is saved in the internal output buffer and shifted out during the next I/O cycle.

power-down features

When a binary address of 1110 is clocked into the input data register during the first four I/O CLOCK cycles, the power-down mode is selected. Power down is activated on the falling edge of the fourth I/O CLOCK pulse.

During power down, all internal circuitry is put in a low-current standby mode. No conversions are performed, and the internal output buffer keeps the previous conversion cycle data results provided that all digital inputs are held above $V_{CC} - 0.5$ V or below 0.5 V. The I/O logic remains active so the current I/O cycle must be completed even when the power-down mode is selected. Upon power-on reset and before the first I/O cycle, the converter normally begins in the power-down mode. The device remains in the power-down mode until a valid input address (other than 1110) is clocked in. Upon completion of that I/O cycle, a normal conversion is performed with the results being shifted out during the next I/O cycle.



TLC2543C, TLC2543I, TLC2543M
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS
 SLAS079D – DECEMBER 1993 – REVISED MAY 1997

PRINCIPLES OF OPERATION

analog input, test, and power-down mode

The 11 analog inputs, three internal voltages, and power-down mode are selected by the input multiplexer according to the input addresses shown in Tables 2, 3, and 4. The input multiplexer is a break-before-make type to reduce input-to-input noise rejection resulting from channel switching. Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK and continues for the remaining I/O CLOCK pulses. The sample is held on the falling edge of the last I/O CLOCK pulse. The three internal test inputs are applied to the multiplexer, then sampled and converted in the same manner as the external analog inputs. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

Table 3. Analog-Channel-Select Address

ANALOG INPUT SELECTED	VALUE SHIFTED INTO DATA INPUT	
	BINARY	HEX
AIN0	0000	0
AIN1	0001	1
AIN2	0010	2
AIN3	0011	3
AIN4	0100	4
AIN5	0101	5
AIN6	0110	6
AIN7	0111	7
AIN8	1000	8
AIN9	1001	9
AIN10	1010	A

Table 4. Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED†	VALUE SHIFTED INTO DATA INPUT		UNIPOLAR OUTPUT RESULT (HEX)‡
	BINARY	HEX	
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	B	800
V_{ref-}	1100	C	000
V_{ref+}	1101	D	FFF

† V_{ref+} is the voltage applied to REF+, and V_{ref-} is the voltage applied to REF-.

‡ The output results shown are the ideal values and may vary with the reference stability and with internal offsets.

Table 5. Power-Down-Select Address

INPUT COMMAND	VALUE SHIFTED INTO DATA INPUT		RESULT
	BINARY	HEX	
Power down	1110	E	$I_{CC} \leq 25 \mu A$



TLC2543C, TLC2543I, TLC2543M
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS079D – DECEMBER 1993 – REVISED MAY 1997

PRINCIPLES OF OPERATION

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference ($REF-$) voltage. In the switching sequence, 12 capacitors are examined separately until all 12 bits are identified and the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 4096). Node 4096 of this capacitor is switched to the $REF+$ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to $REF-$. When the voltage at the summing node is greater than the trip point of the threshold detector (approximately $1/2 V_{CC}$), a bit 0 is placed in the output register and the 4096-weight capacitor is switched to $REF-$. When the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and this 4096-weight capacitor remains connected to $REF+$ through the remainder of the successive-approximation process. The process is repeated for the 2048-weight capacitor, the 1024-weight capacitor, and so forth down the line until all bits are determined. With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.

reference voltage inputs

The two reference inputs used with the device are the voltages applied to the $REF+$ and $REF-$ terminals. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero-scale reading respectively. These voltages and the analog input should not exceed the positive supply or be lower than ground consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than $REF+$ terminal voltage and at zero when the input signal is equal to or lower than $REF-$ terminal voltage.

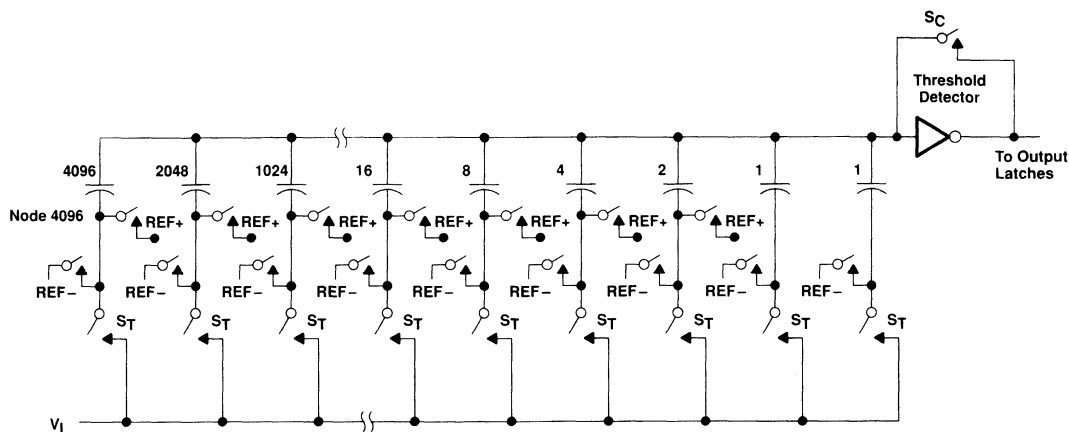
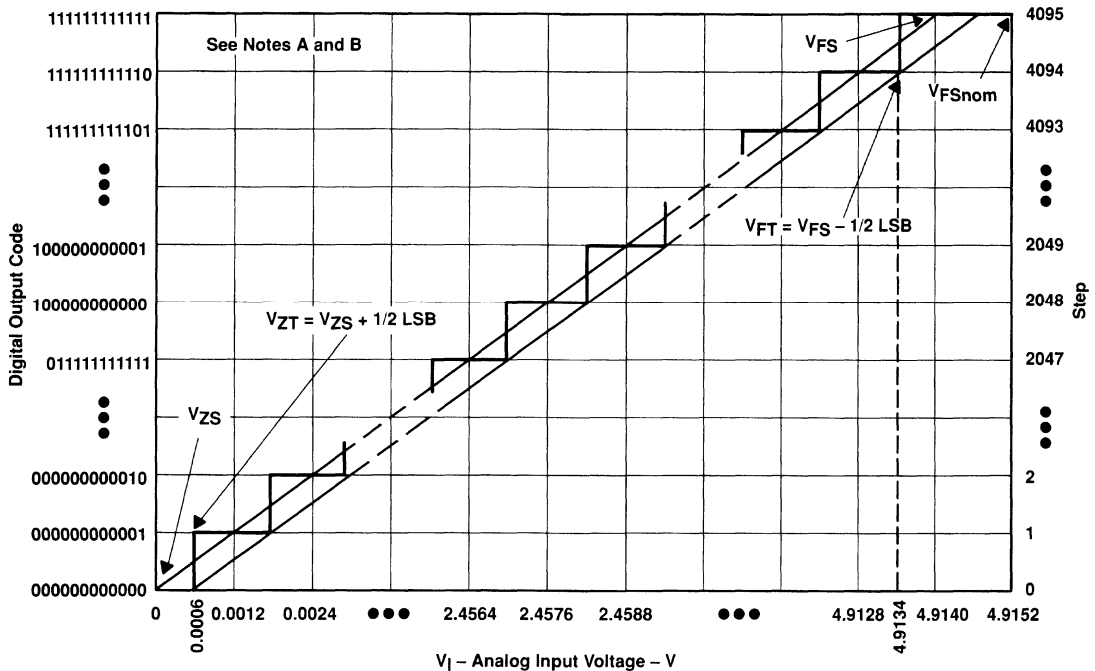


Figure 15. Simplified Model of the Successive-Approximation System

TLC2543C, TLC2543I, TLC2543M
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS079D – DECEMBER 1993 – REVISED MAY 1997

APPLICATION INFORMATION



NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0006 V and the transition to full scale (V_{FT}) is 4.9134 V. 1 LSB = 1.2 mV.
 B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 16. Ideal Conversion Characteristics

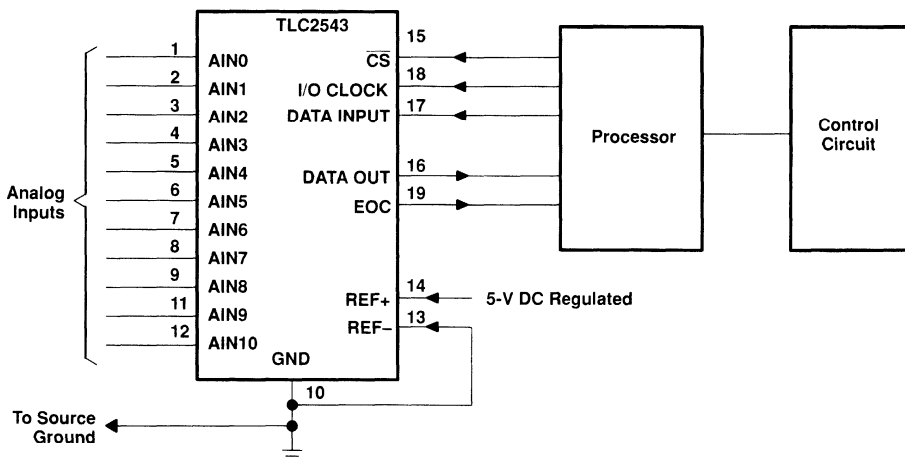


Figure 17. Serial Interface



APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 18, the time required to charge the analog input capacitance from 0 V to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c / R_t C_i} \right) \quad (1)$$

where

$$R_t = R_s + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S / 8192) \quad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S / 8192) = V_S \left(1 - e^{-t_c / R_t C_i} \right) \quad (3)$$

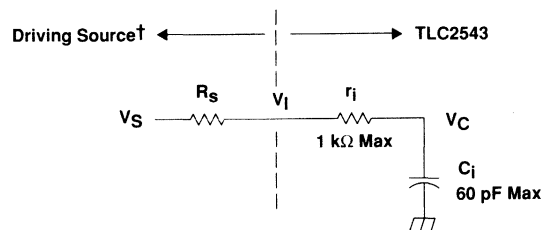
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(8192) \quad (4)$$

Therefore, with the values given, the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_s + 1 \text{ k}\Omega) \times 60 \text{ pF} \times \ln(8192) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at AIN
 V_S = External Driving Source Voltage
 R_S = Source Resistance
 r_i = Input Resistance
 C_i = Input Capacitance
 V_C = Capacitance Charging Voltage

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 18. Equivalent Input Circuit Including the Driving Source

TLC5510, TLC5510A 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS

SLAS095I – SEPTEMBER 1994 – REVISED APRIL 1997

features

- **Analog Input Range**
 - TLC5510 . . . 2 V Full Scale
 - TLC5510A . . . 4 V Full Scale
- **8-Bit Resolution**
- **Linearity Error**
 - ±0.75 LSB Max (25°C)
 - ±1 LSB Max (–20°C to 75°C)
- **Differential Linearity Error**
 - ±0.5 LSB (25°C)
 - ±0.75 LSB Max (–20°C to 75°C)
- **Maximum Conversion Rate**
20 Mega-Samples per Second (MSPS) Min
- **5-V Single-Supply Operation**
- **Low Power Consumption**
TLC5510 . . . 127.5 mW Typ
TLC5510A . . . 150 mW Typ
(includes reference resistor dissipation)
- **TLC5510 is Interchangeable With Sony CXD1175**

applications

- Digital TV
- Medical Imaging
- Video Conferencing
- High-Speed Data Conversion
- QAM Demodulators

description

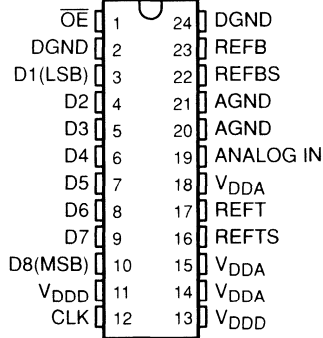
The TLC5510 and TLC5510A are CMOS, 8-bit, 20 MSPS analog-to-digital converters (ADCs) that utilize a semiflash architecture. The TLC5510 and TLC5510A operate with a single 5-V supply and typically consume only 130 mW of power. Included is an internal sample-and-hold circuit, parallel outputs with high-impedance mode, and internal reference resistors.

The semiflash architecture reduces power consumption and die size compared to flash converters. By implementing the conversion in a 2-step process, the number of comparators is significantly reduced. The latency of the data output valid is 2.5 clocks.

The TLC5510 uses the three internal reference resistors to create a standard, 2-V, full-scale conversion range using V_{DDA} . Only external jumpers are required to implement this option and eliminates the need for external reference resistors. The TLC5510A uses only the center internal resistor section with an externally applied 4-V reference such that a 4-V input signal can be used. Differential linearity is 0.5 LSB at 25°C and a maximum of 0.75 LSB over the full operating temperature range. Typical dynamic specifications include a differential gain of 1% and differential phase of 0.7 degrees.

The TLC5510 and TLC5510A are characterized for operation from –20°C to 75°C.

NS PACKAGE†
(TOP VIEW)



† Available in tape and reel only and ordered as the shown in the Available Options table below.

AVAILABLE OPTIONS

TA	NS PACKAGE (TAPE AND REEL ONLY)	MAXIMUM FULL-SCALE INPUT VOLTAGE (VOLTS)
–20°C to 75°C	TLC5510INSLE	2 V
	TLC5510AINSLE	4 V

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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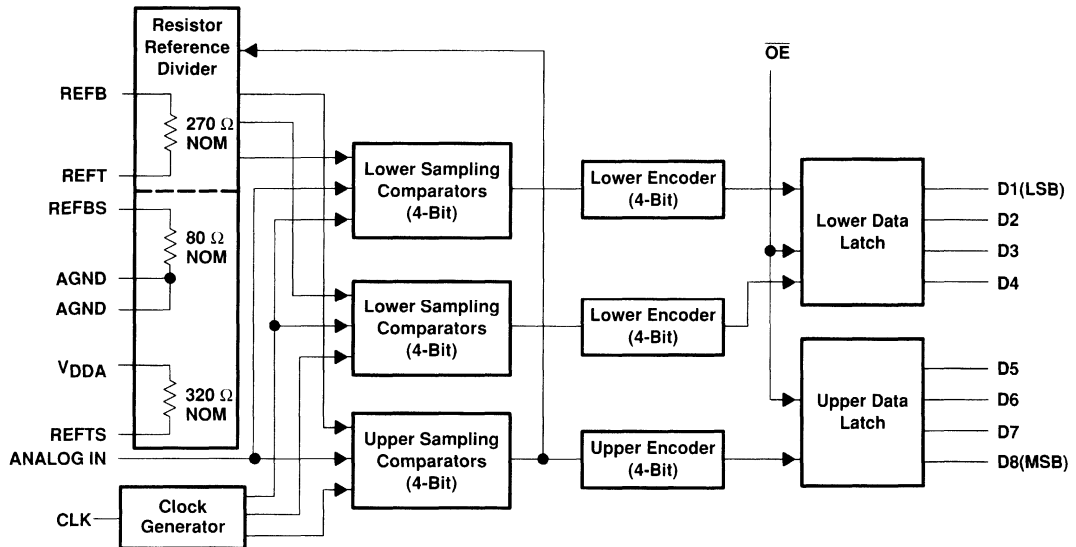
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TLC5510, TLC5510A

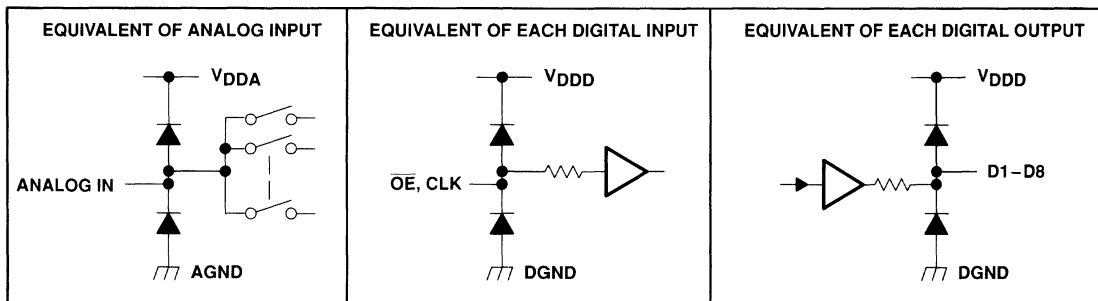
8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS

SLAS095I - SEPTEMBER 1994 - REVISED APRIL 1997

functional block diagram



schematics of inputs and outputs



TLC5510, TLC5510A

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS

SLAS095I – SEPTEMBER 1994 – REVISED APRIL 1997

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	20, 21		Analog ground
ANALOG IN	19	I	Analog input
CLK	12	I	Clock input
DGND	2, 24		Digital ground
D1–D8	3–10	O	Digital data out. D1 = LSB, D8 = MSB
\overline{OE}	1	I	Output enable. When \overline{OE} = low, data is enabled. When \overline{OE} = high, D1–D8 is in high-impedance state.
V _{DDA}	14, 15, 18		Analog supply voltage
V _{DDD}	11, 13		Digital supply voltage
REFB	23	I	Reference voltage in bottom
REFBS	22		Reference voltage in bottom. When using the TLC5510 internal voltage divider to generate a nominal 2-V reference, REFBS is shorted to REFB (see Figure 2). When using the TLC5510A, REFBS is connected to ground.
REFT	17	I	Reference voltage in top
REFTS	16		Reference voltage in top. When using the TLC5510 internal voltage divider to generate a nominal 2-V reference, REFTS is shorted to REFT (see Figure 2). When using the TLC5510A, REFTS is connected to V _{DDA} .

absolute maximum ratings†

Supply voltage, V _{DDA} , V _{DDD}	7 V
Reference voltage input range, V _{ref(T)} , V _{ref(B)}	AGND to V _{DDA}
Analog input voltage range, V _{I(ANLG)}	AGND to V _{DDA}
Digital input voltage range, V _{I(DGTL)}	DGND to V _{DDD}
Digital output voltage range, V _{O(DGTL)}	DGND to V _{DDD}
Operating free-air temperature range, T _A	–20°C to 75°C
Storage temperature range, T _{stg}	–55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V _{DDA} –AGND	4.75	5	5.25	V
	V _{DDD} –AGND	4.75	5	5.25	
	AGND–DGND	–100	0	100	mV
Reference input voltage (top), V _{ref(T)} ‡	TLC5510A	V _{ref(B)} +2		4	V
Reference input voltage (bottom), V _{ref(B)} ‡	TLC5510A	0	V _{ref(T)} –4		V
Analog input voltage range, V _{I(ANLG)}		V _{ref(B)}		V _{ref(T)}	V
High-level input voltage, V _{IH}		4			V
Low-level input voltage, V _{IL}				1	V
Pulse duration, clock high, t _{w(H)} (see Figure 1)		25			ns
Pulse duration, clock low, t _{w(L)} (see Figure 1)		25			ns

‡ The reference voltage levels for the TLC5510 are derived through an internal resistor divider between V_{DDA} and ground and therefore are not derived from a separate external voltage source (see the electrical characteristics and text). For the 4 V input range of the TLC5510A, the reference voltage is externally applied across the center divider resistor.



TLC5510, TLC5510A

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS

SLAS0951 – SEPTEMBER 1994 – REVISED APRIL 1997

electrical characteristics at $V_{DD} = 5\text{ V}$, $V_{ref}(T) = 2.5\text{ V}$, $V_{ref}(B) = 0.5\text{ V}$, $f_{(CLK)} = 20\text{ MHz}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

digital I/O

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
I_{IH} High-level input current	$V_{DD} = \text{MAX}$, $V_{IH} = V_{DD}$			5	μA
I_{IL} Low-level input current	$V_{DD} = \text{MAX}$, $V_{IL} = 0$			5	
I_{OH} High-level output current	$\overline{OE} = \text{GND}$, $V_{DD} = \text{MIN}$, $V_{OH} = V_{DD} - 0.5\text{ V}$	-1.5			mA
I_{OL} Low-level output current	$\overline{OE} = \text{GND}$, $V_{DD} = \text{MIN}$, $V_{OL} = 0.4\text{ V}$	2.5			
I_{OZH} High-level high-impedance-state output leakage current	$\overline{OE} = V_{DD}$, $V_{DD} = \text{MAX}$, $V_{OH} = V_{DD}$			16	μA
I_{OZL} Low-level high-impedance-state output leakage current	$\overline{OE} = V_{DD}$, $V_{DD} = \text{MIN}$, $V_{OL} = 0$			16	

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

power

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT	
I_{DD} Supply current	$f_{(CLK)} = 20\text{ MHz}$, National Television System Committee (NTSC) ramp wave input, reference resistor dissipation is separate		18	27	mA	
I_{ref} Reference voltage current	TLC5510	$V_{ref} = \text{REFT} - \text{REFB} = 2\text{ V}$	5.2	7.5	10.5	mA
	TLC5510A	$V_{ref} = \text{REFT} - \text{REFB} = 4\text{ V}$	10.4	15	21	mA

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

static performance

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT	
Self-bias (1), at REFB	Short REFB to REFBs, Short REFT to REFTS	0.57	0.61	0.65	V	
Self-bias (2), REFT – REFB		1.9	2.02	2.15		
Self-bias (3), at REFT		2.18	2.29	2.4		
R_{ref} Reference voltage resistor	Between REFT and REFB	190	270	350	Ω	
C_i Analog input capacitance	$V_i(\text{ANLG}) = 1.5\text{ V} + 0.07 V_{rms}$		16		pF	
Integral nonlinearity (INL)	TLC5510	$f_{(CLK)} = 20\text{ MHz}$, $V_i = 0.5\text{ V to } 2.5\text{ V}$	$T_A = 25^\circ\text{C}$	± 0.4	± 0.75	LSB
		$T_A = -20^\circ\text{C to } 75^\circ\text{C}$			± 1	
	TLC5510A	$f_{(CLK)} = 20\text{ MHz}$, $V_i = 0\text{ to } 4\text{ V}$	$T_A = 25^\circ\text{C}$	± 0.4	± 0.75	
		$T_A = -20^\circ\text{C to } 75^\circ\text{C}$			± 1	
Differential nonlinearity (DNL)	TLC5510	$f_{(CLK)} = 20\text{ MHz}$, $V_i = 0.5\text{ V to } 2.5\text{ V}$	$T_A = 25^\circ\text{C}$	± 0.3	± 0.5	
		$T_A = -20^\circ\text{C to } 75^\circ\text{C}$			± 0.75	
	TLC5510A	$f_{(CLK)} = 20\text{ MHz}$, $V_i = 0\text{ to } 4\text{ V}$	$T_A = 25^\circ\text{C}$	± 0.3	± 0.5	
		$T_A = -20^\circ\text{C to } 75^\circ\text{C}$			± 0.75	
E_{ZS} Zero-scale error	TLC5510	$V_{ref} = \text{REFT} - \text{REFB} = 2\text{ V}$	-18	-43	-68	mV
	TLC5510A	$V_{ref} = \text{REFT} - \text{REFB} = 4\text{ V}$	-36	-86	-136	mV
E_{FS} Full-scale error	TLC5510	$V_{ref} = \text{REFT} - \text{REFB} = 2\text{ V}$	-20	0	20	mV
	TLC5510A	$V_{ref} = \text{REFT} - \text{REFB} = 4\text{ V}$	-40	0	40	mV

† Conditions marked MIN or MAX are as stated in recommended operating conditions.



TLC5510, TLC5510A

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS

SLAS095I – SEPTEMBER 1994 – REVISED APRIL 1997

operating characteristics at $V_{DD} = 5\text{ V}$, $V_{RT} = 2.5\text{ V}$, $V_{RB} = 0.5\text{ V}$, $f_{(CLK)} = 20\text{ MHz}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{conv}	Maximum conversion rate	TLC5510	$f_j = 1\text{-kHz ramp}$	$V_{I(ANLG)} = 0.5\text{ V} - 2.5\text{ V}$		20	MSPS
		TLC5510A		$V_{I(ANLG)} = 0\text{ V} - 4\text{ V}$		20	
BW	Analog input bandwidth	At -1 dB			14		MHz
$t_{d(D)}$	Digital output delay time	$C_L \leq 10\text{ pF}$ (see Note 1 and Figure 1)			18	30	ns
	Differential gain	NTSC 40 Institute of Radio Engineers (IRE) modulation wave, $f_{conv} = 14.3\text{ MSPS}$			1%		
	Differential phase				0.7		degrees
t_{AJ}	Aperture jitter time				30		ps
$t_{d(s)}$	Sampling delay time				4		ns
t_{en}	Enable time, $\overline{OE} \downarrow$ to valid data	$C_L = 10\text{ pF}$			5		ns
t_{dis}	Disable time, $\overline{OE} \uparrow$ to high impedance	$C_L = 10\text{ pF}$			7		ns
Spurious free dynamic range (SFDR)		Input tone = 1 MHz	$T_A = 25^\circ\text{C}$		45		dB
			Full range		43		
		Input tone = 3 MHz	$T_A = 25^\circ\text{C}$		45		
			Full range		46		
		Input tone = 6 MHz	$T_A = 25^\circ\text{C}$		43		
			Full range		42		
		Input tone = 10 MHz	$T_A = 25^\circ\text{C}$		39		
			Full range		39		
SNR	Signal-to-noise ratio	$T_A = 25^\circ\text{C}$			46		dB
		Full range			44		

NOTE 1: C_L includes probe and jig capacitance.

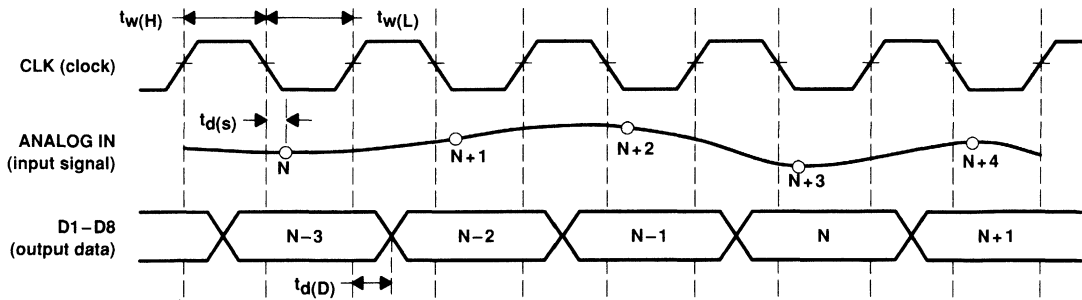


Figure 1. I/O Timing Diagram

TLC5510, TLC5510A

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS

SLAS095I – SEPTEMBER 1994 – REVISED APRIL 1997

PRINCIPLES OF OPERATION

functional description

The TLC5510 and TLC5510A are semiflash ADCs featuring two lower comparator blocks of four bits each.

As shown in Figure 2, input voltage $V_I(1)$ is sampled with the falling edge of CLK1 to the upper comparators block and the lower comparators block(A), S(1). The upper comparators block finalizes the upper data UD(1) with the rising edge of CLK2, and simultaneously, the lower reference voltage generates the voltage RV(1) corresponding to the upper data. The lower comparators block (A) finalizes the lower data LD(1) with the rising edge of CLK3. UD(1) and LD(1) are combined and output as OUT(1) with the rising edge of CLK4. As shown in Figure 2, the output data is delayed 2.5 clocks from the analog input voltage sampling point.

Input voltage $V_I(2)$ is sampled with the falling edge of CLK2. UD(2) is finalized with the rising edge of CLK3, and LD(2) is finalized with the rising edge of CLK4 at the lower comparators block(B). OUT(2) data appears with the rising edge of CLK5.

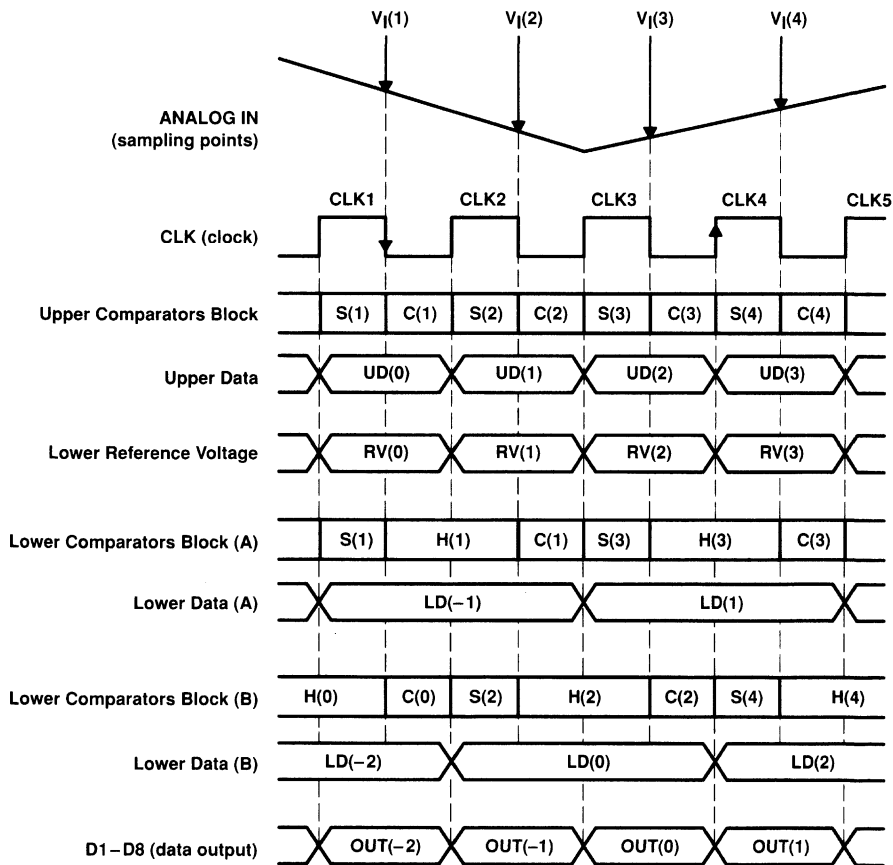


Figure 2. Internal Functional Timing Diagram

TLC5510, TLC5510A 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS

SLAS095I – SEPTEMBER 1994 – REVISED APRIL 1997

PRINCIPLES OF OPERATION

internal referencing

TLC5510

The three internal resistors shown with V_{DDA} can generate a 2-V reference voltage. These resistors are brought out on V_{DDA} , REFTS, REFT, REFB, REFBS, and AGND.

To use the internally generated reference voltage, terminal connections should be made as shown in Figure 3. This connection provides the standard video 2-V reference for the nominal digital output.

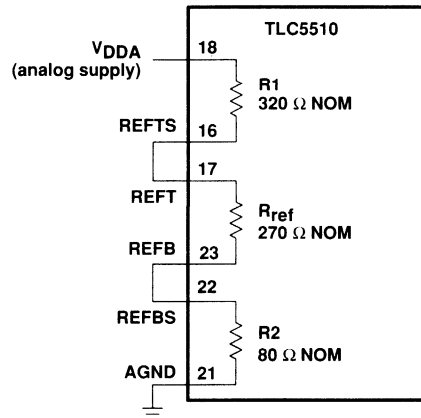


Figure 3. External Connections for a 2-V Analog Input Span Using the Internal-Reference Resistor Divider

TLC5510A

For an analog input span of 4 V, 4 V is supplied to REFT, and REFB is grounded and terminal connections should be made as shown in Figure 4. This connection provides the 4-V reference for the nominal zero to full-scale digital output with a 4 V_{pp} analog input at ANALOG IN.

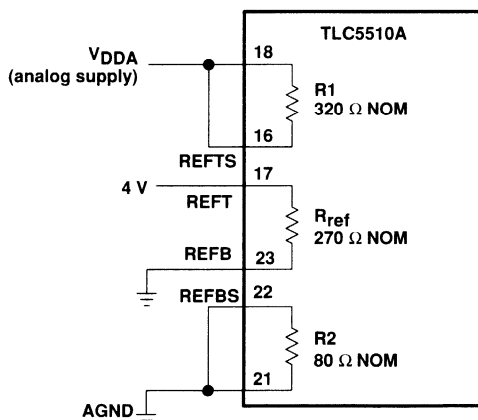


Figure 4. External Connections for 4-V Analog Input Span

TLC5510, TLC5510A

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS

SLAS095I – SEPTEMBER 1994 – REVISED APRIL 1997

PRINCIPLES OF OPERATION

functional operation

The output code change with input voltage is shown in Table 1.

Table 1. Functional Operation

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB							LSB
$V_{ref(B)}$	255	0	0	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	128	0	1	1	1	1	1	1	1
•	127	1	0	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
$V_{ref(T)}$	0	1	1	1	1	1	1	1	1

APPLICATION INFORMATION

The following notes are design recommendations that should be used with the device.

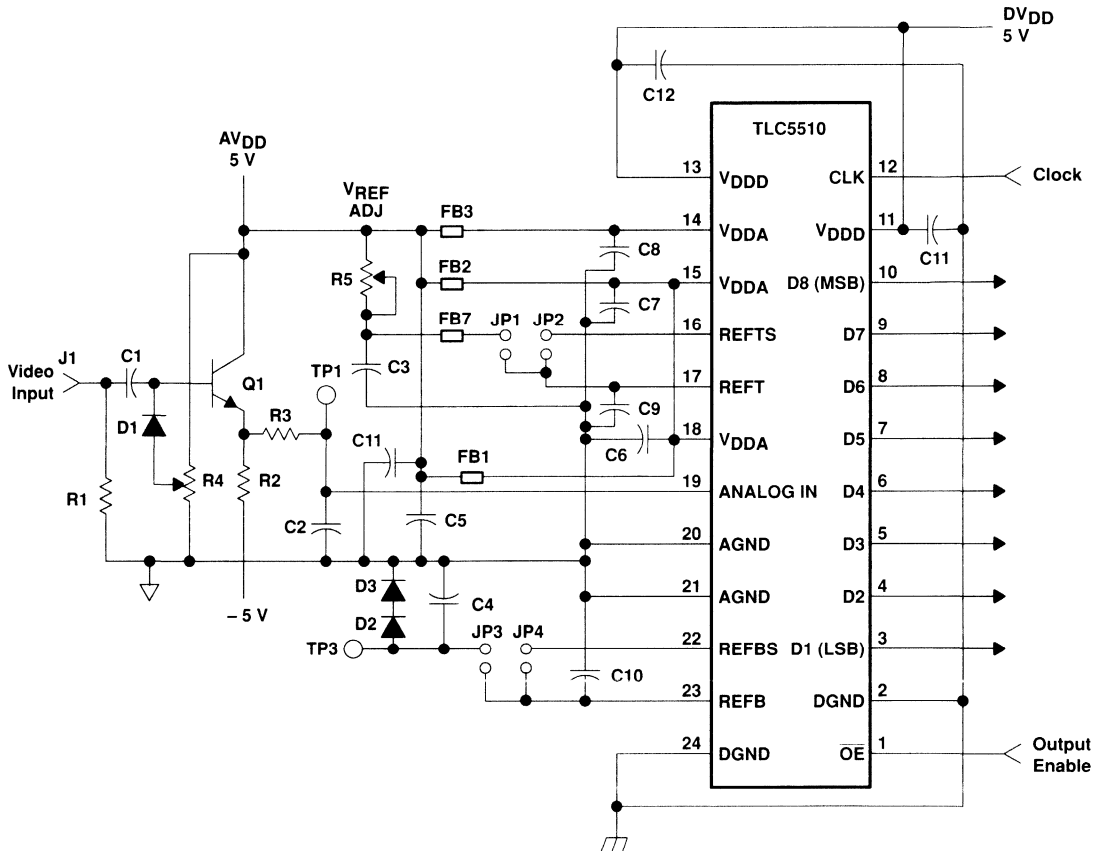
- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or printed-circuit-board (PCB) techniques should be used throughout the evaluation and production process. Breadboards should be copper clad for bench evaluation.
- Since AGND and DGND are connected internally, the ground lead in must be kept as noise free as possible. A good method to use is twisted-pair cables for the supply lines to minimize noise pickup. An analog and digital ground plane should be used on PCB layouts when additional logic devices are used. The AGND and DGND terminals of the device should be tied to the analog ground plane.
- V_{DDA} to AGND and V_{DDD} to DGND should be decoupled with 1- μ F and 0.01- μ F capacitors, respectively, and placed as close as possible to the affected device terminals. A ceramic-chip capacitor is recommended for the 0.01- μ F capacitor. Care should be exercised to ensure a solid noise-free ground connection for the analog and digital ground terminals.
- V_{DDA} , AGND, and ANALOG IN should be shielded from the higher frequency terminals, CLK and D0–D7. When possible, AGND traces should be placed on both sides of the ANALOG IN traces on the PCB for shielding.
- In testing or application of the device, the resistance of the driving source connected to the analog input should be 10 Ω or less within the analog frequency range of interest.

TLC5510, TLC5510A

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS

SLAS095I – SEPTEMBER 1994 – REVISED APRIL 1997

APPLICATION INFORMATION



NOTE A: Shorting JP1 and JP3 allows adjustment of the reference voltage by R5 using temperature-compensating diodes D2 and D3 which compensate for D1 and Q1 variations. By shorting JP2 and JP4, the internal divider generates a nominal 2-V reference.

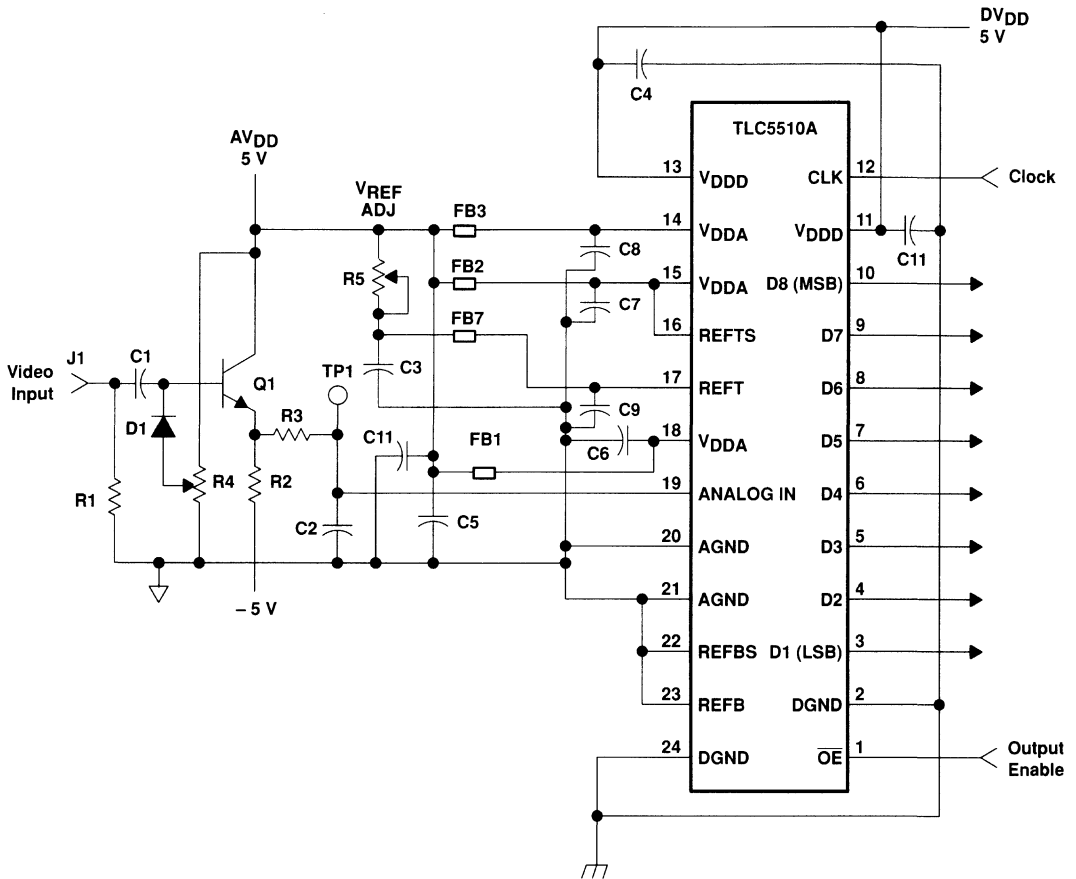
LOCATION	DESCRIPTION
C1, C3–C4, C6–C12	0.1- μ F capacitor
C2	10-pF capacitor
C5	47- μ F capacitor
FB1, FB2, FB3, FB7	Ferrite bead
Q1	2N3414 or equivalent
R1, R3	75- Ω resistor
R2	500- Ω resistor
R4	10-k Ω resistor, clamp voltage adjust
R5	300- Ω resistor, reference-voltage fine adjust

Figure 5. TLC5510 Evaluation and Test Schematic

TLC5510, TLC5510A 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS

SLAS0951 – SEPTEMBER 1994 – REVISED APRIL 1997

APPLICATION INFORMATION



NOTE A: R5 allows adjustment of the reference voltage to 4 V. R4 adjusts for the desired Q1 quiescent operating point.

LOCATION	DESCRIPTION
C1, C3–C4, C6–C11	0.1- μ F capacitor
C2	10-pF capacitor
C5	47- μ F capacitor
FB1, FB2, FB3, FB7	Ferrite bead
Q1	2N3414 or equivalent
R1, R3	75- Ω resistor
R2	500- Ω resistor
R4	10-k Ω resistor, clamp voltage adjust
R5	300- Ω resistor, reference-voltage fine adjust

Figure 6. TLC5510A Evaluation and Test Schematic

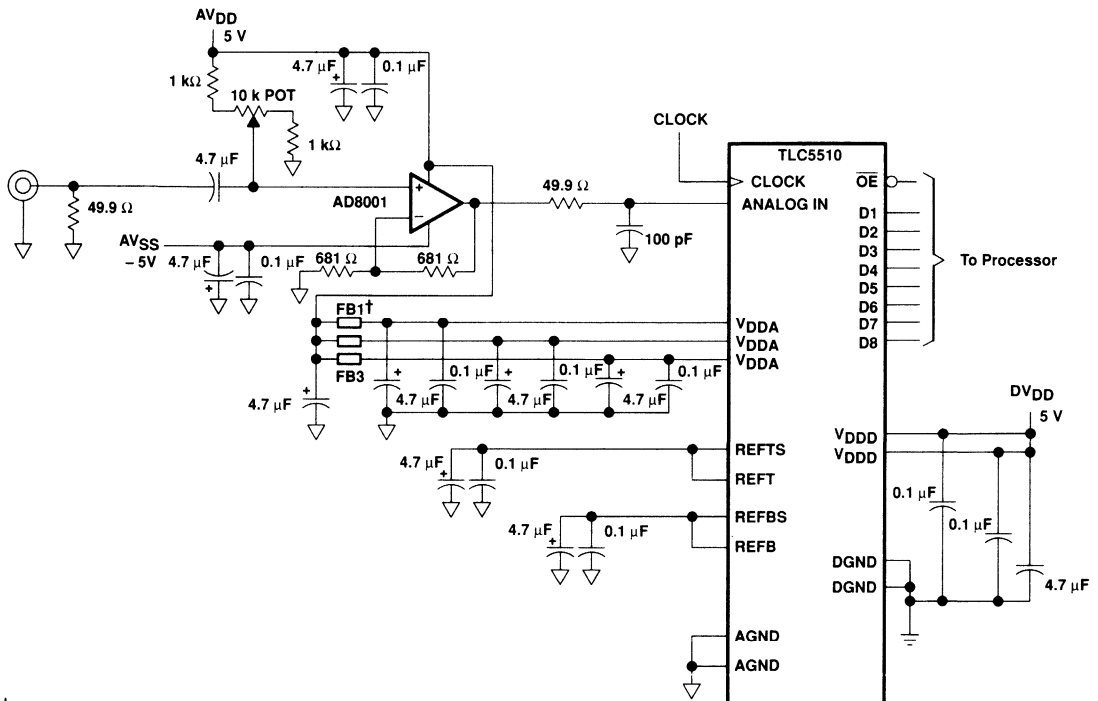


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TLC5510, TLC5510A 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS

SLAS095I – SEPTEMBER 1994 – REVISED APRIL 1997

APPLICATION INFORMATION



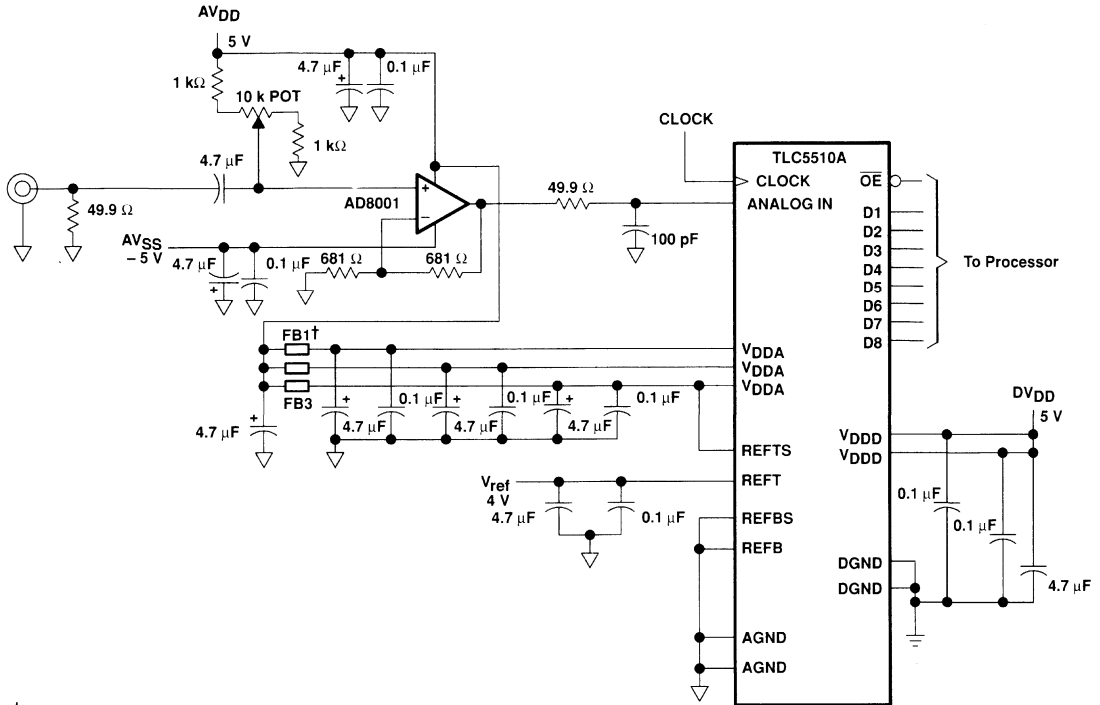
† FB – Ferrite Bead

Figure 7. TLC5510 Application Schematic

TLC5510, TLC5510A 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS

SLAS095I – SEPTEMBER 1994 – REVISED APRIL 1997

APPLICATION INFORMATION



† FB – Ferrite Bead

Figure 8. TLC5510A Application Schematic



TLC5540

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS105B – JANUARY 1995 – REVISED APRIL 1996

features

- **8-Bit Resolution**
- **Differential Linearity Error**
 - ± 0.3 LSB Typ, ± 1 LSB Max (25°C)
 - ± 1 LSB Max
- **Integral Linearity Error**
 - ± 0.6 LSB, ± 0.75 LSB Max (25°C)
 - ± 1 LSB Max
- **Maximum Conversion Rate of 40 Megasamples Per Second (MSPS) Min**
- **Internal Sample and Hold Function**
- **5-V Single Supply Operation**
- **Low Power Consumption . . . 85 mW Typ**
- **Analog Input Bandwidth . . . ≥ 75 MHz Typ**
- **Internal Reference Voltage Generators**

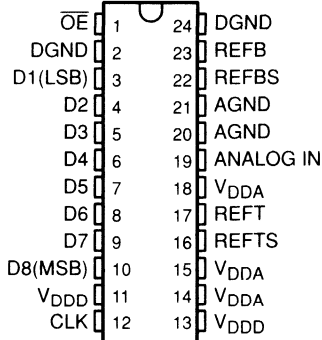
applications

- **Quadrature Amplitude Modulation (QAM) and Quadrature Phase Shift Keying (QPSK) Demodulators**
- **Digital Television**
- **Charge-Coupled Device (CCD) Scanners**
- **Video Conferencing**
- **Digital Set-Top Box**
- **Digital Down Converters**
- **High-Speed Digital Signal Processor Front End**

description

The TLC5540 is a high-speed, 8-bit analog-to-digital converter (ADC) that converts at sampling rates up to 40 megasamples per second (MSPS). Using a semiflash architecture and CMOS process, the TLC5540 is able to convert at high speeds while still maintaining low power consumption and cost. The analog input bandwidth of 75 MHz (typ) makes this device an excellent choice for undersampling applications. Internal resistors are provided to generate 2-V full-scale reference voltages from a 5-V supply, thereby reducing external components. The digital outputs can be placed in a high impedance mode. The TLC5540 requires only a single 5-V supply for operation.

**NS PACKAGE
(TOP VIEW)**



AVAILABLE OPTIONS

T _A	NS PACKAGE
0°C to 70°C	TLC5540CNSLE
–40°C to 85°C	TLC5540INSLE

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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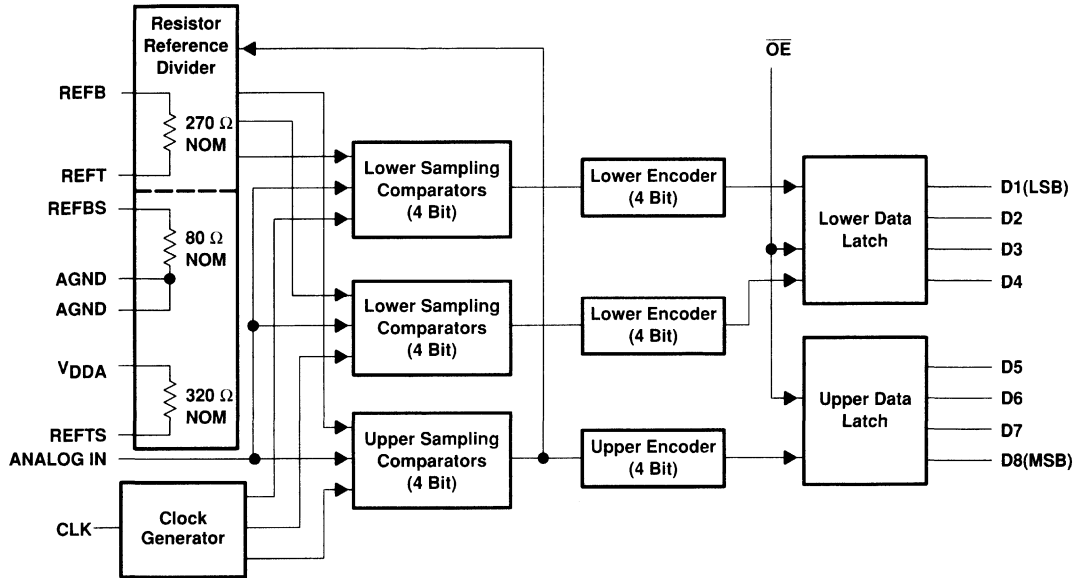
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TLC5540

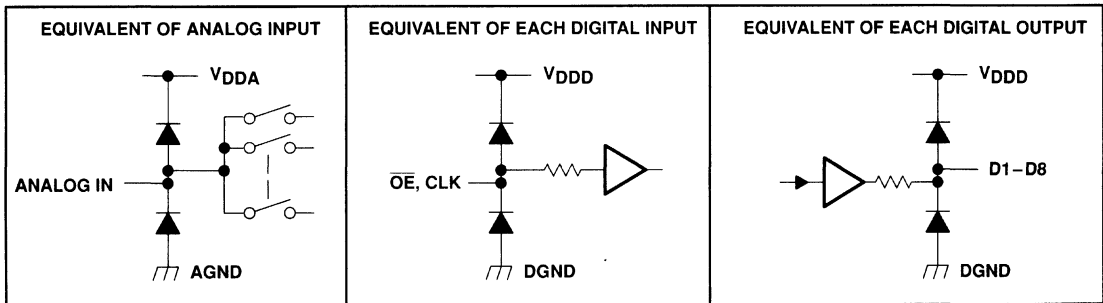
8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS105B – JANUARY 1995 – REVISED APRIL 1996

functional block diagram



schematics of inputs and outputs



TLC5540

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS105B – JANUARY 1995 – REVISED APRIL 1996

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	20, 21		Analog ground
ANALOG IN	19	I	Analog input
CLK	12	I	Clock input
DGND	2, 24		Digital ground
D1–D8	3–10	O	Digital data out. D1:LSB, D8:MSB
OE	1	I	Output enable. When OE = L, data is enabled. When OE = H, D1–D8 is high impedance.
VDDA	14, 15, 18		Analog VDD
VDDD	11, 13		Digital VDD
REFB	23	I	ADC reference voltage in (bottom)
REFBS	22		Reference voltage (bottom). When using the internal voltage divider to generate a nominal 2-V reference, the REFBS terminal is shorted to the REFB terminal and the REFTS terminal is shorted to the REFT terminal (see Figure 13 and Figure 14).
REFT	17	I	Reference voltage in (top)
REFTS	16		Reference voltage (top). When using the internal voltage divider to generate a nominal 2-V reference, the REFTS terminal is shorted to the REFT terminal and the REFBS terminal is shorted to the REFB terminal (see Figure 13 and Figure 14).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{DDA} , V _{DDD}	7 V
Reference voltage input range, V _I (REFT), V _I (REFB), V _I (REFBS), V _I (REFTS)	AGND to V _{DDA}
Analog input voltage range, V _I (ANLG)	AGND to V _{DDA}
Digital input voltage range, V _I (DGTL)	DGND to V _{DDD}
Digital output voltage range, V _O (DGTL)	DGND to V _{DDD}
Operating free-air temperature range, T _A : TLC5540C	0°C to 70°C
TLC5540I	–40°C to 85°C
Storage temperature range, T _{stg}	–55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



TLC5540

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS105B – JANUARY 1995 – REVISED APRIL 1996

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V _{DDA} – AGND	4.75	5	5.25	V
	V _{DDD} – AGND	4.75	5	5.25	
	AGND – DGND	–100	0	100	mV
Reference input voltage (top), V _{I(REFT)}		V _{I(REFB)} +1.8	V _{I(REFB)} +2	V _{DDA}	V
Reference input voltage (bottom), V _{I(REFB)}		0	0.6	V _{I(REFT)} –1.8	V
Analog input voltage range, V _{I(ANLG)} (see Note 1)		V _{I(REFB)}		V _{I(REFT)}	V
Full scale voltage, V _{I(REFT)} – V _{I(REFB)}		1.8		5	V
High-level input voltage, V _{IH}		4			V
Low-level input voltage, V _{IL}				1	V
Pulse duration, clock high, t _{w(H)}		12.5			ns
Pulse duration, clock low, t _{w(L)}		12.5			ns
Operating free-air temperature, T _A	TLC5540C	0		70	°C
	TLC5540I	–40		85	°C

NOTE 1: $1.8\text{ V} \leq V_{I(REFT)} - V_{I(REFB)} < V_{DD}$



TLC5540

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS105B – JANUARY 1995 – REVISED APRIL 1996

electrical characteristics at $V_{DD} = 5\text{ V}$, $V_{I(REFT)} = 2.6\text{ V}$, $V_{I(REFB)} = 0.6\text{ V}$, $f_s = 40\text{ MSPS}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
E _L	Linearity error, integral	f _s = 40 MSPS, V _I = 0.6 V to 2.6 V	T _A = 25°C		±0.6	±1	LSB
			T _A = MIN to MAX			±1	
E _D	Linearity error, differential		T _A = 25°C		±0.3	±0.75	
			T _A = MIN to MAX			±1	
	Self bias (1), V _{RB}	Short REFB to REFBS	See Figure 13	0.57	0.61	0.65	V
	Self bias (1), V _{RT}	Short REFT to REFTS		2.47	2.63	2.80	
	Self bias (2), V _{RB}	Short REFB to AGND	See Figure 14	AGND			
	Self bias (2), V _{RT}	Short REFT to REFTS		2.18	2.29	2.4	
I _{ref}	Reference-voltage current	V _{I(REFT)} – V _{I(REFB)} = 2 V		5.2	7.5	12	mA
R _{ref}	Reference-voltage resistor	Between REFT and REFB terminals		165	270	350	Ω
C _i	Analog input capacitance	V _{I(ANLG)} = 1.5 V + 0.07 V _{rms}			4		pF
E _{ZS}	Zero-scale error	V _{I(REFT)} – V _{I(REFB)} = 2 V		-18	-43	-68	mV
E _{FS}	Full-scale error			-25	0	25	
I _{IH}	High-level input current	V _{DD} = 5.25 V,	V _{IH} = V _{DD}			5	μA
I _{IL}	Low-level input current	V _{DD} = 5.25 V,	V _{IL} = 0			5	
I _{OH}	High-level output current	$\overline{\text{OE}}$ = GND,	V _{DD} = 4.75 V, V _{OH} = V _{DD} – 0.5 V	-1.5			mA
I _{OL}	Low-level output current	$\overline{\text{OE}}$ = GND,	V _{DD} = 4.75 V, V _{OL} = 0.4 V	2.5			
I _{OZH(kg)}	High-level high-impedance-state output leakage current	$\overline{\text{OE}}$ = V _{DD} ,	V _{DD} = 5.25, V _{OH} = V _{DD}			16	μA
I _{OZL(kg)}	Low-level high-impedance-state output leakage current	$\overline{\text{OE}}$ = V _{DD} ,	V _{DD} = 4.75, V _{OL} = 0			16	
I _{DD}	Supply current	f _s = 40 MSPS, C _L ≤ 25 pF,	NTSC‡ ramp wave input, See Note 2		17	27	mA

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

‡ National Television System Committee

NOTE 2: Supply current specification does not include I_{ref}.

TLC5540

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS105B – JANUARY 1995 – REVISED APRIL 1996

operating characteristics at $V_{DD} = 5\text{ V}$, $V_{RT} = 2.6\text{ V}$, $V_{RB} = 0.6\text{ V}$, $f_s = 40\text{ MSPS}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
f_s	Maximum conversion rate	$T_A = \text{MIN to MAX}$	40			MSPS
f_s	Minimum conversion rate	$T_A = \text{MIN to MAX}$		5		MSPS
BW	Analog input full-power bandwidth	At -3 dB, $V_I(\text{ANLG}) = 2 V_{pp}$		75		MHz
t_{pd}	Delay time, digital output	$C_L \leq 10\text{ pF}$ (see Note 3)		9	15	ns
t_{PHZ}	Disable time, output high to hi-z	$C_L \leq 15\text{ pF}$, $I_{OH} = -4.5\text{ mA}$			20	ns
t_{PLZ}	Disable time, output low to hi-z	$C_L \leq 15\text{ pF}$, $I_{OL} = 5\text{ mA}$			20	ns
t_{PZH}	Enable time, hi-z to output high	$C_L \leq 15\text{ pF}$, $I_{OH} = -4.5\text{ mA}$			15	ns
t_{PZL}	Enable time, hi-z to output low	$C_L \leq 15\text{ pF}$, $I_{OL} = 5\text{ mA}$			15	ns
	Differential gain	NTSC 40 IRE‡ modulation wave, $f_s = 14.3\text{ MSPS}$		1%		
	Differential phase			0.7		degrees
t_{AJ}	Aperture jitter time			30		ps
$t_{d(s)}$	Sampling delay time			4		ns
SNR	Signal-to-noise ratio	$f_s = 20\text{ MSPS}$	$f_j = 1\text{ MHz}$		47	dB
			$f_j = 3\text{ MHz}$	44	47	
			$f_j = 6\text{ MHz}$		46	
			$f_j = 10\text{ MHz}$		45	
		$f_s = 40\text{ MSPS}$	$f_j = 3\text{ MHz}$	45.2		
			$f_j = 6\text{ MHz}$	42	44	
ENOB	Effective number of bits	$f_s = 20\text{ MSPS}$	$f_j = 1\text{ MHz}$		7.64	Bits
			$f_j = 3\text{ MHz}$		7.61	
			$f_j = 6\text{ MHz}$		7.47	
			$f_j = 10\text{ MHz}$		7.16	
		$f_s = 40\text{ MSPS}$	$f_j = 3\text{ MHz}$		7	
			$f_j = 6\text{ MHz}$		6.8	
THD	Total harmonic distortion	$f_s = 20\text{ MSPS}$	$f_j = 1\text{ MHz}$		43	dBc
			$f_j = 3\text{ MHz}$	35	42	
			$f_j = 6\text{ MHz}$		41	
			$f_j = 10\text{ MHz}$		38	
		$f_s = 40\text{ MSPS}$	$f_j = 3\text{ MHz}$		40	
			$f_j = 6\text{ MHz}$		38	
Spurious free dynamic range		$f_s = 20\text{ MSPS}$, $f_j = 3\text{ MHz}$	41	46		dBc
		$f_s = 40\text{ MSPS}$, $f_j = 3\text{ MHz}$		42		dBc

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

‡ Institute of Radio Engineers

NOTE 3: C_L includes probe and jig capacitance.



TLC5540

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS105B – JANUARY 1995 – REVISED APRIL 1996

PARAMETER MEASUREMENT INFORMATION

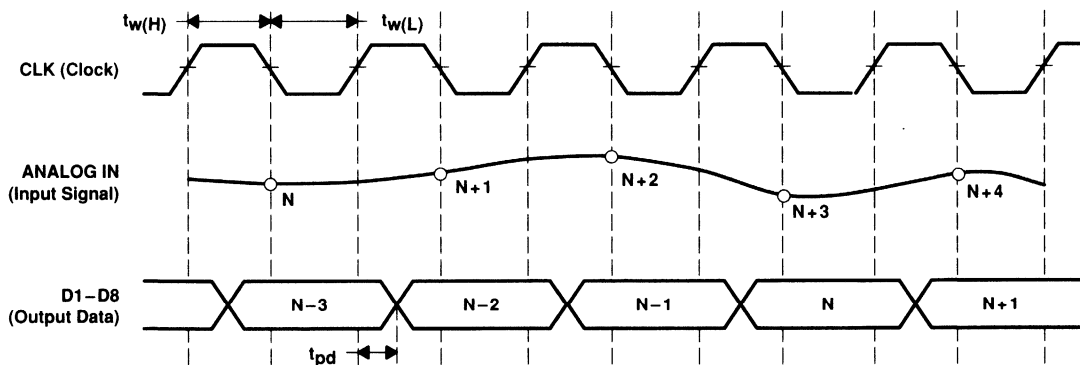


Figure 1. I/O Timing Diagram

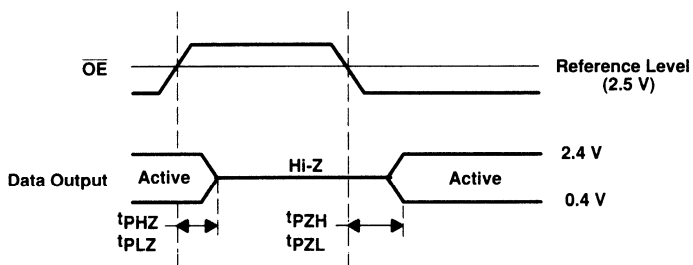


Figure 2. I/O Timing Diagram

TLC5540

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS105B – JANUARY 1995 – REVISED APRIL 1996

TYPICAL CHARACTERISTICS

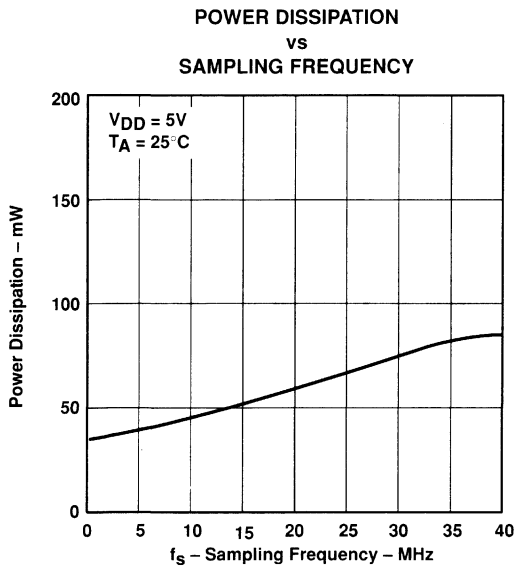


Figure 3

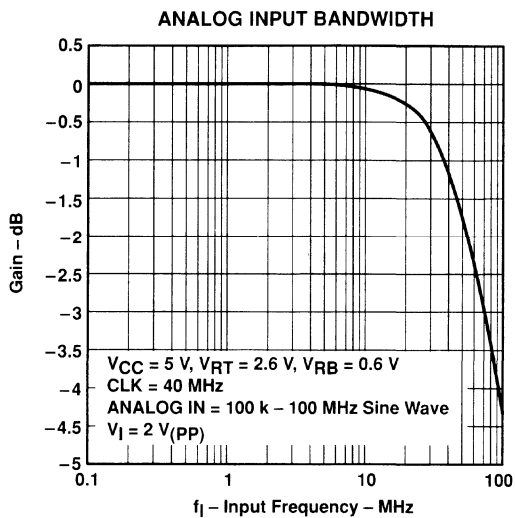


Figure 4

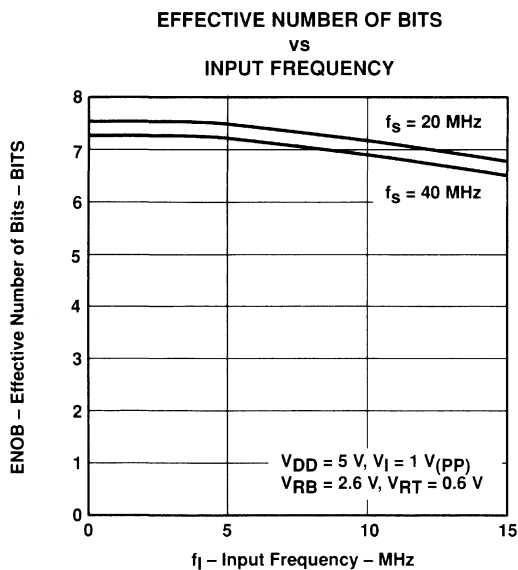


Figure 5

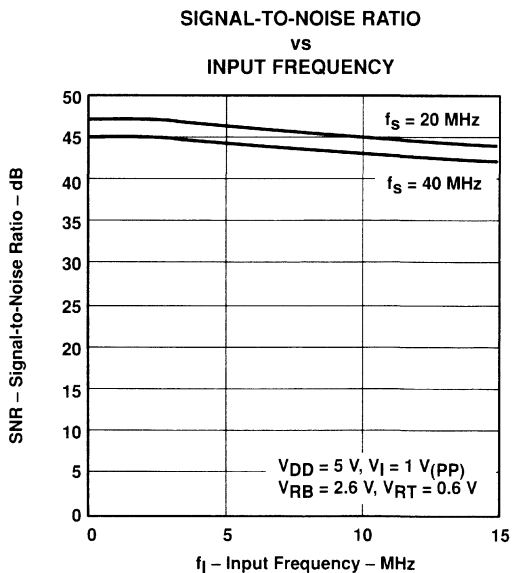
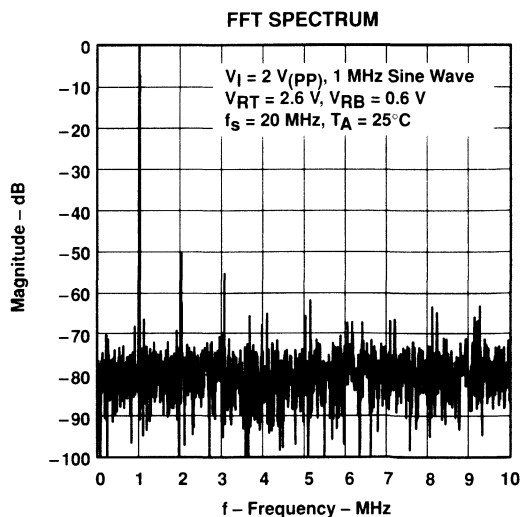
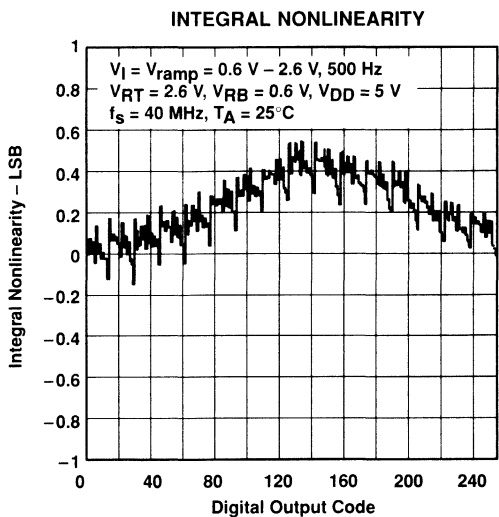
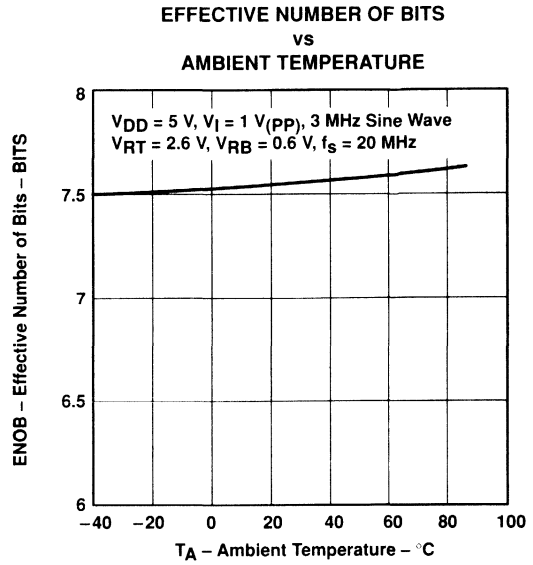
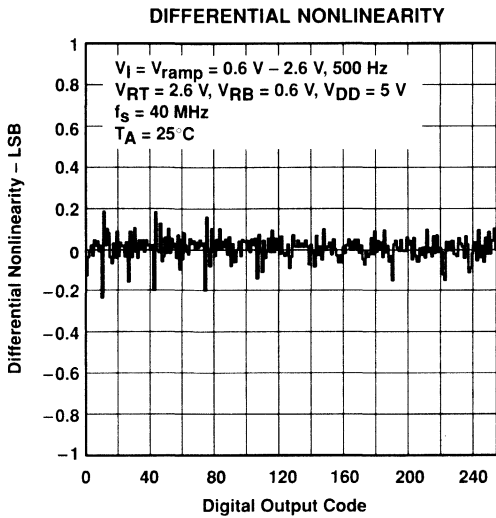


Figure 6

TLC5540 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS105B – JANUARY 1995 – REVISED APRIL 1996

TYPICAL CHARACTERISTICS



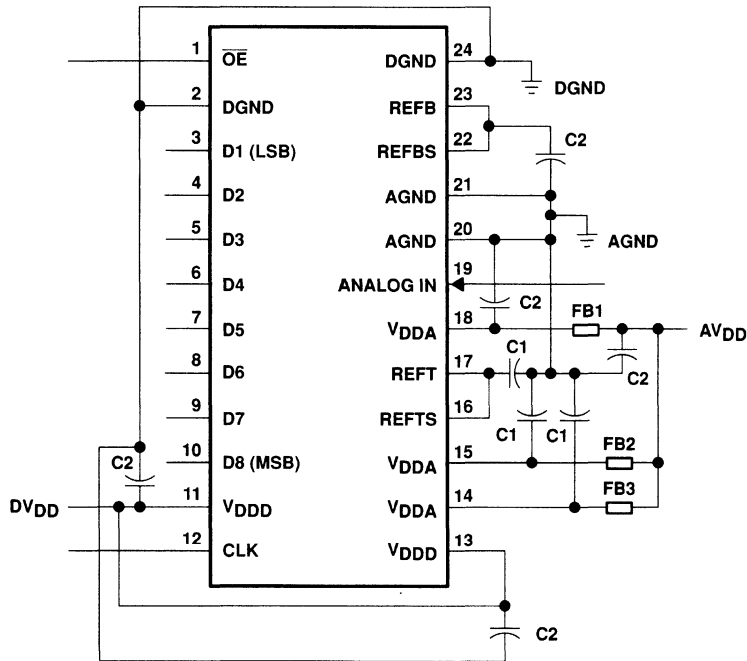
TLC5540 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS105B – JANUARY 1995 – REVISED APRIL 1996

APPLICATION INFORMATION

grounding and power supply considerations

As with most high performance A/D converters, separate analog and digital supply and grounding terminals are provided on the package. This is done to allow the sensitive analog currents to be separated from the noisy digital switching currents. All analog circuitry should be returned to analog ground and all digital currents should be returned to digital ground. A low impedance connection should be made between the two grounds at the power supply or closer when needed to keep the impedance minimal. It is critical to keep the potential of AGND equal to DGND. When a difference in potential exists, then common mode currents develop in the ADC which result in converter noise. The low impedance connection between AGND and DGND minimize this potential difference. It is recommended that switching power supplies be avoided for supply to the ADC. Low noise linear power supplies provide the best operation. V_{DDA} and V_{DDD} should be decoupled as close as possible to the integrated circuit (IC) with a 0.1 μF capacitor. The capacitors chosen should have good characteristics for decoupling high frequencies. Ceramic chip capacitors typically prove the most beneficial. Figure 11 shows power and ground connections using ferrite beads for filtering.



LOCATION	DESCRIPTION
C1	> 0.02- μF capacitor
C2	< 10- μF capacitor
FB1, FB2, FB3	Ferrite beads, C type

Figure 11. AV_{DD} , DV_{DD} , AGND, and DGND Connections

TLC5540 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS105B – JANUARY 1995 – REVISED APRIL 1996

APPLICATION INFORMATION

printed circuit board (PCB) layout considerations

When designing a circuit that includes high-speed digital and precision analog signals such as a high speed ADC, PCB layout is a key component to achieving the desired performance. The following recommendations should be considered during the prototyping and PCB design phase:

- Separate analog and digital circuitry physically to help eliminate capacitive coupling and crosstalk. When separate analog and digital ground planes are used, the digital ground and power planes should be several layers from the analog signals and power plane to avoid capacitive coupling.
- Full ground planes should be used. Do not use individual etches to return analog and digital currents or partial ground planes. For prototyping, breadboards should be constructed with copper clad boards to maximize ground plane.
- The conversion clock, CLK, should be terminated properly to reduce overshoot and ringing. Any jitter on the conversion clock degrades ADC performance. A high-speed CMOS buffer such as a 74ACT04 or 74AC04 positioned close to the CLK terminal can improve performance.
- Minimize all etch runs as much as possible by placing components very close together. It also proves beneficial to place the ADC in a corner of the PCB nearest to the I/O connector analog terminals.
- It is recommended to place the digital output data latch (if used) as close to the TLC5540 as possible to minimize capacitive loading. If D0 through D7 must drive large capacitive loads, internal ADC noise may be experienced.



TLC5540

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS105B – JANUARY 1995 – REVISED APRIL 1996

PRINCIPLES OF OPERATION

functional description

The TLC5540 uses a modified semiflash architecture as shown in the functional block diagram. The four most significant bits (MSBs) of every output conversion result are produced by the upper comparator block CB1. The four least significant bits (LSBs) of each alternate output conversion result are produced by the lower comparator blocks CB-A and CB-B in turn (see Figure 12).

The reference voltage that is applied to the lower comparator resistor string is one sixteenth of the amplitude of the reference applied to the upper comparator resistor string. The sampling comparators of the lower comparator block require more time to sample the lower voltages of the reference and residual input voltage. By applying the residual input voltage to alternate lower comparator blocks, each comparator block has twice as much time to sample and convert as would be the case if only one lower comparator block were used.

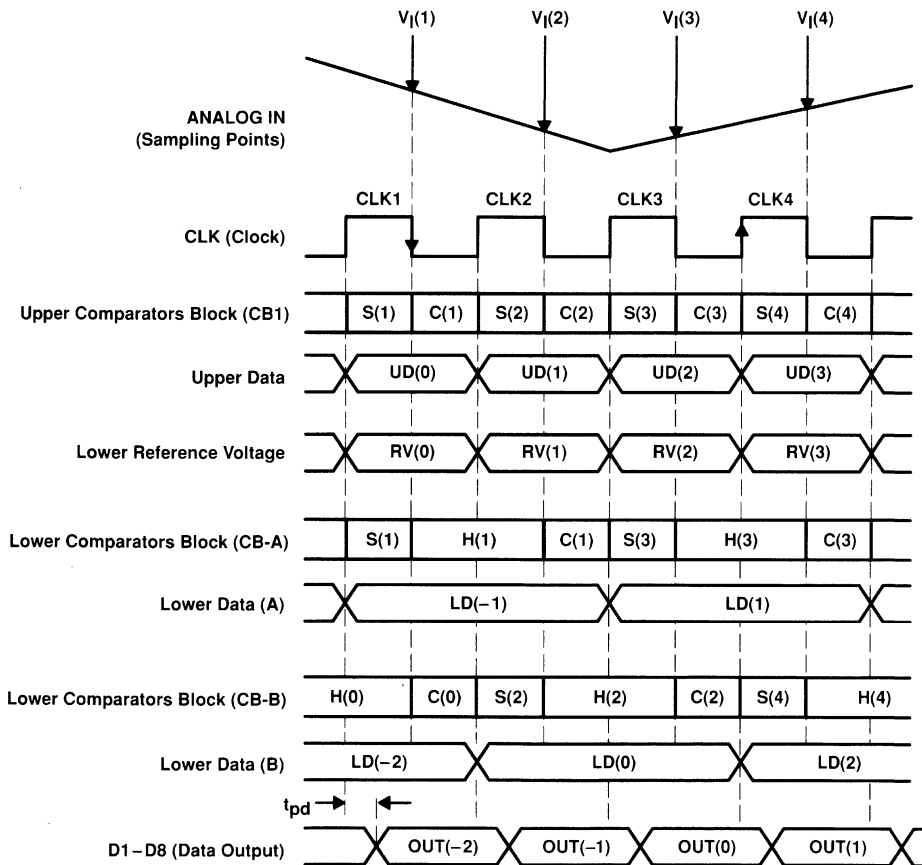


Figure 12. Internal Functional Timing Diagram

This conversion scheme, which reduces the required sampling comparators by 30 percent compared to standard semiflash architectures, achieves significantly higher sample rates than the conventional semiflash conversion method.

TLC5540 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS105B – JANUARY 1995 – REVISED APRIL 1996

PRINCIPLES OF OPERATION

functional description (continued)

The MSB comparator block converts on the falling edge of each applied clock cycle. The LSB comparator blocks CB-A and CB-B convert on the falling edges of the first and second following clock cycles, respectively. The timing diagram of the conversion algorithm is shown in Figure 12.

analog input operation

The analog input stage to the TLC5540 is a chopper-stabilized comparator and is equivalently shown below:

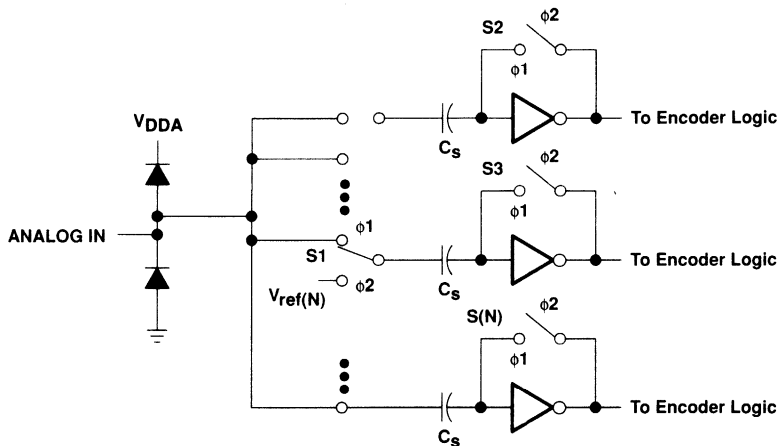


Figure 13. External Connections for Using the Internal Reference Resistor Divider

Figure 13 depicts the analog input for the TLC5540. The switches shown are controlled by two internal clocks, $\phi 1$ and $\phi 2$. These are nonoverlapping clocks that are generated from the CLK input. During the sampling period, $\phi 1$, S1 is closed and the input signal is applied to one side of the sampling capacitor, C_s . Also during the sampling period, S2 through S(N) are closed. This sets the comparator input to approximately 2.5 V. The delta voltage is developed across C_s . During the comparison phase, $\phi 2$, S1 is switched to the appropriate reference voltage for the bit value N. S2 is opened and $V_{ref(N)} - VC_s$ toggles the comparator output to the appropriate digital 1 or 0. The small resistance values for the switch, S1, and small value of the sampling capacitor combine to produce the wide analog input bandwidth of the TLC5540. The source impedance driving the analog input of the TLC5540 should be less than 100 Ω across the range of input frequency spectrum.

reference inputs – REFB, REFT, REFBS, REFTS

The range of analog inputs that can be converted are determined by REFB and REFT, REFT being the maximum reference voltage and REFB being the minimum reference voltage. The TLC5540 is tested with REFT = 2.6 V and REFB = 0.6 V producing a 2-V full-scale range. The TLC5540 can operate with REFT – REFB = 5 V, but the power dissipation in the reference resistor increases significantly (93 mW nominally). It is recommended that a 0.1 μ F capacitor be attached to REFB and REFT whether using externally or internally generated voltages.

TLC5540

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS105B – JANUARY 1995 – REVISED APRIL 1996

PRINCIPLES OF OPERATION

internal reference voltage conversion

Three internal resistors allow the device to generate an internal reference voltage. These resistors are brought out on terminals V_{DDA} , REFTS, REFT, REFB, REFBS, and AGND. Two different bias voltages are possible without the use of external resistors.

Internal resistors are provided to develop $REFT = 2.6\text{ V}$ and $REFB = 0.6\text{ V}$ (bias option one) with only two external connections. This is developed with a 3-resistor network connected to V_{DDA} . When using this feature, connect REFT to REFTS and connect REFB to REFBS. For applications where the variance associated with V_{DDA} is acceptable, this internal voltage reference saves space and cost (see Figure 14).

A second internal bias option (bias two option) is shown in Figure 15. Using this scheme $REFB = AGND$ and $REFT = 2.28\text{ V}$ nominal. These bias voltage options can be used to provide the values listed in the following table.

Table 1. Bias Voltage Options

BIAS OPTION	BIAS VOLTAGE		
	V_{RB}	V_{RT}	$V_{RT} - V_{RB}$
1	0.61	2.63	2.02
2	AGND	2.28	2.28

To use the internally-generated reference voltage, terminal connections should be made as shown in Figure 14 or Figure 15. The connections in Figure 14 provide the standard video 2-V reference.

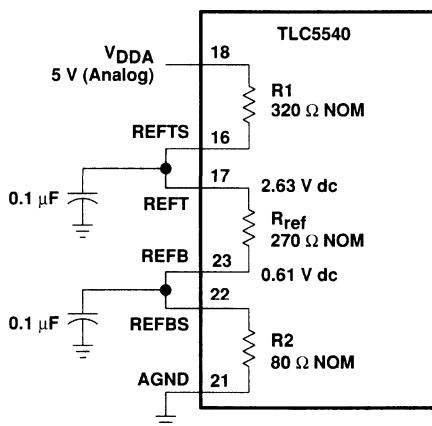


Figure 14. External Connections Using the Internal Bias One Option

TLC5540

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS105B – JANUARY 1995 – REVISED APRIL 1996

PRINCIPLES OF OPERATION

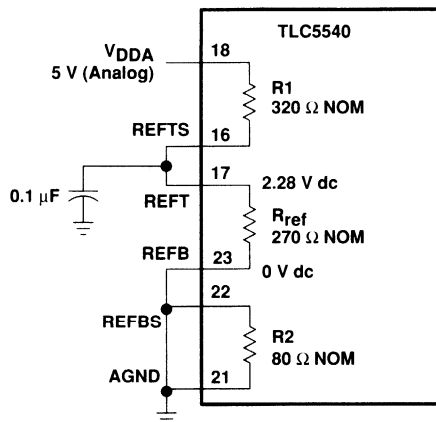


Figure 15. External Connections Using the Internal Bias Two Option

functional operation

Table 2 shows the TLC5540 functions.

Table 2. Functional Operation

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB							LSB
$V_{ref(T)}$	255	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	128	1	0	0	0	0	0	0	0
•	127	0	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
$V_{ref(B)}$	0	0	0	0	0	0	0	0	0

TLC5733A
20 MSPS 3-CHANNEL ANALOG-TO-DIGITAL CONVERTER
WITH HIGH-PRECISION CLAMP
SLAS104A – JULY 1995 – REVISED NOVEMBER 1996

- 3-Channel CMOS ADC
- 5-V Single-Supply Operation or 5-V Analog Supply with Digital Supply from 2.7 V to 5.25 V
- 8-Bit Resolution
- Differential Linearity Error . . . ± 0.5 LSB Max
- Linearity Error . . . ± 0.75 LSB Max
- Maximum Conversion Rate
20 Megasamples per Second (MSPS) Min
- Analog Input Voltage Range
 $2 V_{I(PP)}$ Min
- 64-Pin Shrink QFP Package
- Analog Input Bandwidth . . . >14 MHz
- Suitable for YUV or RGB Applications
- Digital Clamp Optimized for NTSC or PAL YUV Component
- High-Precision Clamp . . . ± 1 LSB
- Automatic Clamp Pulse Generator
- Output-Data Format Multiplexer
- Low Power Consumption

description

The TLC5733A is a 3-channel 8-bit semiflash analog-to-digital converter (ADC) that operates from a single 5-V power supply. It converts a wide-band analog signal (such as a video signal) to digital data at sampling rates up to 20 MSPS minimum. The TLC5733A contains a feed-back type high-precision clamp circuit for each ADC channel for video (YUV) applications and a clamp pulse generator that detects COMPOSITE SYNC† pulses automatically. A clamp pulse can also be supplied externally. The output-data format multiplexer selects a ratio of Y:U:V of 4:4:4, 4:1:1, or 4:2:2. For RGB applications, the 4:4:4 output format without clamp function can be used. The TLC5733A is characterized for operation from -20°C to 75°C .

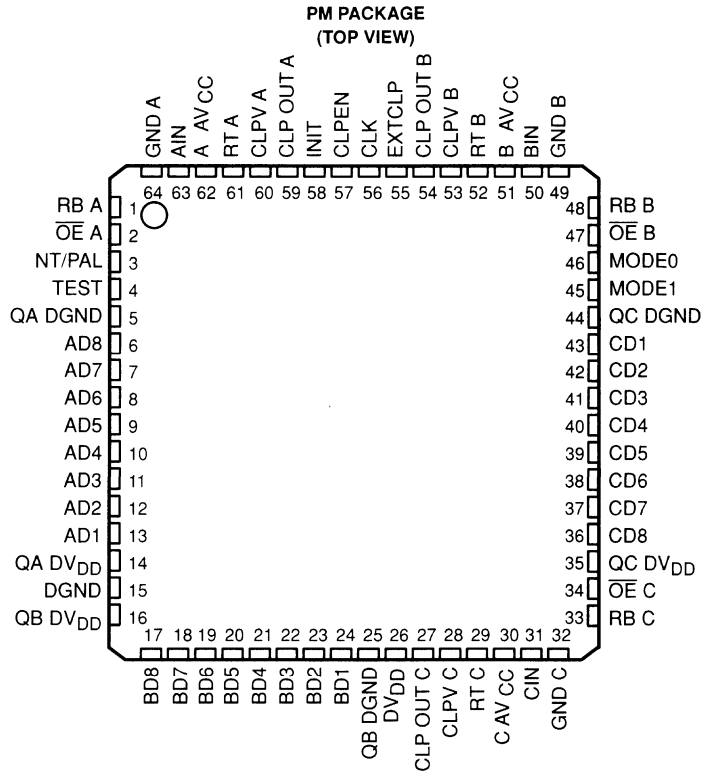
AVAILABLE OPTIONS

T _A	PACKAGE
	-20°C to 75°C

† COMPOSITE SYNC refers to the externally generated synchronizing signal that is a combination of vertical and horizontal sync information used in display and TV systems.

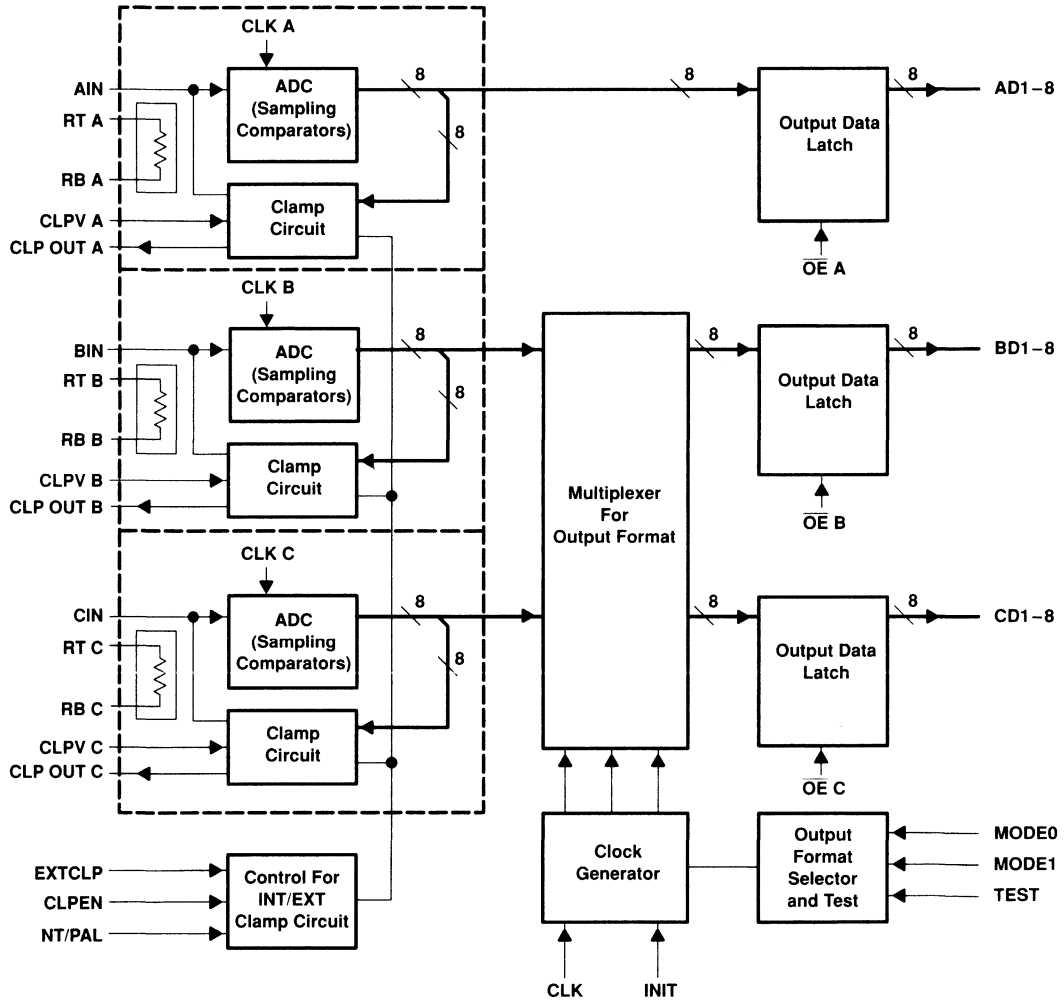
TLC5733A
20 MSPS 3-CHANNEL ANALOG-TO-DIGITAL CONVERTER
WITH HIGH-PRECISION CLAMP

SLAS104A – JULY 1995 – REVISED NOVEMBER 1996



TLC5733A
20 MSPS 3-CHANNEL ANALOG-TO-DIGITAL CONVERTER
WITH HIGH-PRECISION CLAMP
 SLAS104A – JULY 1995 – REVISED NOVEMBER 1996

functional block diagram



TLC5733A
20 MSPS 3-CHANNEL ANALOG-TO-DIGITAL CONVERTER
WITH HIGH-PRECISION CLAMP

SLAS104A – JULY 1995 – REVISED NOVEMBER 1996

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
A AV _{CC}	62	I	Analog supply voltage of ADC A
AD8–AD1	6–13	O	Data output of ADC A (LSB: AD1, MSB:AD8)
AIN	63	I	Analog input of ADC A
B AV _{CC}	51	I	Analog supply voltage of ADC B
BD8–BD1	17–24	O	Data output of ADC B (LSB: BD1, MSB:BD8)
BIN	50	I	Analog input of ADC B
C AV _{CC}	30	I	Analog supply voltage of ADC C
CD8–CD1	36–43	O	Data output of ADC C (LSB:CD1, MSB: CD8) When MODE0 = L, MODE1 = L, CD8 outputs MSB flag of BD8–BD5 When MODE0 = L, MODE1 = L, CD7 outputs MSB flag of BD8–BD5 When MODE0 = L, MODE1 = H, CD8 outputs B channel flag of CD8–BD1 When MODE0 = L, MODE1 = H, CD8 outputs B channel flag of CD8–BD1
CIN	31	I	Analog input of ADC C
CLK	56	I	Clock input. The clock frequency is normally 4 × the frequency subcarrier (fsc) for most video systems (see Table 3). The nominal clock frequency is 14.31818 MHz for National Television System Committee (NTSC) and 17.745 MHz for phase alteration line (PAL).
CLPEN	57	I	Clamp enable. When using an internal clamp pulse, CLPEN should be high. When using an external clamp pulse, CLPEN should be low.
CLP OUT A	59	O	Clamping bias current of ADC A. A resistor-capacitor combination that sets the clamp timing.
CLP OUT B	54	O	Clamping bias current of ADC B. A resistor-capacitor combination that sets the clamp timing.
CLP OUT C	27	O	Clamping bias current of ADC C. A resistor-capacitor combination that sets the clamp timing.
CLPV A	60	O	Clamping level of ADC A. A capacitor is connected to CLPV A to set the clamp timing. The clamp level at CLPV A is connected to an output code of 16 (0010000).
CLPV B	53	O	Clamping level of ADC B. A capacitor is connected to CLPV B to set the clamp timing. The clamp level at CLPV B is connected to an output code of 128 (1000000).
CLPV C	28	O	Clamping level of ADC C. A capacitor is connected to CLPV C to set the clamp timing. The clamp level at CLPV C is connected to an output code of 128 (1000000).
DGND	15	I	Digital ground
DV _{DD}	26	I	Digital supply voltage
EXTCLP	55	I	External clamp pulse input. When EXTCLP and CLPEN are low, the internal clamp circuit cannot be used. The external clamp pulse when used is active high.
GND A	64	I	Ground of ADC A
GND B	49	I	Ground of ADC B
GND C	32	I	Ground of ADC C
INIT	58	I	Output initialized. The output data is synchronous when INIT is taken high from low. INIT is a control terminal that allows the external system to initialize the TLC5733A data conversion cycle. INIT is usually used at power up or system reset.
MODE0	46	I	Output format mode selector 0. When MODE1 is low and MODE0 is low, output data format1 is selected. When MODE1 is low and MODE0 is high, output data format2 is selected. When MODE1 is high and MODE0 is low, output data format3 is selected. A high level on MODE1 and a high level on MODE0 is not used.
MODE1	45	I	Output format mode selector 1. When MODE1 is low and MODE0 is low, output data format1 is selected. When MODE1 is low and MODE0 is high, output data format2 is selected. When MODE1 is high and MODE0 is low, output data format3 is selected. A high level on MODE1 and a high level on MODE0 is not used.
NT/PAL	3	I	NTSC/PAL control. NTSC/PAL should be low for NTSC and high for PAL.
OE A	2	I	Output enable A. OE A enables the output of ADC A.
OE B	47	I	Output enable B. OE B enables the output of ADC B.



TLC5733A
20 MSPS 3-CHANNEL ANALOG-TO-DIGITAL CONVERTER
WITH HIGH-PRECISION CLAMP
 SLAS104A – JULY 1995 – REVISED NOVEMBER 1996

Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
OE C	34	I	Output enable C. OE C enables the output of ADC C.
QA DGND	5	I	Digital ground for output of ADC A
QA DV _{DD}	14	I	Digital supply voltage for output of ADC A
QB DGND	25	I	Digital ground for output of ADC B
QB DV _{DD}	16	I	Digital supply voltage for output of ADC B
QC DGND	44	I	Digital ground for output of ADC C
QC DV _{DD}	35	I	Digital supply voltage for output of ADC C
RB A	1	I	Bottom reference voltage of ADC A. The nominal externally applied dc voltage between RT A and RB A is 2 V for video signals.
RB B	48	I	Bottom reference voltage of ADC B. The nominal externally applied dc voltage between RT B and RB B is 2 V for video signals.
RB C	33	I	Bottom reference voltage of ADC C. The nominal externally applied dc voltage between RT C and RB C is 2 V for video signals.
RT A	61	I	Top reference voltage of ADC A. The nominal externally applied dc voltage between RT A and RB A is 2 V for video signals.
RT B	52	I	Top reference voltage of ADC B. The nominal externally applied dc voltage between RT B and RB B is 2 V for video signals.
RT C	29	I	Top reference voltage of ADC C. The nominal externally applied dc voltage between RT C and RB C is 2 V for video signals.
TEST	4	I	Test. TEST should be tied low when using this device.

absolute maximum ratings†

Supply voltage, V_{CC} , V_{DD}	7 V
Reference voltage input range, $V_{ref}(RT A)$, $V_{ref}(RT B)$, $V_{ref}(RT C)$, $V_{ref}(RB A)$, $V_{ref}(RB B)$, $V_{ref}(RB C)$	AGND to V_{CC}
Analog input voltage range	AGND to V_{CC}
Digital input voltage range, V_I	DGND to V_{DD}
Digital output voltage range, V_O	DGND to V_{DD}
Operating free-air temperature range, T_A	–20°C to 75°C
Storage temperature range, T_{stg}	–55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



TLC5733A

20 MSPS 3-CHANNEL ANALOG-TO-DIGITAL CONVERTER WITH HIGH-PRECISION CLAMP

SLAS104A – JULY 1995 – REVISED NOVEMBER 1996

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage‡	V _{CC} – AGND	4.75	5	5.25	V
	V _{DD} – DGND	2.7	5	5.25	
	AGND – DGND	–100	0	100	mV
Reference input voltage, V _{ref} (RT A), V _{ref} (RT B), V _{ref} (RT C)		V _{ref} (RB)+2		V _{CC}	V
Reference input voltage, V _{ref} (RB A), V _{ref} (RB B), V _{ref} (RB C)		0		V _{ref} (RT)–2	V
Analog input voltage, V _I		0		V _{ref} (RT)	V
High-level input voltage, V _{IH}		2			V
Low-level input voltage, V _{IL}				0.8	V
High-level pulse duration, t _w (H)		25			ns
Low-level pulse duration, t _w (L)		25			ns
Setup time for INIT input, t _{SU1}		5			ns
Operating free-air temperature range, T _A		–20		75	°C

‡ Within the electrical and operating characteristics table, when the term V_{DD} is used, all XD_{VDD} terminals are tied together, and when the term V_{CC} is used, all XA_{VCC} terminals are tied together.

electrical characteristics at V_{DD} = 2.7 V to 5.25 V, V_{CC} = 5 V, V_{ref}(RT) = 2.5 V, V_{ref}(BB) = 0.5 V, f(CLK) = 20 MHz, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Clamp level accuracy			±1		LSB	
R _{ref}	Reference voltage resistor	Measured between RT and RB		160	220 350	Ω
C _i	Analog input capacitance	V _I = 1.5 V + 0.07 V _{rms}		16		pF
I _{IH}	High-level input current	V _{DD} = MAX†, V _{IH} = V _{DD} , V _{CC} = 5V		5		μA
I _{IL}	Low-level input current	V _{DD} = MAX†, V _{IL} = 0, V _{CC} = 5V		5		
V _{OH}	High-level output voltage	All DV _{DD} terminals = 2.7 V to 5.25 V, I _{OH} = –1 mA		DV _{DD} – 0.7 V		V
V _{OL}	Low-level output voltage	All DV _{DD} terminals = 2.7 V to 5.25 V, I _{OL} = 2 mA		0.8		
I _{OH} (I _{kg})	High-level output leakage current	V _{DD} = MAX†, V _{OH} = V _{DD} , V _{CC} = 5V		16		μA
I _{OL} (I _{kg})	Low-level output leakage current	V _{DD} = MIN†, V _{OL} = 0, V _{CC} = 5V		16		
I _{CC}	Supply current	f _c = 20 MSPS, NTSC ramp wave input		50	75	mA

† Conditions marked MIN or MAX are as stated in recommended operating conditions.



TLC5733A
20 MSPS 3-CHANNEL ANALOG-TO-DIGITAL CONVERTER
WITH HIGH-PRECISION CLAMP

SLAS104A – JULY 1995 – REVISED NOVEMBER 1996

operating characteristics at $V_{DD} = 2.7\text{ V to }5.25\text{ V}$, $V_{CC} = 5\text{ V}$, $V_{ref(RT)} = 2.5\text{ V}$, $V_{ref(RB)} = 0.5\text{ V}$, $f_{(CLK)} = 20\text{ MHz}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E _{ZS}	Zero-scale error	$V_{ref} = REFT - REF B = 2\text{ V}$	-18	-43	-68	mV
E _{FS}	Full-scale error	$V_{ref} = REFT - REF B = 2\text{ V}$	-20	0	20	mV
E _L	Linearity error	$f_{(CLK)} = 20\text{ MHz}$, $V_I = 0.5\text{ V to }2.5\text{ V}$		± 0.4	± 0.75	LSB
		$f_{(CLK)} = 20\text{ MHz}$, $T_A = -20^\circ\text{C to }75^\circ\text{C}$, $V_I = 0.5\text{ V to }2.5\text{ V}$		± 0.4	± 1	
E _D	Linearity error, differential	$f_{(CLK)} = 20\text{ MHz}$, $V_I = 0.5\text{ V to }2.5\text{ V}$		± 0.3	± 0.5	LSB
		$f_{(CLK)} = 20\text{ MHz}$, $T_A = -20^\circ\text{C to }75^\circ\text{C}$, $V_I = 0.5\text{ V to }2.5\text{ V}$		± 0.3	± 0.75	
f _c	Maximum conversion rate	$V_I = 0.5\text{ V} - 2.5\text{ V}$, $f_I = 1\text{-kHz ramp waveform}$	20			MSPS
BW	Analog input bandwidth	At -1 dB		14		MHz
t _{pd}	Digital output delay time	$C_L = 10\text{ pF}$		18	30	ns
	Differential gain	NTSC 40 IRE† modulation wave, $f_c = 14.3\text{ MSPS}$		1%		
	Differential phase	NTSC 40 IRE† modulation wave, $f_c = 14.3\text{ MSPS}$		0.7		deg
	Aperture jitter time			30		ps
	Sampling delay time			4		ns

† Institute of Radio Engineers

TLC5733A
20 MSPS 3-CHANNEL ANALOG-TO-DIGITAL CONVERTER
WITH HIGH-PRECISION CLAMP

SLAS104A – JULY 1995 – REVISED NOVEMBER 1996

detailed description

clamp function

The clamp function is optimized for a YUV video signal and has two clamp modes. The first mode uses the COMPOSITE SYNC signal as the input to the EXTCLP terminal to generate an internal clamp pulse and the second mode uses an externally generated clamp pulse as the input to the EXTCLP terminal.

In the first mode, the device detects false pulses in the COMPOSITE SYNC signal by monitoring the rising and falling edges of the COMPOSITE SYNC signal pulses. This monitoring prevents faulty operation caused by disturbances and missing pulses of the COMPOSITE SYNC signal input on EXTCLP and external spike noise. When fault pulses are detected, the device internally generates a train of clamp pulses at the proper positions (1H) by an internal 910-counter for NTSC and a 1136-counter for PAL. The device checks clamp pulses for 1H time and generates clamp pulses at correct positions when COMPOSITE SYNC pulses are in error in time.

The internal counter continually produces a horizontal sync period (1H) that is NTSC or PAL compatible as selected by the condition of the NT/PAL terminal.

clamp voltages and selection

Table 1 shows the clamping level during the clamp interval. Table 2 shows the selection of the internal or external clamp pulse. With either NTSC or PAL, the internal clamp pulse is always used.

Table 1. Clamp Level (Internal Connection Level)

CHANNEL OF ADC	OUTPUT CODE	APPLICATION
ADC A • V _{I(A)}	00010000	Y
ADC B • V _{I(B)}	10000000	(U, V)
ADC C • V _{I(C)}	10000000	(U, V)

Table 2. Clamp Level (Internal Connection Level)

CONDITION			FUNCTION (EACH ADC)	
CLPEN	EXTCLP	NT/PAL	INTERNAL CLAMP	CLAMP PULSE
L	⌋	Don't Care	Inactive	External clamp pulse
	L	Don't Care	Inactive	No clamping
H	COMPOSITE SYNC input	L	Active	Synchronous with NTSC
		H	Active	Synchronous with PAL

The clamp circuit is shown in Figure 6. The clamp voltage is stored on capacitor C2 during the back porch of the horizontal blanking period.

During the clamp pulse the input to channel A is clamped to:

$$V_C(A) = (16/256) \times (\text{voltage difference from terminal RT A to RB A})$$

$$V_C(B) = (128/256) \times (\text{voltage difference from terminal RT B to RB B})$$

$$V_C(C) = (128/256) \times (\text{voltage difference from terminal RT C to RB C})$$

COMPOSITE SYNC time monitoring

When CLPEN is high, COMPOSITE SYNC generates an internal clamp pulse on the horizontal blanking interval back porch. The TLC5733A has a timing window into which the horizontal sync tip must occur. There is a noise time window for the falling edge and one for the rising edge (see Figure 1, Figure 2, and Table 3).



correct COMPOSITE SYNC timing

The Noise Gate 1 signal provides the timing window for the COMPOSITE SYNC falling edge. After an interval A of 867 clocks for NTSC or 1075 for PAL from the last falling edge of COMPOSITE SYNC, Noise Gate 1 signal goes high for 43 clocks for NTSC or 61 clocks for PAL (interval B). The falling edge of the input signal to the EXTCLP terminal can occur at any time within this window to be a valid COMPOSITE SYNC falling edge.

The Noise Gate 2 signal provides the timing window for the COMPOSITE SYNC rising edge. On the falling edge of the horizontal sync tip, the internal logic generates Noise Gate 2 as a low signal for 58 clocks (interval C) for both NTSC and PAL and then returns to a high active state. At this time if the input to EXTCLP is still low, it is considered a valid COMPOSITE SYNC signal.

normal clamp pulse generation

On the rising edge of COMPOSITE SYNC, the internal logic generates an internal delay (interval D) and then generates the internal positive clamp pulse 54 clocks wide (interval F).

clamp operation with incorrect COMPOSITE SYNC timing

noise suppression

If the input to EXTCLP goes low prior to Noise Gate 1 going high (within 43 clocks for NTSC or 61 clocks for PAL of the normal 1H timing for the falling edge of COMPOSITE SYNC) then that input is not considered a valid COMPOSITE SYNC and is ignored.

If the input to EXTCLP is high when Noise Gate 2 goes to the high state, the input signal is considered noise and is ignored.

Therefore, the correct signal must be high for a maximum of 43 clocks for NTSC or 61 clocks for PAL, before the 1H timing, to be a valid sync signal. Also, the input to EXTCLP must be at least 58 clocks wide (interval C) to be valid.

This function of monitoring the timing eliminates spurious noise spikes from falsely synchronizing the system

timing error of COMPOSITE SYNC

The internal counter resets to zero on the first falling edge of COMPOSITE SYNC. After that time, if there is a missing COMPOSITE SYNC signal, then the internal logic waits an interval of 76 clocks (interval E) for NTSC or 93 for PAL from the counter zero count and then generates an internal clamp pulse 54 clocks wide (interval F).

This function maintains the synchronization pattern when COMPOSITE SYNC is not present.

summary of device operation with COMPOSITE SYNC

This internal timing allows the TLC5733A to correctly position the clamp pulse when an external COMPOSITE SYNC input:

- Is delayed with respect to the horizontal sync period
- Is early with respect to the horizontal sync period
- Is nonexistent during the horizontal sync period
- Has falling edge noise spikes within the horizontal sync period

The device operation is summarized as follows for these improper external clamp conditions:

- Under all four conditions on EXTCLP, the internal clamp generation circuit generates a clamp pulse at the proper time after the horizontal sync period as shown in Figure 1.
- The TLC5733A internal clamp circuit generates an internal clamp pulse each 1H time for the entire time interval that the COMPOSITE SYNC input is missing.

TLC5733A
20 MSPS 3-CHANNEL ANALOG-TO-DIGITAL CONVERTER
WITH HIGH-PRECISION CLAMP
 SLAS104A – JULY 1995 – REVISED NOVEMBER 1996

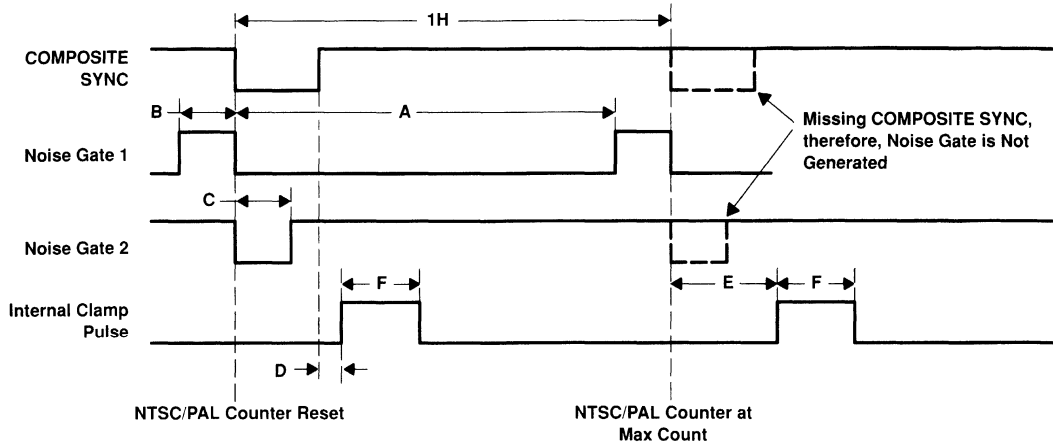


Figure 1. COMPOSITE SYNC and Internal Clamp Timing

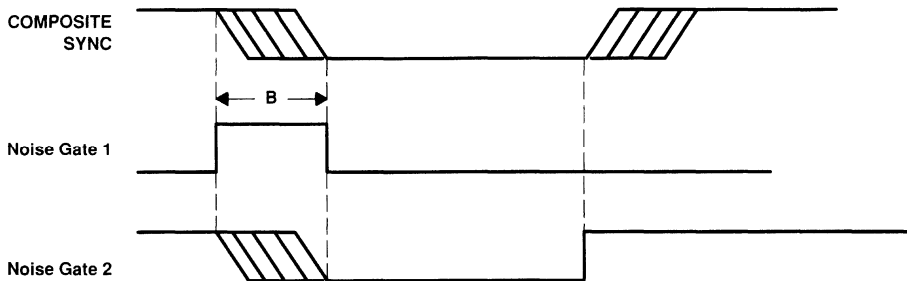


Figure 2. Proper COMPOSITE SYNC Timing

Table 3. Sync and Clamp Timing for NTSC and PAL with CLK = 4 fsc

TIME INTERVAL	NTSC fsc = 3.58 MHz		PAL fsc = 4.43 MHz	
	NO. OF CLOCKS	TIME (μs)	NO. OF CLOCKS	TIME (μs)
A	867	60.6	1075	60.7
B	43	3	61	3.5
C	58	4.05	58	3.27
D	6	0.42	6	0.34
E	76	5.3	93	5.25
F	54	3.77	84	4.74

using an external clamp pulse

When CLPEN is taken low, EXTCLP accepts an externally generated active-high clamp pulse. This pulse must occur within the horizontal-blanking interval back porch. CLPEN low inhibits the internal counters and no internal clamp pulse is generated.

TLC5733A
20 MSPS 3-CHANNEL ANALOG-TO-DIGITAL CONVERTER
WITH HIGH-PRECISION CLAMP
 SLAS104A – JULY 1995 – REVISED NOVEMBER 1996

output digital code (for each channel of ADC)

Table 4. Input Signal Versus Digital Output Code

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB							LSB
$V_{ref}(RT)$	255	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	128	1	0	0	0	0	0	0	0
•	127	0	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
$V_{ref}(RB)$	0	0	0	0	0	0	0	0	0

output data format

The TLC5733A can select three output data formats to various TV/VCR (video) data processing by the combination of MODE0 and MODE1. The output is synchronous when INIT is taken high.

Table 5. Output Data Format Selection

CONDITION		OUTPUT DATA	
MODE1	MODE0	OUTPUT DATA FORMAT	RATIO OF Y:U:V
L	L	Format 1	4:1:1
L	H	Format 2	4:4:4
H	L	Format 3	4:2:2
H	H	Not used	N/A

TLC5733A
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WITH HIGH-PRECISION CLAMP
 SLAS104A – JULY 1995 – REVISED NOVEMBER 1996

output data format (continued)

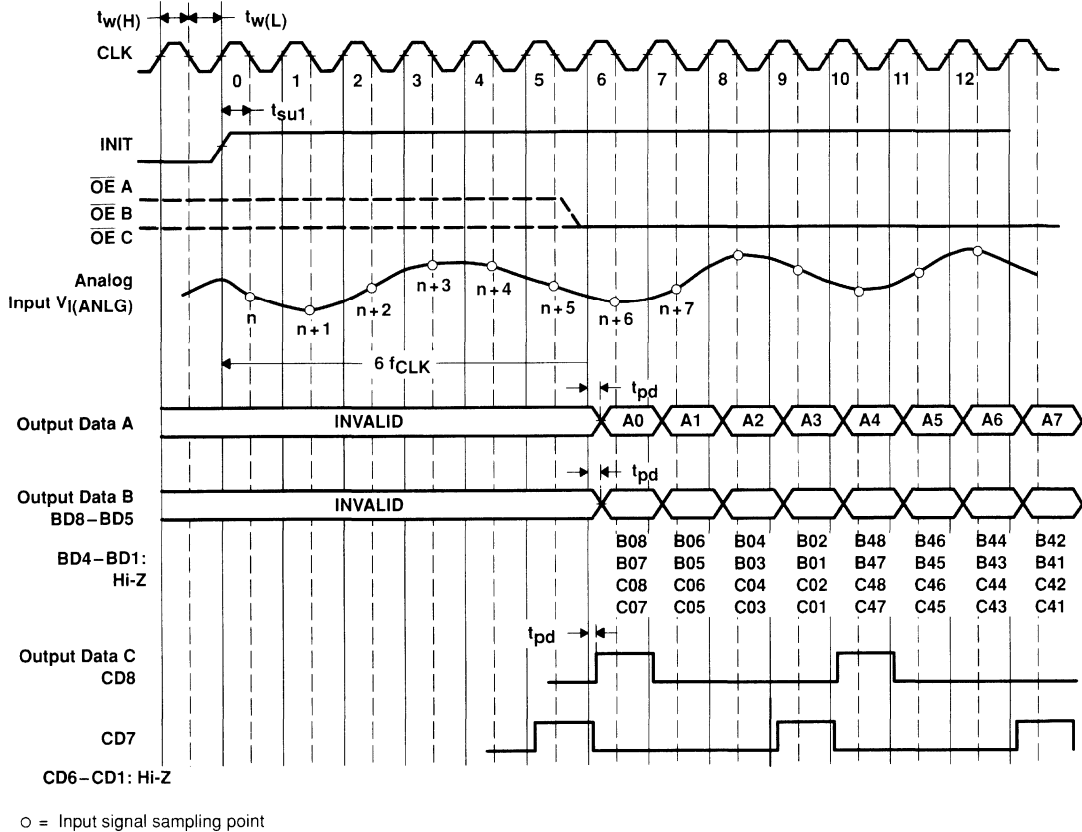


Figure 3. Format 1, 4:1:1



TLC5733A
20 MSPS 3-CHANNEL ANALOG-TO-DIGITAL CONVERTER
WITH HIGH-PRECISION CLAMP

SLAS104A – JULY 1995 – REVISED NOVEMBER 1996

output data format (continued)

Table 6. Format 1

CHANNEL OF ADC	BIT	OUTPUT DATA							
		CLK (see Note 1)							
		6	7	8	9	10	11	12	13
A	AD8	A08	A18	A28	A38	A48	A58	A68	A78
	AD7	A07	A17	A27	A37	A47	A57	A67	A77
	AD6	A06	A16	A26	A36	A46	A56	A66	A76
	AD5	A05	A15	A25	A35	A45	A55	A65	A75
	AD4	A04	A14	A24	A34	A44	A54	A64	A74
	AD3	A03	A13	A23	A33	A43	A53	A63	A73
	AD2	A02	A12	A22	A32	A42	A52	A62	A72
	AD1	A01	A11	A21	A31	A41	A51	A61	A71
B	BD8	B08	B06	B04	B02	B48	B46	B44	B42
	BD7	B07	B05	B03	B01	B47	B45	B43	B41
	BD6	C08	C06	C04	C02	C48	C46	C44	C42
	BD5	C07	C05	C03	C01	C47	C45	C43	C41
	BD4	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	BD3	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	BD2	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	BD1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
C	CD8	H	L	L	L	H	L	L	L
	CD7	L	L	L	L	L	L	L	H
	CD6	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD5	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD4	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD3	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD2	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

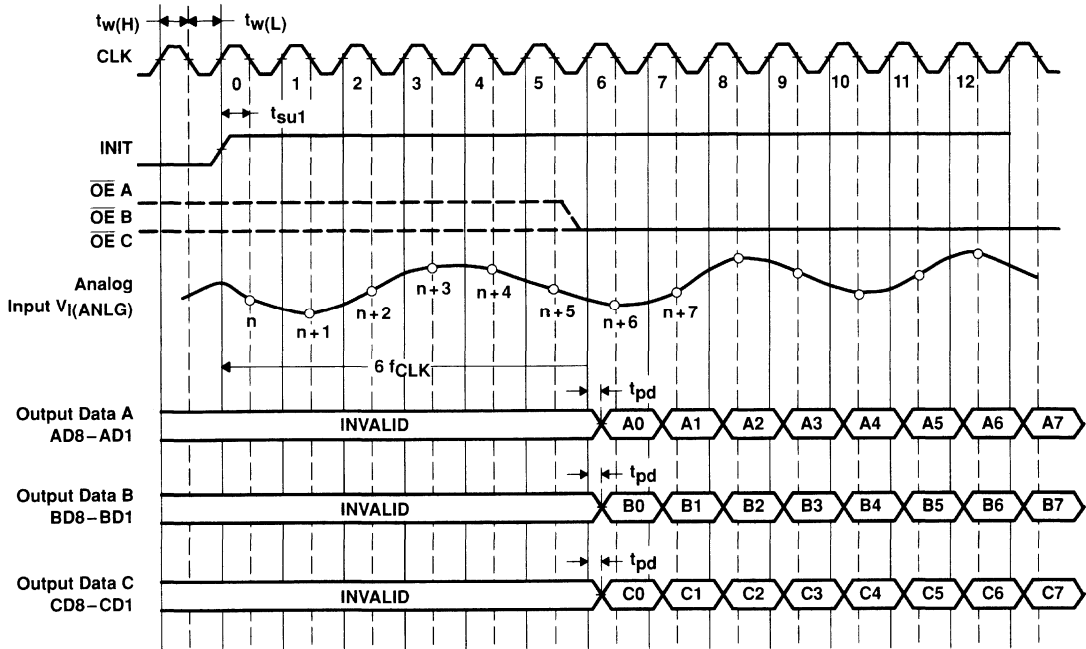
- NOTES: 1. The value of the first sampling clock at A/D conversion is CLK 0.
2. A06 is an example of an entry in the table where A is the ADC channel, 0 is the sampling order, and 6 is the bit number.



TLC5733A
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WITH HIGH-PRECISION CLAMP

SLAS104A – JULY 1995 – REVISED NOVEMBER 1996

output data format (continued)



○ = Input signal sampling point

Figure 4. Format 2, 4:4:4

TLC5733A
20 MSPS 3-CHANNEL ANALOG-TO-DIGITAL CONVERTER
WITH HIGH-PRECISION CLAMP

SLAS104A – JULY 1995 – REVISED NOVEMBER 1996

output data format (continued)

Table 7. Format 2

CHANNEL OF ADC	BIT	OUTPUT DATA							
		CLK (see Note 1)							
		6	7	8	9	10	11	12	13
A	AD8	A08	A18	A28	A38	A48	A58	A68	A78
	AD7	A07	A17	A27	A37	A47	A57	A67	A77
	AD6	A06	A16	A26	A36	A46	A56	A66	A76
	AD5	A05	A15	A25	A35	A45	A55	A65	A75
	AD4	A04	A14	A24	A34	A44	A54	A64	A74
	AD3	A03	A13	A23	A33	A43	A53	A63	A73
	AD2	A02	A12	A22	A32	A42	A52	A62	A72
	AD1	A01	A11	A21	A31	A41	A51	A61	A71
B	BD8	B08	B18	B28	B38	B48	B58	B68	B78
	BD7	B07	B17	B27	B37	B47	B57	B67	B77
	BD6	B06	B16	B26	B36	B46	B56	B66	B76
	BD5	B05	B15	B25	B35	B45	B55	B65	B75
	BD4	B04	B14	B24	B34	B44	B54	B64	B74
	BD3	B03	B13	B23	B33	B43	B53	B63	B73
	BD2	B02	B12	B22	B32	B42	B52	B62	B72
	BD1	B01	B11	B21	B31	B41	B51	B61	B71
C	CD8	C08	C18	C28	C38	C48	C58	C68	C78
	CD7	C07	C17	C27	C37	C47	C57	C67	C77
	CD6	C06	C16	C26	C36	C46	C56	C66	C76
	CD5	C05	C15	C25	C35	C45	C55	C65	C75
	CD4	C04	C14	C24	C34	C44	C54	C64	C74
	CD3	C03	C13	C23	C33	C43	C53	C63	C73
	CD2	C02	C12	C22	C32	C42	C52	C62	C72
	CD1	C01	C11	C21	C31	C41	C51	C61	C71

- NOTES: 1. The value of the first sampling clock at A/D conversion is CLK 0.
2. A06 is an example of an entry in the table where A is the ADC channel, 0 is the sampling order, and 6 is the bit number.



TLC5733A
20 MSPS 3-CHANNEL ANALOG-TO-DIGITAL CONVERTER
WITH HIGH-PRECISION CLAMP
 SLAS104A – JULY 1995 – REVISED NOVEMBER 1996

output data format (continued)

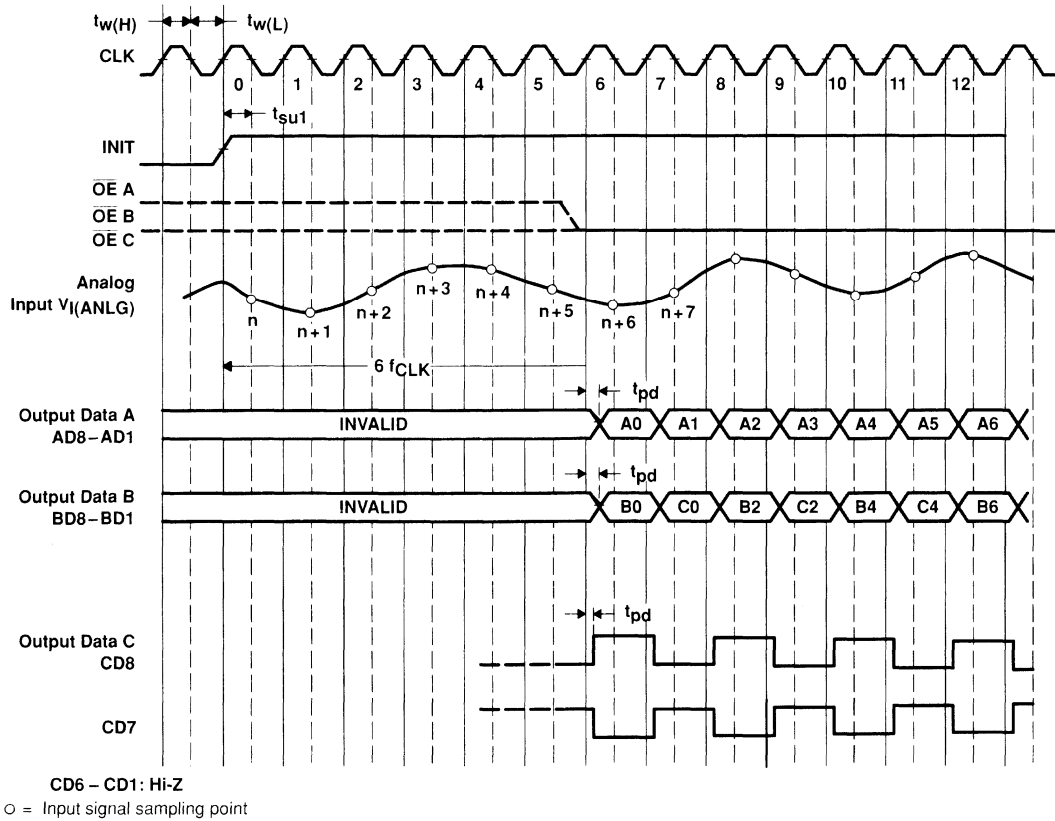


Figure 5. Format 3, 4:2:2

TLC5733A
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output data format (continued)

Table 8. Format 3

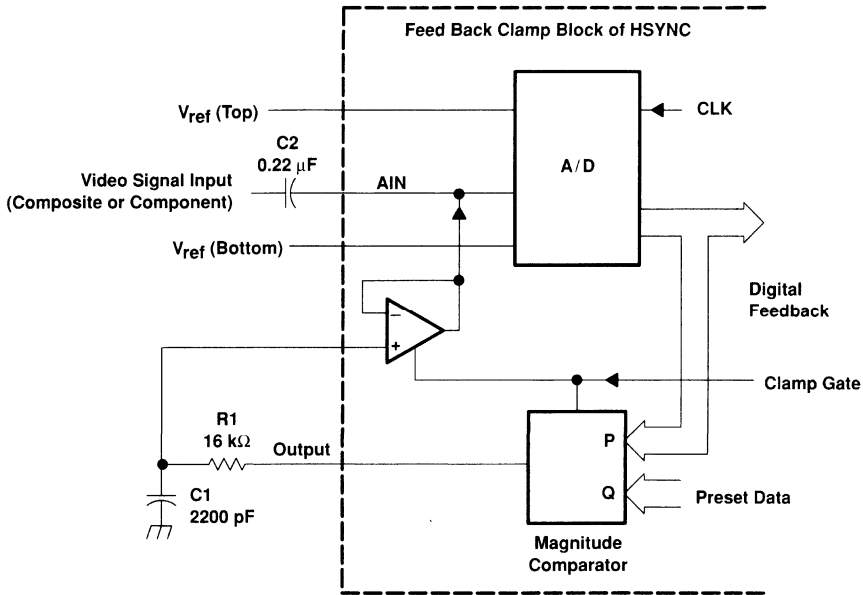
CHANNEL OF ADC	BIT	OUTPUT DATA							
		CLK (see Note 1)							
		6	7	8	9	10	11	12	13
A	AD8	A08	A18	A28	A38	A48	A58	A68	A78
	AD7	A07	A17	A27	A37	A47	A57	A67	A77
	AD6	A06	A16	A26	A36	A46	A56	A66	A76
	AD5	A05	A15	A25	A35	A45	A55	A65	A75
	AD4	A04	A14	A24	A34	A44	A54	A64	A74
	AD3	A03	A13	A23	A33	A43	A53	A63	A73
	AD2	A02	A12	A22	A32	A42	A52	A62	A72
	AD1	A01	A11	A21	A31	A41	A51	A61	A71
	B	BD8	B08	C08	B28	C28	B48	C48	B68
BD7		B07	C07	B27	C27	B47	C47	B67	C67
BD6		B06	C06	B26	C26	B46	C46	B66	C66
BD5		B05	C05	B25	C25	B45	C45	B65	C65
BD4		B04	C04	B24	C24	B44	C44	B64	C64
BD3		B03	C03	B23	C23	B43	C43	B63	C63
BD2		B02	C02	B22	C22	B42	C42	B62	C62
BD1		B01	C01	B21	C21	B41	C41	B61	C61
C		CD8	H	L	H	L	H	L	H
	CD7	L	H	L	H	L	H	L	H
	CD6	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD5	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD4	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD3	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD2	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

- NOTES: 1. The value of the first sampling clock at A/D conversion is CLK 0.
2. A06 is an example of an entry in the table where A is the ADC channel, 0 is the sampling order, and 6 is the bit number.



TLC5733A
20 MSPS 3-CHANNEL ANALOG-TO-DIGITAL CONVERTER
WITH HIGH-PRECISION CLAMP
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APPLICATION INFORMATION



FEEDBACK CLAMP AND CHARGE PUMP ACTIVITY

INPUT DATA CONDITIONS	OUTPUT		CHARGE PUMP CONDITIONS
	Active	Hold	
$P < Q$	Active	H	Charge
$P = Q$	Hold	Z	Hold
$P > Q$	Active	L	Discharge

Figure 6. Feedback Clamp Circuit

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WITH HIGH-PRECISION CLAMP
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APPLICATION INFORMATION

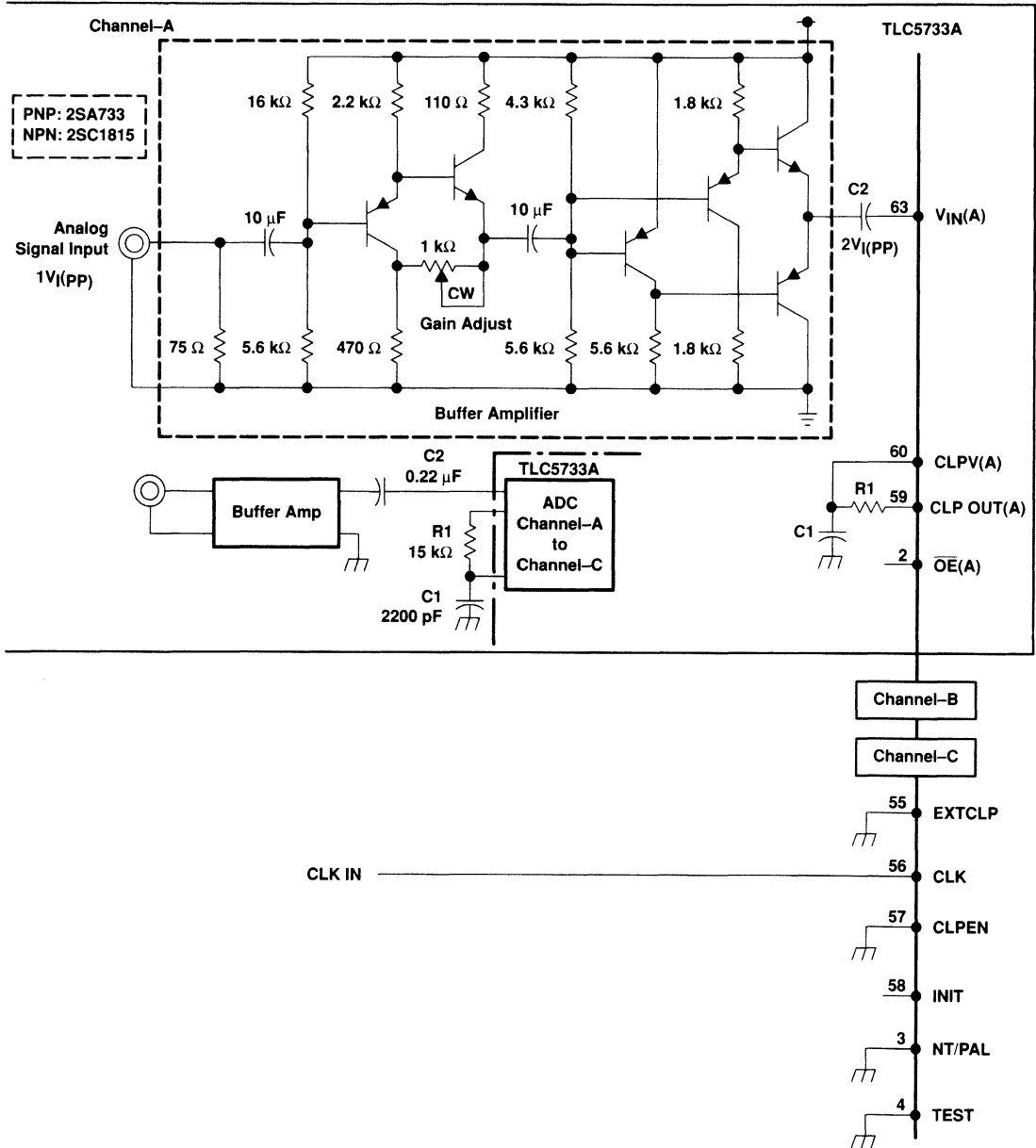


Figure 7. Interface Without Clamping

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APPLICATION INFORMATION

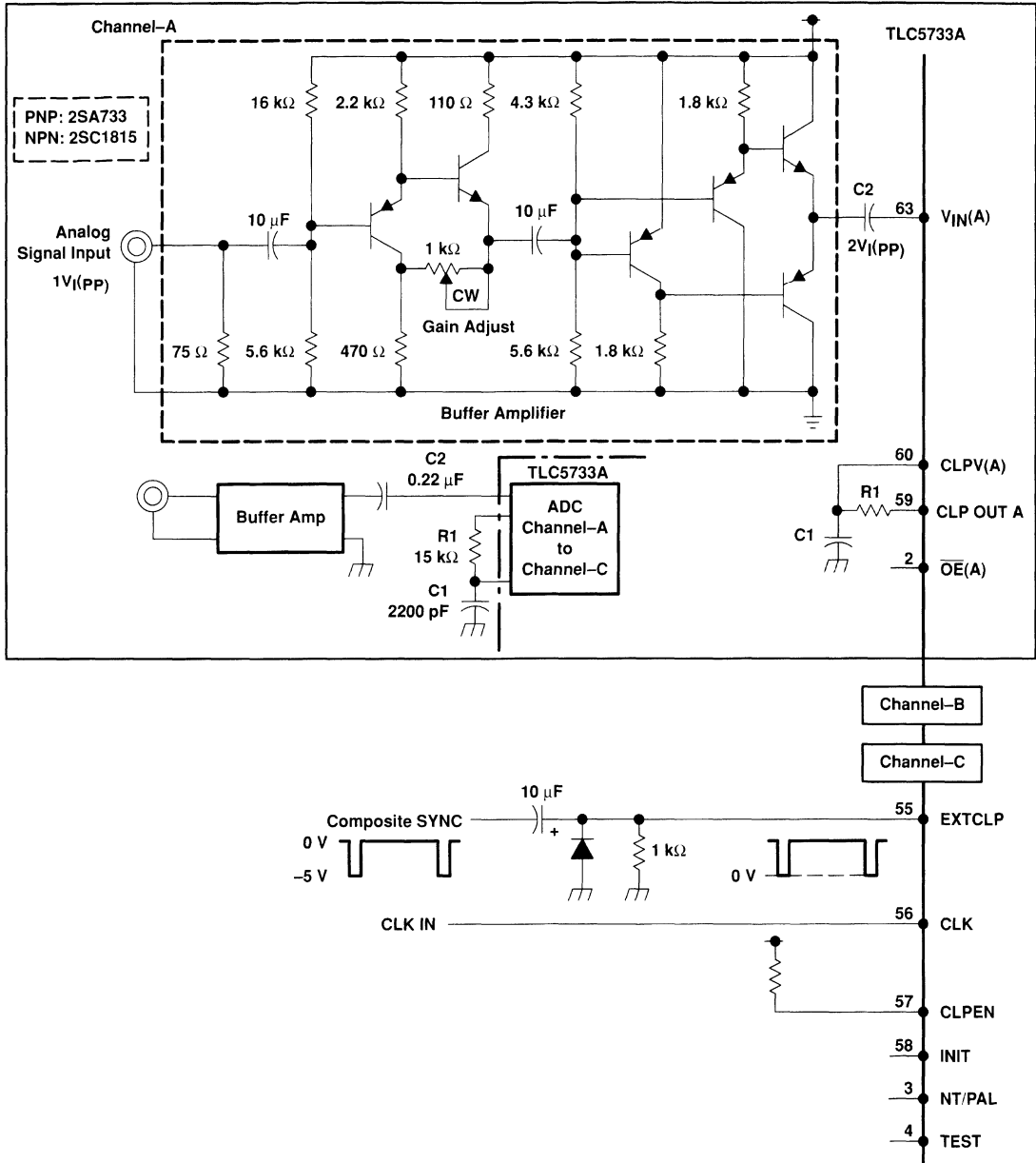


Figure 8. Interface Connection Using Composite Sync Signal

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APPLICATION INFORMATION

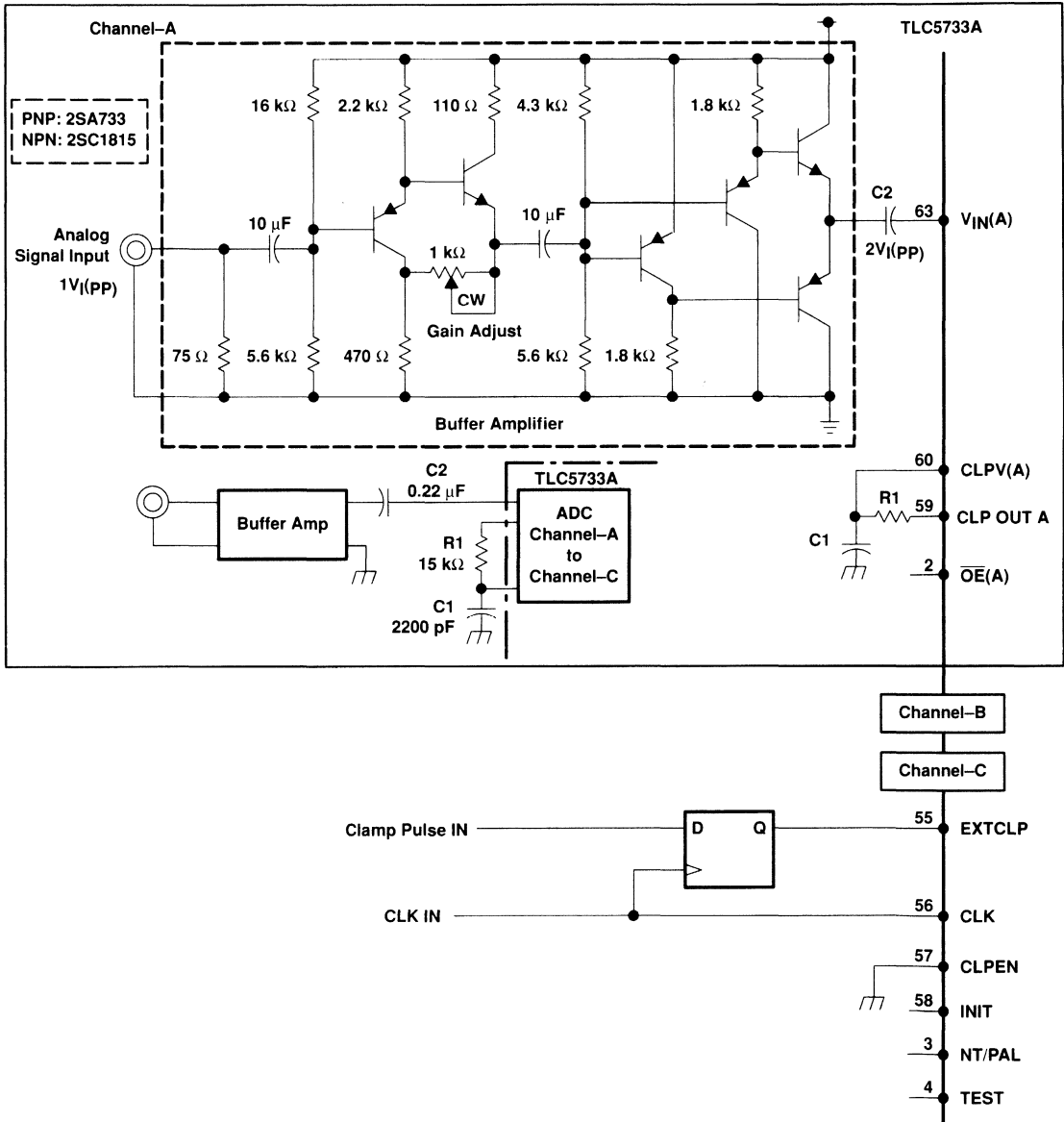


Figure 9. Interface Using External Clamp Pulse With Synchronization

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WITH HIGH-PRECISION CLAMP
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APPLICATION INFORMATION

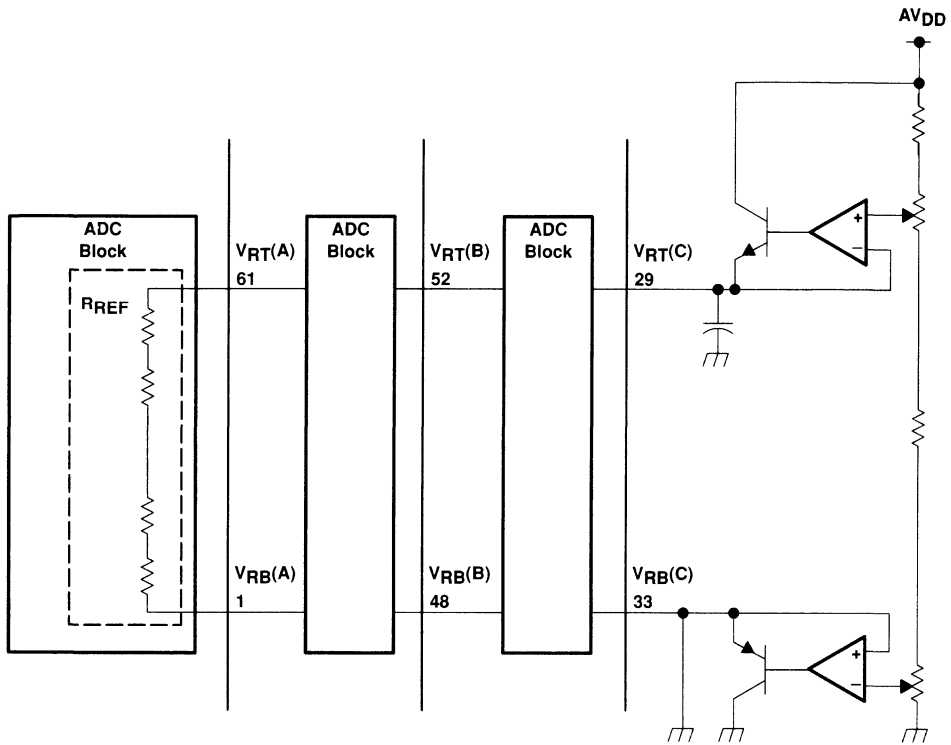


Figure 10. Adjustment Circuit For Top and Bottom Reference Voltages

TLC320AD57C ***Data Manual***

Sigma-Delta Stereo Analog-to-Digital Converter

SLAS086A
January 1995



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Contents

<i>Section</i>	<i>Title</i>	<i>Page</i>
1	Introduction	2–251
1.1	Features	2–251
1.2	Functional Block Diagram	2–251
1.3	Terminal Assignments	2–252
1.4	Ordering Information	2–252
1.5	Terminal Functions	2–252
2	Detailed Description	2–255
2.1	Power-Down and Reset Functions	2–255
2.1.1	Power Down	2–255
2.1.2	Reset Function	2–256
2.2	Differential Input	2–257
2.3	Sigma-Delta Modulator	2–257
2.4	Decimation Filter	2–257
2.5	High-Pass Filter	2–257
2.6	Master-Clock Circuit	2–257
2.7	Test	2–258
2.8	Serial Interface	2–258
2.8.1	Master Mode	2–258
2.8.2	Slave Mode	2–260
3	Specifications	2–261
3.1	Absolute Maximum Ratings Over Operating Free-Air Temperature Range	2–261
3.2	Recommended Operating Conditions	2–261
3.3	Electrical Characteristics	2–262
3.3.1	Digital Interface, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V}$	2–262
3.3.2	Analog Interface	2–262
3.3.3	Channel Characteristics, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V}$, $f_s = 48\text{ kHz}$	2–263
3.4	Switching Characteristics	2–263
4	Parameter Measurement Information	2–265

List of Illustrations

<i>Figure</i>	<i>Title</i>	<i>Page</i>
2-1	Power-Down Timing Relationships	2-256
2-2	Differential Analog Input Configuration	2-257
2-3	Serial Master Transfer Modes	2-259
2-4	Serial Slave Transfer Modes	2-260
4-1	SCLK to Fsync and DOUT – Master Mode 3	2-265
4-2	SCLK to Fsync, DOUT and LRCIk – Master Modes 4 and 6	2-265
4-3	SCLK to Fsync, DOUT, and LRCIk – Master Mode 5	2-265
4-4	SCLK to Fsync, DOUT, and LRCIk – Master Mode 7	2-266
4-5	SCLK to LRCIk and DOUT – Slave Mode 0, Fsync High	2-266
4-6	SCLK to Fsync, LRCIk, and DOUT – Slave Mode 2, Fsync Controlled	2-266

List of Tables

<i>Table</i>	<i>Title</i>	<i>Page</i>
2-1	Master-Clock to Sample-Rate Comparison	2-258

1 Introduction

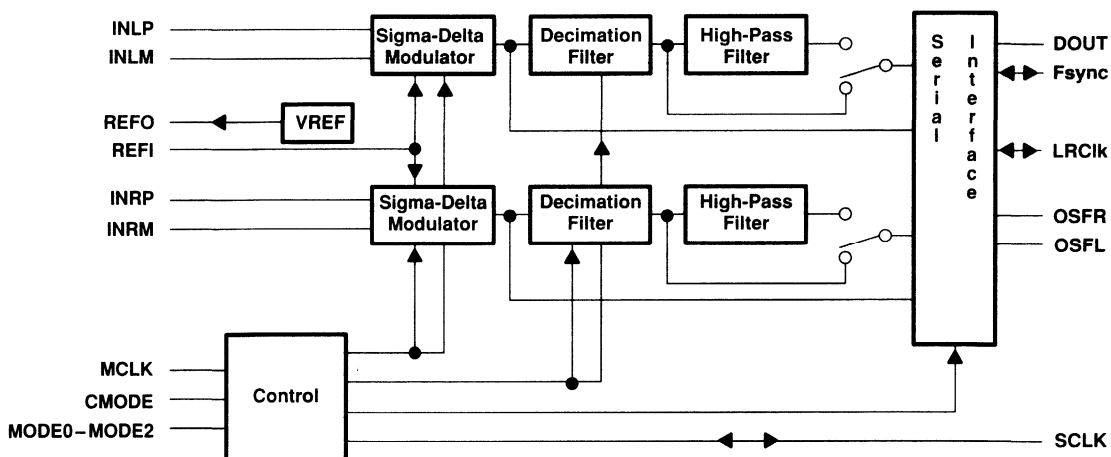
The TLC320AD57C provides high-resolution signal conversion from analog to digital using oversampling sigma-delta technology. This device consists of two synchronous conversion paths. Also included is a decimation filter after the modulator as shown in the functional block diagram. Other functions provide analog filtering and on-chip timing and control.

A functional block diagram of the TLC320AD57C is included in section 1.2. Each block is described in the Detailed Description section.

1.1 Features

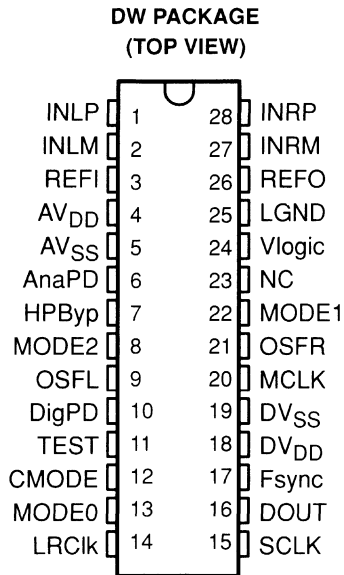
- Single 5-V Power Supply
- Sample Rates (f_s) up to 48 kHz
- 18-Bit Resolution
- Signal-to-Noise (EIAJ) of 97 dB
- Dynamic Range of 95 dB
- Total Signal-to-Noise+Distortion of 91 dB
- Internal Reference Voltage (V_{ref})
- Serial Port Interface
- Differential Architecture
- Power Dissipation of 200 mW. Power-Down Mode for Low-Power Applications
- One Micron Advanced LinEPIC1Z™ Process

1.2 Functional Block Diagram



LinEPIC1Z is a trademark of Texas Instruments Incorporated.

1.3 Terminal Assignments



NC – No internal connection

1.4 Ordering Information

T_A	PACKAGE
	SMALL OUTLINE (DW)
0°C to 70°C	TLC320AD57CDW

1.5 Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AnaPD	6	I	Analog power-down mode. The analog power-down mode disables the analog modulators. The single-bit modulator outputs become invalid, which renders the outputs of the digital filters invalid. When AnaPD is pulled low, normal operation of the device resumes.
AV _{DD}	4	I	Analog supply voltage
AV _{SS}	5	I	Analog ground
CMODE	12	I	Clock mode. CMODE selects between two methods of determining the master clock frequency. When CMODE is high, the master clock input is 384× the conversion frequency. When CMODE is low, the master clock input is 256× the conversion frequency.
DOUT	16	O	Data output. DOUT transmits the sigma-delta audio analog-to-digital converter (ADC) output data to a digital signal processor (DSP) serial port or other compatible serial interface and is synchronized to SCLK. DOUT is low when DigPD is high.
DV _{DD}	18	I	Digital supply voltage

1.5 Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION																																				
DVSS	19	I	Digital ground																																				
DigPD	10	I	Digital power-down mode. The digital power-down mode shuts down the digital filters and clock generators. All digital outputs are brought to unasserted levels. When DigPD is pulled low, normal operation of the device resumes.																																				
Fsync	17	I/O	Frame synchronization. Fsync designates valid data from the ADC.																																				
HPByp	7	I	High-pass filter bypass. When HPByp is high, the high-pass filter is bypassed. This allows dc analog signal conversion.																																				
INLM	2	I	Inverting input to left analog input amplifier																																				
INLP	1	I	Noninverting input to left analog input amplifier																																				
INRM	27	I	Inverting input to right analog input amplifier																																				
INRP	28	I	Noninverting input to right analog input amplifier																																				
LGND	25	I	Logic-power-supply ground for analog modulator																																				
LRCIk	14	I/O	Left/right clock. LRCIk signifies whether the serial data is associated with the left channel ADC (when high) or the right channel ADC (when low). LRCIk is low when DigPD is high.																																				
MCLK	20	I	Master clock. MCLK derives all of the key logic signals of the sigma-delta audio ADC. The nominal input frequency range is 18.432 MHz to 256 kHz.																																				
MODE0–MODE2	8, 13, 22	I	<p>Serial modes. MODE0–MODE2 configure this device for many different modes of operation. The different configurations are:</p> <ul style="list-style-type: none"> Master versus slave 16 bit versus 18 bit MSB first versus LSB first Slave: Fsync controlled versus Fsync high <p>Each of these modes is described in the Serial Interface section with timing diagrams.</p> <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>MODE</th> <th>MASTER/ SLAVE</th> <th>BITS</th> <th>MSB/LSB FIRST</th> </tr> </thead> <tbody> <tr> <td>0 0 0</td> <td>slave</td> <td>up to 18</td> <td>MSB</td> </tr> <tr> <td>0 0 1</td> <td>slave</td> <td>18</td> <td>LSB</td> </tr> <tr> <td>0 1 0</td> <td>slave</td> <td>up to 18</td> <td>MSB</td> </tr> <tr> <td>0 1 1</td> <td>master</td> <td>16</td> <td>MSB</td> </tr> <tr> <td>1 0 0</td> <td>master</td> <td>18</td> <td>MSB</td> </tr> <tr> <td>1 0 1</td> <td>master</td> <td>18</td> <td>LSB</td> </tr> <tr> <td>1 1 0</td> <td>master</td> <td>16</td> <td>MSB</td> </tr> <tr> <td>1 1 1</td> <td>master</td> <td>16</td> <td>LSB</td> </tr> </tbody> </table>	MODE	MASTER/ SLAVE	BITS	MSB/LSB FIRST	0 0 0	slave	up to 18	MSB	0 0 1	slave	18	LSB	0 1 0	slave	up to 18	MSB	0 1 1	master	16	MSB	1 0 0	master	18	MSB	1 0 1	master	18	LSB	1 1 0	master	16	MSB	1 1 1	master	16	LSB
MODE	MASTER/ SLAVE	BITS	MSB/LSB FIRST																																				
0 0 0	slave	up to 18	MSB																																				
0 0 1	slave	18	LSB																																				
0 1 0	slave	up to 18	MSB																																				
0 1 1	master	16	MSB																																				
1 0 0	master	18	MSB																																				
1 0 1	master	18	LSB																																				
1 1 0	master	16	MSB																																				
1 1 1	master	16	LSB																																				
OSFL, OSFR	9, 21	O	Over scale flag left/right. If the left/right channel analog input exceeds the full scale input range for two consecutive conversions, OSFL and OSFR are set high for 4096 LRCIk periods. OSFL and OSFR are low when DigPD is high.																																				
SCLK	15	I/O	Shift clock. If SCLK is configured as an input, SCLK clocks serial data out of the sigma-delta audio ADC. If SCLK is configured as an output, SCLK stops clocking when DigPD is high.																																				
TEST	11	I	Test mode. TEST should be low for normal operation.																																				
REFI	3	I	Input voltage for modulator reference (normally connected to REFO, terminal 26).																																				
REFO	26	I	Internal voltage reference																																				
Vlogic	24	I	Logic power supply (5 V) for analog modulator																																				

2 Detailed Description

The following sections contain a detailed description of the TLC320AD57C.

2.1 Power-Down and Reset Functions

The following sections contain descriptions of the power-down and reset functions of the TLC320AD57C.

2.1.1 Power Down

The power-down state is comprised of a separate digital and analog power down. The power consumption of each is detailed in Section 3.3, Electrical Characteristics.

The digital power-down mode shuts down the digital filters and clock generators. All digital outputs are set to an unasserted level. When the digital power-down terminal (DigPD) is pulled low, normal operation of the device is initiated.

In slave mode, the conversion process must synchronize to an input on the LRCIk terminal and the SCLK terminal. Therefore, the conversion process is not initiated until the first rising edges on both SCLK and LRCIk are detected after DigPD is pulled low. This synchronizes the conversion cycle. All conversions are performed at a fixed LRCIk rate [$MCLK/256$ (CMODE low) or $MCLK/384$ (CMODE high)] after the initial synchronization. After the digital power-down terminal is brought low, the output of the digital filters remains invalid for 50 LRCIk cycles [see Figures 2–1(a) and 2–1(b)].

In master mode, LRCIk is an output; therefore, the conversion process initiates based on internal timing. The first valid data out occurs as shown in Figure 2–1(c).

The analog power-down mode disables the analog modulators. The single-bit modulator outputs become invalid, which renders the outputs of the digital filters invalid. When the analog power-down terminal is brought low, the modulators are brought back online; however, the outputs of the digital filters require 50 LRCIk cycles for valid results.

2.1.2 Reset Function

The conversion process is not initiated until the first rising edges on both SCLK and LRCIk are detected after DigPD is pulled low. This synchronizes the conversion cycle. All conversions are performed at a fixed LRCIk rate [MCLK/256 (CMODE low) or MCLK/384 (CMODE high)] after the initial synchronization.

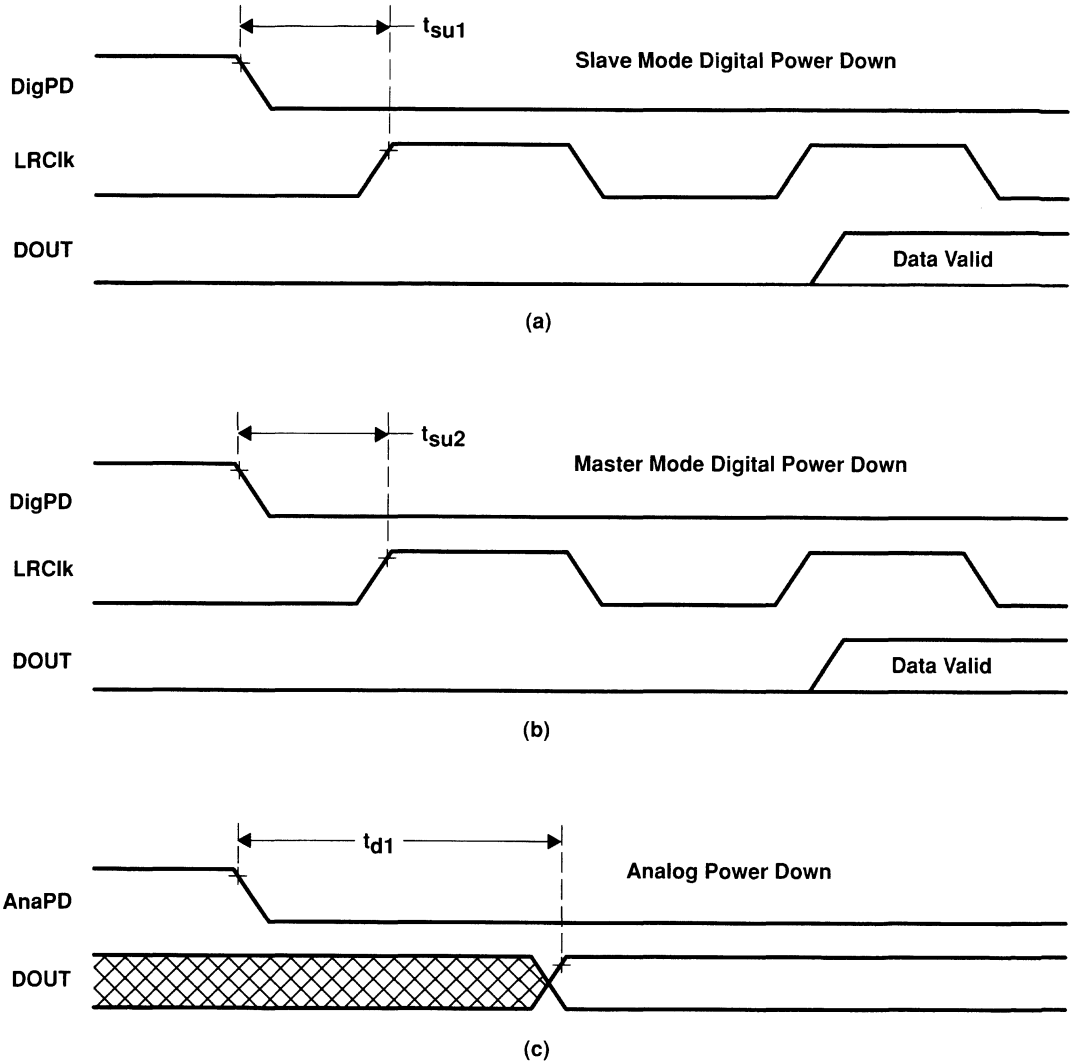


Figure 2-1. Power-Down Timing Relationships

2.2 Differential Input

The input is differential in order to provide common-mode noise rejection and increase the input dynamic range. Figure 2–2 shows the analog input signals used in a differential configuration to achieve 6.4-V peak-to-peak differential swing with a 3.2-V peak-to-peak swing per input line.

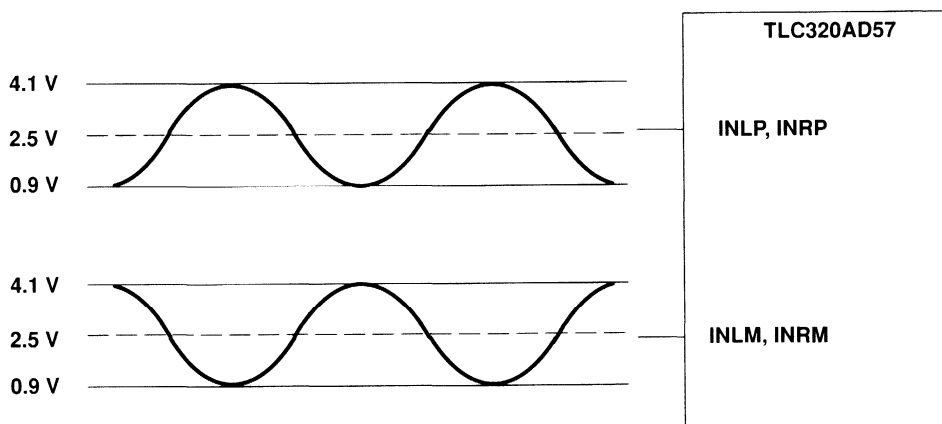


Figure 2–2. Differential Analog Input Configuration

2.3 Sigma-Delta Modulator

The modulator is a fourth order sigma-delta modulator with 64 times oversampling. The ADC provides high-resolution, low-noise performance from a one-bit converter using oversampling techniques.

2.4 Decimation Filter

The decimation filter used after the sigma-delta modulator reduces the digital data rate to the sampling rate of LRClk. This is accomplished by decimating with a ratio of 1:64. The output of this filter is a 2s complement data word of up to 18 bits serially clocked out.

If the input value exceeds the full range of the converter, the output of the decimator is held at the appropriate extreme until the input returns to within the dynamic range of the device.

2.5 High-Pass Filter

The high-pass filter removes dc from the input. With this filtering, offset calibration is not needed. The high-pass filter can be circumvented by asserting the HPByp terminal to pass dc signals through the converter. However, an offset due to the converter can be present when bypassing the high-pass filter.

2.6 Master-Clock Circuit

The master-clock circuit generates and distributes necessary clocks throughout the device. MCLK is the external master-clock input. CMODE selects the relationship of MCLK to the sample rate, LRClk. When CMODE is low, the sample rate of the data paths is set to $LRClk = MCLK/256$. When CMODE is high, the sample rate is set to $LRClk = MCLK/384$. With a fixed oversampling ratio of 64x, the effect of changing MCLK is shown in Table 2–1.

When the device is in master mode, SCLK is derived from MCLK in order to provide clocking of the serial communications between the sigma-delta audio ADC and a digital signal processor (DSP) or control logic. This is equivalent to a clock running at $64 \times LRClk$.

When the device is in slave mode, SCLK is externally derived.

**Table 2–1. Master-Clock to Sample-Rate Comparison
(modes 1, 3, 4, 5)**

MCLK (MHz)	CMODE	SCLK (MHz)	LRCIk (kHz)
12.2880	Low	3.0720	48
18.4320	High		
11.2896	Low	2.8224	44.1
16.9344	High		
8.1920	Low	2.0480	32
12.2880	High		
0.2560	Low	0.0640	1
0.3840	High		

2.7 Test

When the TEST input is high, the test mode is selected, which routes the high speed one-bit modulator result to the serial port output. When in the test mode, the SCLK output frequency is equal to the data output rate. LRCIk is an input when the test mode is selected. This allows for the selection of the left or right modulator output to be routed to the serial port (high = left and low = right).

2.8 Serial Interface

Although the serial data is shifted out in two separate time packets that represent the left and right channels, the inputs are sampled and converted simultaneously.

The serial interface protocol has master and slave modes each with different read-out modes. The master mode sources the control signals for conversion synchronization while the slave mode allows an external controller to provide conversion synchronization signals.

The five master modes are shown in Figures 2–3(a) through 2–3(e) and the three slave modes are shown in Figures 2–4(a) through 2–4(c). For a 16-bit word, D15 is the most significant bit and D0 is the least significant bit. Unless otherwise specified, all values are in 2s complement format.

In the master mode, SCLK is generated internally and is sourced as an output. The relationship of SCLK to LRCIk is 64× (modes 1, 3, 4, 5) or 32× (modes 6, 7). In the slave mode, SCLK is an input. SCLK timing must meet the timing specifications listed in the Recommended Operating Conditions section.

2.8.1 Master Mode

As the master, the TLC320AD57C generates LRCIk, Fsync, and SCLK from MCLK. These signals are provided for synchronizing the serial port of a DSP or other control devices.

Fsync designates valid data from the ADC, and accomplishes this in the master modes by one of two methods. The first method is to place a single pulse on Fsync prior to valid data. This indicates the starting point for the data. The second method of frame synchronization is to hold Fsync high during the entire valid data cycle which provides boundaries for the data.

LRCIk is generated internally from MCLK. The frequency of this signal is fixed at the sampling frequency f_s [$MCLK/256$ (CMODE low) or $MCLK/384$ (CMODE high)]. During the high period of this signal, the left channel data is serially shifted to the output; during the low period, the right channel data is shifted to the output. The conversion cycle synchronizes with the rising edge of LRCIk.

Five modes are available when the device is configured as a master. Two modes are for 18-bit communications. These modes differ from each other in that the MSB is transferred first in one mode while the LSB is transferred first in the second mode [see Figures 2–3(b) and 2–3(c)]. When the LSB is transferred first, the data is right justified to the LRCIk [see Figures 2–3(a) through 2–3(e)]. The three other modes

available as a master are 16-bit modes. Two of the modes differ as MSB first versus LSB first. These two modes set $SCLK = LRCIk \times 32$. This is one half the frequency used in the other transfer modes [see Figures 2-3(d) and 2-3(e)]. The third 16-bit mode provides the data MSB first with one clock delay after $LRCIk$ [see Figure 2-3(a)].

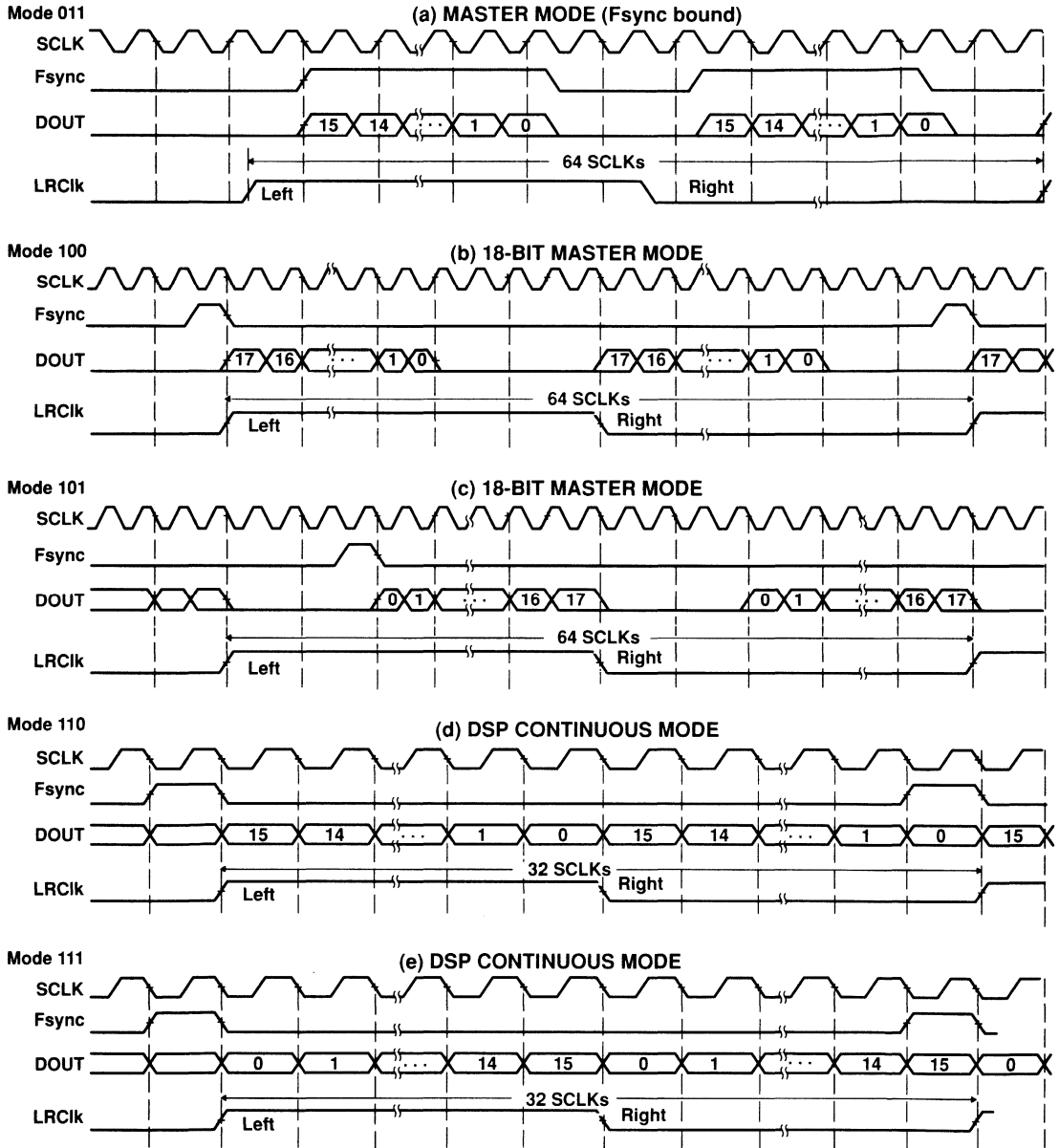


Figure 2-3. Serial Master Transfer Modes

2.8.2 Slave Mode

As a slave, the TLC320AD57C receives LRCIk, Fsync, and SCLK as inputs. The conversion cycle synchronizes to the rising edge of LRCIk, and the data synchronizes to the falling edge of SCLK. SCLK must meet the setup time requirements specified in Section 3.2, Recommended Operating Conditions. Synchronization of the slave modes is accomplished with the digital power-down control.

In slave mode, Fsync is an input. Three modes are provided as shown in Figures 2–4(a) through 2–4(c).

SCLK and LRCIk are externally generated and sourced. The first rising edges of SCLK and LRCIk after a power-down cycle initiate the conversion cycle. Refer to Section 2.8.1, Master Mode for signal functions.

Several modes are available when the TLC320AD57C is configured as a slave. Using the Mode0, Mode1, and Mode2 terminals, the TLC320AD57C can be set to shift out the MSB first or the LSB first [see Figures 2–4(a) and 2–4(b)]. The number of bits shifted out can be controlled by the number of valid SCLK cycles provided within the left or right channel period. If only enough clocks are provided to shift out 16 data bits before LRCIk changes state, this is equivalent to a 16-bit mode.

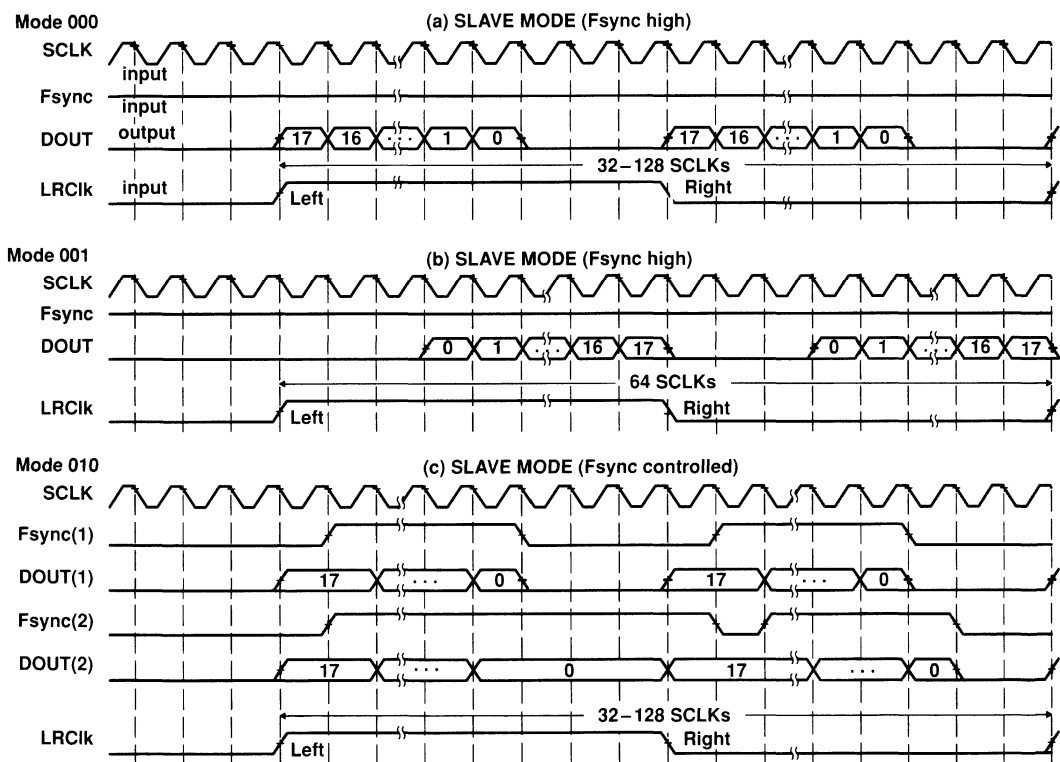


Figure 2–4. Serial Slave Transfer Modes

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Analog supply voltage range, AV_{DD} (see Note 1)	-0.3 V to 6.5 V
Digital supply voltage range, DV_{DD} (see Note 2)	-0.3 V to 6.5 V
Digital output voltage range, (externally applied)	-0.3 V to $DV_{DD} + 0.3$ V
Digital input voltage range, MODE0 – MODE2	-0.3 V to $DV_{DD} + 0.3$ V
Analog input voltage range, INLP, INLM, INRP, INRM	-0.3 V to $AV_{DD} + 0.3$ V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Case temperature for 10 seconds, T_C	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values for maximum ratings are with respect to AV_{SS} .
 2. Voltage values for maximum ratings are with respect to DV_{SS} .

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Analog supply voltage, AV_{DD} (see Note 3)	4.75	5	5.25	V
Digital supply voltage, DV_{DD}	4.75	5	5.25	V
Analog logic supply voltage, at Vlogic	4.75	5	5.25	V
Reference voltage, V_{ref}		3.2		V
Setup time, DigPD↓ to LRCIk↑, slave mode, t_{su1} (see Figure 2–1(a))		30		ns
Setup time, DigPD↓ to LRCIk↑, master mode, t_{su2} (see Figure 2–1(b))		30		ns
Setup time, SCLK↑ to LRCIk, slave mode, t_{su3} (see Figures 4–5 and 4–6)	30			ns
Setup time, LRCIk to SCLK↑, slave mode, t_{su4} (see Figure 4–5)	30			ns
Setup time, SCLK↑ to Fsync, slave mode, t_{su5} (see Figure 4–6)	30			ns
Setup time, Fsync to SCLK↑, slave mode, t_{su6} (see Figure 4–6)	30			ns
Load resistance at DOUT, R_L		10		kΩ
Operating free-air temperature, T_A	0		70	°C

NOTE 3: Voltages at analog inputs and outputs and AV_{DD} are with respect to the AV_{SS} terminal.

3.3 Electrical Characteristics

3.3.1 Digital Interface, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH} High-level input voltage		2	4.6		V
V_{IL} Low-level input voltage			0.2	0.8	V
V_{OH} High-level output voltage, DOUT	$I_{OH} = 2\text{ mA}$	2.4	4.6		V
V_{OL} Low-level output voltage, DOUT	$I_{OL} = 2\text{ mA}$		0.2	0.4	V
I_{IH} High-level input current, any digital input			1		μA
I_{IL} Low-level input current, any digital input			1		μA
C_i Input capacitance			5		pF
C_o Output capacitance			5		pF

3.3.2 Analog Interface

3.3.2.1 ADC Modulator, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V}$, $f_s = 48\text{ kHz}$, Bandwidth = 24 kHz, HPByp = 1, CMODE = 0, MODE0 – 2 = 101

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			18		Bits
DYNAMIC PERFORMANCE					
Signal to noise (EIAJ)	INLP = INRP = 2.5 V dc INLM = INRM = 2.5 V dc	93	97		dB
Dynamic range	–1dB down from 6-V differential input between INRP (INLP) and INRM (INLM)	91	95		dB
Signal to noise + distortion (THD + N)			91		dB
Total harmonic distortion (THD)			0.001%		
Interchannel isolation			108		dB
DC ACCURACY					
Gain error			± 0.2		dB
Interchannel gain mismatch			± 0.2		dB
Offset error (18-bit resolution)			± 5		mV
Offset drift			± 0.17		LSB/ $^\circ\text{C}$

3.3.2.2 Inputs/Supplies, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V}$, $f_s = 48\text{ kHz}$, Bandwidth = 24 kHz, HPByp = 1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Input voltage	Differential input	6.4			V
	Single-ended input	3.2			
Input impedance		50			k Ω
POWER SUPPLIES					
Power-supply current	I _{DD} (analog), operating	22	30		mA
	I _{DD} (digital), operating	24	32		mA
	I _{DD} (analog), power down	100			μA
	I _{DD} (digital), power down	40			μA
Power dissipation		230			mW

3.3.3 Channel Characteristics, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V}$, $f_s = 48\text{ kHz}$, HPByp = 1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband (-3 dB)	HPByp = 0	0.001		24	kHz
Passband ripple	30 Hz – 21.8 kHz	±0.01			dB
Stopband attenuation	26.2 kHz – 3046 kHz	80			dB
Group delay		25/F _s			s

3.4 Switching Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
t _{d1} Delay time, AnaPD↓ to DOUT valid (see Figure 2-1(c))	30			ns
t _d (MFSD) Delay time, SCLK↓ to Fsync, master mode (see Figures 4-1, 4-2, 4-3, and 4-4)	-20		20	ns
t _d (MDD) Delay time, SCLK↓ to DOUT, master mode (see Figures 4-1, 4-2, 4-3, and 4-4)	0		50	ns
t _d (MIRD) Delay time, SCLK↓ to LRCIk, master mode (see Figures 4-2 and 4-4)	-20		20	ns
t _d (SDD1) Delay time, LRCIk to DOUT, slave mode (see Figure 4-5)	50			ns
t _d (SDD2) Delay time, SCLK↓ to DOUT, slave mode (see Figures 4-5 and 4-6)	50			ns

4 Parameter Measurement Information

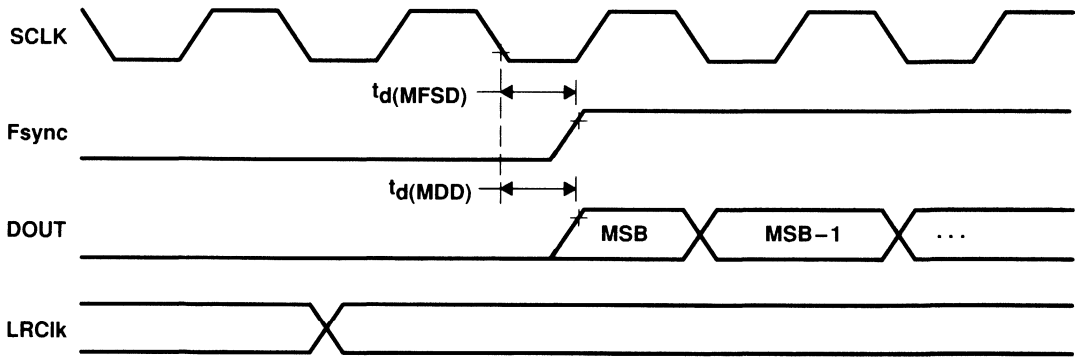


Figure 4-1. SCLK to Fsync and DOUT – Master Mode 3

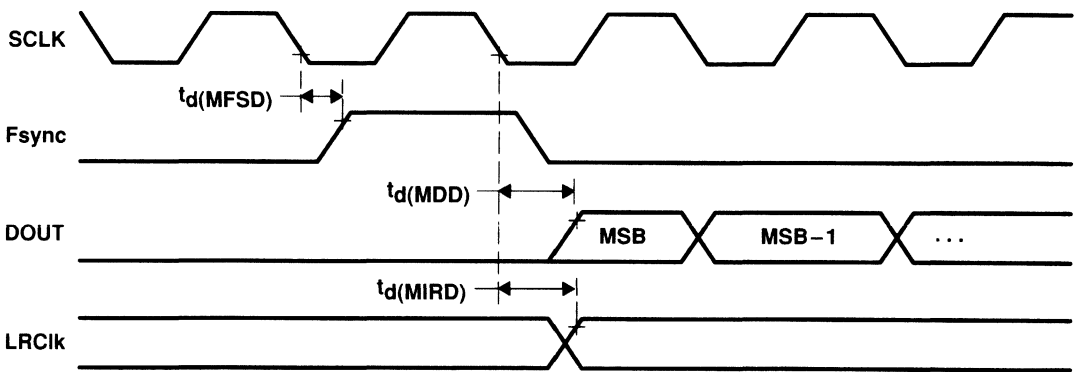


Figure 4-2. SCLK to Fsync, DOUT, and LRCIk – Master Modes 4 and 6

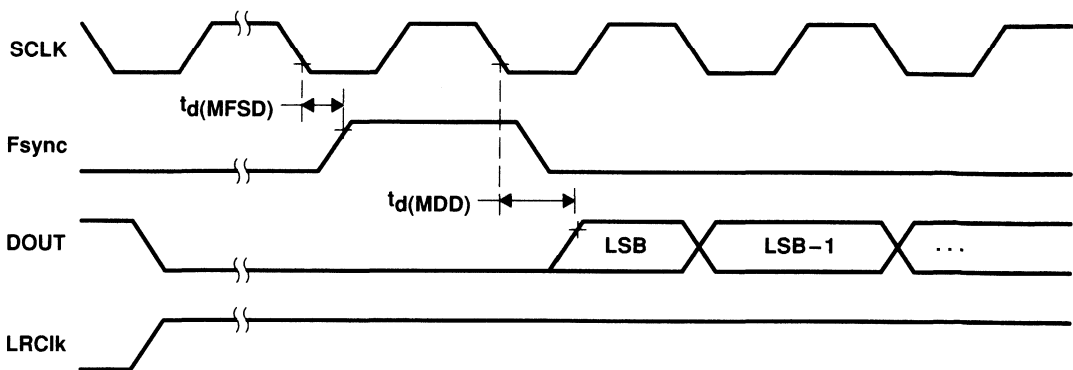


Figure 4-3. SCLK to Fsync, DOUT, and LRCIk – Master Mode 5

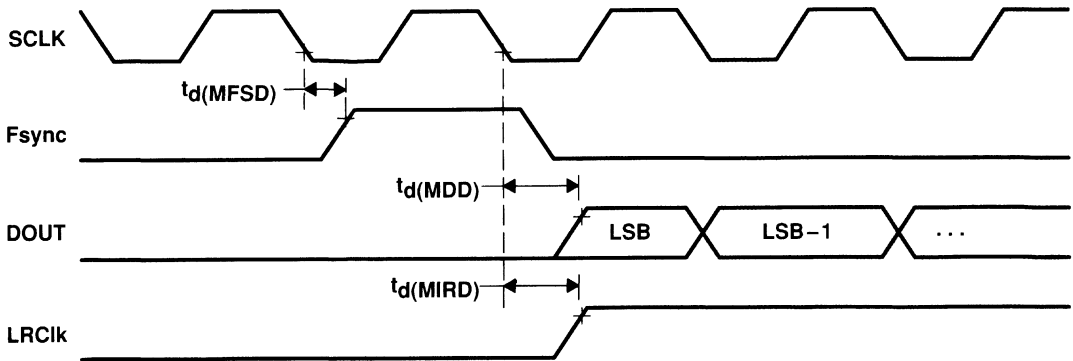


Figure 4-4. SCLK to Fsync, DOUT, and LRCIk – Master Mode 7

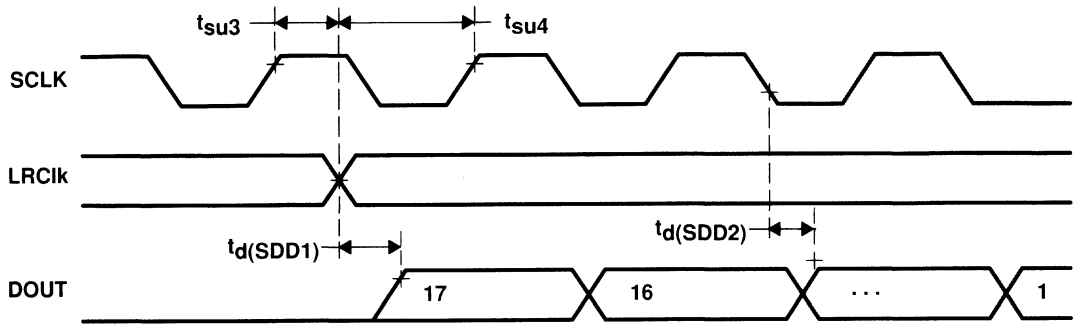


Figure 4-5. SCLK to LRCIk and DOUT – Slave Mode 0, Fsync High

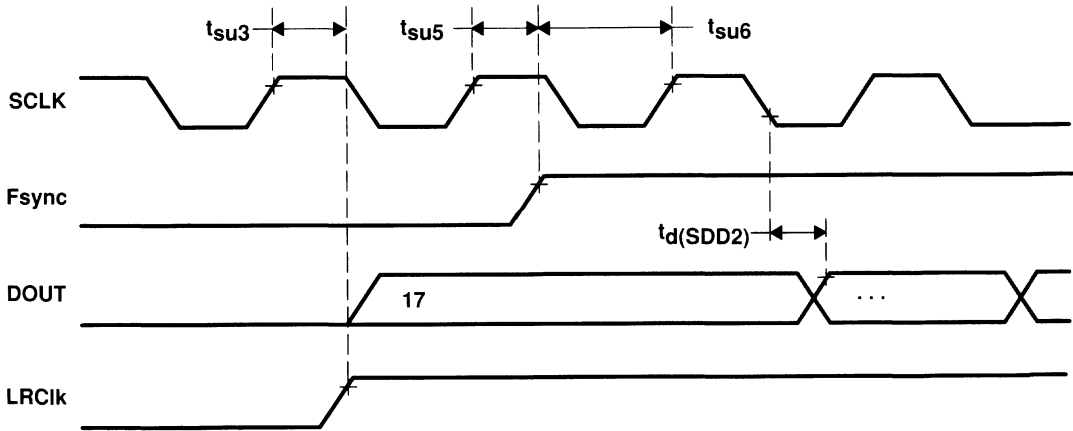


Figure 4-6. SCLK to Fsync, LRCIk, and DOUT – Slave Mode 2, Fsync Controlled

TLC320AD58C ***Data Manual***

Sigma-Delta Stereo Analog-to-Digital Converter

SLAS102
May 1995



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Contents

<i>Section</i>	<i>Title</i>	<i>Page</i>
1	Introduction	2–271
1.1	Features	2–271
1.2	Functional Block Diagram	2–271
1.3	Terminal Assignments	2–272
1.4	Ordering Information	2–272
1.5	Terminal Functions	2–272
2	Detailed Description	2–275
2.1	Power-Down and Reset Functions	2–275
2.1.1	Power Down	2–275
2.1.2	Reset Function	2–275
2.2	Differential Input	2–276
2.3	Sigma-Delta Modulator	2–277
2.4	Decimation Filter	2–277
2.5	High-Pass Filter	2–277
2.6	Master-Clock Circuit	2–277
2.7	Test	2–277
2.8	Serial Interface	2–277
2.8.1	Master Mode	2–278
2.8.2	Slave Mode	2–279
3	Specifications	2–281
3.1	Absolute Maximum Ratings Over Operating Free-Air Temperature Range	2–281
3.2	Recommended Operating Conditions	2–281
3.3	Electrical Characteristics	2–282
3.3.1	Digital Interface, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V}$	2–282
3.3.2	Analog Interface	2–282
3.3.3	Channel Characteristics, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V}$, $f_s = 48\text{ kHz}$	2–283
3.4	Switching Characteristics	2–283
4	Parameter Measurement Information	2–285
5	Application Information	2–287

List of Illustrations

<i>Figure</i>	<i>Title</i>	<i>Page</i>
2-1.	Power-Down Timing Relationships	2-276
2-2.	Differential Analog Input Configuration	2-276
2-3.	Serial Master Transfer Modes	2-279
2-4.	Serial Slave Transfer Modes	2-280
4-1.	SCLK to Fsync and DOUT – Master Mode 3	2-285
4-2.	SCLK to Fsync, DOUT, and LRCIk – Master Modes 4 and 6	2-285
4-3.	SCLK to Fsync, DOUT, and LRCIk – Master Mode 5	2-285
4-4.	SCLK to Fsync, DOUT, and LRCIk – Master Mode 7	2-286
4-5.	SCLK to LRCIk and DOUT – Slave Mode 0, Fsync High	2-286
4-6.	SCLK to Fsync, LRCIk, and DOUT – Slave Mode 2, Fsync Controlled	2-286
5-1.	TLC320AD58C Configuration Schematic	2-288
5-2.	TLC320AD58C External Digital Timing and Control-Signal Generation Schematic	2-289
5-3.	TLC320AD58C External Analog Input Buffer Schematic	2-290

List of Tables

<i>Table</i>	<i>Title</i>	<i>Page</i>
2-1.	Master-Clock to Sample-Rate Comparison	2-277

1 Introduction

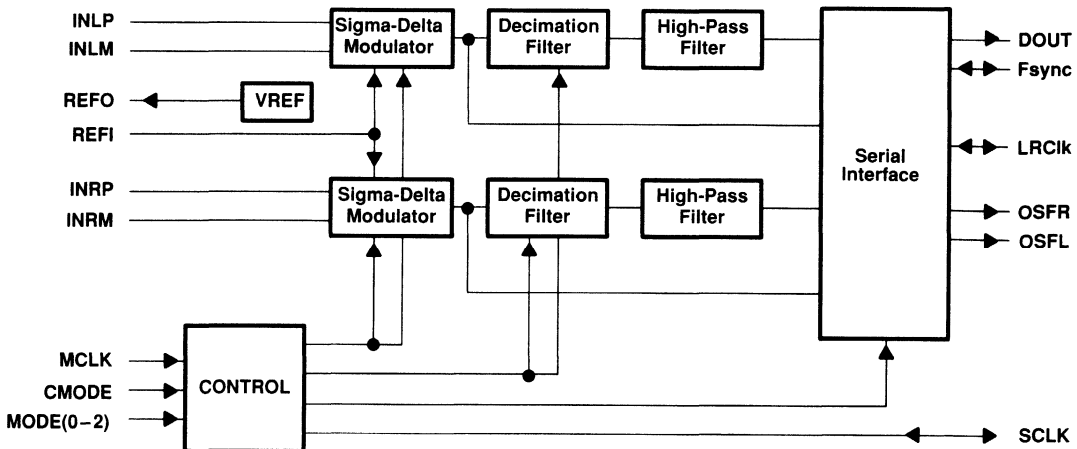
The TLC320AD58C provides high-resolution signal conversion from analog to digital using oversampling sigma-delta technology. This device consists of two synchronous conversion paths. Also included is a decimation filter after the modulator as shown in the functional block diagram. Other functions provide analog filtering and on-chip timing and control.

A functional block diagram of the TLC320AD58C is included in Section 1.2. Each block is described in the detailed description section.

1.1 Features

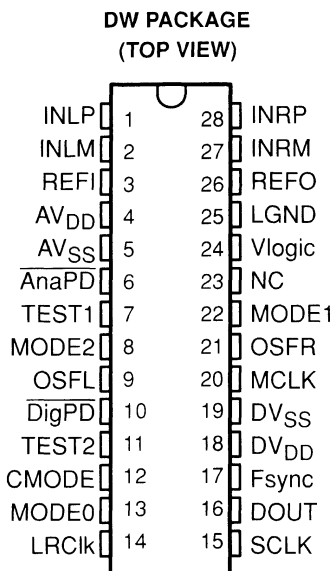
- Single 5-V Power Supply
- Sample Rates up to 48 kHz
- 18-Bit Resolution
- Signal-to-Noise Ratio (EIAJ) of 97 dB
- Dynamic Range of 95 dB
- Total Signal-to-Noise+Distortion of 95 dB
- Internal Reference Voltage (V_{ref})
- Serial-Port Interface
- Differential Architecture
- Power Dissipation of 200 mW. Power-Down Mode for Low-Power Applications
- One-Micron Advanced LinEPIC1Z™ Process

1.2 Functional Block Diagram



LinEPIC1Z is a trademark of Texas Instruments Incorporated.

1.3 Terminal Assignments



NC – No internal connection

1.4 Ordering Information

T_A	PACKAGE
	SMALL OUTLINE (DW)
0°C to 70°C	TLC320AD58CDW

1.5 Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AnaPD	6	I	Analog power-down mode. The analog power-down mode disables the analog modulators. The single-bit modulator outputs become invalid, rendering the outputs of the digital filters invalid. When AnaPD is pulled high, normal operation of the device is resumed.
AV _{DD}	4	I	Analog supply voltage
AV _{SS}	5	I	Analog ground
CMODE	12	I	Clock mode. CMODE is used to select between two methods of determining the master clock frequency. When CMODE is high, the master clock input is 384× the conversion frequency. When CMODE is low, the master clock input is 256× the conversion frequency.
DOUT	16	O	Data output. DOUT is used to transmit the sigma-delta audio ADC output data to a DSP serial port or other compatible serial interface and is synchronized to SCLK. This output is low when DigPD is high.
DV _{DD}	18	I	Digital supply voltage
DV _{SS}	19	I	Digital ground
DigPD	10	I	Digital power-down mode. The digital power-down mode shuts down the digital filters and clock generators. All digital outputs are brought to unasserted states. When DigPD is pulled high, normal operation of the device is resumed.
Fsync	17	I/O	Frame sync. Frame sync is used to designate the valid data from the ADC.

1.5 Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION																																				
INLM	2	I	Inverting input to left analog input amplifier																																				
INLP	1	I	Noninverting input to left analog input amplifier																																				
INRM	27	I	Inverting input to right analog input amplifier																																				
INRP	28	I	Noninverting input to right analog input amplifier																																				
LGND	25	I	Logic power supply ground for analog modulator																																				
LRCIk	14	I/O	Left/right clock. LRCIk signifies whether the serial data is associated with the left channel ADC (when LRCIk is high) or the right channel ADC (when LRCIk is low). LRCIk is low when $\overline{\text{DigPD}}$ is low.																																				
MCLK	20	I	Master clock. MCLK is used to derive all the key logic signals of the sigma-delta audio ADC. The nominal input frequency range is 18.432 MHz to 256 kHz.																																				
MODE(0–2)	13, 22, 8	I	<p>Serial modes. MODE(0–2) configure this device for many different modes of operation. The different configurations are:</p> <ul style="list-style-type: none"> Master versus slave 16 bit versus 18 bit MSB first versus LSB first Slave: Fsync controlled versus Fsync high <p>Each of these modes is described in the serial interface section along with timing diagrams.</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>MODE</th> <th>MASTER/ SLAVE</th> <th>BITS</th> <th>MSB/LSB FIRST</th> </tr> </thead> <tbody> <tr> <td>0 0 0</td> <td>slave</td> <td>up to 18</td> <td>MSB</td> </tr> <tr> <td>0 0 1</td> <td>slave</td> <td>18</td> <td>LSB</td> </tr> <tr> <td>0 1 0</td> <td>slave</td> <td>up to 18</td> <td>MSB</td> </tr> <tr> <td>0 1 1</td> <td>master</td> <td>16</td> <td>MSB</td> </tr> <tr> <td>1 0 0</td> <td>master</td> <td>18</td> <td>MSB</td> </tr> <tr> <td>1 0 1</td> <td>master</td> <td>18</td> <td>LSB</td> </tr> <tr> <td>1 1 0</td> <td>master</td> <td>16</td> <td>MSB</td> </tr> <tr> <td>1 1 1</td> <td>master</td> <td>16</td> <td>LSB</td> </tr> </tbody> </table>	MODE	MASTER/ SLAVE	BITS	MSB/LSB FIRST	0 0 0	slave	up to 18	MSB	0 0 1	slave	18	LSB	0 1 0	slave	up to 18	MSB	0 1 1	master	16	MSB	1 0 0	master	18	MSB	1 0 1	master	18	LSB	1 1 0	master	16	MSB	1 1 1	master	16	LSB
MODE	MASTER/ SLAVE	BITS	MSB/LSB FIRST																																				
0 0 0	slave	up to 18	MSB																																				
0 0 1	slave	18	LSB																																				
0 1 0	slave	up to 18	MSB																																				
0 1 1	master	16	MSB																																				
1 0 0	master	18	MSB																																				
1 0 1	master	18	LSB																																				
1 1 0	master	16	MSB																																				
1 1 1	master	16	LSB																																				
OSFL, OSFR	9, 21	O	Over scale flag left/right. If the left/right channel digital output exceeds full scale output range for two consecutive conversions, this flag is set high for 4096 LRCIk periods. OSFL and OSFR are low when $\overline{\text{DigPD}}$ is low.																																				
SCLK	15	I/O	Shift clock. If SCLK is configured as an input, SCLK is used to clock serial data out of the sigma-delta audio ADC. If SCLK is configured as an output, SCLK stops clocking when $\overline{\text{DigPD}}$ is low.																																				
TEST1	7	I	Test mode 1. TEST1 should be low for normal operation.																																				
TEST2	11	I	Test mode 2. TEST2 should be low for normal operation.																																				
REFI	3	I	Input voltage for modulator reference (normally connected to REFO, terminal 26).																																				
REFO	26	I	Internal voltage reference																																				
Vlogic	24	I	Logic power supply voltage (5 V) for analog modulator																																				

2 Detailed Description

The sigma-delta converter allows for simple antialias external filtering. Typically, a first order RC filter is sufficient.

2.1 Power-Down and Reset Functions

2.1.1 Power Down

The power-down state is comprised of a separate digital and analog power down. The power consumption of each is detailed in the electrical characteristics section.

The digital power-down mode shuts down the digital filters and clock generators. All digital outputs are set to an unasserted level. When the digital power-down terminal is pulled high, normal operation of the device is initiated. In slave mode, the conversion process must synchronize to an input on the LRCIk terminal as well as the SCLK terminal. Therefore, the conversion process is not initiated until the first rising edges of both SCLK and LRCIk are detected after $\overline{\text{DigPD}}$ is pulled high. This synchronizes the conversion cycle; all conversions are performed at a fixed LRCIk rate [MCLK/256 (CMODE low) or MCLK/384 (CMODE high)] after the initial synchronization. After the digital power-down terminal is brought high, the output of the digital filters remains invalid for 50 LRCIk cycles [see Figures 2–1(a) and 2–1(b)].

In master mode, LRCIk is an output; therefore, the conversion process initiates based on internal timing. The first valid data out occurs as shown in Figure 2–1(c).

The analog power-down mode disables the analog modulators. The single-bit modulator outputs become invalid which renders the outputs of the digital filters invalid. When the analog power-down terminal is brought high, the modulators are brought back online; however, the outputs of the digital filters require 50 LRCIk cycles for valid results.

2.1.2 Reset Function

The conversion process is not initiated until the first rising edges of both SCLK and LRCIk are detected after $\overline{\text{DigPD}}$ is pulled high. This synchronizes the conversion cycle; all conversions are performed at a fixed LRCIk rate [MCLK/256 (CMODE low) or MCLK/384 (CMODE high)] after the initial synchronization.

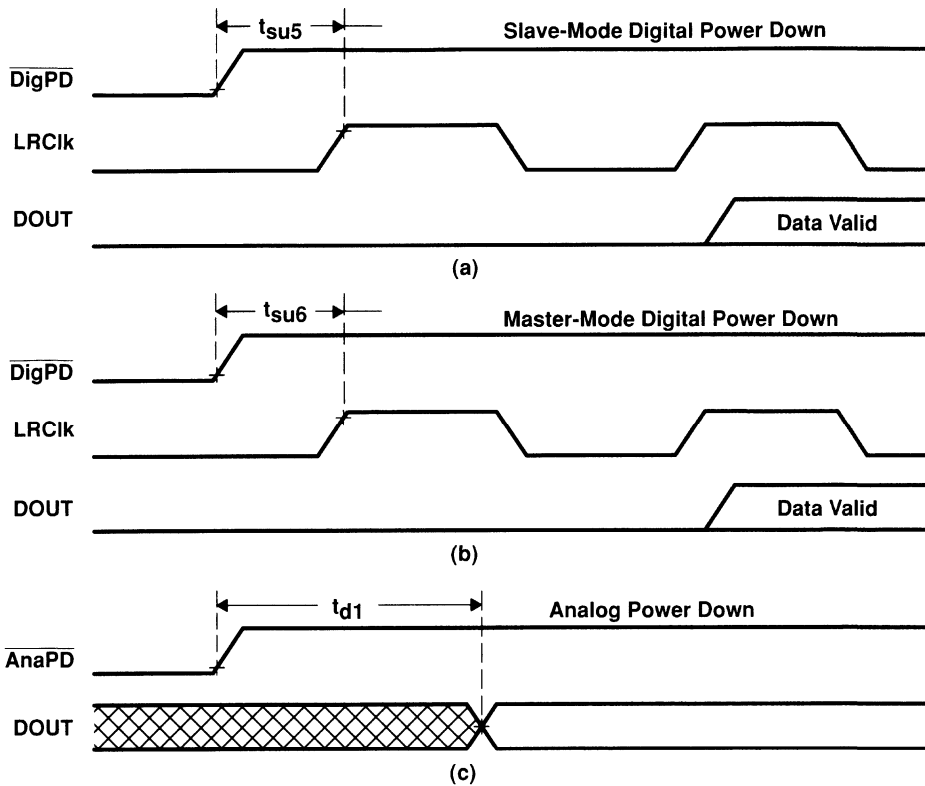


Figure 2–1. Power-Down Timing Relationships

2.2 Differential Input

The input is differential in order to provide common-mode noise rejection and increase the input dynamic range. Figure 2–2 shows the analog input signals used in a differential configuration to achieve a $6.4 V_{I(PP)}$ differential swing with a $3.2 V_{I(PP)}$ swing per input line. Both a differential and a single-ended configuration are shown in the application information section.

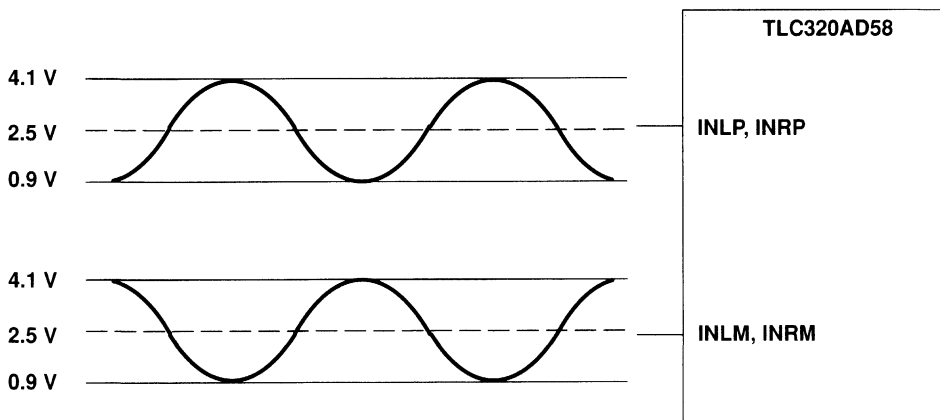


Figure 2–2. Differential Analog Input Configuration

2.3 Sigma-Delta Modulator

The modulator is a fourth-order sigma-delta modulator with 64 times oversampling. The ADC provides high-resolution, low-noise performance from a one-bit converter using oversampling techniques.

2.4 Decimation Filter

The decimation filter used after the sigma-delta modulator reduces the digital data rate to the sampling rate of LRCIk. This is accomplished by decimating with a ratio of 1:64. The output of this filter is a 2s complement data word of up to 18 bits serially clocked out.

If the input value exceeds the full range of the converter, the output of the decimator is held at the appropriate extreme until the input returns to the dynamic range of this device.

2.5 High-Pass Filter

The high-pass filter removes dc from the input.

2.6 Master-Clock Circuit

The master-clock circuit is used to generate and distribute necessary clocks throughout the device. MCLK is the external master clock input. CMODE is used to select the relationship of MCLK to the sample rate of LRCIk. When CMODE is low, the sample rate of the data paths is set as $LRCIk = MCLK/256$. When CMODE is high, the sample rate is set as $LRCIk = MCLK/384$. With a fixed oversampling ratio of $64\times$, the effect of changing MCLK is shown in Table 2–1.

When the TLC320AD58C is in master mode, SCLK is derived from MCLK in order to provide clocking of the serial communications between the sigma-delta audio ADC and a digital signal processor (DSP) or control logic. This is equivalent to a clock running at $64 \times LRCIk$.

When the TLC320AD58C is in slave mode, SCLK is externally derived.

**Table 2–1. Master-Clock to Sample-Rate Comparison
(Modes 1, 3, 4, 5)**

MCLK (MHz)	CMODE	SCLK (MHz)	LRCIk (kHz)
12.2880	Low	3.0720	48
18.4320	High		
11.2896	Low	2.8224	44.1
16.9344	High		
8.1920	Low	2.0480	32
12.2880	High		
0.2560	Low	0.0640	1
0.3840	High		

2.7 Test

TEST1 and TEST2 are reserved for factory test and should be tied to digital ground (DV_{SS}).

2.8 Serial Interface

Although the serial data is shifted out in two separate time packets that represent the left and right channels, the inputs are sampled and converted simultaneously.

The serial interface protocol has master and slave modes each with different read out modes. The master mode is used to source the control signals for conversion synchronization, while the slave mode allows an external controller to provide conversion synchronization signals.

The five master modes are shown in Figures 2–3(a) through 2–3(e), and the three slave modes are shown in Figures 2–4(a) through 2–4(c). For a 16-bit word, D15 is the most significant bit and D0 is the least significant bit. Unless otherwise specified, all values are in 2s complement format.

In master mode, SCLK is generated internally and is sourced as an output. The relationship of SCLK to LRCk is $64\times$ (modes 1, 3, 4, 5) or $32\times$ (modes 6, 7). In slave mode, SCLK is an input. SCLK timing must meet the timing specifications shown in the recommended operating conditions section.

2.8.1 Master Mode

As the master, the TLC320AD58C generates LRCk, Fsync, and SCLK from MCLK. These signals are provided for synchronizing the serial port of a digital signal processor (DSP) or other control devices.

Fsync is used to designate the valid data from the ADC, and this is accomplished in the master modes by one of two methods. The first is a single pulse on Fsync prior to valid data. This indicates the starting point for the data. The second method of frame synchronization is to hold Fsync high during the entire valid data cycle, which provides boundaries for the data.

LRCk is generated internally from MCLK. The frequency of this signal is fixed at the sampling frequency f_s [$MCLK/256$ (CMODE low) or $MCLK/384$ (CMODE high)]. During the high period of this signal, the left channel data is serially shifted to the output; during the low period, the right channel data is shifted to the output. The conversion cycle is synchronized with the rising edge of LRCk.

Five modes are available when the device is configured as a master. Two modes are for 18-bit communications. These modes differ from each other in that the MSB is transferred first in one mode while the LSB is transferred first in the second mode [see Figures 2–3(b) and 2–3(c)]. When the LSB is transferred first, the data is right justified to the LRCk [see Figures 2–3(a) through 2–3(e)]. The three other master modes are 16-bit modes. Once again, two of the modes differ as MSB first versus LSB first. These two modes set $SCLK = LRCk \times 32$. This is half the frequency used in the other transfer modes [see Figures 2–3(d) and 2–3(e)]. The third 16-bit mode provides the data MSB first with one clock delay after LRCk [see Figure 2–3(a)].

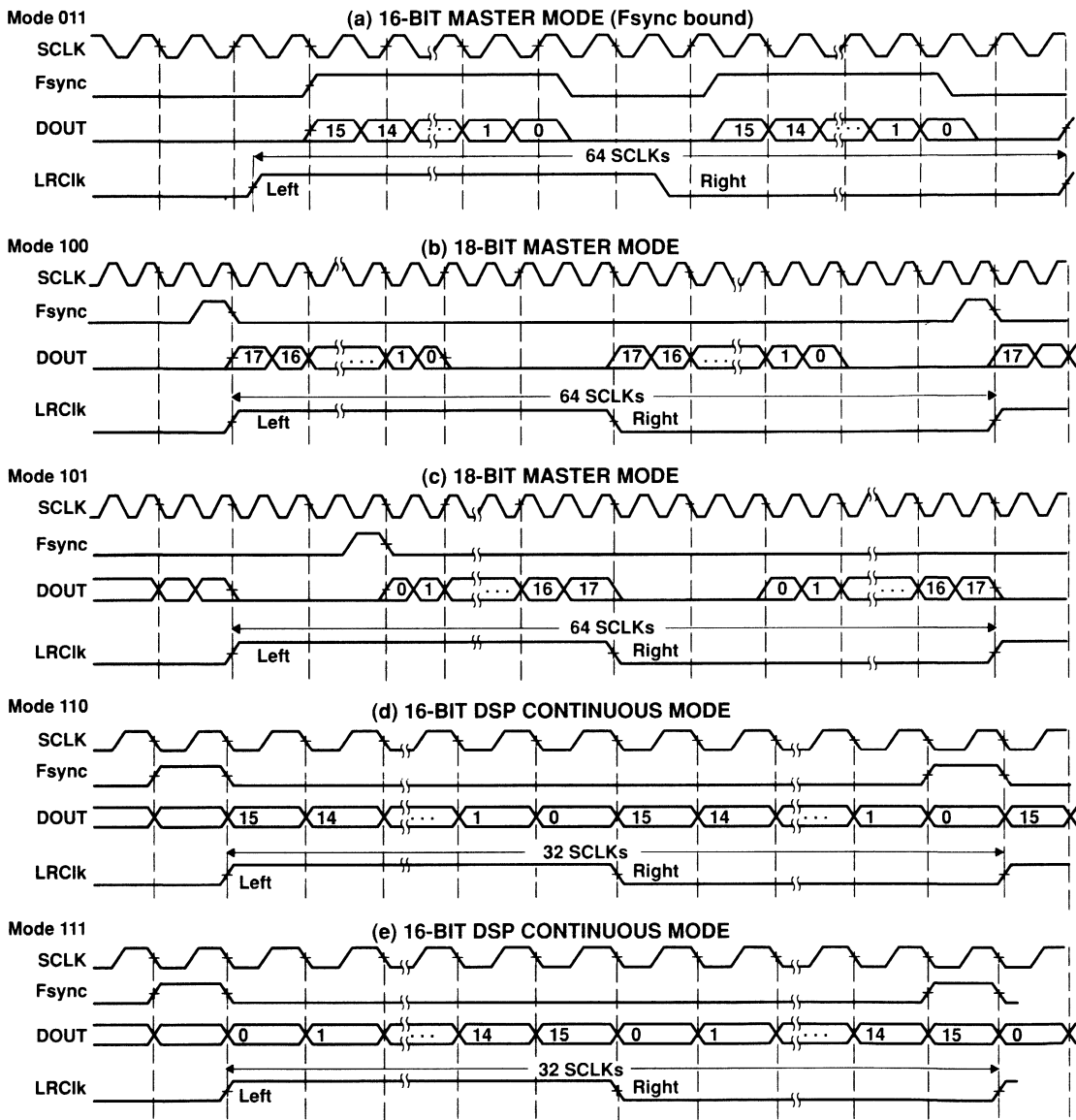


Figure 2-3. Serial Master Transfer Modes

2.8.2 Slave Mode

As a slave, the TLC320AD58C receives LRCIk, Fsync, and SCLK as inputs. The conversion cycle is synchronized to the rising edge of LRCIk, and the data is synchronized to the falling edge of SCLK. SCLK must meet the setup requirements specified in the recommended operating conditions section. Synchronization of the slave modes is accomplished with the digital power-down control.

In slave mode, Fsync is an input. Three modes are provided as shown in Figures 2-4(a) through 2-4(c). SCLK and LRCIk are externally generated and sourced. The first rising edges of SCLK and LRCIk after a power-down cycle initiate the conversion cycle. Refer to the master-mode section for signal functions.

Several modes are available when the TLC320AD58C is configured as a slave. Using the Mode0, Mode1, and Mode2 terminals, the TLC320AD58C can be set to shift out the MSB first or the LSB first [see Figures 2–4(a) and 2–4(b)]. The number of bits shifted out, however, can be controlled by the number of valid SCLK cycles provided within the left or right channel period. If only enough clocks are provided to shift out 16 data bits before LRCIk changes state, then this is equivalent to a 16-bit mode. Modes 1 and 2 both require 64 SCLK periods per LRCIk period.

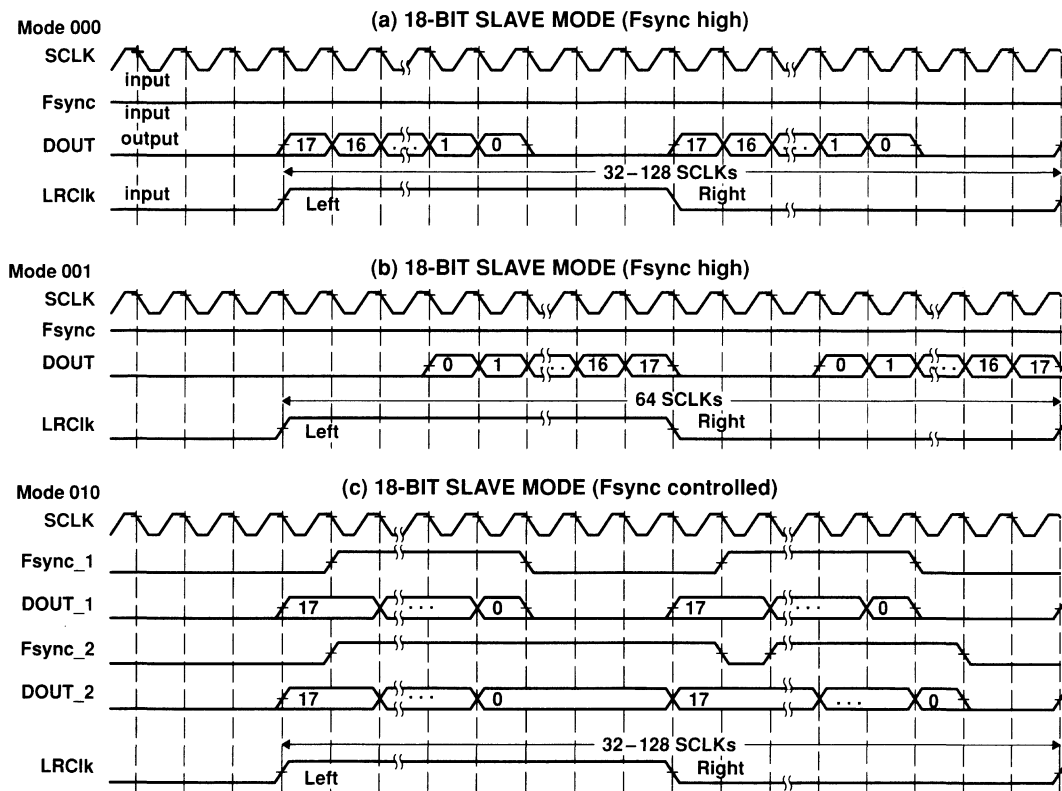


Figure 2–4. Serial Slave Transfer Modes

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage range, AV _{DD} (see Note 1)	−0.3 V to 6.5 V
Supply voltage range, DV _{DD} (see Note 2)	−0.3 V to 6.5 V
Analog input voltage range, INLP, INLM, INRP, INRM	−0.3 V to 6.5 V
Operating free-air temperature range, T _A	−0°C to 70°C
Storage temperature range, T _{stg}	−65°C to 150°C
Case temperature for 10 seconds	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values for maximum ratings are with respect to AV_{SS}.
2. Voltage values for maximum ratings are with respect to DV_{SS}.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Analog supply voltage, AV _{DD} (see Note 3)	4.75	5	5.25	V
Digital supply voltage, DV _{DD}	4.75	5	5.25	V
Analog logic supply voltage, V _{logic}	4.75	5	5.25	V
Reference voltage, V _{ref}		3.2		V
Setup time, SCLK↑ to LRCIk, slave mode, t _{su1}	30			ns
Setup time, LRCIk to SCLK↑, slave mode, t _{su2}	30			ns
Setup time, SCLK↑ to Fsync, slave mode, t _{su3}	30			ns
Setup time, Fsync to SCLK↑, slave mode, t _{su4}	30			ns
Setup time, $\overline{\text{DigPD}}$ to LRCIk↑, slave mode, t _{su5}		30		ns
Setup time, $\overline{\text{DigPD}}$ to LRCIk↑, master mode, t _{su6}		30		ns
Load resistance at DO _{UT} , R _L		10		kΩ
Input dc offset range	−50	0	50	mV
Operating free-air temperature, T _A	0		70	°C

NOTE 3: Voltages at analog inputs and outputs and AV_{DD} are with respect to the AV_{SS} terminal.

3.3 Electrical Characteristics

3.3.1 Digital Interface, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2	4.6		V
V_{IL}	Low-level input voltage			0.2	0.8	V
V_{OH}	High-level output voltage at DOUT	$I_{OH} = 2\text{ mA}$	2.4	4.6		V
V_{OL}	Low-level output voltage at DOUT	$I_{OL} = 2\text{ mA}$		0.2	0.4	V
I_{IH}	High-level input current, any digital input			1		μA
I_{IL}	Low-level input current, any digital input			1		μA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

3.3.2 Analog Interface

3.3.2.1 ADC Modulator, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V}$, $f_s = 48\text{ kHz}$, Bandwidth = 24 kHz, $\text{CMODE} = 0$, $\text{MODE}(0-2) = 000$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			18		Bits
DYNAMIC PERFORMANCE	ANSI A-weighting filter				
Signal to noise (EIAJ)	INLP = INRP = 2.5 V dc INLM = INRM = 2.5 V dc	96	100		dB
Dynamic range	-1 dB down from 6-V differential input	90	95		dB
Signal to noise + distortion (THD + N)		88	93		dB
Total harmonic distortion (THD)			0.0015%		
Interchannel isolation			120		dB
DC ACCURACY					
Absolute gain error			± 0.6		dB
Interchannel gain mismatch			± 0.2		dB
Offset error (18-bit resolution)			120 ± 5		mV
Offset drift			± 0.17		LSB/ $^\circ\text{C}$

3.3.2.2 Inputs/Supplies, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V}$, $f_s = 48\text{ kHz}$, Bandwidth = 24 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Input voltage range	(differential)		6.2		V
	(0 to peak)		3.1		
Input impedance			200		k Ω
POWER SUPPLIES					
Power-supply current	I_{DD} (analog), normal mode		24	32	mA
	I_{DD} (digital), normal mode		26	32	mA
	I_{DD} (analog), power down		250		μA
	I_{DD} (digital), power down		150		μA
Power dissipation			250		mW

3.3 Electrical Characteristics (Continued)

3.3.3 Channel Characteristics, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V}$, $f_S = 48\text{ kHz}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband (-3 dB)		0.001		24	kHz
Passband ripple	30 Hz – 21.8 kHz		± 0.01		dB
Stopband attenuation	26.2 kHz – 3046 kHz	80			dB
Group delay			$25/f_S$		s

3.4 Switching Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
t_{d1} Delay time, $\overline{\text{AnaPD}}$ to DOUT valid		30		ns
$t_{d(\text{MFSD})}$ Delay time, SCLK \downarrow to Fsync, master mode	-20		20	ns
$t_{d(\text{MDD})}$ Delay time, SCLK \downarrow to DOUT, master mode	0		50	ns
$t_{d(\text{MIRD})}$ Delay time, SCLK \downarrow to LRCIk, master mode	-20		20	ns
$t_{d(\text{SDD1})}$ Delay time, LRCIk to DOUT, slave mode			50	ns
$t_{d(\text{SDD2})}$ Delay time, SCLK \downarrow to DOUT, slave mode			50	ns

4 Parameter Measurement Information

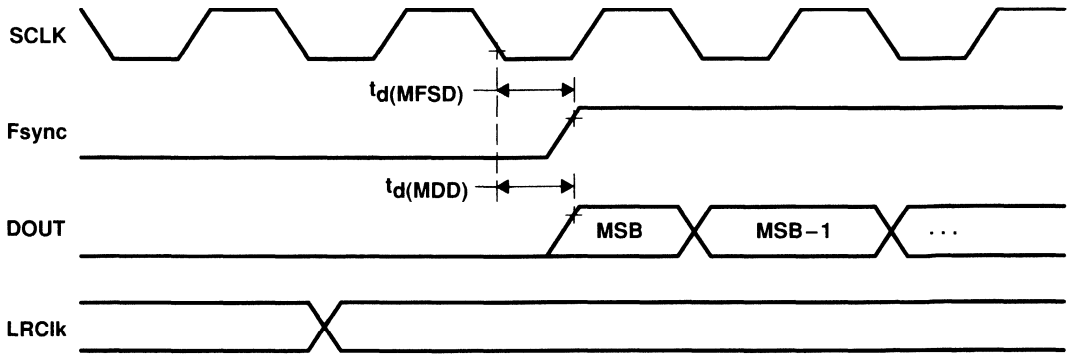


Figure 4-1. SCLK to Fsync and DOUT – Master Mode 3

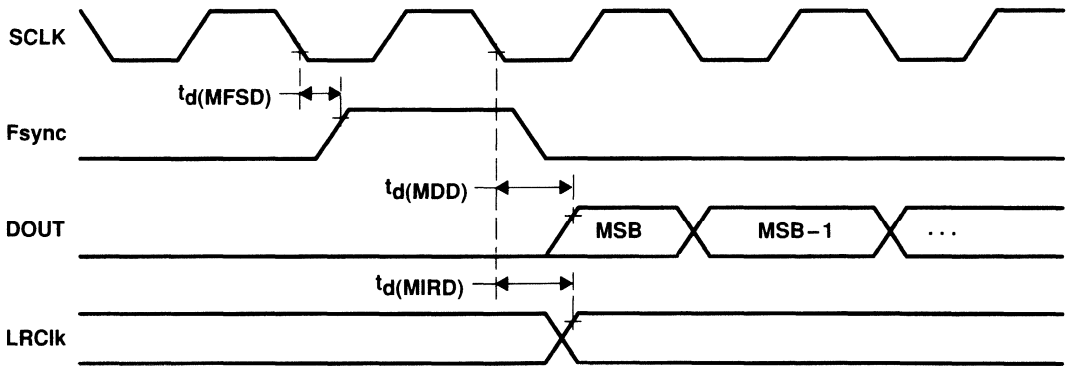


Figure 4-2. SCLK to Fsync, DOUT, and LRCIk – Master Modes 4 and 6

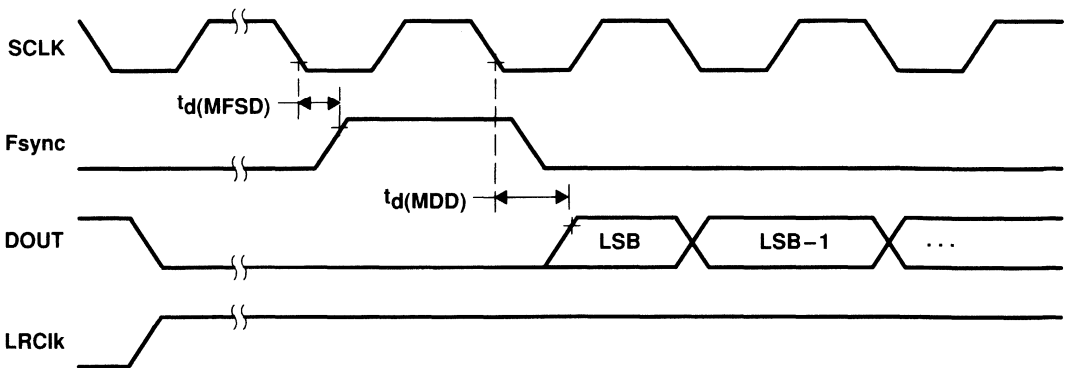


Figure 4-3. SCLK to Fsync, DOUT, and LRCIk – Master Mode 5

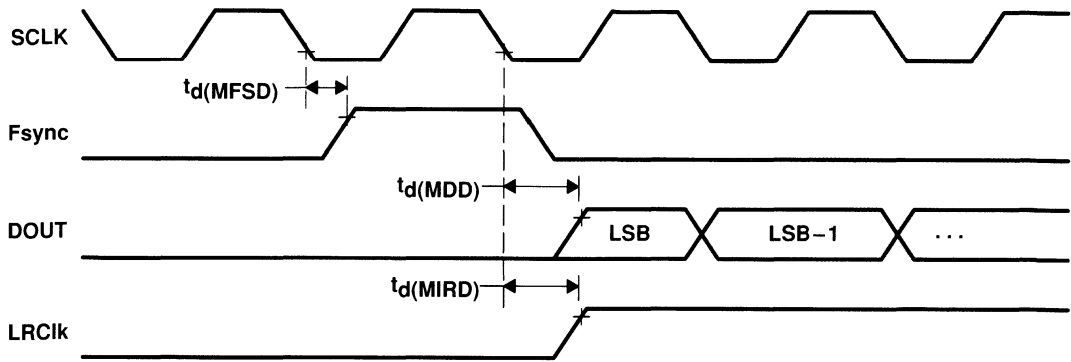


Figure 4-4. SCLK to Fsync, DOUT, and LRCIk – Master Mode 7

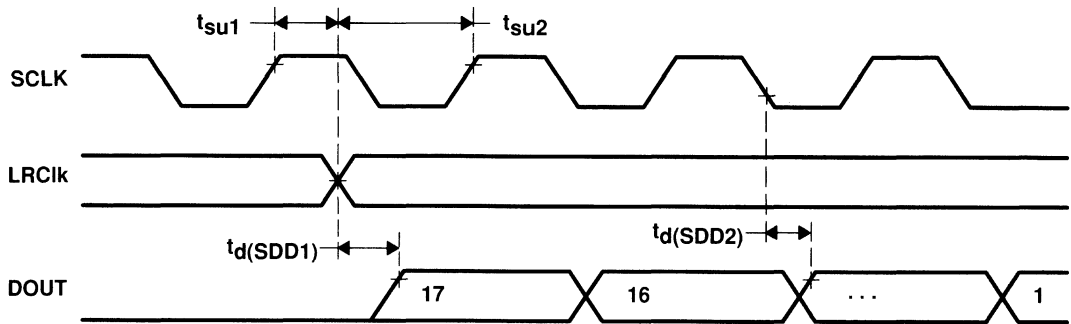


Figure 4-5. SCLK to LRCIk and DOUT – Slave Mode 0, Fsync High

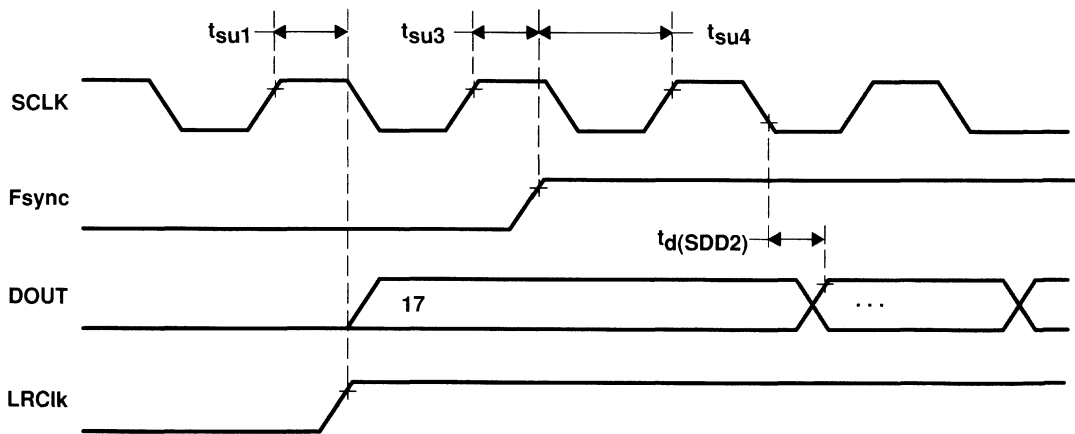


Figure 4-6. SCLK to Fsync, LRCIk, and DOUT – Slave Mode 2, Fsync Controlled

5 Application Information

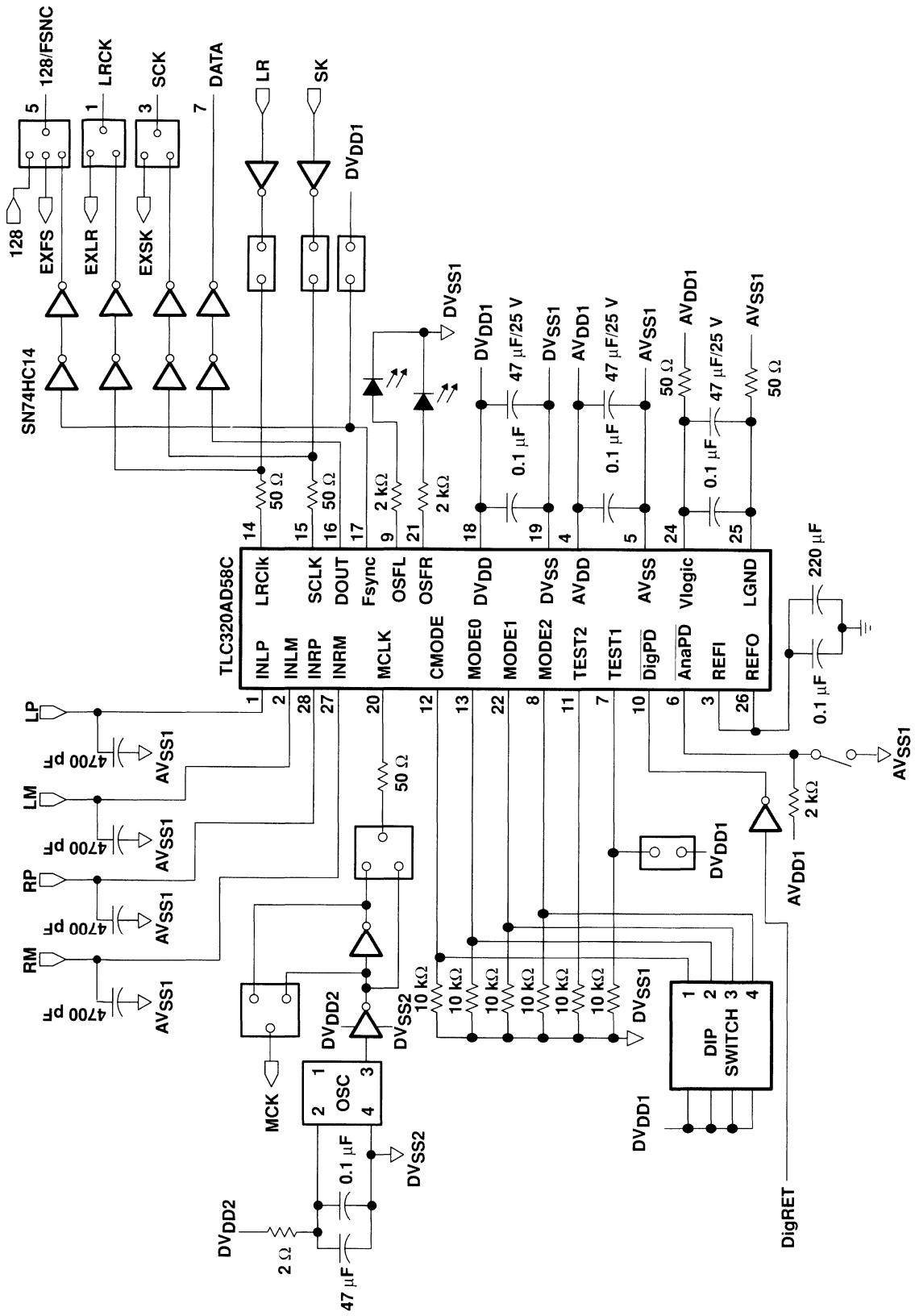


Figure 5-1. TLC320AD58C Configuration Schematic

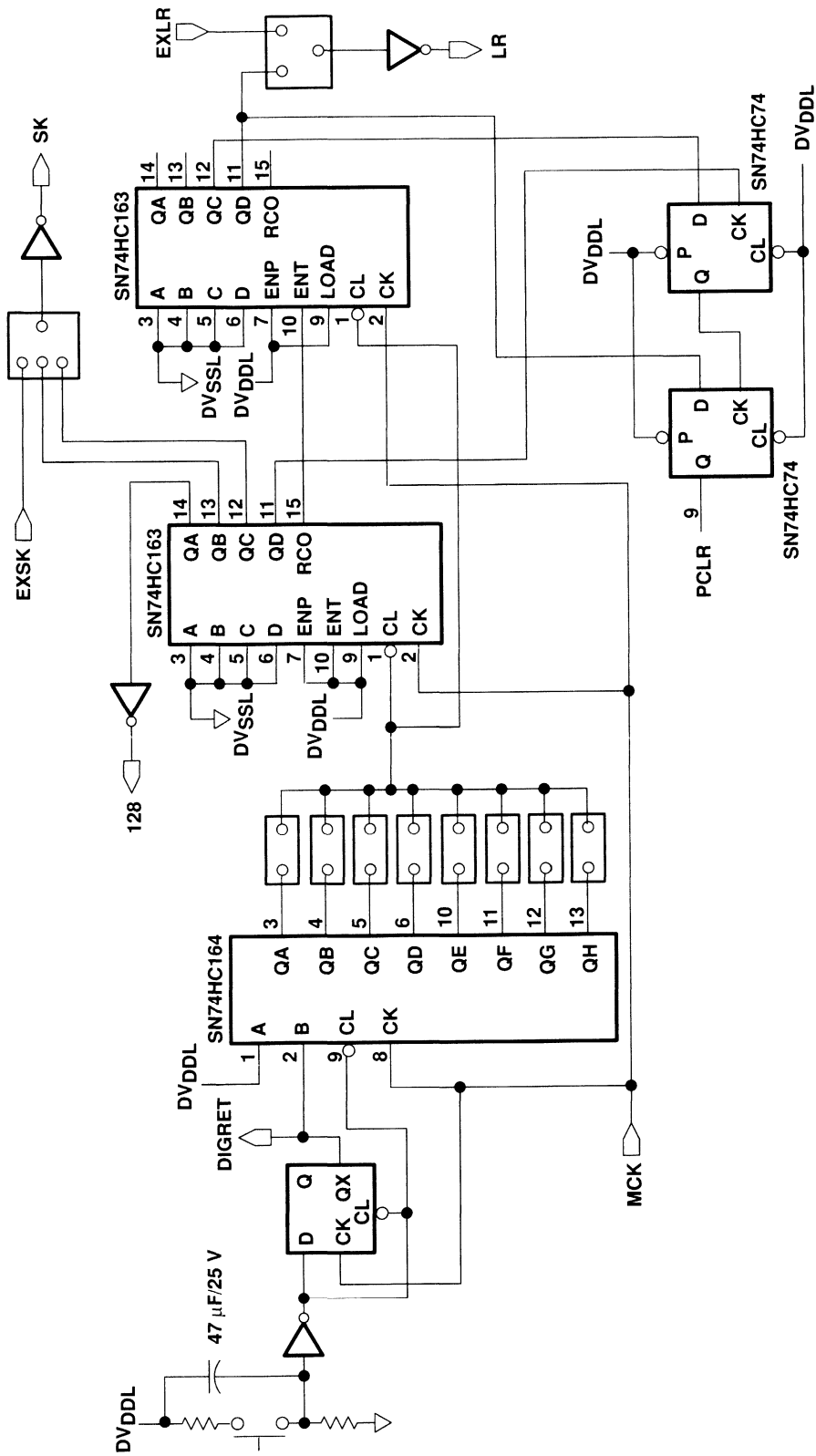


Figure 5-2. TLC320AD58C External Digital Timing and Control-Signal Generation Schematic

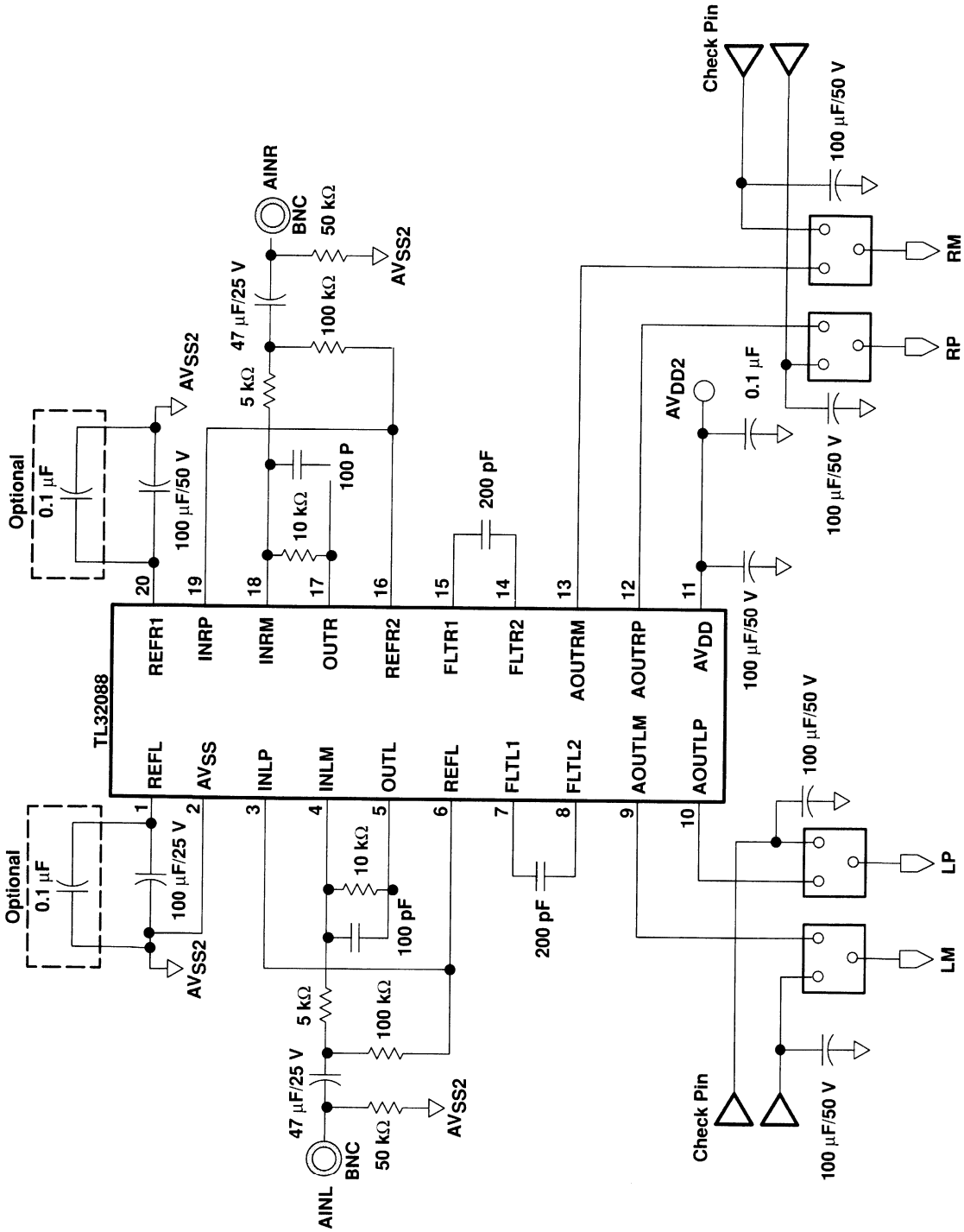


Figure 5-3. TLC320AD58C External Analog Input Buffer Schematic

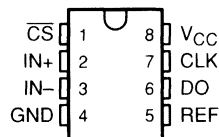
TLV0831C, TLV0831I
TLV0832C, TLV0832I

3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

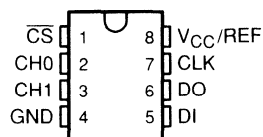
SLAS148 – SEPTEMBER 1996

- **8-Bit Resolution**
- **2.7 V to 3.6 V V_{CC}**
- **Easy Microprocessor Interface or Standalone Operation**
- **Operates Ratiometrically or With V_{CC} Reference**
- **Single Channel or Multiplexed Twin Channels With Single-Ended or Differential Input Options**
- **Input Range 0 V to V_{CC} With V_{CC} Reference**
- **Inputs and Outputs Are Compatible With TTL and MOS**
- **Conversion Time of 32 μ s at $f_{(CLK)} = 250$ kHz**
- **Designed to Be Functionally Equivalent to the National Semiconductor ADC0831 and ADC0832 at 3 V Supply**
- **Total Unadjusted Error . . . ± 1 LSB**

TLV0831 . . . D OR P PACKAGE
(TOP VIEW)



TLV0832 . . . D OR P PACKAGE
(TOP VIEW)



description

These devices are 8-bit successive-approximation analog-to-digital converters. The TLV0831 has single input channels; the TLV0832 has multiplexed twin input channels. The serial output is configured to interface with standard shift registers or microprocessors.

The TLV0832 multiplexer is software configured for single-ended or differential inputs. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

The operation of the TLV0831 and TLV0832 devices is very similar to the more complex TLV0834 and TLV0838 devices. Ratiometric conversion can be attained by setting the REF input equal to the maximum analog input signal value, which gives the highest possible conversion resolution. Typically, REF is set equal to V_{CC} (done internally on the TLV0832).

The TLV0831C and TLV0832C are characterized for operation from 0°C to 70°C. The TLV0831I and TLV0832I are characterized for operation from -40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGE			
	SMALL OUTLINE (D)		PLASTIC DIP (P)	
0°C to 70°C	TLV0831CD	TLV0832CD	TLV0831CP	TLV0832CP
-40°C to 85°C	TLV0831ID	TLV0832ID	TLV0831IP	TLV0832IP

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

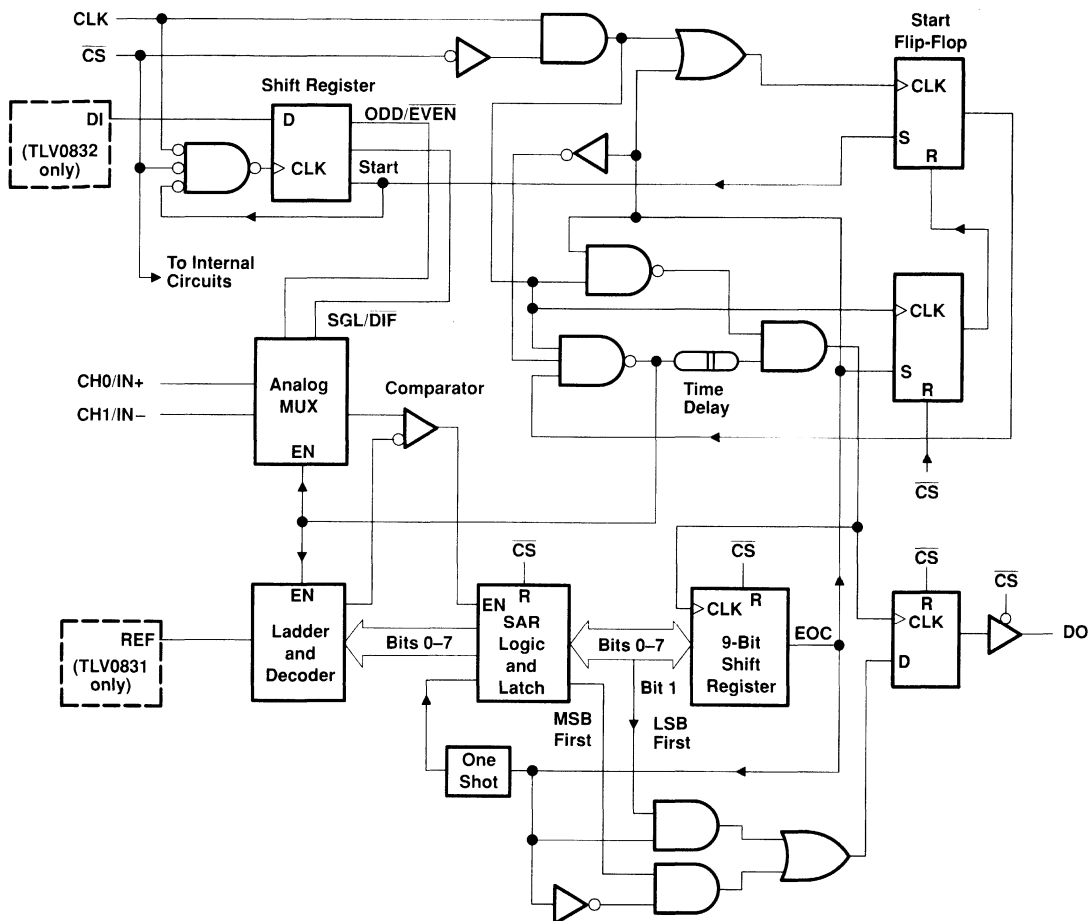


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TLV0831C, TLV0831
 TLV0832C, TLV0832I
3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL
 SLAS148 - SEPTEMBER 1996

functional block diagram



functional description

The TLV0831 and TLV0832 use a sample-data-comparator structure that converts differential analog inputs by a successive-approximation routine. The input voltage to be converted is applied to an input terminal and is compared to ground (single ended), or to an adjacent input (differential). The TLV0832 input terminals can be assigned a positive (+) or negative (–) polarity. The TLV0831 contains only one differential input channel with fixed polarity assignment; therefore it does not require addressing. The signal can be applied differentially, between IN+ and IN–, to the TLV0831 or can be applied to IN+ with IN– grounded as a single ended input. When the signal input applied to the assigned positive terminal is less than the signal on the negative terminal, the converter output is all zeros.

Channel selection and input configuration are under software control using a serial-data link from the controlling processor. A serial-communication format allows more functions to be included in a converter package with no increase in size. In addition, it eliminates the transmission of low-level analog signals by locating the converter at the analog sensor and communicating serially with the controlling processor. This process returns noise-free digital data to the processor.

A conversion is initiated by setting \overline{CS} low, which enables all logic circuits. \overline{CS} must be held low for the complete conversion process. A clock input is then received from the processor. An interval of one clock period is automatically inserted to allow the selected multiplexed channel to settle. DO comes out of the high-impedance state and provides a leading low for one clock period of multiplexer settling time. The SAR comparator compares successive outputs from the resistive ladder with the incoming analog signal. The comparator output indicates whether the analog input is greater than or less than the resistive-ladder output. As the conversion proceeds, conversion data is simultaneously output from DO, with the most significant bit (MSB) first. After eight clock periods, the conversion is complete. When \overline{CS} goes high, all internal registers are cleared. At this time, the output circuits go to the high-impedance state. If another conversion is desired, \overline{CS} must make a high-to-low transition followed by address information.

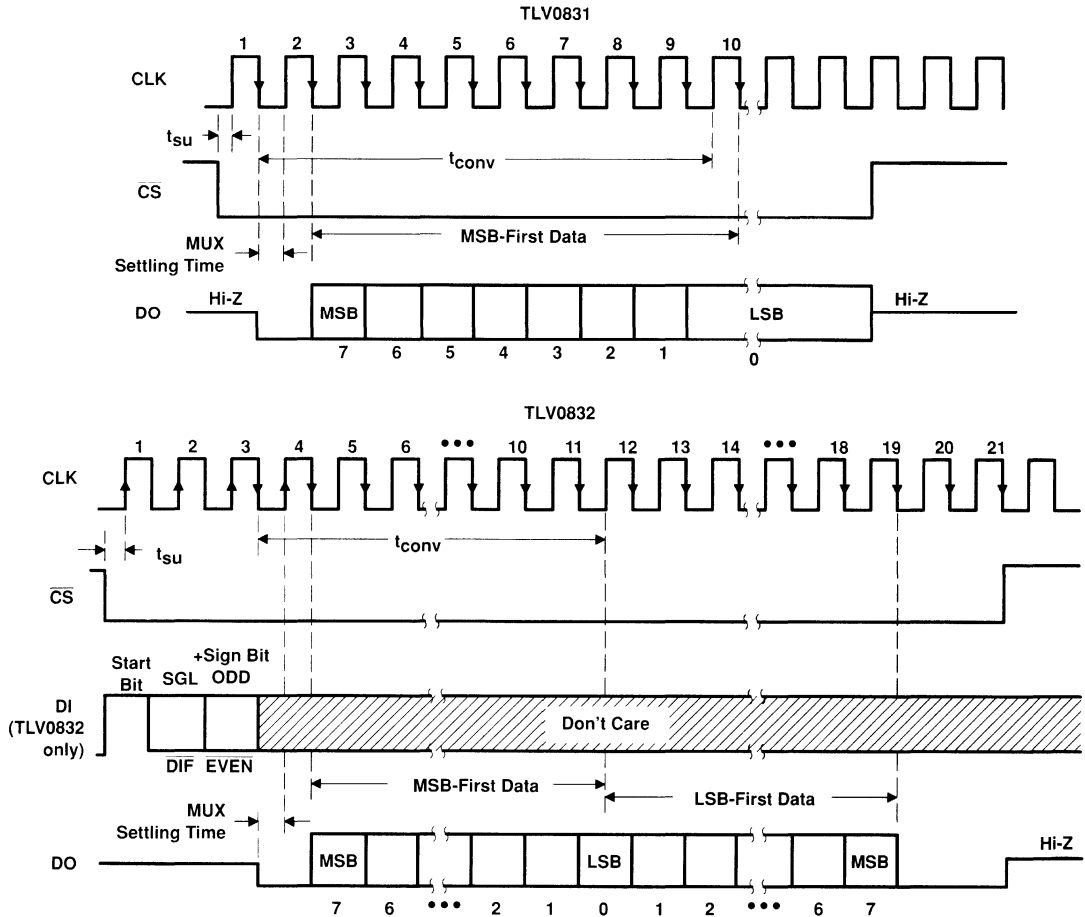
A TLV0832 input configuration is assigned during the multiplexer-addressing sequence. The multiplexer address shifts into the converter through the data input (DI) line. The multiplexer address selects the analog inputs to be enabled and determines whether the input is single ended or differential. When the input is differential, the polarity of the channel input is assigned. In addition to selecting the differential mode, the polarity may also be selected. Either channel of the channel pair may be designated as the negative or positive input.

On each low-to-high transition of the clock input, the data on DI is clocked into the multiplexer-address shift register. The first logic high on the input is the start bit. A 2-bit assignment word follows the start bit on the TLV0832. On each successive low-to-high transition of the clock input, the start bit and assignment word are shifted through the shift register. When the start bit is shifted into the start location of the multiplexer register, the input channel is selected and conversion starts. The TLV0832 DI terminal to the multiplexer shift register is disabled for the duration of the conversion.

The TLV0832 outputs the least-significant-bit (LSB) first data after the MSB-first data stream. The DI and DO terminals can be tied together and controlled by a bidirectional processor I/O bit received on a single wire. This is possible because DI is only examined during the multiplexer-addressing interval and DO is still in the high-impedance state.

TLV0831C, TLV0831I
TLV0832C, TLV0832I
3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL
 SLAS148 – SEPTEMBER 1996

sequence of operation



TLV0832 MUX-ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS		CHANNEL NUMBER	
SGL/DIF	ODD/EVEN	CH0	CH1
L	L	+	-
L	H	-	+
H	L	+	-
H	H	-	+

H = high level, L = low level,
 - or + = terminal polarity for the selected input channel

TLV0831C, TLV0831I
TLV0832C, TLV0832I

3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS148 – SEPTEMBER 1996

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range, V_I : Logic	–0.3 V to $V_{CC} + 0.3$ V
Analog	–0.3 V to $V_{CC} + 0.3$ V
Input current, I_I	±5 mA
Total input current	±20 mA
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see clock operating conditions)		2.7	3.3	3.6	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Clock frequency, $f_{(CLK)}$	$V_{CC} = 2.7$ V			250	kHz
	$V_{CC} = 3.3$ V	10		600	kHz
Clock duty cycle (see Note 2)		40%		60%	
Pulse duration, \overline{CS} high, $t_{wH}(CS)$		220			ns
Setup time, \overline{CS} low or TLV0832 data valid before $CLK\uparrow$, t_{SU}		350			ns
Hold time, TLV0832 data valid after $CLK\uparrow$, t_H		90			ns
Operating free-air temperature, T_A	C suffix	0		70	°C
	I suffix	–40		85	

NOTE 2: The clock-duty-cycle range ensures proper operation at all clock frequencies. When a clock frequency is used outside the recommended duty-cycle range, the minimum pulse duration (high or low) is 1 μ s.

TLV0831C, TLV0831I
TLV0832C, TLV0832I
3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL
 SLAS148 – SEPTEMBER 1996

electrical characteristics over recommended range of operating free-air temperature, $V_{CC} = 3.3\text{ V}$, $f_{(CLK)} = 250\text{ kHz}$ (unless otherwise noted)

digital section

PARAMETER	TEST CONDITION†	C SUFFIX			I SUFFIX			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH} High-level output voltage	$V_{CC} = 3\text{ V}$, $I_{OH} = -360\ \mu\text{A}$	2.8			2.4			V
	$V_{CC} = 3\text{ V}$, $I_{OH} = -10\ \mu\text{A}$	2.9			2.8			
V_{OL} Low-level output voltage	$V_{CC} = 3\text{ V}$, $I_{OL} = 1.6\text{ mA}$				0.4			V
I_{IH} High-level input current	$V_{IH} = 3.6\text{ V}$	0.005			1			μA
I_{IL} Low-level input current	$V_{IL} = 0$	-0.005			-1			μA
I_{OH} High-level output (source) current	At V_{OH} , $DO = 0\text{ V}$, $T_A = 25^\circ\text{C}$	-6.5	-15		-6.5	-15		mA
I_{OL} Low-level output (sink) current	At V_{OL} , $DO = 0\text{ V}$, $T_A = 25^\circ\text{C}$	8	-16		8	-16		mA
I_{OZ} High-impedance-state output current (DO)	$V_O = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$	0.01			3			μA
	$V_O = 0$, $T_A = 25^\circ\text{C}$	-0.01			-3			
C_i Input capacitance		5			5			pF
C_o Output capacitance		5			5			pF

† All parameters are measured under open-loop conditions with zero common-mode input voltage.

‡ All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

analog and converter section

PARAMETER	TEST CONDITION†	MIN	TYP‡	MAX	UNIT
V_{IC} Common-mode input voltage	See Note 3	-0.05 to $V_{CC} + 0.05$			V
$I_{I(stdb)}$ Standby input current (see Note 4)	On channel	$V_I = 3.3\text{ V}$			1
	Off channel	$V_I = 0$			-1
	On channel	$V_I = 0$			-1
	Off channel	$V_I = 3.3\text{ V}$			1
$r_{i(REF)}$ Input resistance to REF		1.3	2.4	5.9	k Ω

† All parameters are measured under open-loop conditions with zero common-mode input voltage.

‡ All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

- NOTES: 3. When channel IN- is more positive than channel IN+, the digital output code is 0000 0000. Connected to each analog input are two on-chip diodes that conduct forward current for analog input voltages one diode drop above V_{CC} . Care must be taken during testing at low V_{CC} levels (3 V) because high-level analog input voltage (3.6 V) can, especially at high temperatures, cause the input diode to conduct and cause errors for analog inputs that are near full scale. As long as the analog voltage does not exceed the supply voltage by more than 50 mV, the output code is correct. To achieve an absolute 0- to 3.3-V input range requires a minimum V_{CC} of 3.25 V for all variations of temperature and load.
4. Standby input currents go in or out of the on or off channels when the A/D converter is not performing conversion and the clock is in a high or low steady-state conditions.

total device

PARAMETER	MIN	TYP‡	MAX	UNIT
I_{CC} Supply current	TLV0831	0.2	0.75	mA
	TLV0832	1.5	2.5	

‡ All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.



TLV0831C, TLV0831I
TLV0832C, TLV0832I
3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL
SLAS148 – SEPTEMBER 1996

operating characteristics $V_{CC} = V_{ref} = 3.3\text{ V}$, $f_{(CLK)} = 250\text{ kHz}$, $t_r = t_f = 20\text{ ns}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Supply-voltage variation error		$V_{CC} = 3\text{ V to }3.6\text{ V}$		$\pm 1/16$	$\pm 1/4$	LSB
Total unadjusted error (see Note 5)		$V_{ref} = 3.3\text{ V}$, $T_A = \text{MIN to MAX}$			± 1	LSB
Common-mode error		Differential mode		$\pm 1/16$	$\pm 1/4$	LSB
t_{pd}	Propagation delay time, output data after $CLK\uparrow$ (see Note 6)	MSB-first data	$C_L = 100\text{ pF}$	200	500	ns
		LSB-first data		80	200	
t_{dis}	Output disable time, DO after $\overline{CS}\uparrow$	$C_L = 10\text{ pF}$, $R_L = 10\text{ k}\Omega$	80	125	250	ns
		$C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$				
t_{conv}	Conversion time (multiplexer-addressing time not included)				8	clock periods

† All parameters are measured under open-loop conditions with zero common-mode input voltage. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

- NOTES: 5. Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.
6. The MSB-first data is output directly from the comparator and, therefore, requires additional delay to allow for comparator response time. LSB-first data applies only to TLV0832.



TLV0831C, TLV0831I
 TLV0832C, TLV0832I
3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL
 SLAS148 – SEPTEMBER 1996

PARAMETER MEASUREMENT INFORMATION

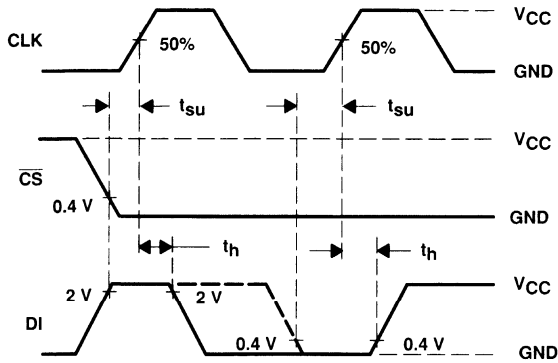


Figure 1. TLV0832 Data-Input Timing

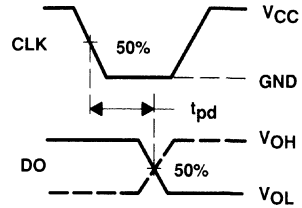
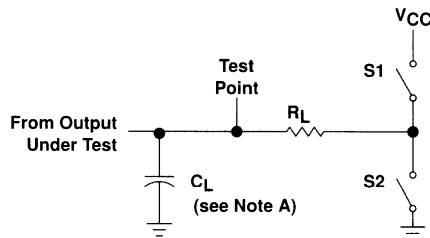
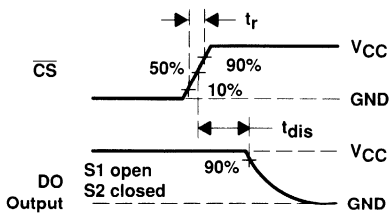


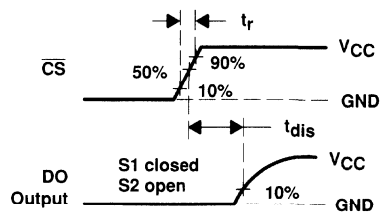
Figure 2. Data-Output Timing



LOAD CIRCUIT



VOLTAGE WAVEFORMS



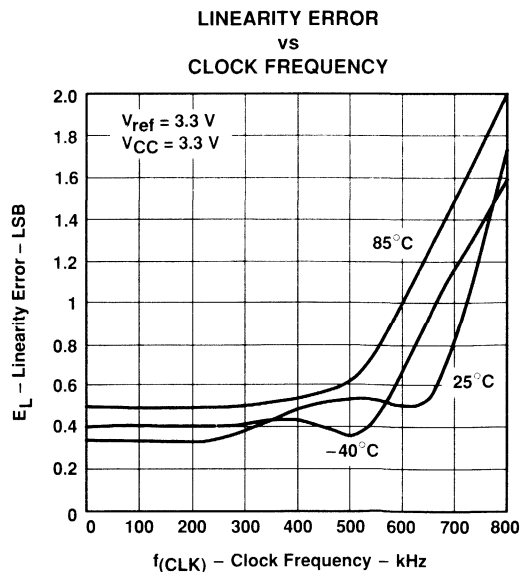
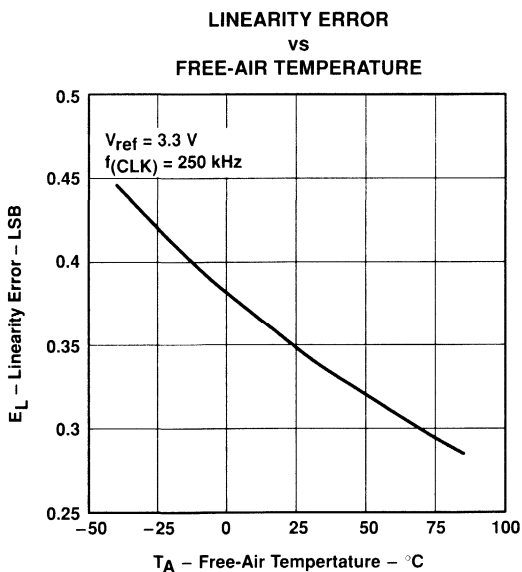
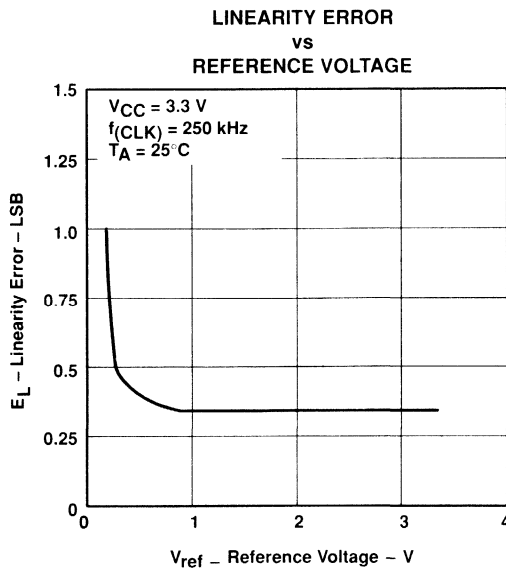
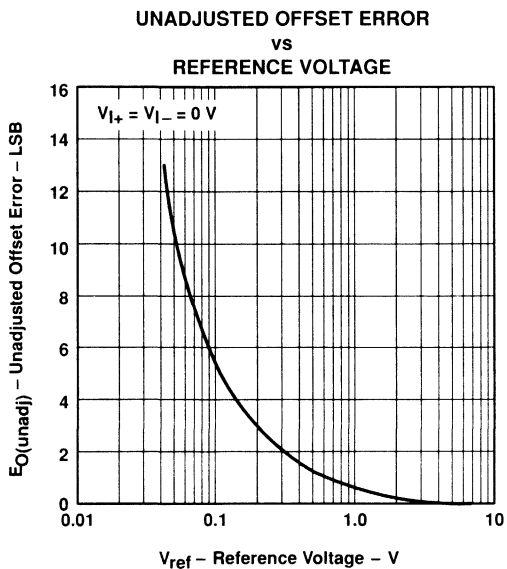
VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 3. Output Disable Time Test Circuit and Voltage Waveforms



TYPICAL CHARACTERISTICS



TLV0831C, TLV0831I
TLV0832C, TLV0832I
3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL
 SLAS148 – SEPTEMBER 1996

TYPICAL CHARACTERISTICS

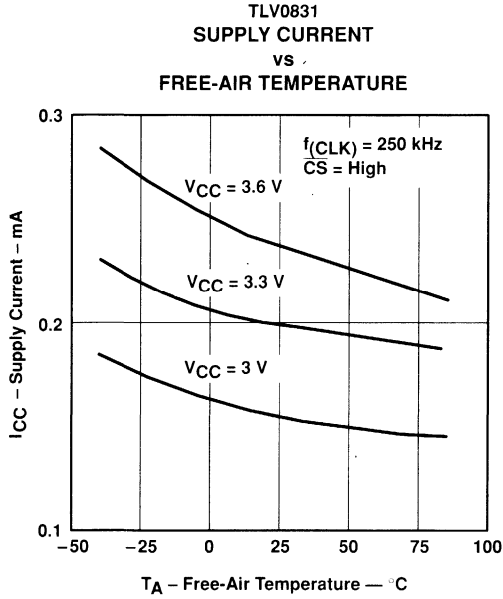


Figure 8

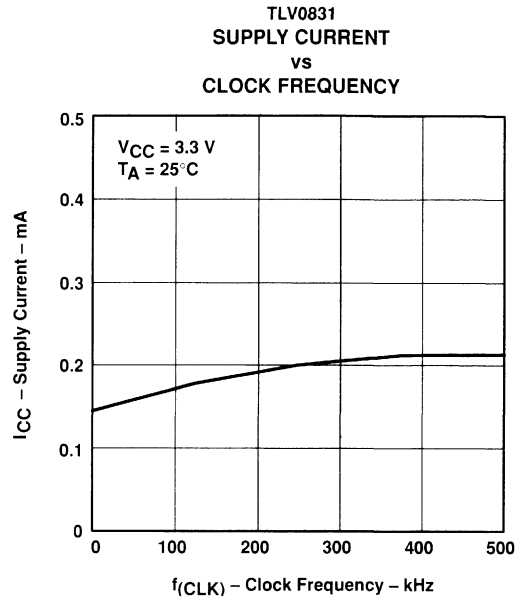


Figure 9

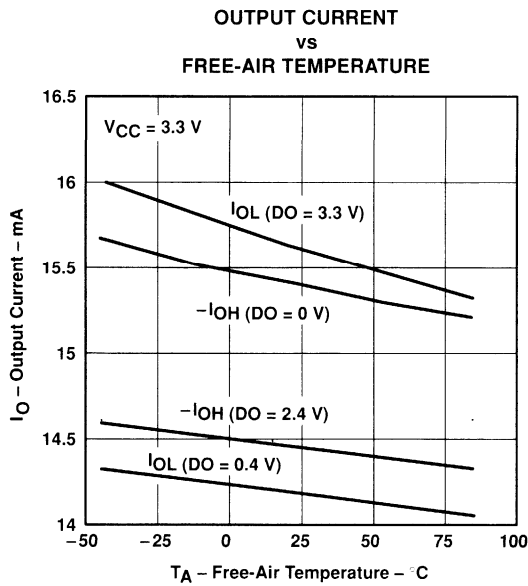


Figure 10

TYPICAL CHARACTERISTICS

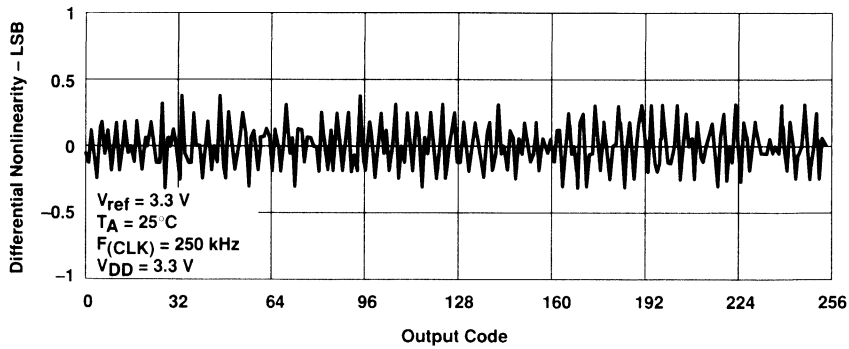


Figure 11. Differential Nonlinearity With Output Code

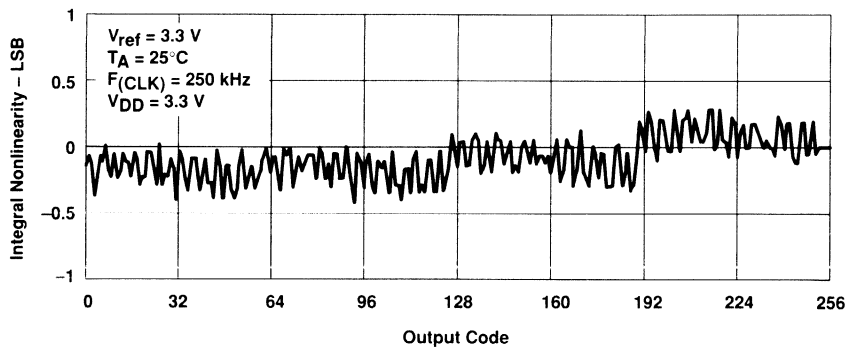


Figure 12. Integral Nonlinearity With Output Code

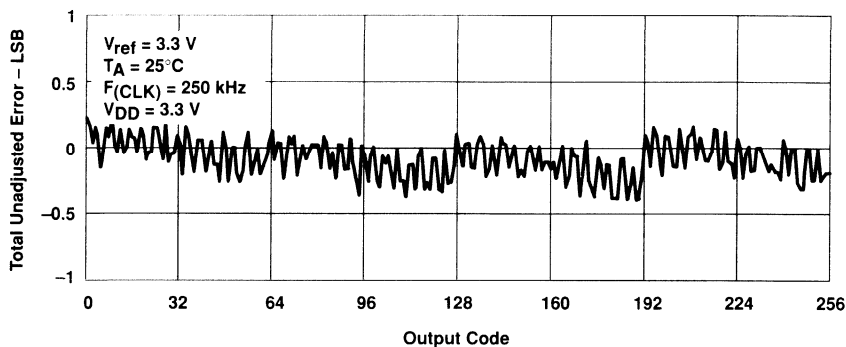


Figure 13. Total Unadjusted Error With Output Code

TLV0834C, TLV0834I, TLV0838C, TLV0838I

3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS147 – SEPTEMBER 1996

- **8-Bit Resolution**
- **2.7 V to 3.6 V V_{CC}**
- **Easy Microprocessor Interface or Standalone Operation**
- **Operates Ratiometrically or With V_{CC} Reference**
- **4- or 8-Channel Multiplexer Options With Address Logic**
- **Input Range 0 V to V_{CC} With V_{CC} Reference**
- **Remote Operation With Serial Data Link**
- **Inputs and Outputs Are Compatible With TTL and MOS**
- **Conversion Time of 32 μ s at $f_{(CLK)} = 250$ kHz**
- **Functionally Equivalent to the ADC0834 and ADC0838 at 3-V Supply Without the Internal Zener Regulator Network**
- **Total Unadjusted Error . . . ± 1 LSB**

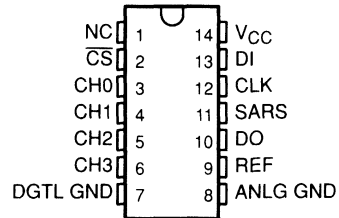
description

These devices are 8-bit successive-approximation analog-to-digital converters, each with an input-configurable multichannel multiplexer and serial input/output. The serial input/output is configured to interface with standard shift registers or microprocessors. Detailed information on interfacing with most popular microprocessors is readily available from the factory.

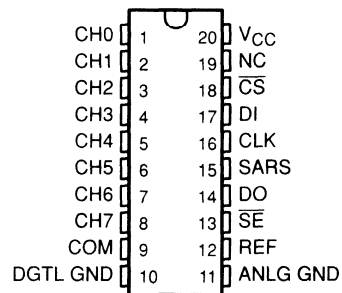
The TLV0834 (4-channel) and TLV0838 (8-channel) multiplexer is software configured for single-ended or differential inputs as well as pseudo-differential input assignments. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding of any smaller analog voltage span to the full 8 bits of resolution.

The TLV0834C and TLV0838C are characterized for operation from 0°C to 70°C. The TLV0834I and TLV0838I are characterized for operation from -40°C to 85°C.

TLV0834 . . . D OR N PACKAGE
(TOP VIEW)



TLV0838 . . . DW OR N PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T _A	PACKAGE		
	SMALL OUTLINE (D)	SMALL OUTLINE (DW)	PLASTIC DIP (N)
0°C to 70°C	TLV0834CD	TLV0838CDW	TLV0834CN TLV0838CN
-40°C to 85°C	TLV0834ID	TLV0838IDW	TLV0834IN TLV0838IN

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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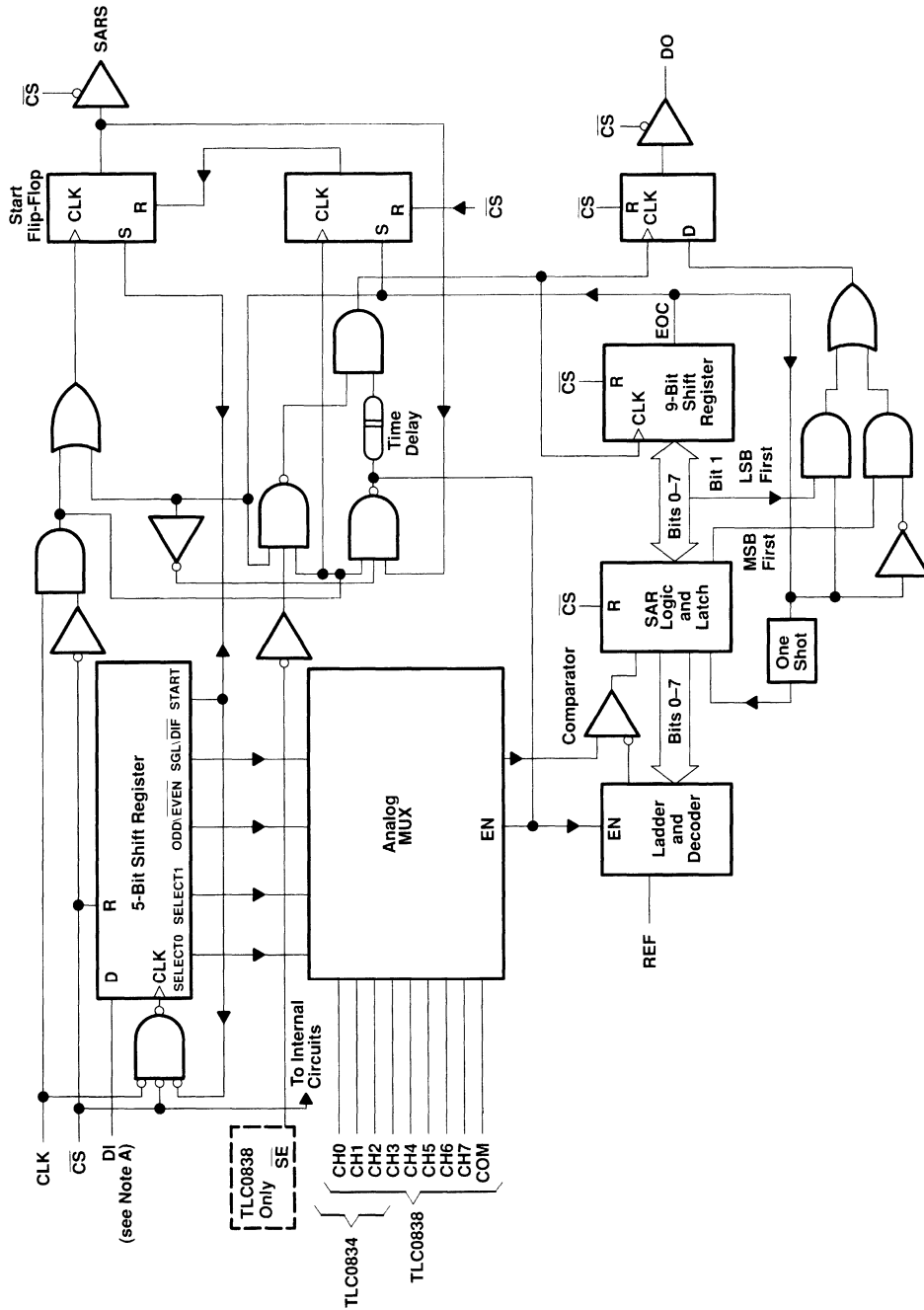
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TLV0834C, TLV0834I, TLV0838C, TLV0838I

3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS147 – SEPTEMBER 1996

functional block diagram



NOTE A: For the TLC0834, \overline{DI} is input directly to the D input of $\overline{SELECT1}$; $\overline{SELECT0}$ is forced to a high.

TLV0834C, TLV0834I, TLV0838C, TLV0838I

3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS147 – SEPTEMBER 1996

functional description

The TLV0834 and TLV0838 use a sample-data-comparator structure that converts differential analog inputs by a successive-approximation routine. Operation of both devices is similar with the exception of \overline{SE} , an analog common input, and multiplexer addressing. The input voltage to be converted is applied to a channel terminal and is compared to ground (single ended), to an adjacent input (differential), or to a common terminal (pseudo differential) that can be an arbitrary voltage. The input terminals are assigned a positive (+) or negative (–) polarity. When the signal input applied to the assigned positive terminal is less than the signal on the negative terminal, the converter output is all zeros.

Channel selection and input configuration are under software control using a serial-data link from the controlling processor. A serial-communication format allows more functions to be included in a converter package with no increase in size. In addition, it eliminates the transmission of low-level analog signals by locating the converter at the analog sensor and communicating serially with the controlling processor. This process returns noise-free digital data to the processor.

A particular input configuration is assigned during the multiplexer-addressing sequence. The multiplexer address shifts into the converter through the data input (DI) line. The multiplexer address selects the analog inputs to be enabled and determines whether the input is single ended or differential. When the input is differential, the polarity of the channel input is assigned. Differential inputs are assigned to adjacent channel pairs. For example, channel 0 and channel 1 may be selected as a differential pair. These channels cannot act differentially with any other channel. In addition to selecting the differential mode, the polarity may also be selected. Either channel of the channel pair may be designated as the negative or positive input.

The common input on the TLV0838 can be used for a pseudo-differential input. In this mode, the voltage on the common input is considered to be the negative differential input for all channel inputs. This voltage can be any reference potential common to all channel inputs. Each channel input can then be selected as the positive differential input. This feature is useful when all analog circuits are biased to a potential other than ground.

A conversion is initiated by setting \overline{CS} low, which enables all logic circuits. \overline{CS} must be held low for the complete conversion process. A clock input is then received from the processor. On each low-to-high transition of the clock input, the data on DI is clocked into the multiplexer-address shift register. The first logic high on the input is the start bit. A 3- to 4-bit assignment word follows the start bit. On each successive low-to-high transition of the clock input, the start bit and assignment word are shifted through the shift register. When the start bit is shifted into the start location of the multiplexer register, the input channel is selected and conversion starts. The SAR status output (SARS) goes high to indicate that a conversion is in progress, and DI to the multiplexer shift register is disabled for the duration of the conversion.

An interval of one clock period is automatically inserted to allow the selected multiplexed channel to settle. DO comes out of the high-impedance state and provides a leading low for one clock period of multiplexer settling time. The SAR comparator compares successive outputs from the resistive ladder with the incoming analog signal. The comparator output indicates whether the analog input is greater than or less than the resistive-ladder output. As the conversion proceeds, conversion data is simultaneously output from DO, with the most significant bit (MSB) first. After eight clock periods, the conversion is complete and SARS goes low.

The TLV0834 outputs the least-significant-bit (LSB) first data after the MSB-first data stream. When \overline{SE} is held high on the TLV0838, the value of the LSB remains on the data line. When \overline{SE} is forced low, the data is then clocked out as LSB-first data. (To output LSB first, \overline{SE} must first go low, then the data stored in the 9-bit shift register outputs LSB first.) When \overline{CS} goes high, all internal registers are cleared. At this time, the output circuits go to the high-impedance state. If another conversion is desired, \overline{CS} must make a high-to-low transition followed by address information.

DI and DO can be tied together and controlled by a bidirectional processor I/O bit received on a single wire. This is possible because DI is only examined during the multiplexer-addressing interval and DO is still in the high-impedance state.

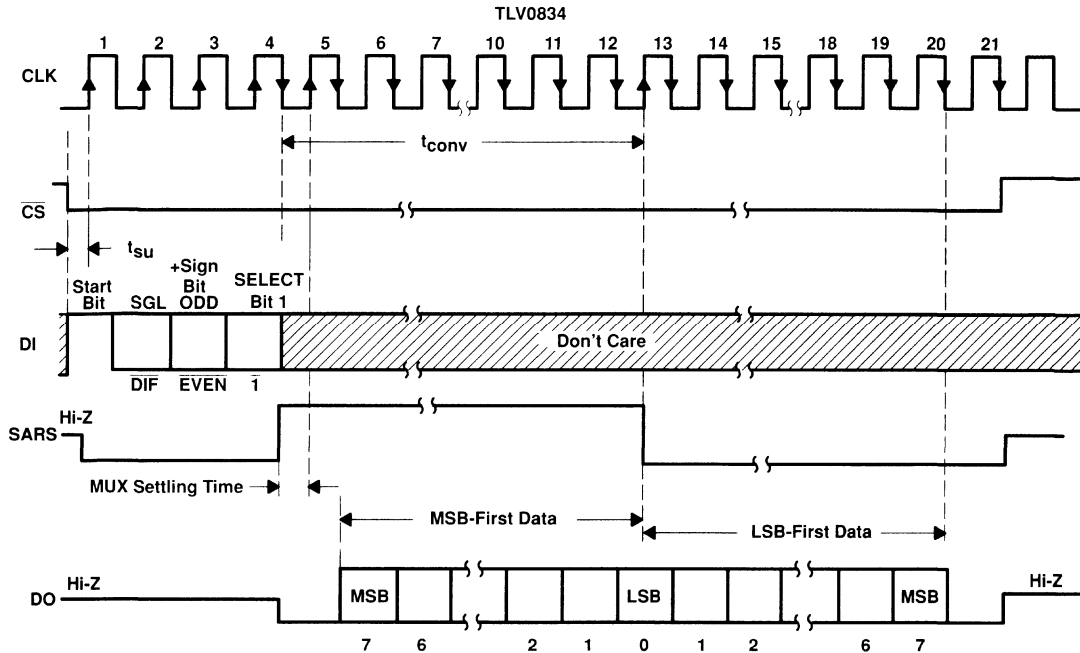


TLV0834C, TLV0834I, TLV0838C, TLV0838I

3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS147 – SEPTEMBER 1996

sequence of operation



TLV0834 MUX-ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS			CHANNEL NUMBER			
SGL/DIF	ODD/EVEN	SELECT BIT 1	CH0	CH1	CH2	CH3
L	L	L	+	-		
L	L	H			+	-
L	H	L	-	+		
L	H	H			-	+
H	L	L	+			
H	L	H			+	
H	H	L		+		
H	H	H				+

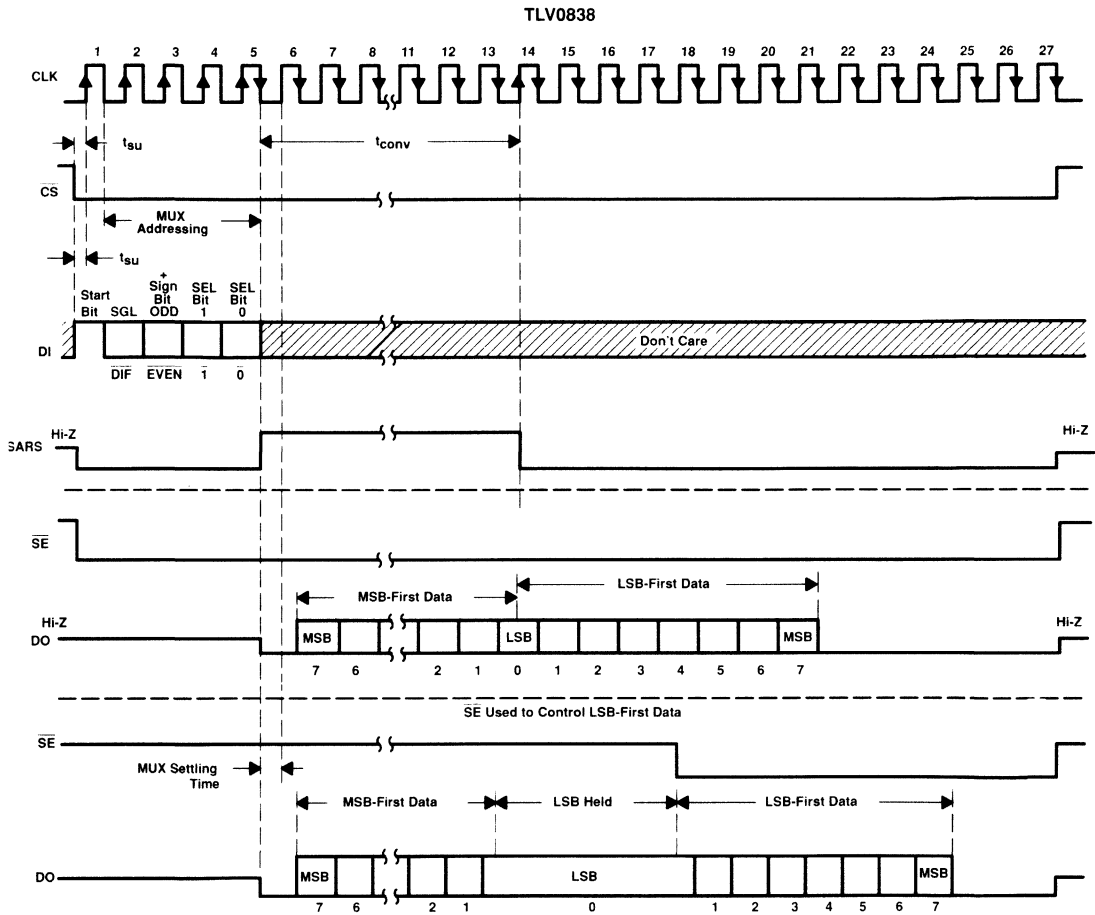
H = high level, L = low level, - or + = terminal polarity for the selected input channel

TLV0834C, TLV0834I, TLV0838C, TLV0838I

3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS147 – SEPTEMBER 1996

sequence of operation



TLV0834C, TLV0834I, TLV0838C, TLV0838I
3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS147 – SEPTEMBER 1996

TLV0838 MUX-ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS				SELECTED CHANNEL NUMBER								COM
SGL/DIF	ODD/ $\overline{\text{EVEN}}$	SELECT		0		1		2		3		
		1	0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	
L	L	L	L	+	-							
L	L	L	H			+	-					
L	L	H	L					+	-			
L	L	H	H							+	-	
L	H	L	L	-	+							
L	H	L	H			-	+					
L	H	H	L					-	+			
L	H	H	H							-	+	
H	L	L	L	+								-
H	L	L	H			+						-
H	L	H	L					+				-
H	L	H	H							+		-
H	H	L	L		+							-
H	H	L	H				+					-
H	H	H	L						+			-
H	H	H	H								+	-

H = high level, L = low level, - or + = polarity of external input

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range: Logic	-0.3 V to $V_{CC} + 0.3$ V
Analog	-0.3 V to $V_{CC} + 0.3$ V
Input current, I_I	± 5 mA
Total input current	± 20 mA
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	-40°C to 85°C
Storage temperature range, T_{Stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.



TLV0834C, TLV0834I, TLV0838C, TLV0838I

3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS147 – SEPTEMBER 1996

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see clock frequency operating conditions)		2.7	3.3	3.6	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}		0.8			V
Clock frequency, $f_{(CLK)}$	$V_{CC} = 2.7$ V	10	250		kHz
Clock frequency, $f_{(CLK)}$	$V_{CC} = 3.3$ V	10	600		kHz
Clock duty cycle (see Note 2)		40%	60%		
Pulse duration, \overline{CS} high, $t_{WH}(\overline{CS})$		220			ns
Setup time, \overline{CS} low, \overline{SE} low, or data valid before $CLK\uparrow$, t_{SU}		350			ns
Hold time, data valid after $CLK\uparrow$, t_H		90			ns
Operating free-air temperature, T_A	C suffix	0	70		°C
	I suffix	-40	85		

NOTE 2: The clock-duty-cycle range ensures proper operation at all clock frequencies. When a clock frequency is used outside the recommended duty-cycle range, the minimum pulse duration (high or low) is 1 μ s.

electrical characteristics over recommended range of operating free-air temperature, $V_{CC} = 3.3$ V, $f_{(CLK)} = 250$ kHz (unless otherwise noted)

digital section

PARAMETER	TEST CONDITIONS†	C SUFFIX			I SUFFIX			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH} High-level output voltage	$V_{CC} = 3$ V, $I_{OH} = -360$ μ A	2.8			2.4			V
	$V_{CC} = 3$ V, $I_{OH} = -10$ μ A	2.9			2.8			
V_{OL} Low-level output voltage	$V_{CC} = 3$ V, $I_{OL} = 1.6$ mA			0.34			0.4	V
I_{IH} High-level input current	$V_{IH} = 3.6$ V		0.005	1		0.005	1	μ A
I_{IL} Low-level input current	$V_{IL} = 0$		-0.005	-1		-0.005	-1	μ A
I_{OH} High-level output (source) current	At V_{OH} , $DO = 0$ V, $T_A = 25^\circ$ C	-6.5	-15		-6.5	-15		mA
I_{OL} Low-level output (sink) current	At V_{OL} , $DO = V_{CC}$, $T_A = 25^\circ$ C	8	16		8	16		mA
I_{OZ} High-impedance-state output current (DO or SARS)	$V_O = 3.3$ V, $T_A = 25^\circ$ C		0.01	3		0.01	3	μ A
	$V_O = 0$, $T_A = 25^\circ$ C		-0.01	-3		-0.01	-3	
C_i Input capacitance					5			pF
C_o Output capacitance					5			pF

† All parameters are measured under open-loop conditions with zero common-mode input voltage (unless otherwise specified).

‡ All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ$ C.



TLV0834C, TLV0834I, TLV0838C, TLV0838I

3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS147 – SEPTEMBER 1996

analog and converter section

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IC}	Common-mode input voltage	See Note 3	-0.05 to $V_{CC} + 0.05$			V
$I_{I(stbdy)}$	Standby input current (see Note 4)	On channel	$V_I = 3.3$ V		1	μ A
		Off channel	$V_I = 0$		-1	
		On channel	$V_I = 0$		-1	
		Off channel	$V_I = 3.3$ V		1	
$r_i(REF)$	Input resistance to REF		1.3	2.4	5.9	k Ω

total device

PARAMETER		MIN	TYP‡	MAX	UNIT
I_{CC}	Supply current		0.2	0.75	mA

† All parameters are measured under open-loop conditions with zero common-mode input voltage.

‡ All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ$ C.

NOTES: 3. When channel IN₋ is more positive than channel IN₊, the digital output code is 0000 0000. Connected to each analog input are two on-chip diodes that conduct forward current for analog input voltages one diode drop above V_{CC} . Care must be taken during testing at low V_{CC} levels (3 V) because high-level analog input voltage (3.6 V) can, especially at high temperatures, cause the input diode to conduct and cause errors for analog inputs that are near full scale. As long as the analog voltage does not exceed the supply voltage by more than 50 mV, the output code is correct. To achieve an absolute 0- to 3.3-V input range requires a minimum V_{CC} of 3.25 V for all variations of temperature and load.

4. Standby input currents go in or out of the on or off channels when the A/D converter is not performing conversion and the clock is in a high or low steady-state condition.

operating characteristics, $V_{CC} = 3.3$ V, $f_{(CLK)} = 250$ kHz, $t_r = t_f = 20$ ns, $T_A = 25^\circ$ C (unless otherwise noted)

PARAMETER		TEST CONDITIONS§	MIN	TYP	MAX	UNIT
Supply-voltage variation error		$V_{CC} = 3$ V to 3.6 V		$\pm 1/16$	$\pm 1/4$	LSB
Total unadjusted error (see Note 5)		$V_{ref} = 3.3$ V, $T_A = \text{MIN to MAX}$			± 1	LSB
Common-mode error		Differential mode		$\pm 1/16$	$\pm 1/4$	LSB
t_{pd}	Propagation delay time, output data after CLK \downarrow (see Note 6)	MSB-first data	$C_L = 100$ pF		500	ns
		LSB-first data		200		
t_{dis}	Output disable time, DO or SARS after CS \uparrow	$C_L = 10$ pF, $R_L = 10$ k Ω			80	ns
		$C_L = 100$ pF, $R_L = 2$ k Ω			250	
t_{conv}	Conversion time (multiplexer-addressing time not included)				8	clock periods

§ All parameters are measured under open-loop conditions with zero common-mode input voltage. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 5. Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

6. The MSB-first data is output directly from the comparator and, therefore, requires additional delay to allow for comparator response time.



TLV0834C, TLV0834I, TLV0838C, TLV0838I
3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS147 – SEPTEMBER 1996

PARAMETER MEASUREMENT INFORMATION

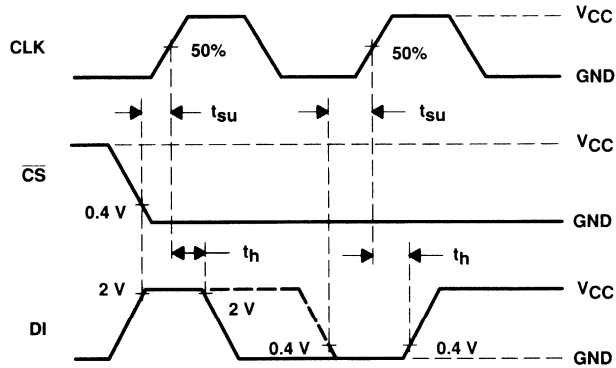


Figure 1. Data-Input Timing

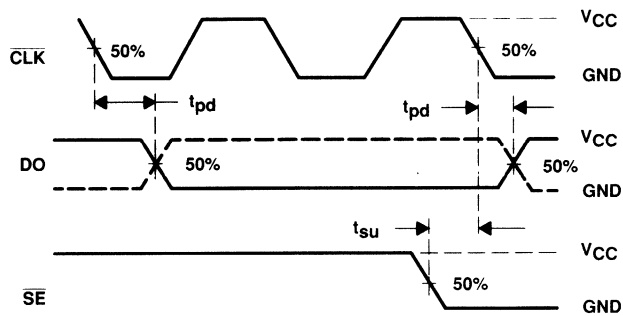
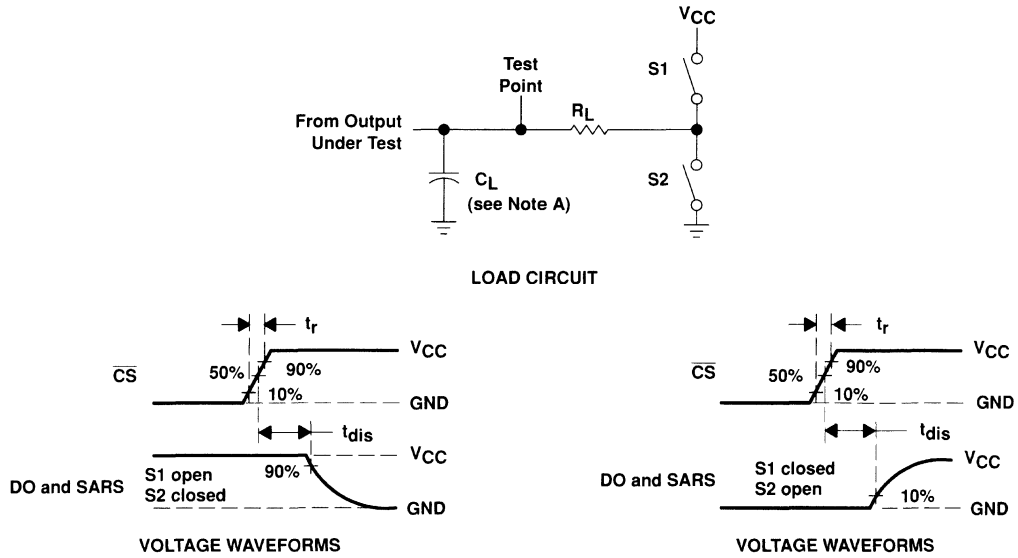


Figure 2. Data-Output Timing

TLV0834C, TLV0834I, TLV0838C, TLV0838I
3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS147 – SEPTEMBER 1996

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 3. Output Disable Time Test Circuit and Voltage Waveforms

TLV0834C, TLV0834I, TLV0838C, TLV0838I
 3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS147 – SEPTEMBER 1996

TYPICAL CHARACTERISTICS

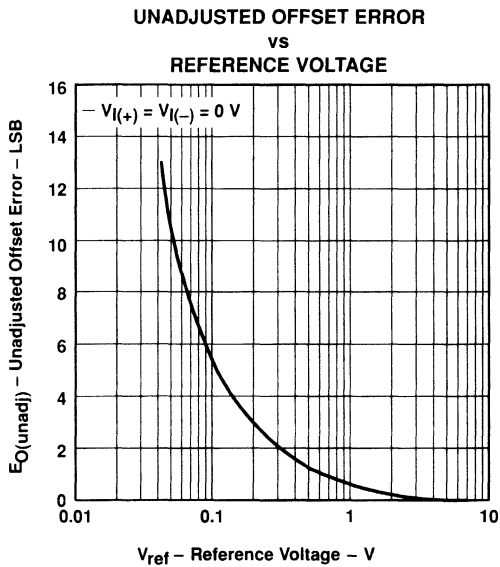


Figure 4

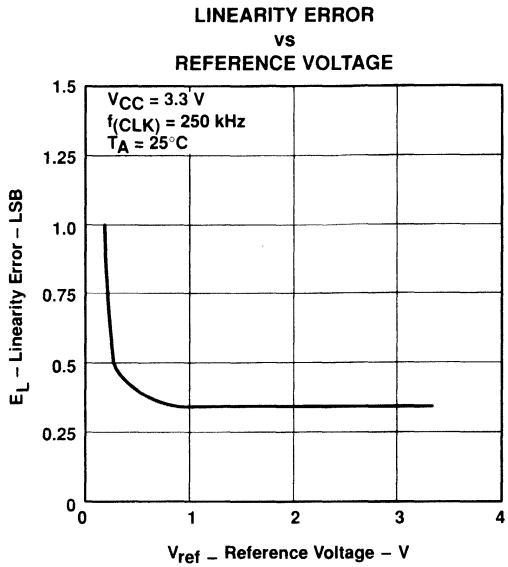


Figure 5

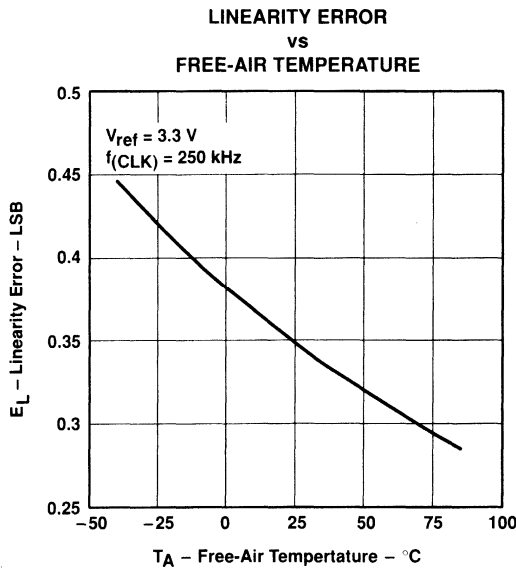


Figure 6

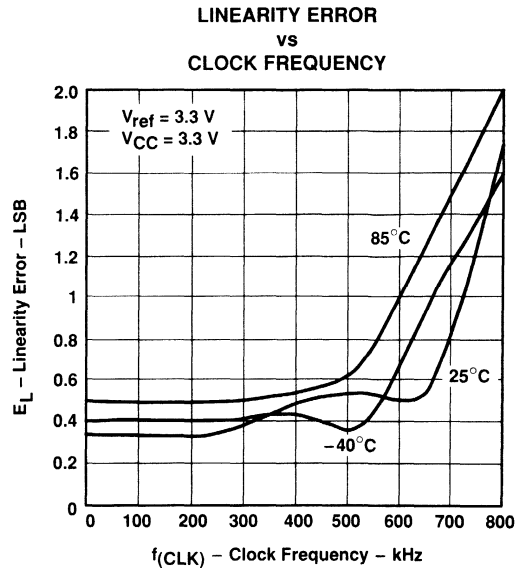


Figure 7



TLV0834C, TLV0834I, TLV0838C, TLV0838I
3-VOLT 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS147 – SEPTEMBER 1996

TYPICAL CHARACTERISTICS

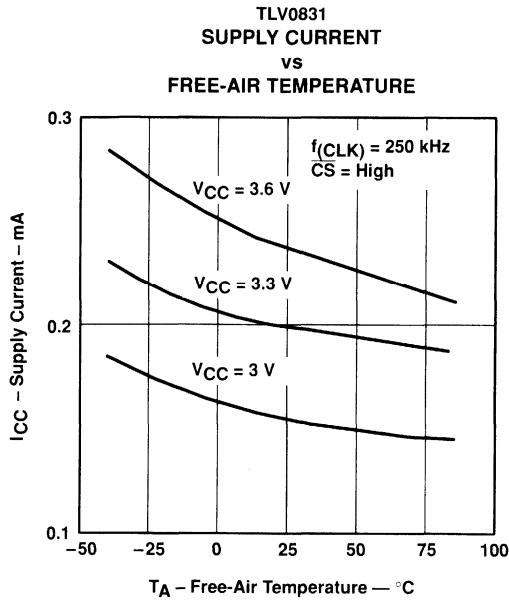


Figure 8

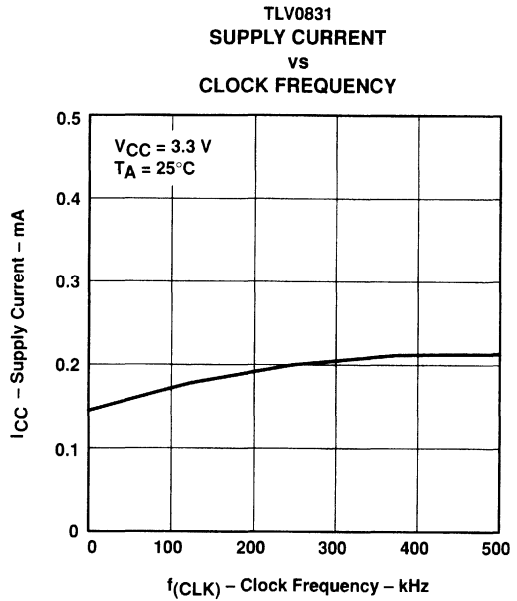


Figure 9

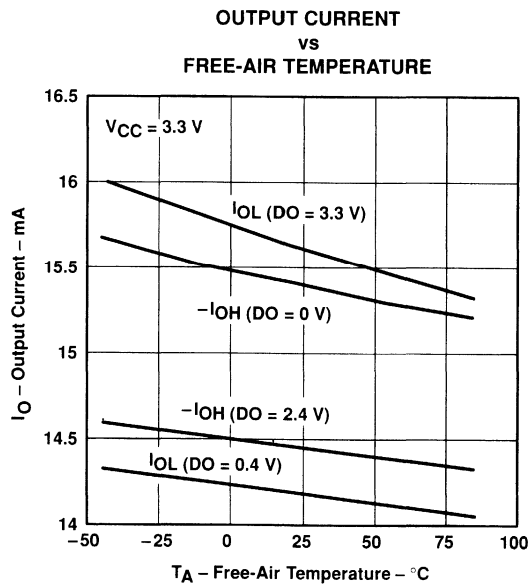


Figure 10

TYPICAL CHARACTERISTICS

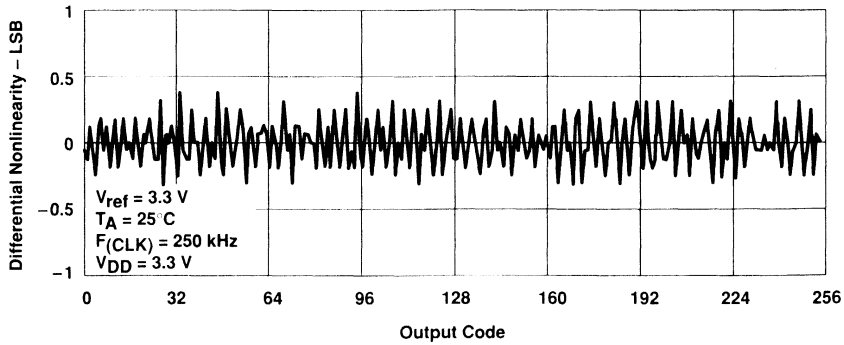


Figure 11. Differential Nonlinearity With Output Code

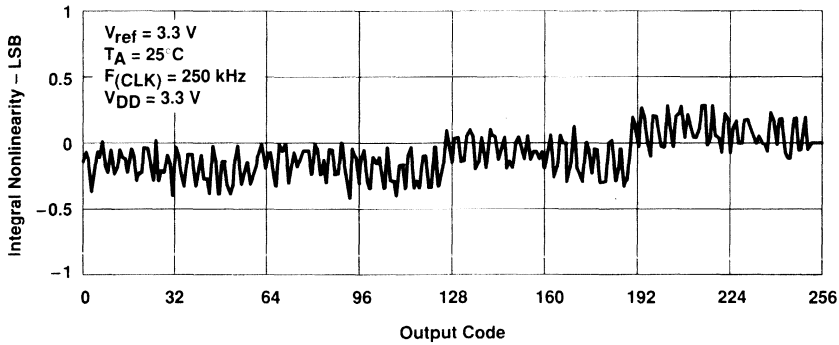


Figure 12. Integral Nonlinearity With Output Code

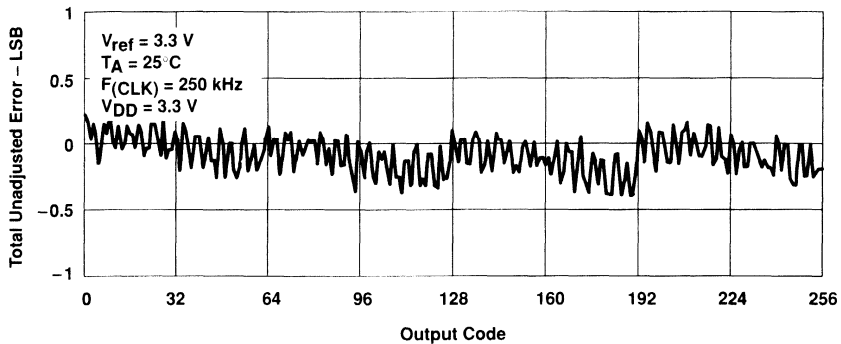


Figure 13. Total Unadjusted Error With Output Code

TLV1543C, TLV1543M

3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS072C – DECEMBER 1992 – REVISED MARCH 1995

- 3.3-V Supply Operation
- 10-Bit-Resolution A/D Converter
- 11 Analog Input Channels
- Three Built-In Self-Test Modes
- Inherent Sample and Hold
- Total Unadjusted Error . . . ± 1 LSB Max
- On-Chip System Clock
- End-of-Conversion (EOC) Output
- Pin Compatible With TLC1543
- CMOS Technology

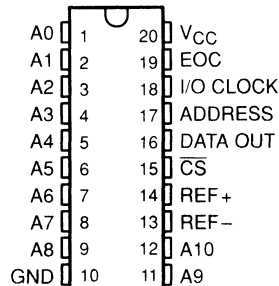
description

The TLV1543C and TLV1543M are CMOS 10-bit, switched-capacitor, successive-approximation, analog-to-digital converters. These devices have three inputs and a 3-state output [chip select ($\overline{\text{CS}}$), input-output clock (I/O CLOCK), address input (ADDRESS), and data output (DATA OUT)] that provide a direct 4-wire interface to the serial port of a host processor. The devices allow high-speed data transfers from the host.

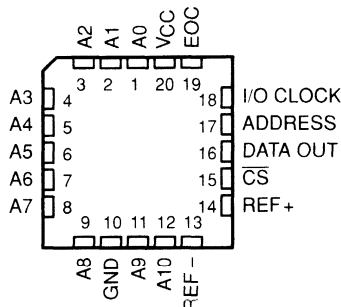
In addition to a high-speed A/D converter and versatile control capability, these devices have an on-chip 14-channel multiplexer that can select any one of 11 analog inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of A/D conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the devices features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

The TLV1543C is characterized for operation from 0°C to 70°C. The TLV1543M is characterized for operation over the full military temperature range of –55°C to 125°C.

DB, DW, FK, J, OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T _A	PACKAGE					
	SMALL OUTLINE (DB)	SMALL OUTLINE (DW)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	PLASTIC CHIP CARRIER (FN)
0°C to 70°C	TLV1543CDB	TLV1543CDW	—	—	TLV1543CN	TLV1543CFN
–55°C to 125°C	—	—	TLV1543MFK	TLV1543MJ	—	—

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



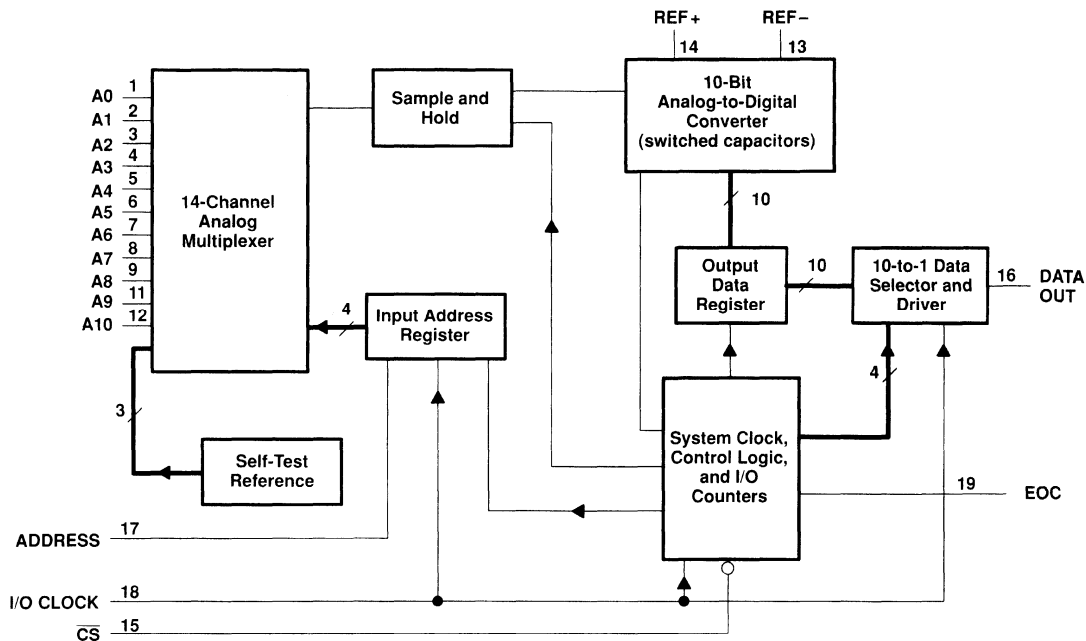
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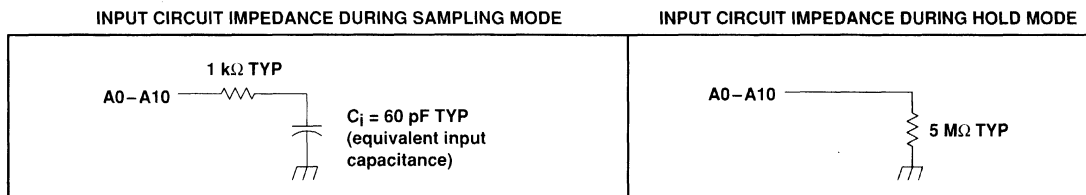
TLV1543C, TLV1543M
3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS072C – DECEMBER 1992 – REVISED MARCH 1995

functional block diagram



typical equivalent inputs



TLV1543C, TLV1543M
3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS072C – DECEMBER 1992 – REVISED MARCH 1995

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ADDRESS	17	I	Serial address. A 4-bit serial address selects the desired analog input or test voltage that is to be converted next. The address data is presented with the MSB first and is shifted in on the first four rising edges of I/O CLOCK. After the four address bits have been read into the address register, ADDRESS is ignored for the remainder of the current conversion period.
A0–A10	1–9, 11, 12	I	Analog signal. The 11 analog inputs are applied to A0–A10 and are internally multiplexed. The driving source impedance should be less than or equal to 1 k Ω .
\overline{CS}	15	I	Chip select. A high-to-low transition on \overline{CS} resets the internal counters and controls and enables DATA OUT, ADDRESS, and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables ADDRESS and I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OUT	16	O	The 3-state serial output for the A/D conversion result. DATA OUT is in the high-impedance state when \overline{CS} is high and active when \overline{CS} is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next most significant bit, and the remaining bits are shifted out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs.
EOC	19	O	End of conversion. EOC goes from a high- to a low- logic level on the trailing edge of the tenth I/O CLOCK and remains low until the conversion is complete and data are ready for transfer.
GND	10	I	The ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	18	I	Input/output clock. I/O CLOCK receives the serial I/O CLOCK input and performs the following four functions: 1) It clocks the four input address bits into the address register on the first four rising edges of I/O CLOCK with the multiplex address available after the fourth rising edge. 2) On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 3) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 4) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF+	14	I	The upper reference voltage value (nominally V_{CC}) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to REF+ and the voltage applied to the REF– terminal.
REF–	13	I	The lower reference voltage value (nominally ground) is applied to REF–.
V_{CC}	20	I	Positive supply voltage

detailed description

With chip select (\overline{CS}) inactive (high), the ADDRESS and I/O CLOCK inputs are initially disabled and DATA OUT is in the high-impedance state. When the serial interface takes \overline{CS} active (low), the conversion sequence begins with the enabling of I/O CLOCK and ADDRESS and the removal of DATA OUT from the high-impedance state. The host then provides the 4-bit channel address to ADDRESS and the I/O CLOCK sequence to I/O CLOCK. During this transfer, the host serial interface also receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host. The first four I/O clocks load the address register with the 4-bit address on ADDRESS selecting the desired analog channel and the next six clocks providing the control timing for sampling the analog input.



TLV1543C, TLV1543M
3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS072C – DECEMBER 1992 – REVISED MARCH 1995

detailed description (continued)

There are six basic serial interface timing modes that can be used with the device. These modes are determined by the speed of I/O CLOCK and the operation of \overline{CS} as shown in Table 1. These modes are (1) a fast mode with a 10-clock transfer and \overline{CS} inactive (high) between conversion cycles, (2) a fast mode with a 10-clock transfer and \overline{CS} active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and \overline{CS} inactive (high) between conversion cycles, (4) a fast mode with a 16-bit transfer and \overline{CS} active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and \overline{CS} inactive (high) between conversion cycles, and (6) a slow mode with a 16-clock transfer and \overline{CS} active (low) continuously.

The MSB of the previous conversion appears on DATA OUT on the falling edge of \overline{CS} in mode 1, mode 3, and mode 5, on the rising edge of EOC in mode 2 and mode 4, and following the 16th clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of I/O CLOCK. Ten bits of data are transmitted to the host through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the 10th clock falling edge, the EOC output goes low and returns to the high logic level when conversion is complete and the result can be read by the host. On the 10th clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLOCK transfer is more than ten clocks long.

Table 1 lists the operational modes with respect to the state of \overline{CS} , the number of I/O serial transfer clocks that can be used, and the timing edge on which the MSB of the previous conversion appears at the output.

Table 1. Mode Operation

MODES		\overline{CS}	NO. OF I/O CLOCKS	MSB AT DATA OUT†	TIMING DIAGRAM
Fast Modes	Mode 1	High between conversion cycles	10	\overline{CS} falling edge	Figure 9
	Mode 2	Low continuously	10	EOC rising edge	Figure 10
	Mode 3	High between conversion cycles	11 to 16‡	\overline{CS} falling edge	Figure 11
	Mode 4	Low continuously	16‡	EOC rising edge	Figure 12
Slow Modes	Mode 5	High between conversion cycles	11 to 16‡	\overline{CS} falling edge	Figure 13
	Mode 6	Low continuously	16‡	16th clock falling edge	Figure 14

† These edges also initiate serial-interface communication.

‡ No more than 16 clocks should be used.

fast modes

The device is in a fast mode when the serial I/O CLOCK data transfer is completed before the conversion is completed. With a 10-clock serial transfer, the device can only run in a fast mode since a conversion does not begin until the falling edge of the 10th I/O CLOCK.

mode 1: fast mode, \overline{CS} inactive (high) between conversion cycles, 10-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O CLOCK transfers and each transfer is ten clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 2: fast mode, \overline{CS} active (low) continuously, 10-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O CLOCK transfers and each transfer is ten clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.



TLV1543C, TLV1543M
**3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS**

SLAS072C – DECEMBER 1992 – REVISED MARCH 1995

mode 3: fast mode, \overline{CS} inactive (high) between conversion cycles, 11- to 16-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 4: fast mode, \overline{CS} active (low) continuously, 16-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

slow modes

In a slow mode, the conversion is completed before the serial I/O CLOCK data transfer is completed. A slow mode requires a minimum 11-clock transfer into I/O CLOCK, and the rising edge of the eleventh clock must occur before the conversion period is complete; otherwise, the device loses synchronization with the host serial interface, and \overline{CS} has to be toggled to initialize the system. The eleventh rising edge of the I/O CLOCK must occur within 9.5 μ s after the tenth I/O clock falling edge.

mode 5: slow mode, \overline{CS} inactive (high) between conversion cycles, 11- to 16-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 6: slow mode, \overline{CS} active (low) continuously, 16-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions. The falling edge of the sixteenth I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16-clock transfer initiated by the serial interface.

address bits

The 4-bit analog channel-select address for the next conversion cycle is presented to the ADDRESS terminal (MSB first) and is clocked into the address register on the first four leading edges of I/O CLOCK. This address selects one of 14 inputs (11 analog inputs or 3 internal test inputs).

analog inputs and test modes

The 11 analog inputs and the 3 internal test inputs are selected by the 14-channel multiplexer according to the input address as shown in Tables 2 and 3. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching.

Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK, and sampling continues for six I/O CLOCK periods. The sample is held on the falling edge of the tenth I/O CLOCK. The three test inputs are applied to the multiplexer, sampled, and converted in the same manner as the external analog inputs.



TLV1543C, TLV1543M
3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS072C – DECEMBER 1992 – REVISED MARCH 1995

Table 2. Analog-Channel-Select Address

ANALOG INPUT SELECTED	VALUE SHIFTED INTO ADDRESS INPUT	
	BINARY	HEX
A0	0000	0
A1	0001	1
A2	0010	2
A3	0011	3
A4	0100	4
A5	0101	5
A6	0110	6
A7	0111	7
A8	1000	8
A9	1001	9
A10	1010	A

Table 3. Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED†	VALUE SHIFTED INTO ADDRESS INPUT		OUTPUT RESULT (HEX)‡
	BINARY	HEX	
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	B	200
V_{ref-}	1100	C	000
V_{ref+}	1101	D	3FF

† V_{ref+} is the voltage applied to the REF+ input, and V_{ref-} is the voltage applied to the REF- input.

‡ The output results shown are the ideal values and vary with the reference stability and with internal offsets.

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF-) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF-. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half the V_{CC} voltage), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF-. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and the 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are counted.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.



TLV1543C, TLV1543M
3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS072C – DECEMBER 1992 – REVISED MARCH 1995

converter and analog input (continued)

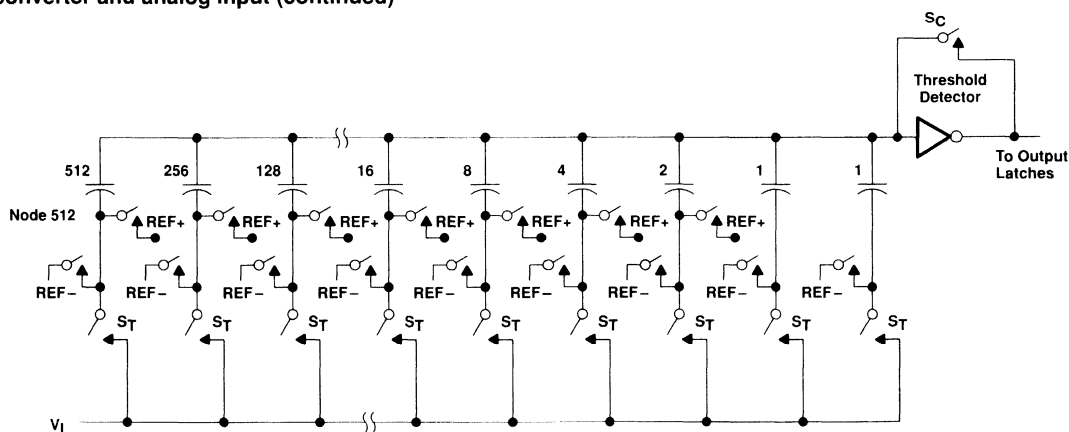


Figure 1. Simplified Model of the Successive-Approximation System

chip-select operation

The trailing edge of \overline{CS} starts all modes of operation, and \overline{CS} can abort a conversion sequence in any mode. A high-to-low transition on \overline{CS} within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Exercise care to prevent \overline{CS} from being taken low close to completion of conversion because the output data can be corrupted.

reference voltage inputs

There are two reference inputs used with these devices: REF+ and REF-. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero-scale reading respectively. The values of REF+, REF-, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF-.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1): TLV1543C	-0.5 V to 6.5 V
TLV1543M	-0.5 V to 6 V
Input voltage range, V_I (any input)	-0.3 V to $V_{CC} + 0.3$ V
Output voltage range, V_O	-0.3 V to $V_{CC} + 0.3$ V
Positive reference voltage, V_{ref+}	$V_{CC} + 0.1$ V
Negative reference voltage, V_{ref-}	-0.1 V
Peak input current (any input)	± 20 mA
Peak total input current (all inputs)	± 30 mA
Operating free-air temperature range, T_A : TLV1543C	0°C to 70°C
TLV1543M	-55°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF- and GND wired together (unless otherwise noted).

TLV1543C, TLV1543M
3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS072C – DECEMBER 1992 – REVISED MARCH 1995

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	TLV1543C	3	3.3	5.5	V
	TLV1543M	3	3.3	3.6	V
Positive reference voltage, V_{ref+} (see Note 2)		V_{CC}			V
Negative reference voltage, V_{ref-} (see Note 2)		0			V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)		2.5	V_{CC}	$V_{CC} + 0.2$	V
Analog input voltage (see Note 2)		0			V_{CC}
High-level control input voltage, V_{IH}	TLV1543C	$V_{CC} = 3\text{ V to }5.5\text{ V}$		2	V
	TLV1543M	$V_{CC} = 3\text{ V to }3.6\text{ V}$		2	V
Low-level control input voltage, V_{IL}	TLV1543C	$V_{CC} = 3\text{ V to }5.5\text{ V}$		0.6	V
	TLV1543M	$V_{CC} = 3\text{ V to }3.6\text{ V}$		0.8	V
Setup time, address bits at data input before I/O CLOCK \uparrow , $t_{SU(A)}$ (see Figure 4)		100			ns
Hold time, address bits after I/O CLOCK \uparrow , $t_{H(A)}$ (see Figure 4)		0			ns
Hold time, \overline{CS} low after last I/O CLOCK \downarrow , $t_{H(CS)}$		0			ns
Setup time, \overline{CS} low before clocking in first address bit, $t_{SU(CS)}$ (see Note 3)		1.425			μs
Clock frequency at I/O CLOCK (see Note 4)	TLC1543C	0		1.1	MHz
	TLC1543M	0		2.1	
Pulse duration, I/O CLOCK high, $t_{WH(I/O)}$		190			ns
Pulse duration, I/O CLOCK low, $t_{WL(I/O)}$		190			ns
Transition time, I/O CLOCK, $t_{f(I/O)}$ (see Note 5)					1
Transition time, ADDRESS and \overline{CS} , $t_f(CS)$					10
Operating free-air temperature, T_A	TLV1543C	0		70	$^{\circ}\text{C}$
	TLV1543M	-55		125	

- NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.
3. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.
4. For 11- to 16-bit transfers, after the tenth I/O CLOCK falling edge ($\leq 2\text{ V}$), at least one I/O clock rising edge ($\geq 2\text{ V}$) must occur within 9.5 μs .
5. This is the time required for the clock input signal to fall from V_{IHmin} to V_{ILmax} or to rise from V_{ILmax} to V_{IHmin} . In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 μs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.



TLV1543C, TLV1543M
3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS072C – DECEMBER 1992 – REVISED MARCH 1995

electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 3\text{ V to }5.5\text{ V}$, I/O CLOCK frequency = 1.1 MHz for the TLV1543C,
 $V_{CC} = V_{ref+} = 3\text{ V to }3.6\text{ V}$, I/O CLOCK frequency = 2.1 MHz for the TLV1543M (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V_{OH} High-level output voltage	TLV1543C	$V_{CC} = 3\text{ V}$, $I_{OH} = -1.6\text{ mA}$		2.4			V	
		$V_{CC} = 3\text{ V to }5.5\text{ V}$, $I_{OH} = 20\text{ }\mu\text{A}$		$V_{CC}-0.1$			V	
	TLV1543M	$V_{CC} = 3\text{ V}$, $I_{OH} = -1.6\text{ mA}$		2.4			V	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$, $I_{OH} = 20\text{ }\mu\text{A}$		$V_{CC}-0.1$			V	
V_{OL} Low-level output voltage	TLV1543C	$V_{CC} = 3\text{ V}$, $I_{OL} = 1.6\text{ mA}$				0.4	V	
		$V_{CC} = 3\text{ V to }5.5\text{ V}$, $I_{OL} = 20\text{ }\mu\text{A}$				0.1	V	
	TLV1543M	$V_{CC} = 3\text{ V}$, $I_{OL} = 1.6\text{ mA}$				0.4	V	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$, $I_{OL} = 20\text{ }\mu\text{A}$				0.1	V	
I_{OZ} Off-state (high-impedance-state) output current	$V_O = V_{CC}$, \overline{CS} at V_{CC}					10	μA	
	$V_O = 0$, \overline{CS} at V_{CC}					-10	μA	
I_{IH} High-level input current	$V_I = V_{CC}$			0.005	2.5		μA	
I_{IL} Low-level input current	$V_I = 0$			-0.005	-2.5		μA	
I_{CC} Operating supply current	\overline{CS} at 0 V			0.8	2.5		mA	
Selected channel leakage current		Selected channel at V_{CC} , Unselected channel at 0 V				1	μA	
		Selected channel at 0 V, Unselected channel at V_{CC}				-1		
Maximum static analog reference current into REF +		$V_{ref+} = V_{CC}$, $V_{ref-} = \text{GND}$				10	μA	
C_i	Input capacitance, Analog inputs	TLV1543C			7	55	pF	
		TLV1543M			7			
	Input capacitance, Control inputs	TLV1543C				5	15	pF
		TLV1543M				5		

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

TLV1543C, TLV1543M

3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS072C – DECEMBER 1992 – REVISED MARCH 1995

**operating characteristics over recommended operating free-air temperature range,
V_{CC} = V_{ref+} = 3 V to 5.5 V, I/O CLOCK frequency = 1.1 MHz for the TLV1543C,
V_{CC} = V_{ref+} = 3 V to 3.6 V, I/O CLOCK frequency = 2.1 MHz for the TLV1543M**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Linearity error (see Note 6)				±1	LSB
	Zero error (see Note 7)	See Note 2			±1	LSB
	Full-scale error (see Note 7)	See Note 2			±1	LSB
	Total unadjusted error (see Note 8)				±1	LSB
	Self-test output code (see Table 3 and Note 9)	ADDRESS = 1011		512		
		ADDRESS = 1100		0		
		ADDRESS = 1101		1023		
t _{conv}	Conversion time	See Figures 9–14			21	μs
t _c	Total cycle time (access, sample, and conversion)	See Figures 9–14 and Note 10			21 +10 I/O CLOCK periods	μs
t _{acq}	Channel acquisition time (sample)	See Figures 9–14 and Note 10			6	I/O CLOCK periods
t _v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 6	10			ns
t _{d(I/O-DATA)}	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 6			240	ns
t _{d(I/O-EOC)}	Delay time, tenth I/O CLOCK↓ to EOC↓	See Figure 7		70	240	ns
t _{d(EOC-DATA)}	Delay time, EOC↑ to DATA OUT (MSB)	See Figure 8			100	ns
t _{PZH, t_{PZL}}	Enable time, CS↓ to DATA OUT (MSB driven)	See Figure 3			1.3	μs
t _{PHZ, t_{PLZ}}	Disable time, CS↑ to DATA OUT (high impedance)	See Figure 3			150	ns
t _{r(EOC)}	Rise time, EOC	See Figure 8			300	ns
t _{f(EOC)}	Fall time, EOC	See Figure 7			300	ns
t _{r(bus)}	Rise time, data bus	See Figure 6			300	ns
t _{f(bus)}	Fall time, data bus	See Figure 6			300	ns
t _{d(I/O-CS)}	Delay time, tenth I/O CLOCK↓ to CS↓ to abort conversion (see Note 11)				9	μs

† All typical values are at T_A = 25°C.

- NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V (V_{ref+} – V_{ref-}); however, the electrical specifications are no longer applicable.
6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Zero-scale error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
8. Total unadjusted error comprises linearity, zero-scale, and full-scale errors.
9. Both the input address and the output codes are expressed in positive logic.
10. I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 6).
11. Any transitions of CS are recognized as valid only if the level is maintained for a setup time plus two falling edges of the internal clock (1.425 μs) after the transition.



PARAMETER MEASUREMENT INFORMATION

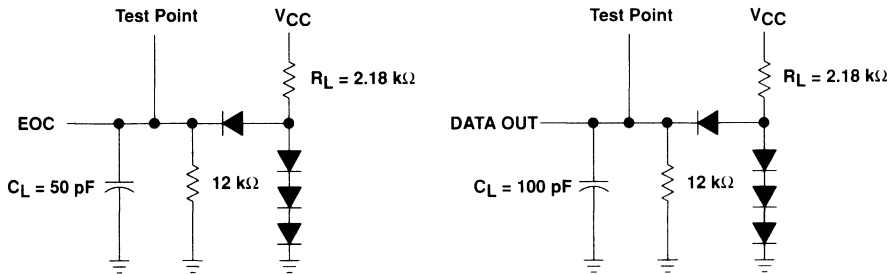


Figure 2. Load Circuits

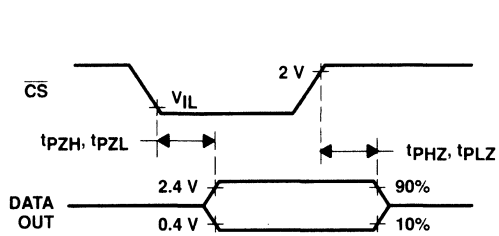


Figure 3. DATA OUT to Hi-Z Voltage Waveforms

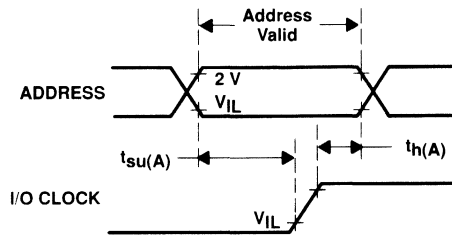


Figure 4. ADDRESS Setup Voltage Waveforms

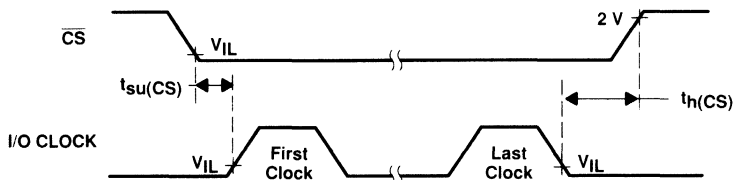


Figure 5. $\overline{\text{CS}}$ and I/O CLOCK Voltage Waveforms

TLV1543C, TLV1543M
3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS072C – DECEMBER 1992 – REVISED MARCH 1995

PARAMETER MEASUREMENT INFORMATION

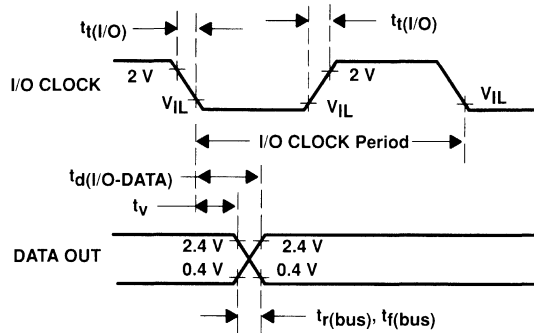


Figure 6. DATA OUT and I/O CLOCK Voltage Waveforms

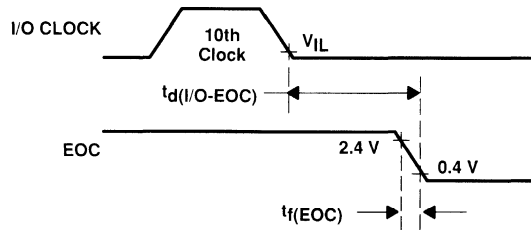


Figure 7. I/O CLOCK and EOC Voltage Waveforms

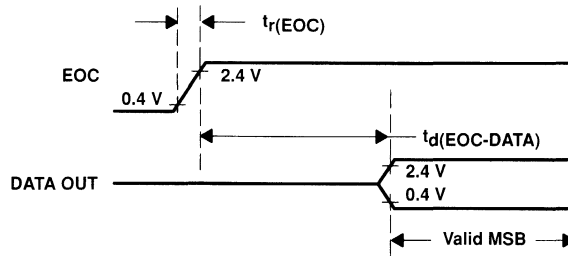


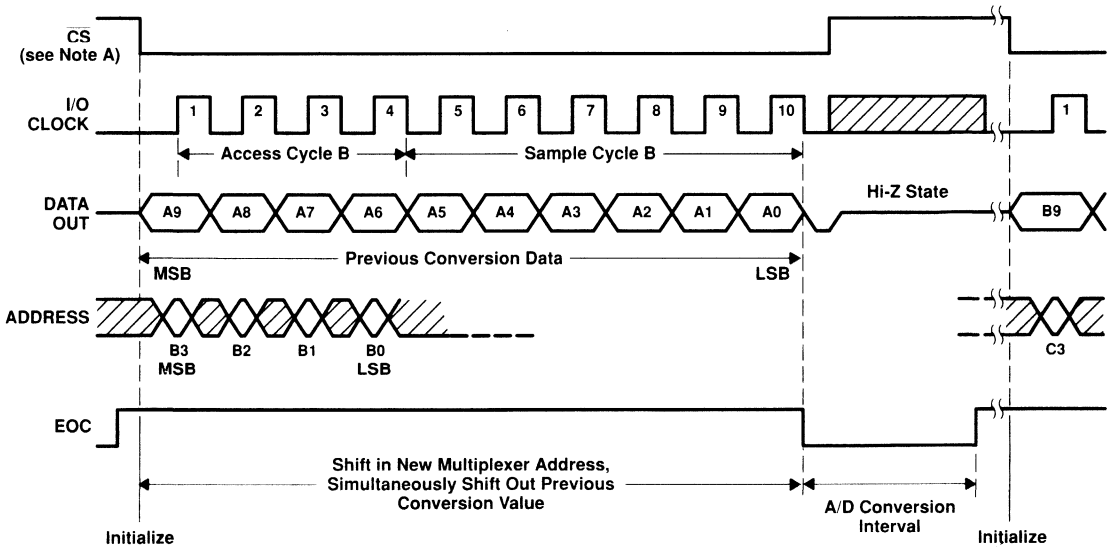
Figure 8. EOC and DATA OUT Voltage Waveforms



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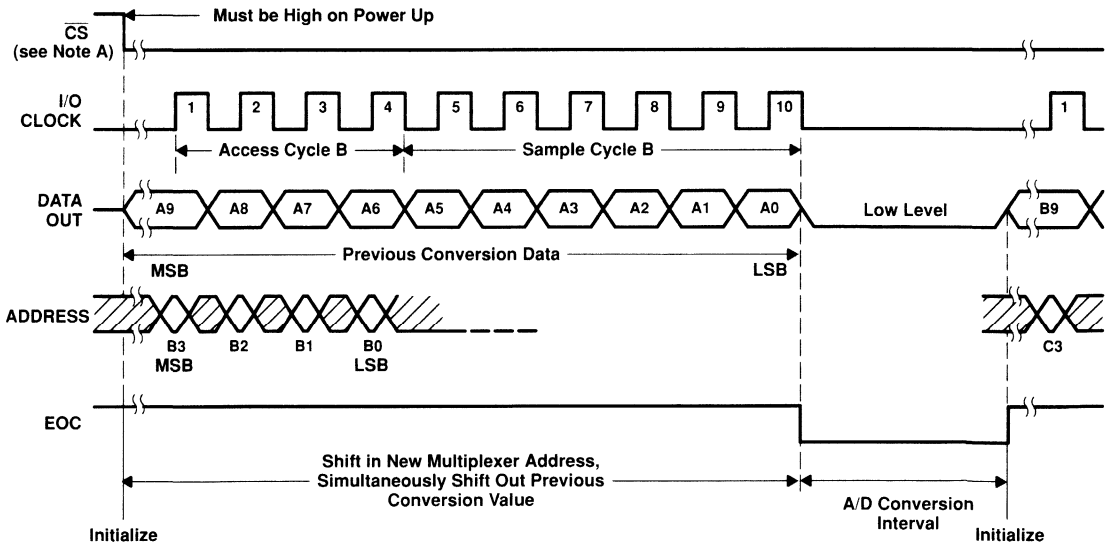
TLV1543C, TLV1543M
3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS072C – DECEMBER 1992 – REVISED MARCH 1995



NOTE A: To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.

Figure 9. Timing for 10-Clock Transfer Using \overline{CS}

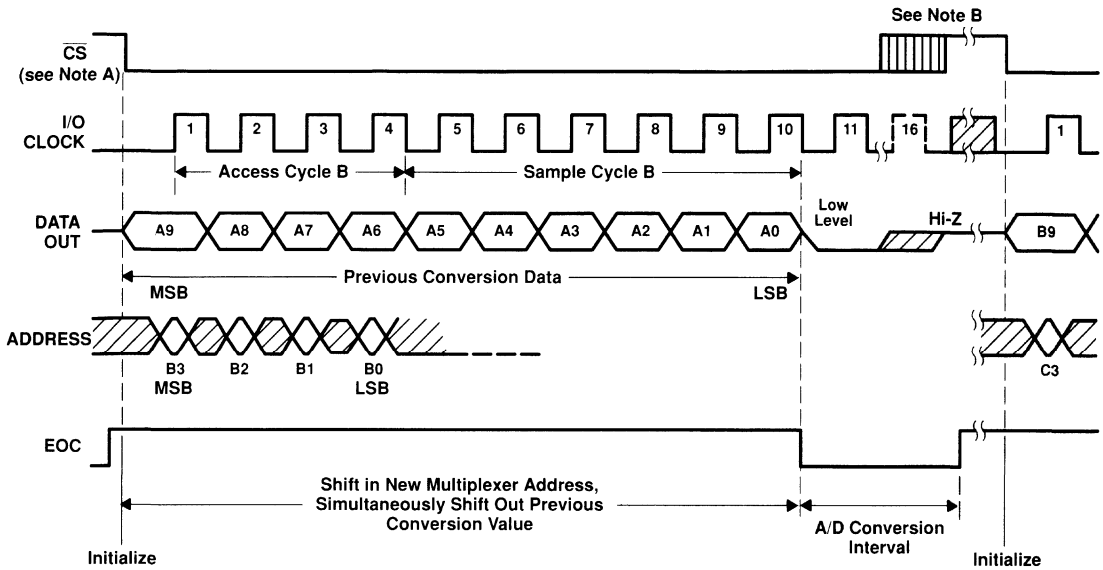


NOTE A: To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.

Figure 10. Timing for 10-Clock Transfer Not Using \overline{CS}

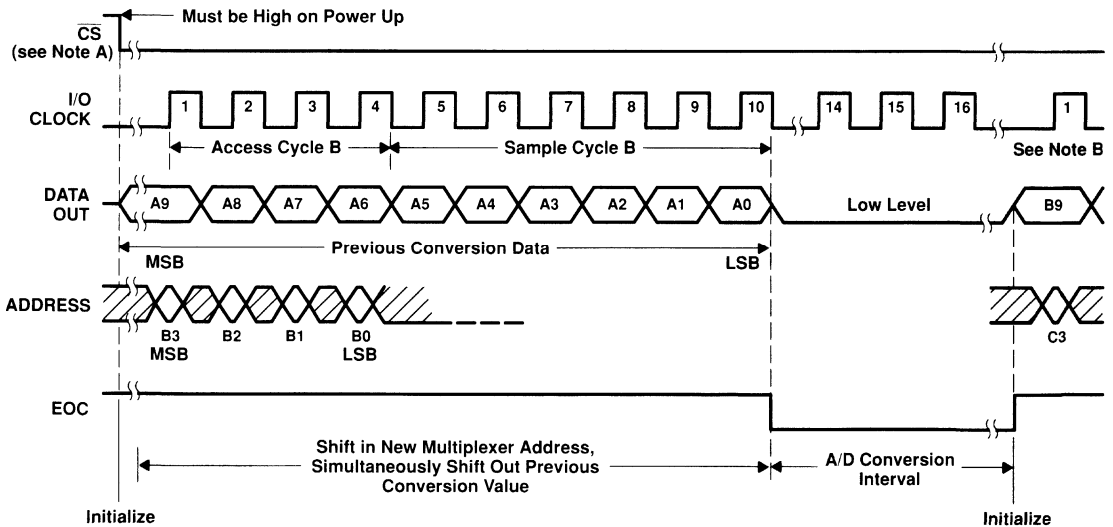
TLV1543C, TLV1543M
3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS072C – DECEMBER 1992 – REVISED MARCH 1995



- NOTES: A. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a set up time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.
- B. A low-to-high transition of \overline{CS} disables ADDRESS and the I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

Figure 11. Timing for 11- to 16-Clock Transfer Using \overline{CS} (Serial Transfer Interval Shorter Than Conversion)



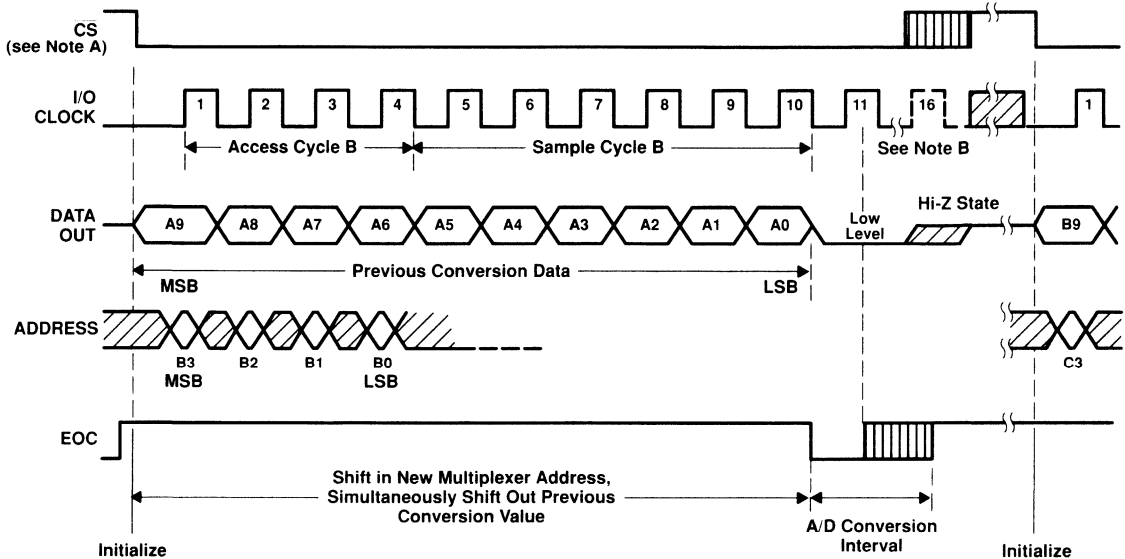
- NOTES: A. The first I/O CLOCK must occur after the rising edge of EOC.
- B. A low-to-high transition of CS disables ADDRESS and the I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

Figure 12. Timing for 16-Clock Transfer Not Using \overline{CS} (Serial Transfer Interval Shorter Than Conversion)



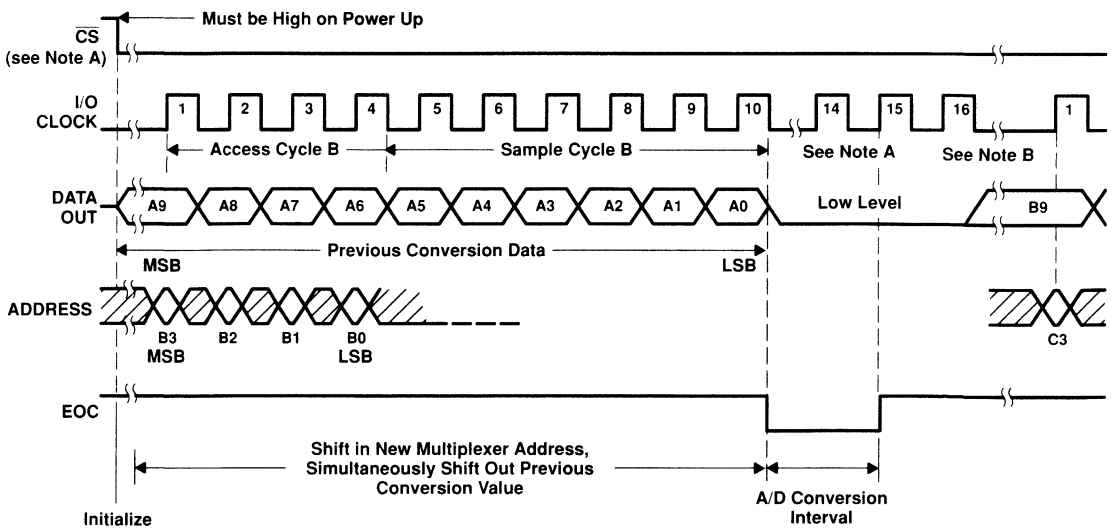
TLV1543C, TLV1543M
3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS072C – DECEMBER 1992 – REVISED MARCH 1995



- NOTES: A. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a set up time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in an address until the minimum chip \overline{CS} setup time has elapsed.
- B. The eleventh rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.

Figure 13. Timing for 11- to 16-Clock Transfer Using \overline{CS} (Serial Transfer Interval Longer Than Conversion)

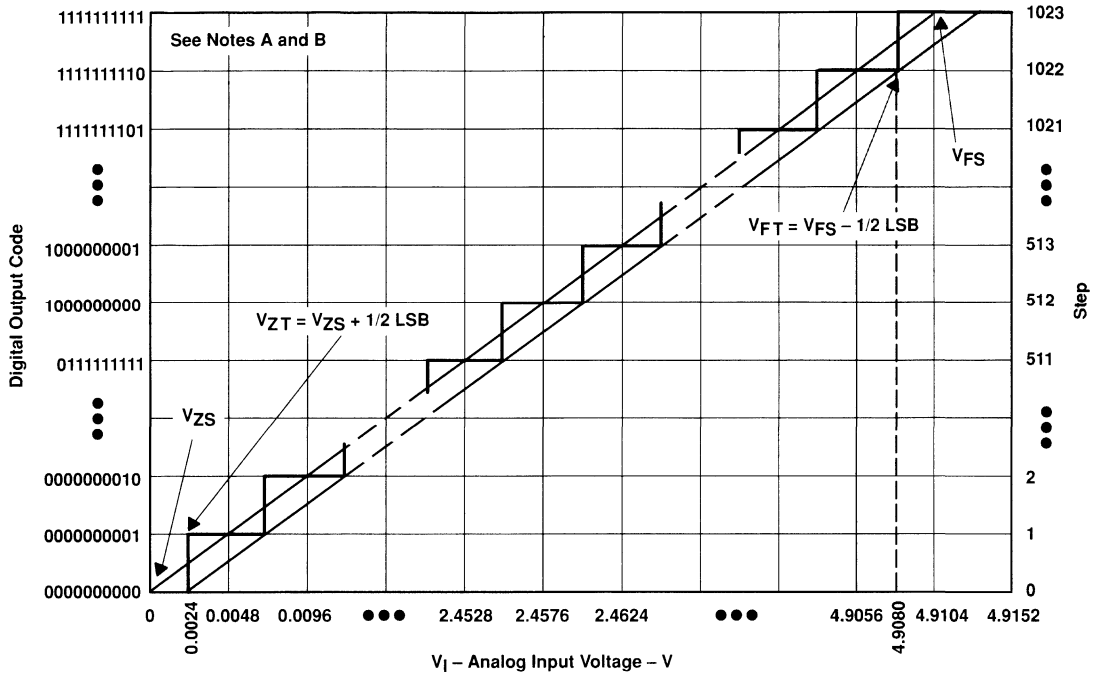


- NOTES: A. The eleventh rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.
- B. The I/O CLOCK sequence is exactly 16 clock pulses long.

Figure 14. Timing for 16-Clock Transfer Not Using \overline{CS} (Serial Transfer Interval Longer Than Conversion)

TLV1543C, TLV1543M
3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS
 SLAS072C – DECEMBER 1992 – REVISED MARCH 1995

APPLICATION INFORMATION



- NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0024 V and the transition to full scale (V_{FT}) is 4.908 V. 1 LSB = 4.8 mV.
 B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 15. Ideal Conversion Characteristics

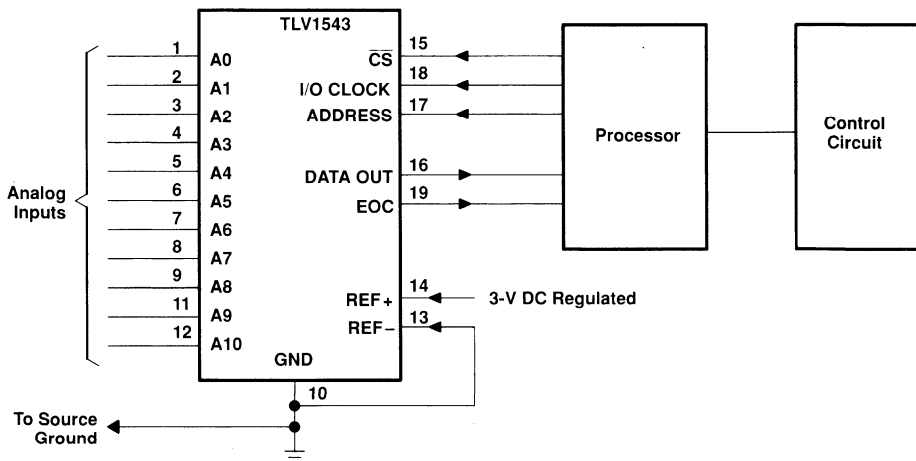


Figure 16. Serial Interface

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 17, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c/R_t C_i}\right) \tag{1}$$

where

$$R_t = R_s + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S/2048) \tag{2}$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S/2048) = V_S \left(1 - e^{-t_c/R_t C_i}\right) \tag{3}$$

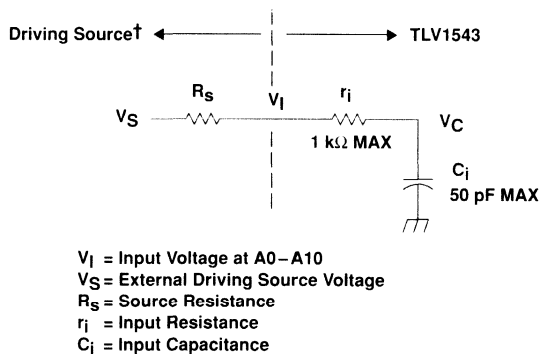
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(2048) \tag{4}$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_s + 1 \text{ k}\Omega) \times 60 \text{ pF} \times \ln(2048) \tag{5}$$

This time must be less than the converter sample time shown in the timing diagrams.



† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 17. Equivalent Input Circuit Including the Driving Source

TLV1544C, TLV1544I, TLV1548C, TLV1548I LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

- Conversion Time $\leq 10 \mu\text{s}$
- 10-Bit-Resolution ADC
- Programmable Power-Down Mode . . . $1 \mu\text{A}$
- Wide Range Single-Supply Operation of 2.7 V dc to 5.5 V dc
- Analog Input Range of 0 V to V_{CC}
- Built-in Analog Multiplexer with 8 Analog Input Channels
- TMS320 DSP and Microprocessor SPI and QSPI Compatible Serial Interfaces
- End-of-Conversion (EOC) Flag
- Inherent Sample-and-Hold Function
- Built-In Self-Test Modes
- Programmable Power and Conversion Rate
- Asynchronous Start of Conversion for Extended Sampling
- Hardware I/O Clock Phase Adjust Input

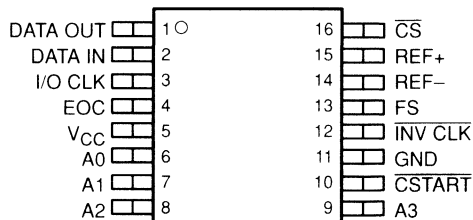
description

The TLV1544 and TLV1548 are CMOS 10-bit switched-capacitor successive-approximation (SAR) analog-to-digital (A/D) converters. Each device has a chip select (\overline{CS}), input-output clock (I/O CLK), data input (DATA IN) and serial data output (DATA OUT) that provide a direct 4-wire synchronous serial peripheral interface (SPI™, QSPI™) port of a host microprocessor. When interfacing with a TMS320 DSP, an additional frame sync signal (FS) indicates the start of a serial data frame. The devices allow high-speed data transfers from the host. The $\overline{INV CLK}$ input provides further timing flexibility for the serial interface.

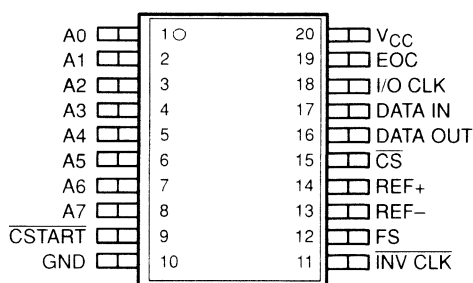
In addition to a high-speed converter and versatile control capability, the device has an on-chip 11-channel multiplexer that can select any one of eight analog inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic except for the extended sampling cycle where the sampling cycle is started by the falling edge of asynchronous \overline{CSTART} . At the end of the A/D conversion, the end-of-conversion (EOC) output goes high to indicate that the conversion is complete. The TLV1544 and TLV1548 are designed to operate with a wide range of supply voltages with very low power consumption. The power saving feature is further enhanced with a software-programmed power-down mode and conversion rate. The converter incorporated in the device features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating temperature range.

The TLV1544 has four analog input channels while the TLV1548 has eight analog input channels. The TLV1544C and TLV1548C are characterized for operation from 0°C to 70°C. The TLV1544I and TLV1548I are characterized for operation over the full industrial temperature range of –40°C to 85°C.

D OR PW PACKAGE
(TOP VIEW)



DB PACKAGE
(TOP VIEW)



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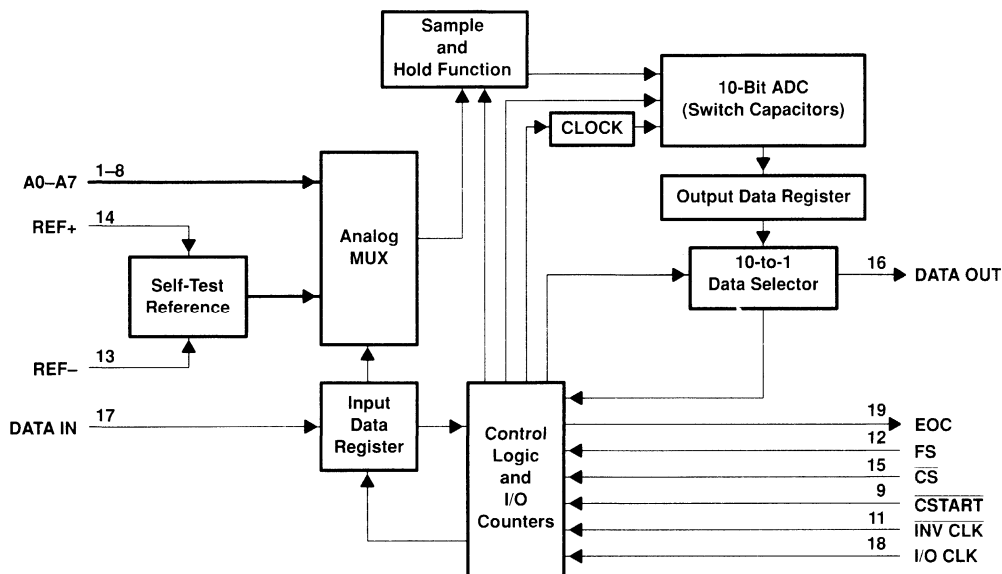
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TLV1544C, TLV1544I, TLV1548C, TLV1548I

LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

functional block diagram



Terminals shown are for the DB package.

AVAILABLE OPTIONS

T _A	PACKAGE		
	SMALL OUTLINE		
	(DB)	(D)	(PW)
0°C to 70°C	TLV1548CDB	TLV1544CD	TLV1544CPW
-40°C to 85°C	TLV1548IDB	TLV1544ID	TLV1544IPW

TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.†	NO.‡		
A0–A3 A4–A7	6–9 –	1–4 5–8	I	Analog inputs. The analog inputs are internally multiplexed. (For a source impedance greater than 1 k Ω , the asynchronous start should be used to increase the sampling time.)
\overline{CS}	16	15	I	Chip select. A high-to-low transition on \overline{CS} resets the internal counters and controls and enables DATA IN, DATA OUT, and I/O CLK within the maximum setup time. A low-to-high transition disables DATA IN, DATA OUT, and I/O CLK within the setup time.
CSTART	10	9	I	Sampling/conversion start control. CSTART controls the start of the sampling of an analog input from a selected multiplex channel. A high-to-low transition starts the sampling of the analog input signal. A low-to-high transition puts the sample-and-hold function in hold mode and starts the conversion. CSTART is independent from I/O CLK and works when \overline{CS} is high. The low CSTART duration controls the duration of the sampling cycle for the switched capacitor array. CSTART is tied to V _{CC} if not used.
DATA IN	2	17	I	Serial data input. The 4-bit serial data selects the desired analog input and test voltage to be converted next in a normal cycle. These bits can also set the conversion rate and enable the power-down mode. When operating in the microprocessor mode, the input data is presented MSB first and is shifted in on the first four rising (INV CLK = V _{CC}) or falling (INV CLK = GND) edges of I/O CLK (after $\overline{CS}\downarrow$). When operating in the DSP mode, the input data is presented MSB first and is shifted in on the first four falling (INV CLK = V _{CC}) or rising (INV CLK = GND) edges of I/O CLK (after FS \downarrow). After the four input data bits have been read into the input data register, DATA IN is ignored for the remainder of the current conversion period.
DATA OUT	1	16	O	Three-state serial output of the A/D conversion result. DATA OUT is in the high-impedance state when \overline{CS} is high and active when \overline{CS} is low or after FS \downarrow (in DSP mode). With a valid \overline{CS} signal, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB or LSB value of the previous conversion result. DATA OUT changes on the falling (microprocessor mode) or rising (DSP mode) edge of I/O CLK.
EOC	4	19	O	End of conversion. EOC goes from a high to a low logic level on the tenth rising (microprocessor mode) or tenth falling (DSP mode) edge of I/O CLK and remains low until the conversion is complete and data is ready for transfer. EOC can also indicate that the converter is busy.
FS	13	12	I	DSP frame synchronization input. FS indicates the start of a serial data frame into or out of the device. FS is tied to V _{CC} when interfacing the device with a microprocessor.
GND	11	10		Ground return for internal circuitry. All voltage measurements are with respect to GND, unless otherwise noted.
INV CLK	12	11	I	Inverted clock input. INV CLK is tied to GND when an inverted I/O CLK is used as the source of the input clock. This affects both microprocessor and DSP interfaces. INV CLK is tied to V _{CC} if I/O CLK is not inverted. INV CLK can also invoke a built-in test mode.

† Terminal numbers are for the D package.

‡ Terminal numbers are for the DB package.



TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.†	NO.‡		
I/O CLK	3	18	I	Input/output clock. I/O CLK receives the serial I/O clock input in the two modes and performs the following four functions in each mode: Microprocessor mode <ul style="list-style-type: none"> When $\overline{\text{INVCLK}} = V_{\text{CC}}$, I/O CLK clocks the four input data bits into the input data register on the first four rising edges of I/O CLK after $\overline{\text{CS}}\downarrow$ with the multiplexer address available after the fourth rising edges. When $\overline{\text{INV CLK}} = \text{GND}$, input data bits are clocked in on the first four falling edges instead. On the fourth falling edge of I/O CLK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth rising edge of I/O CLK except in the extended sampling cycle where the duration of $\overline{\text{CSTART}}$ determines when to end the sampling cycle. Output data bits change on the first ten falling I/O clock edges regardless of the condition of $\overline{\text{INV CLK}}$. I/O CLK transfers control of the conversion to the internal state machine on the tenth rising edge of I/O CLK regardless of the condition of $\overline{\text{INV CLK}}$. Digital signal processor (DSP) mode <ul style="list-style-type: none"> When $\overline{\text{INV CLK}} = V_{\text{CC}}$, I/O CLK clocks the four input data bits into the input data register on the first four falling edges of I/O CLK after $\overline{\text{FS}}\downarrow$ with the multiplexer address available after the fourth falling edges. When $\overline{\text{INV CLK}} = \text{GND}$, input data bits are clocked in on the first four rising edges instead. On the fourth rising edge of I/O CLK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLK except in the extended sampling cycle where the duration of $\overline{\text{CSTART}}$ determines when to end the sampling cycle. Output data MSB shows after $\overline{\text{FS}}\downarrow$ and the rest of the output data bits change on the first ten rising I/O CLK edges regardless of the condition of $\overline{\text{INV CLK}}$. I/O CLK transfers control of the conversion to the internal state machine on the tenth falling edge of I/O CLK regardless of the condition of $\overline{\text{INV CLK}}$.
REF+	15	14	I	Upper reference voltage (nominally V_{CC}). The maximum input voltage range is determined by the difference between the voltages applied to REF+ and REF-.
REF-	14	13	I	Lower reference voltage (nominally ground)
V _{CC}	5	20	I	Positive supply voltage

† Terminal numbers are for the D package.

‡ Terminal numbers are for the DB package.

detailed description

Initially, with $\overline{\text{CS}}$ high (inactive), DATA IN and I/O CLK are disabled and DATA OUT is in the high-impedance state. When the serial interface takes $\overline{\text{CS}}$ low (active), the conversion sequence begins with the enabling of I/O CLK and DATA IN and the removal of DATA OUT from the high-impedance state. The host then provides the 4-bit channel address to DATA IN and the I/O clock sequence to I/O CLK. During this transfer, the host serial interface also receives the previous conversion result from DATA OUT. I/O CLK receives an input sequence from the host that is between 10 to 16 clocks long. The first four valid I/O CLK cycles load the input data register with the 4-bit input data on DATA IN that selects the desired analog channel. The next six clock cycles provide the control timing for sampling the analog input. Sampling of the analog input is held after the first valid I/O CLK sequence of ten clocks. The tenth clock edge also takes EOC low and begins the conversion. The exact locations of the I/O clock edges depend on the mode of operation.

serial interface

The TLV1548 is compatible with generic microprocessor serial interfaces such as SPI and QSPI, and a TMS320 DSP serial interface. The internal latched flag If_mode is generated by sampling the state of FS at the falling edge of $\overline{\text{CS}}$. If_mode is set to one (for microprocessor) when FS is high at the falling edge of $\overline{\text{CS}}$, and If_mode is cleared to zero (for DSP) when FS is low at the falling edge of $\overline{\text{CS}}$. This flag controls the multiplexing of I/O CLK and the state machine reset function. FS is pulled high when interfacing with a microprocessor.



TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

I/O CLK

The I/O CLK can go up to 10 MHz for most of the voltage range when fast I/O is possible. The maximum I/O CLK is limited to 2.8 MHz for a supply voltage range from 2.7 V. Table 1 lists the maximum I/O CLK frequencies for all different supply voltage ranges. This also depends on input source impedance. For example, I/O CLK speed faster than 2.39 MHz is achievable if the input source impedance is less than 1 k Ω .

Table 1. Maximum I/O CLK Frequency

V _{CC}	MAXIMUM INPUT RESISTANCE (Max)	SOURCE IMPEDANCE	I/O CLK
2.7 V	5 K	1 k Ω	2.39 MHz
		100 Ω	2.81 MHz
4.5 V	1 K	1 k Ω	7.18 MHz
		100 Ω	10 MHz

microprocessor serial interface

Input data bits from DATA IN are clocked in on the first four rising edges of the I/O CLK sequence if $\overline{\text{INV CLK}}$ is held high when the device is in microprocessor interface mode. Input data bits are clocked in on the first four falling edges of the I/O CLK sequence if $\overline{\text{INV CLK}}$ is held low. The MSB of the previous conversion appears on DATA OUT on the falling edge of $\overline{\text{CS}}$. The remaining nine bits are shifted out on the next nine edges (depending on the state of $\overline{\text{INV CLK}}$) of I/O CLK. Ten bits of data are transmitted to the host through DATA OUT.

A minimum of 9.5 clock pulses is required for the conversion to begin. On the tenth clock rising edge, the EOC output goes low and returns to the high logic level when the conversion is complete, and then the result can be read by the host. On the tenth clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLK transfer is more than ten clocks long.

$\overline{\text{CS}}$ is inactive (high) between serial I/O CLK transfers. Each transfer takes at least ten I/O CLK cycles. The falling edge of $\overline{\text{CS}}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{\text{CS}}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{\text{CS}}$ disables I/O CLK and DATA IN within a setup time. A conversion does not begin until the tenth I/O CLK rising edge.

A high-to-low transition on $\overline{\text{CS}}$ within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the output data register holds the previous conversion result). $\overline{\text{CS}}$ should not be taken low close to completion of conversion because the output data can be corrupted.

TLV1544C, TLV1544I, TLV1548C, TLV1548I

LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

DSP interface

The TLV1544/1548 can also interface with a DSP, from the TMS320 family for example, through a serial port. The analog-to-digital converter (ADC) serves as a slave device where the DSP supplies FS and the serial I/O CLK. Transmit and receive operations are concurrent. The falling edge of FS must occur no later than seven I/O CLK periods after the falling edge of \overline{CS} .

DSP I/O cycles differ from microprocessor I/O cycles in the following ways:

- When interfaced with a DSP, the output data MSB shows after $\overline{FS}\downarrow$ and the rest of the output data changes on the rising edge of I/O CLK, and input data is sampled on the first four falling edges of I/O CLK after FS falling when $\overline{INV\ CLK}$ is high, or the first four rising edges of I/O CLK after FS falling when $\overline{INV\ CLK}$ is low. This operation is the opposite when interfaced with a microprocessor.
- A new DSP I/O cycle is started on the rising edge of I/O CLK after the rising edge of FS. The internal state machine is reset on each falling edge of I/O CLK when FS is high. This operation is opposite when interfaced with a microprocessor.
- The TLV1544/1548 supports a 16-clock cycle when interfaced with a DSP. The output data is padded with six trailing zeros when it is operated in DSP mode.

Table 2. TLV1544/TLV1548 Serial Interface Modes

I/O	INTERFACE MODE	
	MICROPROCESSOR ACTION	DSP ACTION
$\overline{CS}\downarrow$	Initializes counter	Samples state of FS
$\overline{CS}\uparrow$	Resets state machine and disable I/O	Disables I/O
FS	Connects to V_{CC}	Connects to DSP FSX output. Initializes the state machine at each $CLK\downarrow$ after $FS\uparrow$. Starts a new cycle at each $CLK\uparrow$ following the initialization (initializes the counter).
I/O CLK	Starts sampling of the analog input started at fourth I/O $CLK\uparrow$. Conversion started at tenth I/O $CLK\uparrow$.	Starts sampling of the analog input at fourth I/O $CLK\downarrow$. Starts sampling of the analog input at tenth I/O $CLK\downarrow$.
DATA IN	Samples input data on I/O $CLK\uparrow$ ($\overline{INV\ CLK}$ high). Samples input data on I/O $CLK\downarrow$ ($\overline{INV\ CLK}$ low).	Samples input data at I/O $CLK\downarrow$ ($\overline{INV\ CLK}$ high). Samples input data at I/O $CLK\uparrow$ ($\overline{INV\ CLK}$ low).
DATA OUT	Makes MSB available on $\overline{CS}\downarrow$. Changes remaining data on I/O $CLK\downarrow$.	Makes MSB available $FS\downarrow$. Changes remaining data at each following I/O $CLK\uparrow$ after $FS\downarrow$.

TLV1544C, TLV1544I, TLV1548C, TLV1548I LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

input data bits

DATA IN is internally connected to a 4-bit serial input data register. The input data selects a different mode or selects different analog input channels. The host provides the data word with the MSB first. Each data bit clocks in on the edge (rising or falling depending on the status of INV CLK and FS) of the I/O CLK sequence. The input clock can be inverted by grounding INV CLK (see Table 3 for the list of software programmed operations set by the input data).

Table 3. TLV1544/1548 Software-Programmed Operation Modes

FUNCTION SELECT	INPUT DATA BYTE		COMMENT
	A3 – A0		
	BINARY	HEX	
Analog channel A0 for TLV1548 selected	0000b	0h	Channel 0 for TLV1544
Analog channel A1 for TLV1548 selected	0001b	1h	
Analog channel A2 for TLV1548 selected	0010b	2h	Channel 1 for TLV1544
Analog channel A3 for TLV1548 selected	0011b	3h	
Analog channel A4 for TLV1548 selected	0100b	4h	Channel 2 for TLV1544
Analog channel A5 for TLV1548 selected	0101b	5h	
Analog channel A6 for TLV1548 selected	0110b	6h	Channel 3 for TLV1544
Analog channel A7 for TLV1548 selected	0111b	7h	
Software power down set	1000b	8h	No conversion result (cleared by any access)
Fast conversion rate (10 μ s) set	1001b	9h	No conversion result (cleared by setting to fast)
Slow conversion rate (40 μ s) set	1010b	Ah	No conversion result (cleared by setting to slow)
Self-test voltage ($V_{ref+} - V_{ref-}$)/2 selected	1011b	Bh	Output result = 200h
Self-test voltage V_{ref-} selected	1100b	Ch	Output result = 000h
Self-test voltage V_{ref+} selected	1101b	Dh	Output result = 3FFh
Reserved	1110b	Eh	No conversion result
Reserved	1111b	Fh	No conversion result



TLV1544C, TLV1544I, TLV1548C, TLV1548I LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

analog inputs and internal test voltages

The eight analog inputs and the three internal test inputs are selected by the 11-channel multiplexer according to the input data bit as shown in Table 3. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching.

The device can be operated in two distinct sampling modes: normal sampling mode (fixed sampling time) and extended sampling mode (flexible sampling time). When $\overline{\text{CSTART}}$ is held high, the device is operated in normal sampling mode. When operated in normal sampling mode, sampling of the analog input starts on the rising edge of the fourth I/O CLK pulse in the microprocessor interface mode (and on the fourth falling edge of I/O CLK in the DSP interface mode). Sampling continues for 6 I/O CLK periods. The sample is held on the falling edge of the tenth I/O CLK pulse in the microprocessor interface mode. The sample is held on the falling edge of the tenth I/O CLK pulse in the DSP interface mode. The three test inputs are applied to the multiplexer, then sampled and converted in the same manner as the external analog inputs.

converter

The CMOS threshold detector in the successive-approximation conversion system determines the value of each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all of the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF-) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF-. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF-. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and the 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are counted.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.

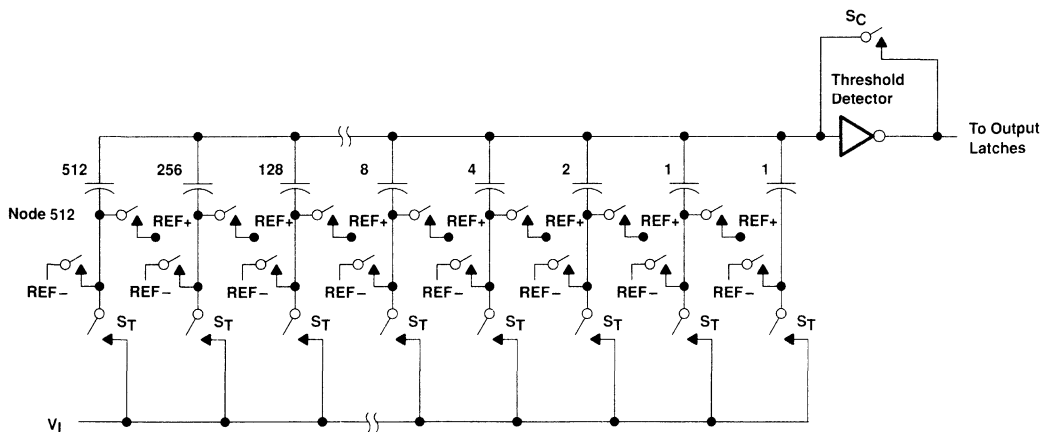


Figure 1. Simplified Model of the Successive-Approximation System

TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

extended sampling, asynchronous start of sampling: $\overline{\text{CSTART}}$ operation

The extended sampling mode of operation programs the acquisition time (t_{ACQ}) of the sample-and-hold circuit. This allows the analog inputs of the device to be directly interfaced to a wide range of input source impedances. The extended sampling mode consumes higher power depending on the duration of the sampling period chosen.

$\overline{\text{CSTART}}$ controls the sampling period and starts the conversion. The falling edge of $\overline{\text{CSTART}}$ initiates the sampling period of a preset channel. The low time of $\overline{\text{CSTART}}$ controls the acquisition time of the input sample-and-hold circuit. The sample is held on the rising edge of $\overline{\text{CSTART}}$. Asserting $\overline{\text{CSTART}}$ causes the converter to perform a new sample of the signal on the preset valid MUX channel (one of the eight) and discard the current conversion result ready for output. Sampling continues as long as $\overline{\text{CSTART}}$ is active (negative). The rising edge of $\overline{\text{CSTART}}$ ends the sampling cycle. The conversion cycle starts two internal system clocks after the rising edge of $\overline{\text{CSTART}}$.

Once the conversion is complete, the processor can initiate a normal I/O cycle to read the conversion result and set the MUX address for the next conversion. Since the internal flag AsyncFlag is set high, this flag setting indicates the cycle is an output cycle so no conversion is performed during the cycle. The internal state machine tests the AsyncFlag on the falling edge of $\overline{\text{CS}}$. AsyncFlag is set high at the rising edge of $\overline{\text{CSTART}}$, and it is reset low at the rising edge of each $\overline{\text{CS}}$. A conversion cycle follows a sampling cycle only if AsyncFlag is tested as low at the falling edge of $\overline{\text{CS}}$. As shown in Figure 2, an asynchronous I/O cycle can be removed by two consecutive normal I/O cycles.

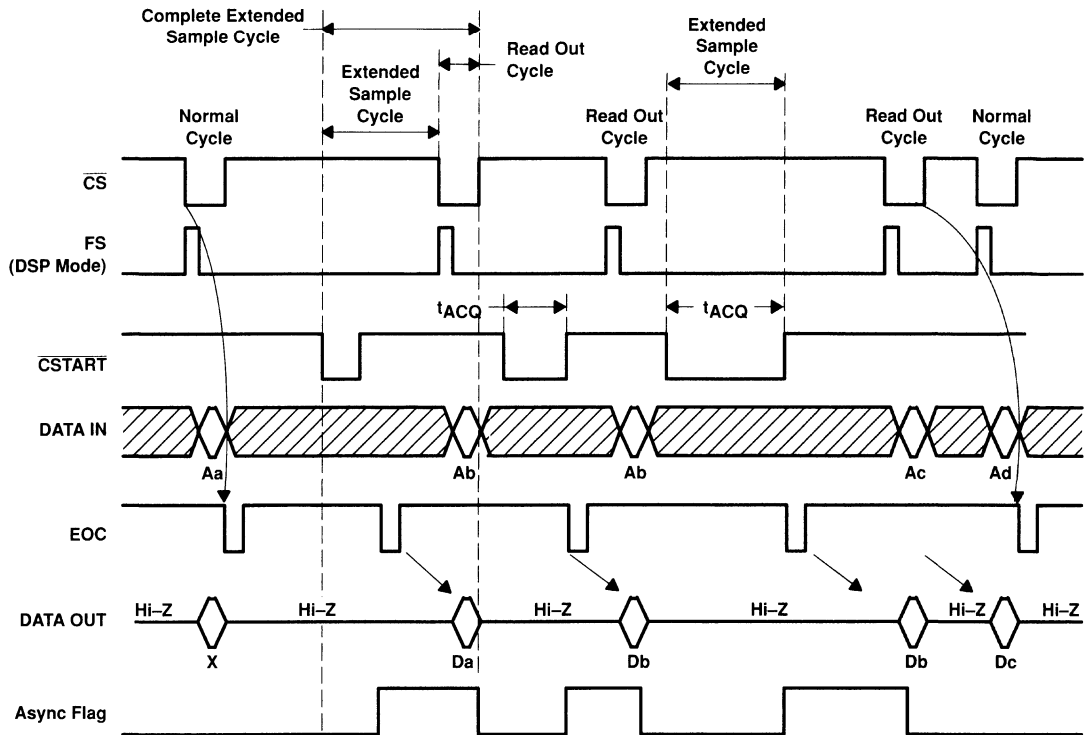
Table 4. TLV1544/1548 Hardware Configuration for Different Operating Modes

OPERATING MODES	$\overline{\text{CS}}$	$\overline{\text{CSTART}}$	AsyncFlag at $\overline{\text{CS}}\downarrow$	ACTION
Normal sampling	Low	High	Low	Fixed 6 I/O CLK sampling, synchronous conversion follows
Normal I/O (read out only)	Low	High	High	No sampling, no conversion
Extended sampling	High	Low	N/A	Flexible sampling period controlled by $\overline{\text{CSTART}}$, asynchronous conversion follows



TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997



NOTES: C. Aa = Address for input channel a.
 D. Da = Conversion result from channel a.

Figure 2. Extended Sampling Operation

reference voltage inputs

There are two reference inputs used with the TLV1544/TLV1548, REF+ and REF-. These voltage values establish the upper and lower limits of the analog inputs to produce a full-scale and zero-scale reading respectively. The values of REF+, REF-, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and is at zero when the input signal is equal to or lower than REF-.

programmable conversion rate

The TLV1544/TLV1548 offers two conversion rates to maximize battery life when high-speed operation is not necessary. The conversion rate is programmable. Once the conversion rate has been selected, it takes effect immediately in the same cycle and stays at the same rate until the other rate is chosen. The conversion rate should be set at power up. Activation and deactivation of the power-down state (digital logic active) has no effect on the preset conversion rate.



TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS
SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

Table 5. Conversion Rate and Power Consumption Selection

CONVERSION RATE	CONVERSION TIME, t_{conv}	AVAILABLE V_{CC} RANGE	INPUT DATA	TYPICAL SUPPLY CURRENT, I_{CC}		
				OPERATING		POWER DOWN
Fast conversion speed	7 μ s typ	5.5 V to 3.3 V	9h	0.6 mA typ	1.5 mA max	1 μ A typ
Slow conversion speed	15 μ s typ	5.5 V to 2.7 V	Ah	0.4 mA typ	1 mA max	1 μ A typ

programmable power-down state

The device is put into the power-down state by writing 8h to DATA IN. The power-up state is restored during the next active access by pulling \overline{CS} low. The conversion rate selected before the device is put into the power-down state is not affected by the power-down mode. Power-down can be used to achieve even lower power consumption. This is because the sustaining power (when not converting) is only 1.3 mA maximum and standby power is only 1 μ A maximum. By averaging out the power consumption can be much lower than the 1 mA peak when the conversion throughput is lower.

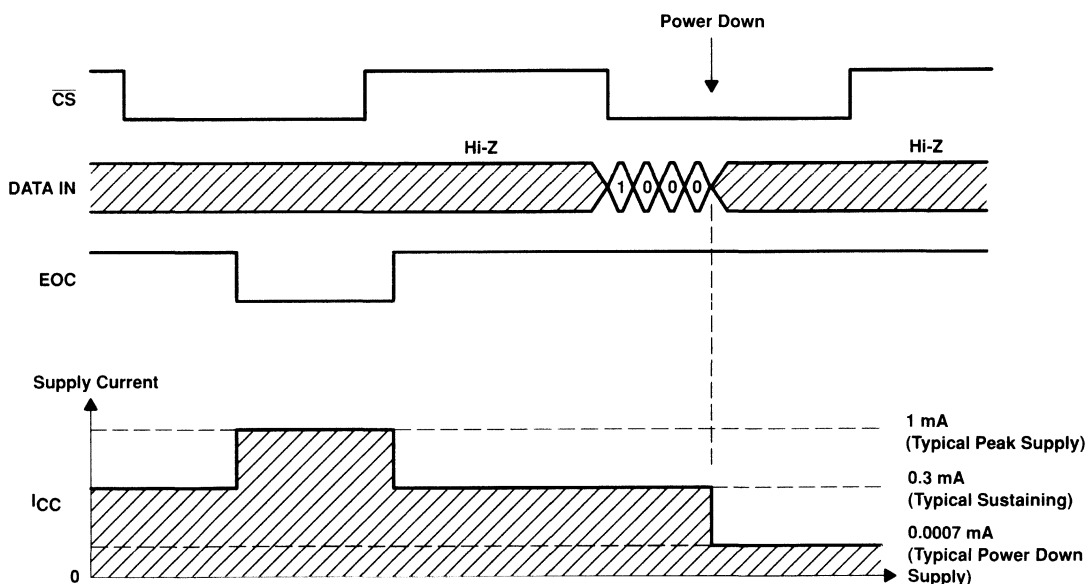


Figure 3. Typical Supply Current During Conversion/Power Down

power up and initialization

After power up, if operating in DSP mode, \overline{CS} and FS must be taken from high to low to begin an I/O cycle. EOC is initially high, and the input data register is set to all zeroes. The contents of the output data register is random, and the first conversion result should be ignored. For initialization during operation, \overline{CS} is taken high and returned low to begin the next I/O cycle. The first conversion after the device has returned from the power-down state can be invalid and should be disregarded.

When power is first applied to the device, the conversion rate must be programmed, and the internal Async Flag must be taken low once. The rising edge of \overline{CS} of the same cycle then takes Async Flag low.

TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

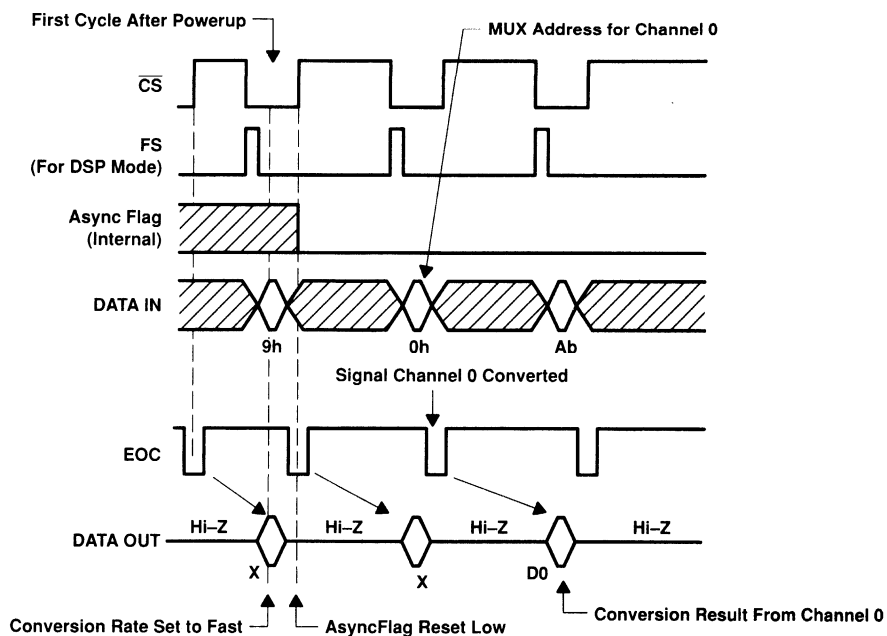


Figure 4. Power Up Initialization

input clock inversion – $\overline{\text{INV CLK}}$

The input data register uses I/O CLK as the source of the sampling clock. This clock can be inverted to provide more setup time. $\overline{\text{INV CLK}}$ can invert the clock. When $\overline{\text{INV CLK}}$ is grounded, the input clock for the input data register is inverted. This allows an additional one-half I/O CLK period for the input data setup time. This is useful for some serial interfaces. When the input sampling clock is inverted, the output data changes at the same time that the input data is sampled.

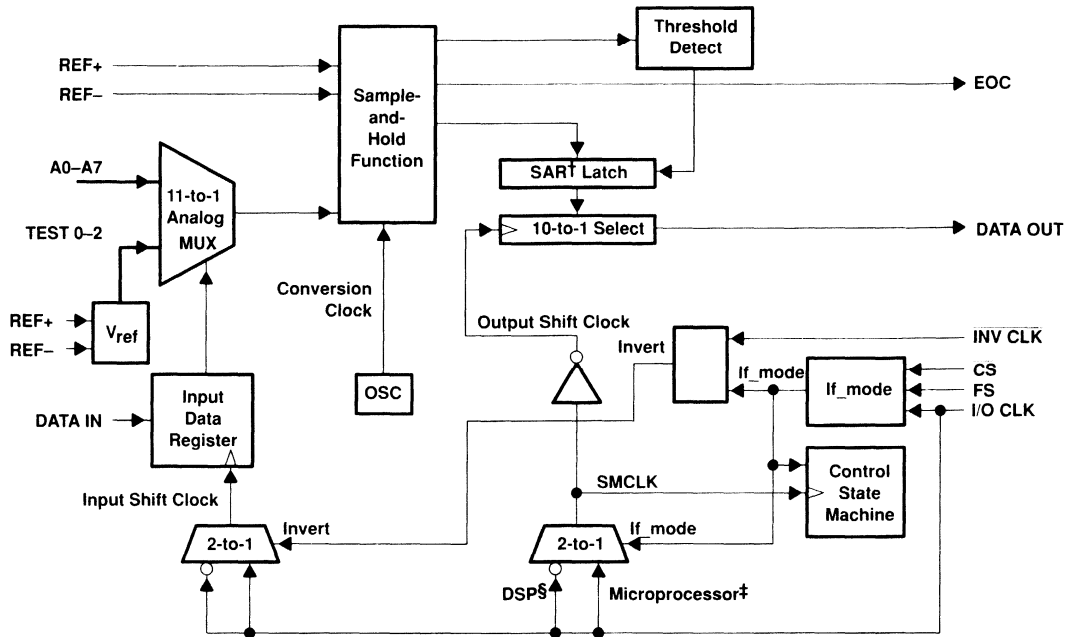
Table 6. Function of $\overline{\text{INV CLK}}$

CONDITION CLOCK		I/O CLK ACTIVE EDGE	
INV CLK	FS at $\overline{\text{CS}}$ ↓	OUTPUT DATA CHANGES ON	INPUT DATA SAMPLED ON
High	High (MP† mode)	↓	↑
High	Low (DSP‡ mode)	↑	↓
Low	High (MP† mode)	↓	↓
Low	Low (DSP‡ mode)	↑	↑

† MP = microprocessor mode
 ‡ DSP = digital signal processor mode

TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997



† Successive approximation register
‡ If_mode = 1, microprocessor interface mode
§ If_mode = 0, DSP interface mode

Figure 5. Clock Scheme

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 6.5 V
Input voltage range, V_I (any input)	–0.3 V to $V_{CC} + 0.3$ V
Output voltage range, V_O	–0.3 V to $V_{CC} + 0.3$ V
Positive reference voltage, V_{ref+}	$V_{CC} + 0.1$ V
Negative reference voltage, V_{ref-}	–0.1 V
Peak input current, I_I (any input)	±20 mA
Peak total input current (all inputs)	–30 mA
Operating free-air temperature range, T_A : TLV1544C, TLV1548C	0°C to 70°C
TLV1544I, TLV1548I	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from the case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND with REF– and GND wired together (unless otherwise noted).

TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

recommended operating conditions

	MIN	NOM	MAX	UNIT	
Supply voltage, V_{CC}	2.7		5.5	V	
Positive reference voltage, V_{ref+} (see Note 2)		V_{CC}		V	
Negative reference voltage, V_{ref-} (see Note 2)		0		V	
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)	2.5	V_{CC}	$V_{CC} + 0.2$	V	
Analog input voltage, V_I (analog) (see Note 2)	0		V_{CC}	V	
High-level control input voltage, V_{IH}	2.1			V	
Low-level control input voltage, V_{IL}			0.6	V	
Setup time, input data bits valid before I/O CLK $\uparrow\downarrow$, $t_{su}(A)$ (see Figure 9)	100			ns	
Hold time, input data bits valid after I/O CLK $\uparrow\downarrow$, $t_h(A)$ (see Figure 9)	5	30		ns	
Setup time, $\overline{CS}\downarrow$ to I/O CLK \uparrow , $t_{su}(CS)$	See Figure 10	5	30	ns	
Hold time, I/O CLK \downarrow to $\overline{CS}\uparrow$, $t_h(CS)$	See Figure 10	65		ns	
Pulse duration, FS high, $t_{wH}(FS)$	See Figure 12	1		I/O CLK periods	
Pulse duration, \overline{CSTART} , $t_w(CSTART)$	Source impedance $\leq 1\text{ k}\Omega$, $V_{CC} = 5.5\text{ V}$, See Figure 14	0.84		μs	
Setup time, $\overline{CS}\uparrow$ to $\overline{CSTART}\downarrow$, $t_{su}(CSTART)$	See Figure 14	10		ns	
Clock frequency at I/O CLK, f_{CLK}	$V_{CC} = 5.5\text{ V}$	0.1	6	10	MHz
	$V_{CC} = 2.7\text{ V}$	0.1	2	2.81	
Pulse duration, I/O CLK high, $t_{wH}(I/O)$	$V_{CC} = 5.5\text{ V}$	50			ns
	$V_{CC} = 2.7\text{ V}$	100			
Pulse duration, I/O CLK low, $t_{wL}(I/O)$	$V_{CC} = 5.5\text{ V}$	50			ns
	$V_{CC} = 2.7\text{ V}$	100			
Transition time, I/O CLK, $t_t(I/O)$ (see Figure 11 and Note 4)			1	μs	
Transition time, DATA IN, $t_t(\text{DATA IN})$ (see Figure 9)			10	μs	
Transition time, \overline{CS} , $t_t(\overline{CS})$ (see Figure 10)			10	μs	
Transition time, FS, $t_t(FS)$ (see Figure 13)			10	μs	
Transition time, \overline{CSTART} , $t_t(\overline{CSTART})$ (see Figure 14)			10	μs	
Operating free-air temperature, T_A	TLV1544C, TLV1548C	0	70	$^{\circ}\text{C}$	
	TLC1544I, TLV1548I	-40	85		

- NOTES: 2. Analog input voltages greater than the voltage applied to REF+ convert as all ones (1111111111), while input voltages less than the voltage applied to REF- convert as all zeros (0000000000). The device is functional with reference ($V_{ref+} - V_{ref-}$) down to 1 V; however, the electrical specifications are no longer applicable.
3. To minimize errors caused by noise at $\overline{CS}\downarrow$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in an input dat until the minimum \overline{CS} setup time has elapsed.
4. This is the time required for the I/O CLK signal to fall from V_{IHmax} to V_{ILmin} or to rise from V_{ILmax} to V_{IHmin} . In the vicinity of normal room temperature, the devices function with an input clock transition time as slow as 1 μs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.



TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

**electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 2.7\text{ V to }5.5\text{ V}$, I/O CLK frequency = 2.2 MHz (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage	V _{CC} = 5.5 V,	I _{OH} = -0.2 mA	2.4		V	
		V _{CC} = 2.7 V,	I _{OH} = -20 μA	V _{CC} -0.1			
V _{OL}	Low-level output voltage	V _{CC} = 5.5 V,	I _{OL} = 0.8 mA	0.4		V	
		V _{CC} = 2.7 V,	I _{OL} = 20 μA	0.1			
I _{OZ}	High-impedance output current	V _O = V _{CC} ,	C _S = V _{CC}	1		μA	
		V _O = 0,	C _S = V _{CC}	-1 -2.5			
I _{IH}	High-level input current	V _I = V _{CC}		0.005		2.5	μA
I _{IL}	Low-level input current	V _I = 0		-0.005		2.5	μA
I _{CC}	Operating supply current	Conversion speed = fast, For all digital inputs, 0 ≤ V _I ≤ 0.3 V or V _I ≥ V _{CC} - 0.3 V	V _{CC} = 3.3 V to 5.5 V	0.6		1.5	mA
			V _{CC} = 3.3 V to 5.5 V	0.4		1	
		Conversion speed = slow, For all digital inputs, 0 ≤ V _I ≤ 0.3 V or V _I ≥ V _{CC} - 0.3 V	V _{CC} = 2.7 V to 3.3 V	0.35		0.75	
I _{CC(ES)}	Extended sampling mode operating current	V _{CC} = 3.3 V to 5.5 V		1.5		mA	
		V _{CC} = 2.7 V to 3.3 V		1		mA	
I _{CC(ST)}	Sustaining supply current	Conversion speed = slow, For all digital inputs, 0 ≤ V _I ≤ 0.3 V or V _I ≥ V _{CC} - 0.3 V	V _{CC} = 2.7 V to 3.3 V	0.3		mA	
I _{CC(PD)}	Power-down supply current	For all digital inputs, 0 ≤ V _I ≤ 0.3 V or V _I ≥ V _{CC} - 0.3 V		1		25	μA
I _{lkg}	Selected channel leakage current	Selected channel at V _{CC} , unselected channel at 0 V		1		μA	
		Selected channel at 0 V, unselected channel at V _{CC}		-1		μA	
Maximum static analog reference current into REF+		V _{ref+} = V _{CC} = 5.5 V,	V _{ref-} = GND	1		μA	
C _i	Input capacitance, analog inputs			20		55	pF
	Input capacitance, control inputs			20		15	
Z _i	Input multiplexer on resistance	V _{CC} = 4.5 V		1		kΩ	
		V _{CC} = 2.7 V		5			

† All typical values are at V_{CC} = 5 V, T_A = 25°C.



TLV1544C, TLV1544I, TLV1548C, TLV1548I LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

operating characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 2.7\text{ V to }5.5\text{ V}$, I/O CLK frequency = 2.2 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error (see Note 6)			±0.5	±1	LSB
E_D	Differential linearity error	See Note 2		±0.5	±1	LSB
E_O	Offset error (see Note 7)	See Note 2			±1.5	LSB
E_G	Gain error (see Note 7)	See Note 2			±1	LSB
E_T	Total unadjusted error (see Note 8)				±1.75	LSB
Self-test output code (see Table 3 and Note 9)		DATA IN = 1011		512		
		DATA IN = 1100		0		
		DATA IN = 1101		1023		
t_{conv}	Conversion time	Fast conversion speed	See Figures 15 through 17	7	10	µs
		Slow conversion speed		15	25	µs
t_c	Total cycle time (access, sample, conversion and $EOC\uparrow$ to $CS\downarrow$ delay)	Fast conversion speed	See Figures 15 through 18 and Notes 10, 11, 12		10.1 + 10 I/O CLK	µs
		Slow conversion speed	See Figures 15 through 18 and Notes 10 and 12		40.1 + 10 I/O CLK	
t_{acq}	Channel acquisition time (sample)	See Figures 15 through 18 and Note 10			6	I/O CLK periods
t_v	Valid time, DATA OUT remains valid after I/O CLK \downarrow	See Figure 11	50			ns
$t_{d1}(FS)$	Delay time, I/O CLK high to FS high	See Figure 13	5	30	50	ns
$t_{d2}(FS)$	Delay time, I/O CLK high to FS low	See Figure 13	10	30	60	ns
$t_d(EOC\uparrow - CS\downarrow)$	Delay time, $EOC\uparrow$ to CS low	See Figure 14 and Note 5	100			ns
$t_d(CS\downarrow - FS\uparrow)$	Delay time, $CS\downarrow$ to $FS\uparrow$	See Figures 17 and 18	1		7	I/O CLK periods
$t_d(I/O - CS)$	Delay time, 10th I/O CLK low to CS low to abort conversion (see Note 13)	See Figure 10			1.1	µs

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000). The device is functional with reference down to 1 V ($V_{ref+} - V_{ref-} = 1$); however, the electrical specifications are no longer applicable.

5. For all operating modes.

6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.

7. Zero error is the difference between 0000000000 and the converted output for zero input voltage. Full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.

8. Total unadjusted error comprises linearity, zero-scale, and full-scale errors.

9. Both the input data and the output codes are expressed in positive logic.

10. I/O CLK period = 1/(I/O CLK frequency) (see Figure 8).

11. For 3.3 V to 5.5 V only

12. For microprocessor mode

13. Any transitions of \overline{CS} are recognized as valid only when the level is maintained for a setup time after the transition.



TLV1544C, TLV1544I, TLV1548C, TLV1548I LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

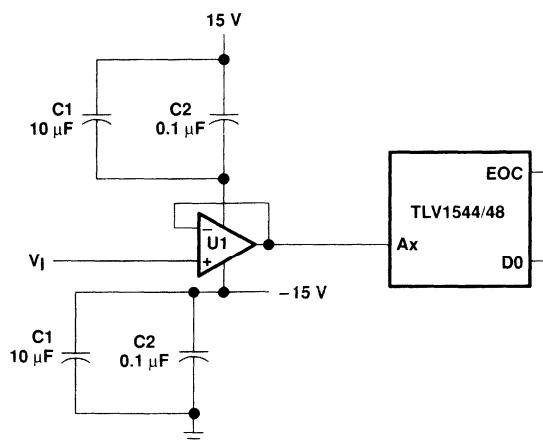
SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

operating characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 2.7\text{ V to }5.5\text{ V}$, I/O CLK frequency = 2.2 MHz (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_d(\text{I/O-DATA})$	Delay time, I/O CLK low to DATA OUT valid			50	ns
$t_d(\text{I/O-EOC})$	Delay time, 10th I/O CLK↓ to EOC low		70	240	ns
t_{PZH}, t_{PZL}	Enable time, $\overline{\text{CS}}$ low to DATA OUT valid (MSB driven)		0.7	1.3	μs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{\text{CS}}$ high to DATA OUT invalid (high impedance)		70	150	ns
$t_f(\text{EOC})$	Fall time, EOC		15	50	ns
$t_r(\text{bus})$	Rise time, output data bus at 2.2 MHz I/O CLK		50	250	ns
$t_f(\text{bus})$	Fall time, output data bus at 2.2 MHz I/O CLK		50	250	ns

† All typical values are at $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



LOCATION	DESCRIPTION	PART NUMBER
U1	OP27	—
C1	10- μF 35-V tantalum capacitor	—
C2	0.1- μF ceramic NPO SMD capacitor	AVX 12105C104KA105 or equivalent

Figure 6. Analog Input Buffer to Analog Inputs

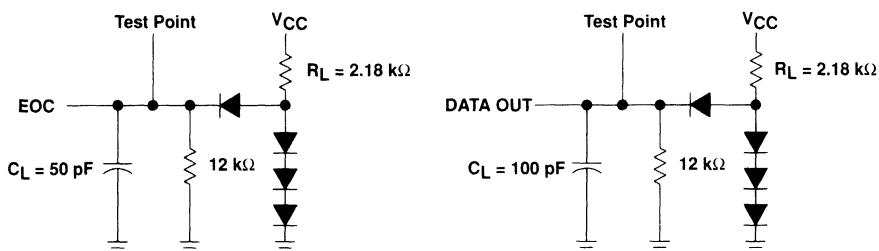


Figure 7. Load Circuits



TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

PARAMETER MEASUREMENT INFORMATION

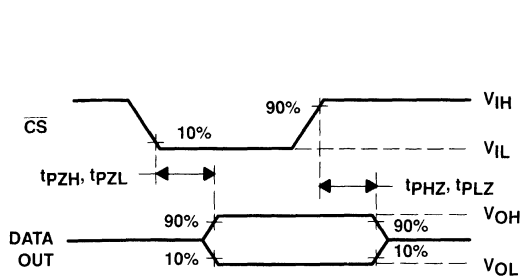


Figure 8. DATA OUT to Hi-Z Voltage Waveforms

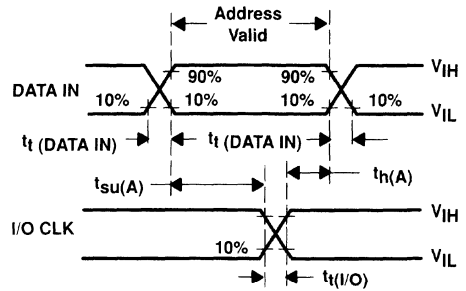


Figure 9. DATA IN Setup Voltage Waveforms

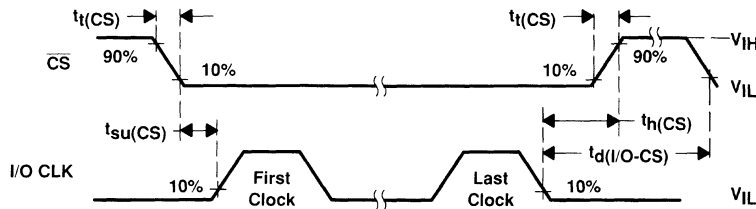


Figure 10. CS and I/O CLK Voltage Waveforms

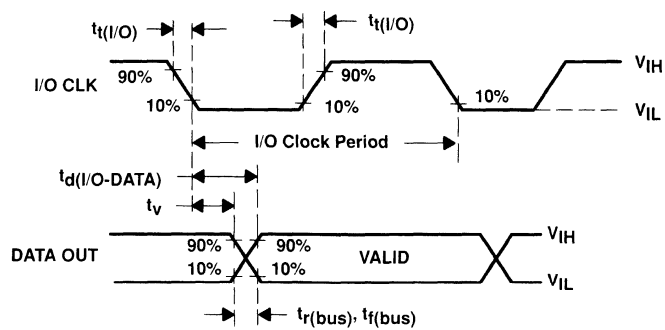


Figure 11. DATA OUT and I/O CLK Voltage Waveforms

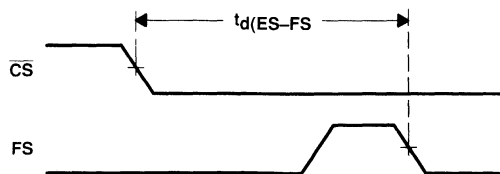


Figure 12. CS Low to FS Low

TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

PARAMETER MEASUREMENT INFORMATION

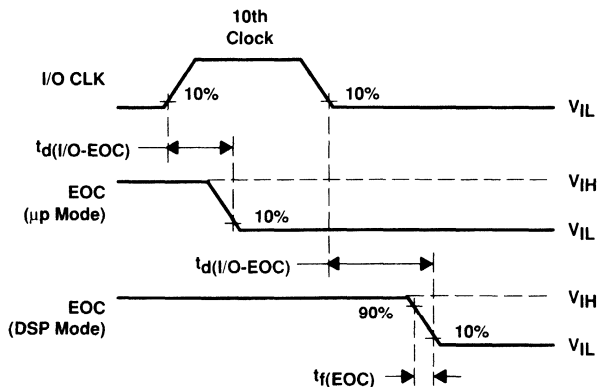


Figure 13. I/O CLK and EOC Voltage Waveforms

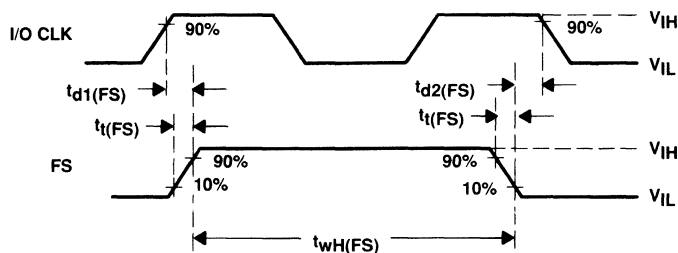


Figure 14. FS and I/O CLK Voltage Waveforms

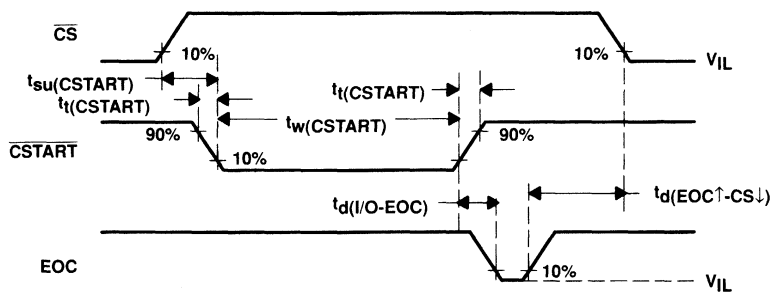
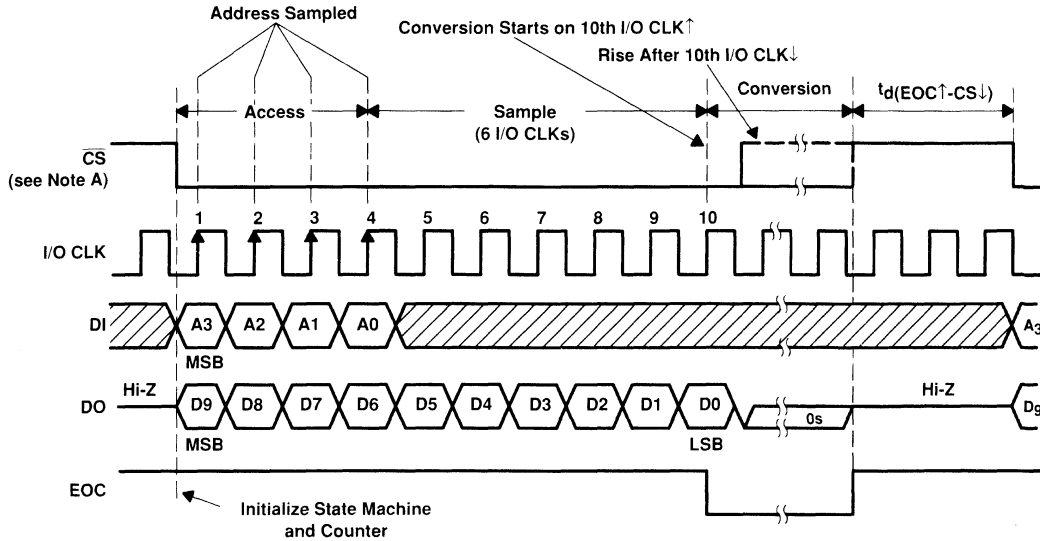


Figure 15. CSTART and CS Waveforms

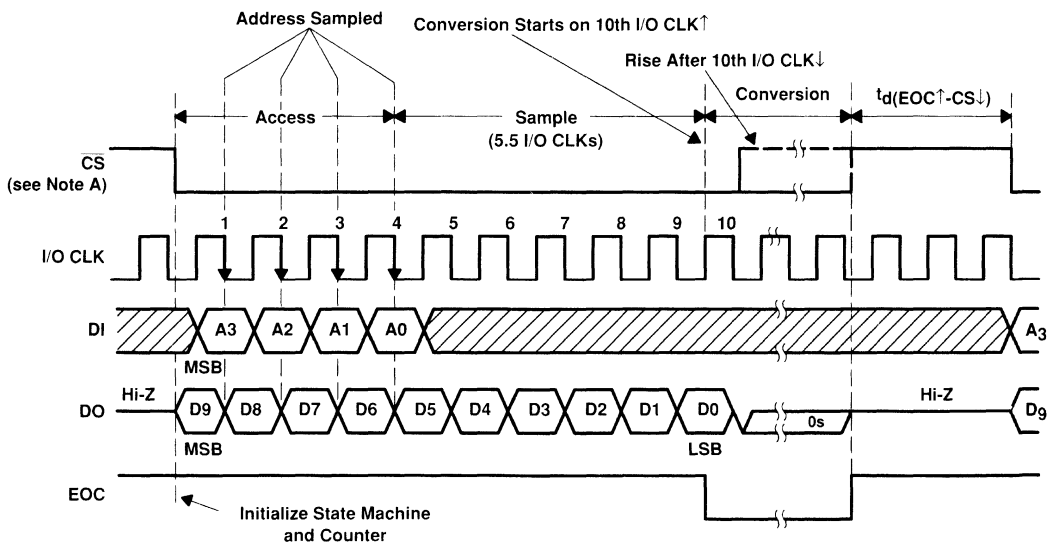
TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS
 SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

PARAMETER MEASUREMENT INFORMATION



NOTE A: To minimize errors caused by noise at $\overline{\text{CS}}$, the internal circuitry waits for a setup time after $\overline{\text{CS}}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{\text{CS}}$ setup time elapses.

Figure 16. Microprocessor Interface Timing (Normal Sample Mode, $\overline{\text{INV CLK}} = \text{High}$)



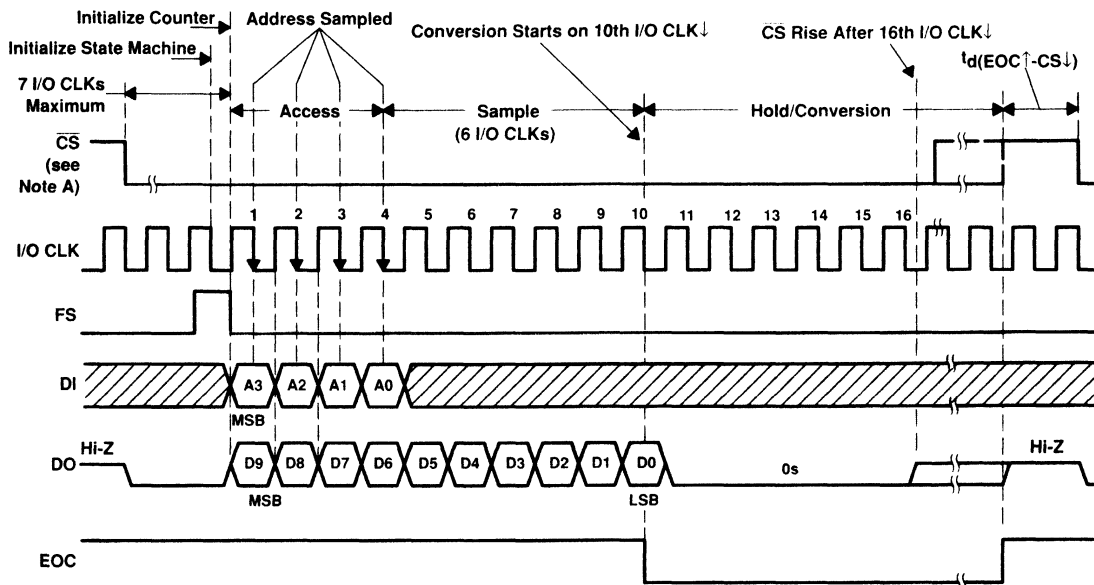
NOTE A: To minimize errors caused by noise at $\overline{\text{CS}}$, the internal circuitry waits for a setup time after $\overline{\text{CS}}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{\text{CS}}$ setup time has elapsed.

Figure 17. Microprocessor Interface Timing (Normal Sample Mode, $\overline{\text{INV CLK}} = \text{Low}$)

TLV1544C, TLV1544I, TLV1548C, TLV1548I LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

PARAMETER MEASUREMENT INFORMATION



NOTE A: To minimize errors caused by noise at $\overline{\text{CS}}$, the internal circuitry waits for a setup time after $\overline{\text{CS}} \downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum CS setup time elapses.

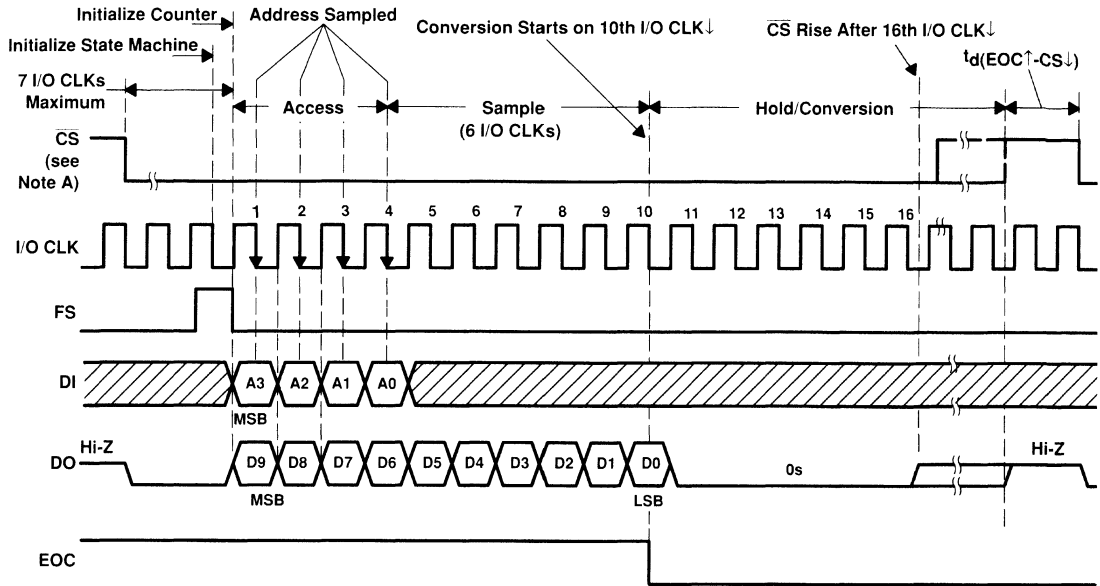
Figure 18. DSP Interface Timing (16-Clock Transfer, Normal Sample Mode, $\overline{\text{INV CLK}} = \text{High}$)



TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

PARAMETER MEASUREMENT INFORMATION



NOTE A: To minimize errors caused by noise at $\overline{\text{CS}}$, the internal circuitry waits for a setup time after $\overline{\text{CS}}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{\text{CS}}$ setup time elapses.

Figure 19. DSP Interface Timing (16-Clock Transfer, Normal Sample Mode, $\overline{\text{INV CLK}} = \text{Low}$)



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TLV1544C, TLV1544I, TLV1548C, TLV1548I
 LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
 WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

TYPICAL CHARACTERISTICS

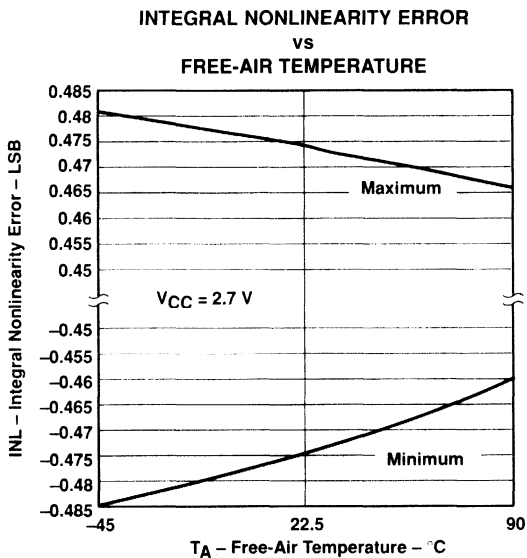


Figure 20

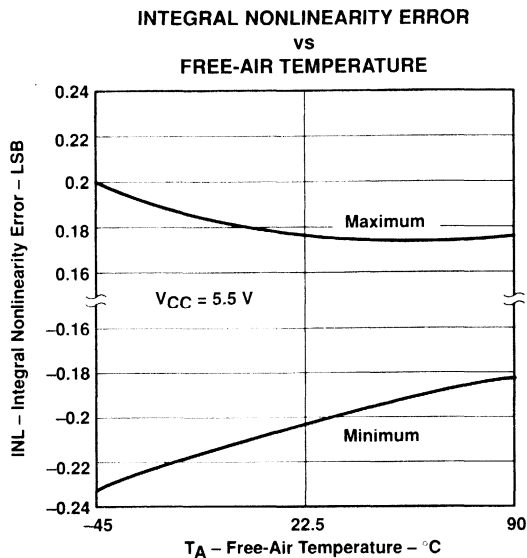


Figure 21

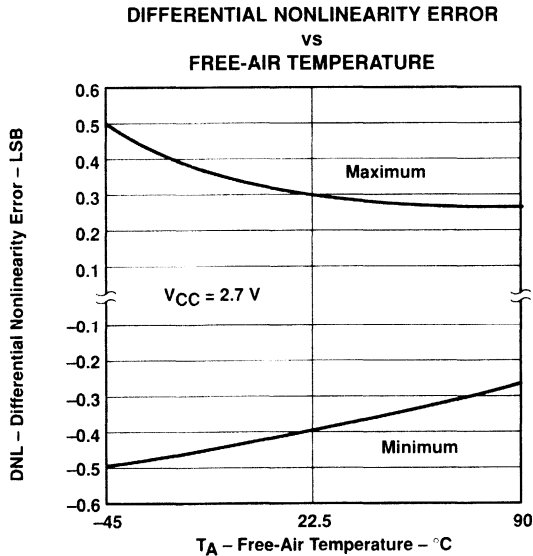


Figure 22

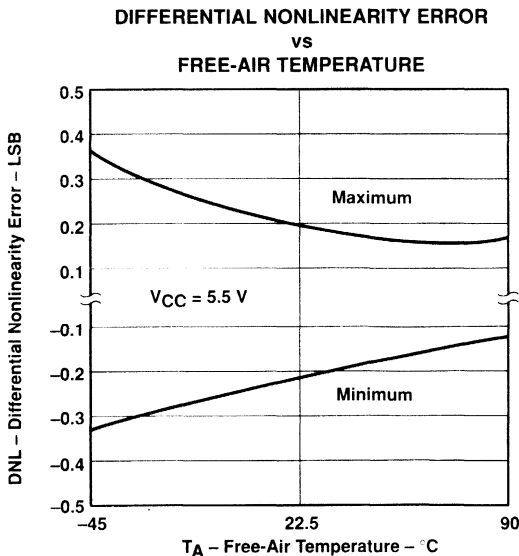


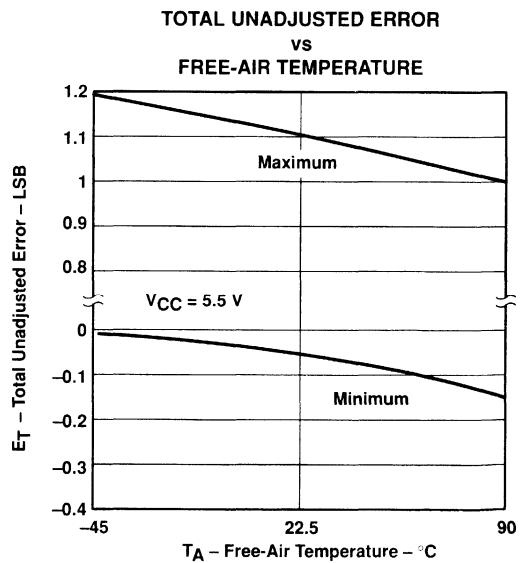
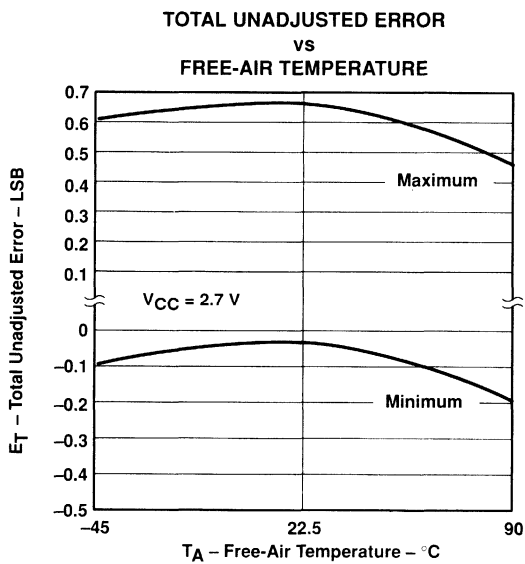
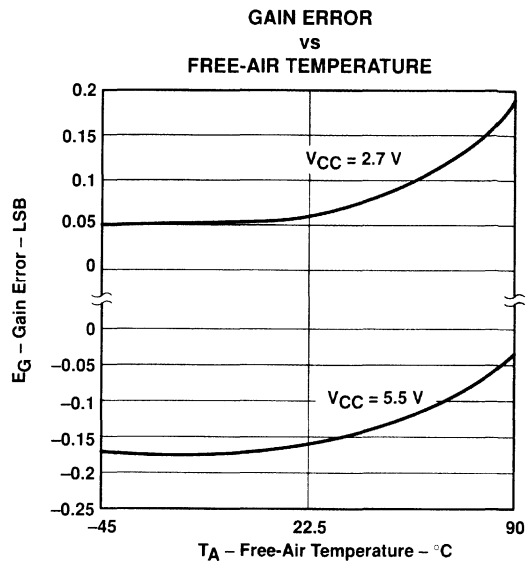
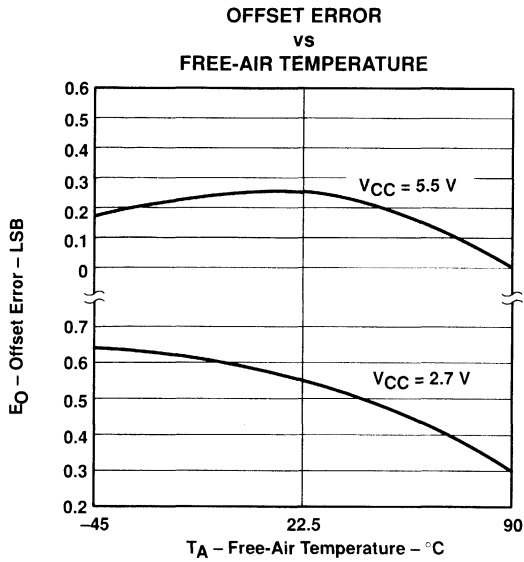
Figure 23



TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

TYPICAL CHARACTERISTICS



TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS
SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

TYPICAL CHARACTERISTICS

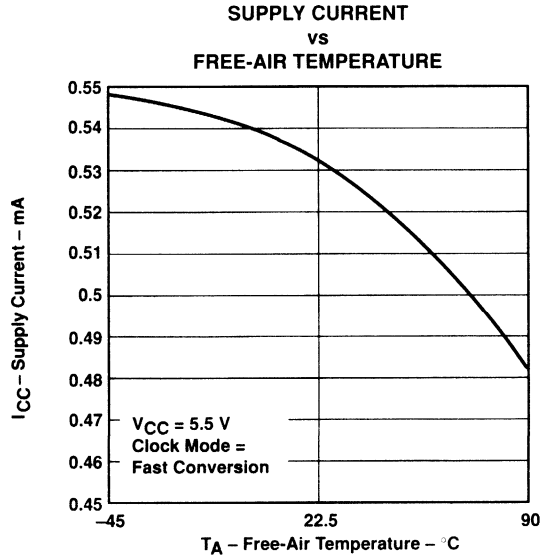


Figure 28

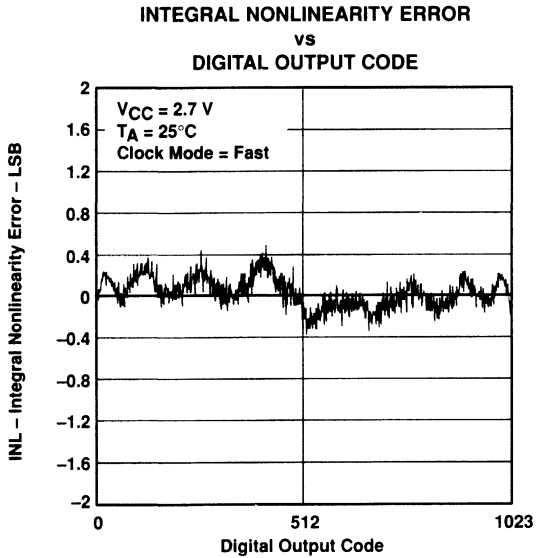


Figure 29

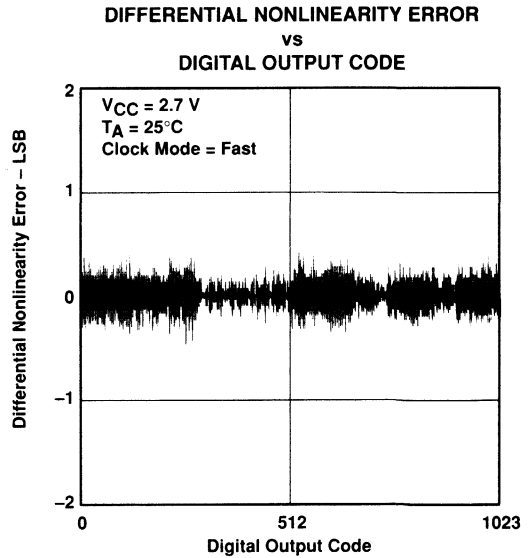
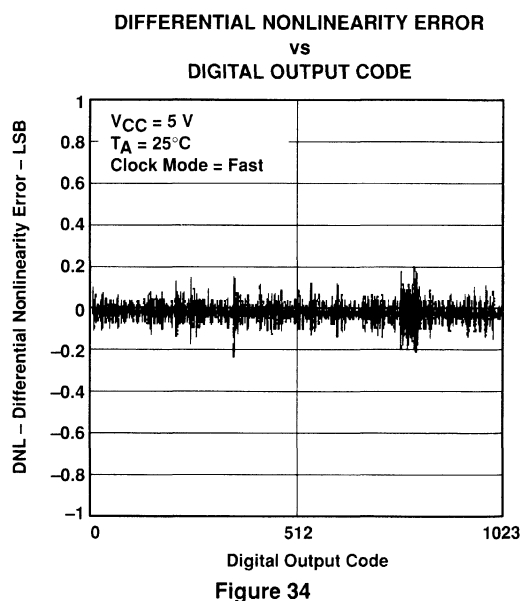
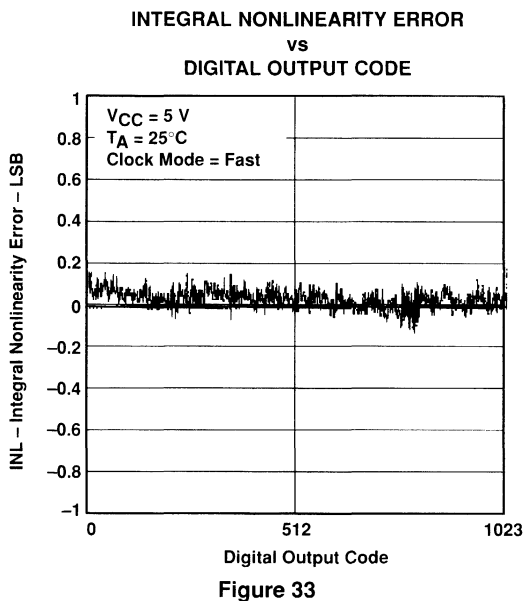
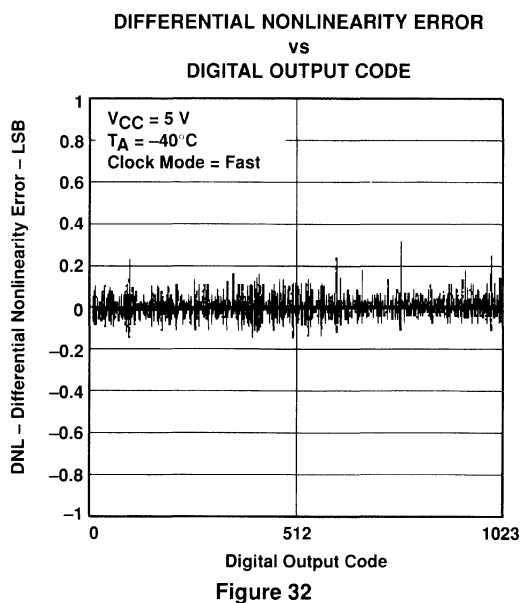
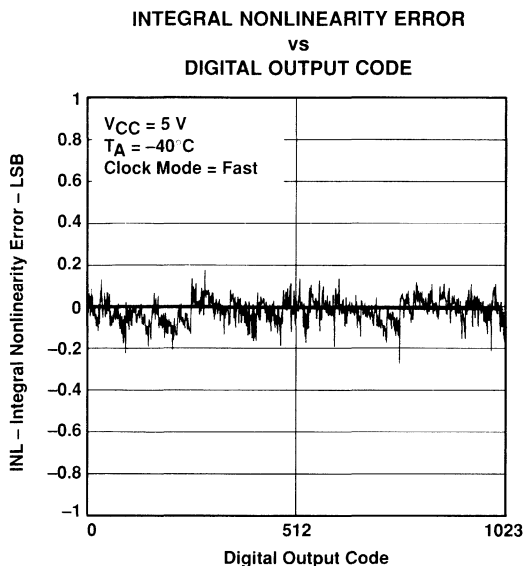


Figure 30

TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

TYPICAL CHARACTERISTICS



TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS
SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY ERROR
vs
DIGITAL OUTPUT CODE

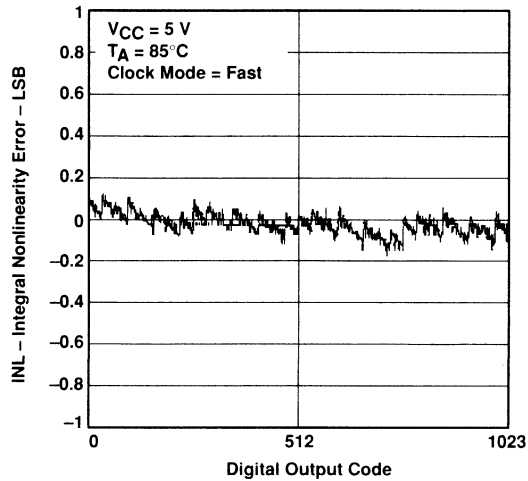


Figure 35

DIFFERENTIAL NONLINEARITY ERROR
vs
DIGITAL OUTPUT CODE

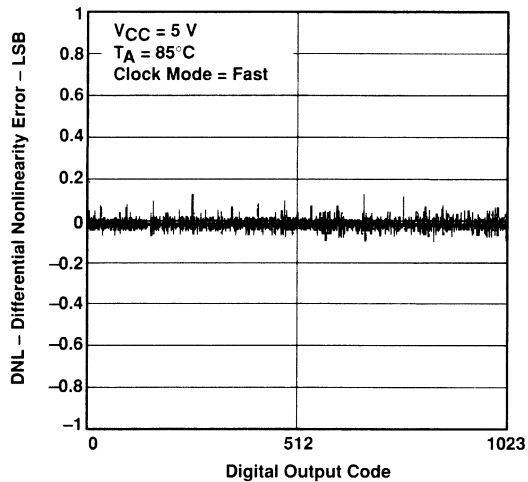


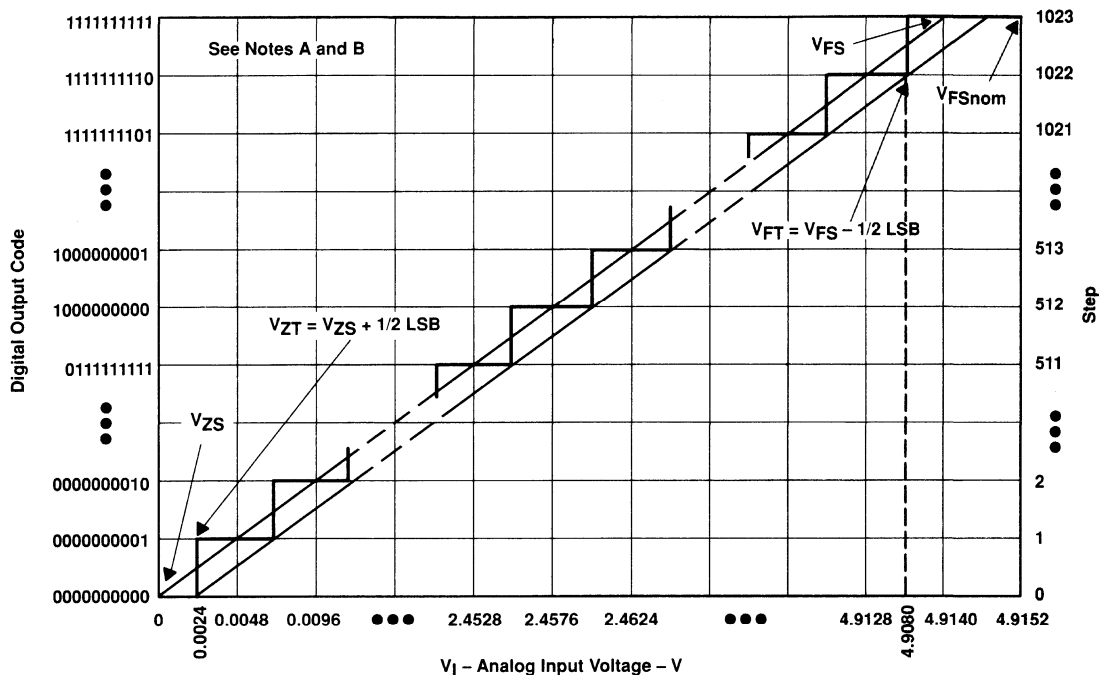
Figure 36



TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

APPLICATION INFORMATION



- NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0024 V, and the transition to full scale (V_{FT}) is 4.908 V. 1 LSB = 4.8 mV.
 B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 37. Ideal Conversion Characteristics

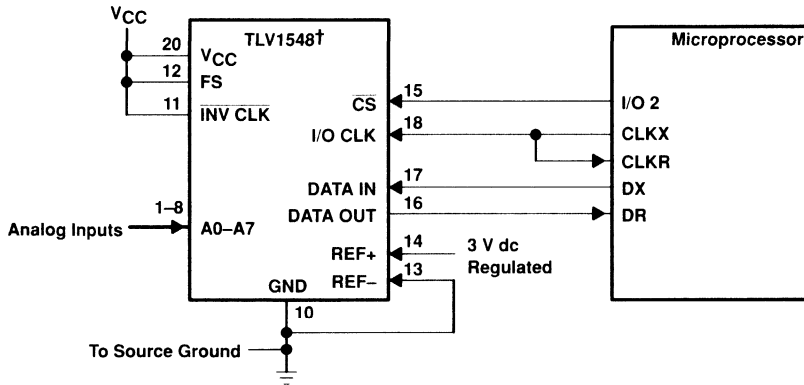


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TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

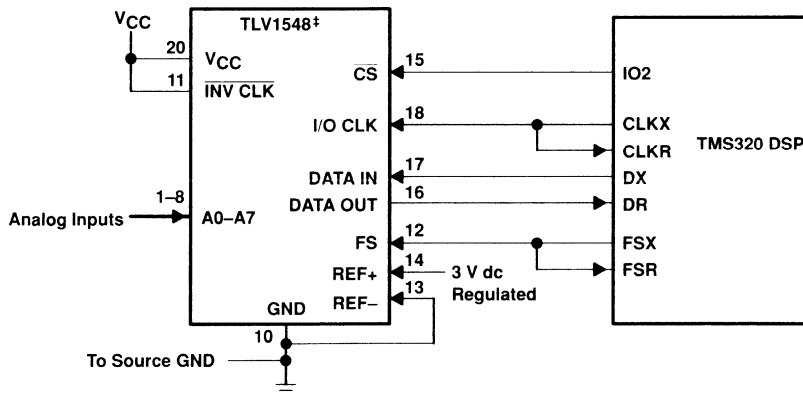
SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

APPLICATION INFORMATION



† DB package is shown for TLV1548

Figure 38. Typical Interface to a Microprocessor



‡ DB package is shown for TLV1548

Figure 39. Typical Interface to a TMS320 DSP

TLV1544C, TLV1544I, TLV1548C, TLV1548I
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

APPLICATIONS INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 33, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by:

$$V_C = V_S \left(1 - e^{-t_c / R_t C_i} \right)$$

where

$$R_t = R_s + r_i$$

t_c = Cycle time

(1)

The input impedance Z_i is 1 k Ω at 5 V, and is higher (~ 5 k Ω) at 2.7 V. The final voltage to 1/2 LSB is given by:

$$V_C (1/2 \text{ LSB}) = V_S - (V_S/2048)$$

(2)

Equating equation 1 to equation 2 and solving for cycle time t_c gives:

$$V_S - (V_S/2048) = V_S \left(1 - e^{-t_c / R_t C_i} \right)$$

(3)

and time to change to 1/2 LSB (minimum sampling time) is:

$$t_{ch} (1/2 \text{ LSB}) = R_t \times C_i \times \ln(2048)$$

where

$$\ln(2048) = 7.625$$

Therefore, with the values given, the time for the analog input signal to settle is:

$$t_{ch} (1/2 \text{ LSB}) = (R_s + 1 \text{ k}\Omega) \times 55 \text{ pF} \times \ln(2048)$$

(4)

This time must be less than the converter sample time shown in the timing diagrams. Which is 6x I/O CLK.

$$t_{ch} (1/2 \text{ LSB}) \leq 6 \times 1/f_{I/O}$$

(5)

Therefore the maximum I/O CLK frequency is:

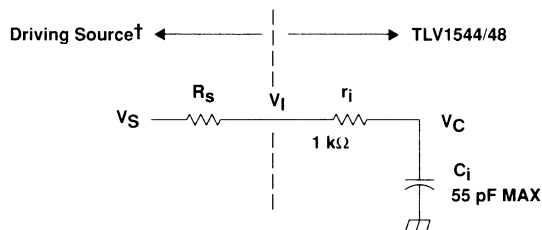
$$\max(f_{I/O}) = 6/t_{ch} (1/2 \text{ LSB}) = 6/(\ln(2048) \times R_t \times C_i)$$

(6)

TLV1544C, TLV1544I, TLV1548C, TLV1548I LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 4/8 ANALOG INPUTS

SLAS139B – DECEMBER 1996 – REVISED DECEMBER 1997

APPLICATIONS INFORMATION



V_I = Input Voltage at AIN
V_S = External Driving Source Voltage
R_S = Source Resistance
r_i = Input Resistance (MUX on Resistance)
C_i = Input Capacitance
V_C = Capacitance Charging Voltage

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 40. Equivalent Input Circuit Including the Driving Source

maximum conversion throughput

For a supply voltage at 5 V, if the source impedance is less than 1 kΩ, this equates to a minimum sampling time $t_{ch}(0.5 \text{ LSB})$ of 0.84 μs. Since the sampling time requires six I/O clocks, the fastest I/O clock frequency is $6/t_{ch} = 7.18 \text{ MHz}$. The minimal total cycle time is given as:

$$\begin{aligned}
 t_c &= t_{\text{address}} + t_{\text{sample}} + t_{\text{conv}} + t_d(\text{EOC}\uparrow - \text{CS}\downarrow) \\
 &= 0.56 \mu\text{s} + 0.84 \mu\text{s} + 10 \mu\text{s} + 0.1 \mu\text{s} \\
 &= 11.5 \mu\text{s}
 \end{aligned}$$

A maximum throughput of 87 KSPS. The throughput can be even higher with a smaller source impedance.

When source impedance is 100Ω, the minimum sampling time is 0.46 μs. The maximum I/O clock frequency possible is almost 13 MHz. Then 10 MHz clock (maximum I/O CLK for TLV1544/1548) can be used. The minimal total cycle time is:

$$\begin{aligned}
 t_c &= t_{\text{address}} + t_{\text{sample}} + t_{\text{conv}} + t_d(\text{EOC}\uparrow - \text{CS}\downarrow) \\
 &= 4 \times 1/f + 0.46 \mu\text{s} + 10 \mu\text{s} + 0.1 \mu\text{s} \\
 &= 0.4 \mu\text{s} + 0.46 \mu\text{s} + 10 \mu\text{s} + 0.1 \mu\text{s} \\
 &= 10.96 \mu\text{s}
 \end{aligned}$$

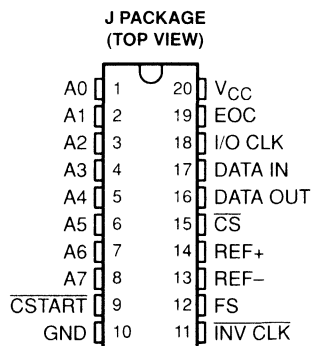
The maximum throughput is $1/10.96 \mu\text{s} = 91 \text{ KSPS}$ for this case.

TLV1548M

LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTER WITH SERIAL CONTROL AND 8 ANALOG INPUTS

SGLS104 – DECEMBER 1997

- Conversion Time $\leq 10 \mu\text{s}$
- 10-Bit-Resolution ADC
- Programmable Power-Down Mode . . . 1 μA
- Wide Range Single-Supply Operation of 2.7 V dc to 5.5 V dc
- Analog Input Range of 0 V to V_{CC}
- Built-in Analog Multiplexer with 8 Analog Input Channels
- SMJ320xxx DSP and Microprocessor SPI and QSPI Compatible Serial Interfaces
- End-of-Conversion (EOC) Flag
- Inherent Sample-and-Hold Function
- Built-In Self-Test Modes
- Programmable Power and Conversion Rate
- Asynchronous Start of Conversion for Extended Sampling
- Hardware I/O Clock Phase Adjust Input



description

The TLV1548 is a CMOS 10-bit switched-capacitor successive-approximation (SAR) analog-to-digital (A/D) converter. Each device has a [chip select (\overline{CS}), input-output clock (I/O CLK), data input (DATA IN) and serial data output (DATA OUT) that provide a direct 4-wire synchronous serial peripheral interface (SPI™, QSPI™) port of a host microprocessor. When interfacing with a SMJ320 DSP, an additional frame sync signal (FS) indicates the start of a serial data frame. The devices allow high-speed data transfers from the host. The INV CLK input provides further timing flexibility for the serial interface.

In addition to a high-speed converter and versatile control capability, the device has an on-chip 11-channel multiplexer that can select any one of eight analog inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic except for the extended sampling cycle where the sampling cycle is started by the falling edge of asynchronous CSTART. At the end of the A/D conversion, the end-of-conversion (EOC) output goes high to indicate that the conversion is complete. The TLV1548 is designed to operate with a wide range of supply voltages with very low power consumption. The power saving feature is further enhanced with a software-programmed power-down mode and conversion rate. The converter incorporated in the device features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating temperature range.

The TLV1548 has eight analog input channels. The TLV1548M will be characterized for operation over the full military temperature range of -55°C to 125°C . The target release timeframe for the TLV1548M is estimated to be during the first half of 1998.

SPI and QSPI are registered trademarks of Motorola, Inc.

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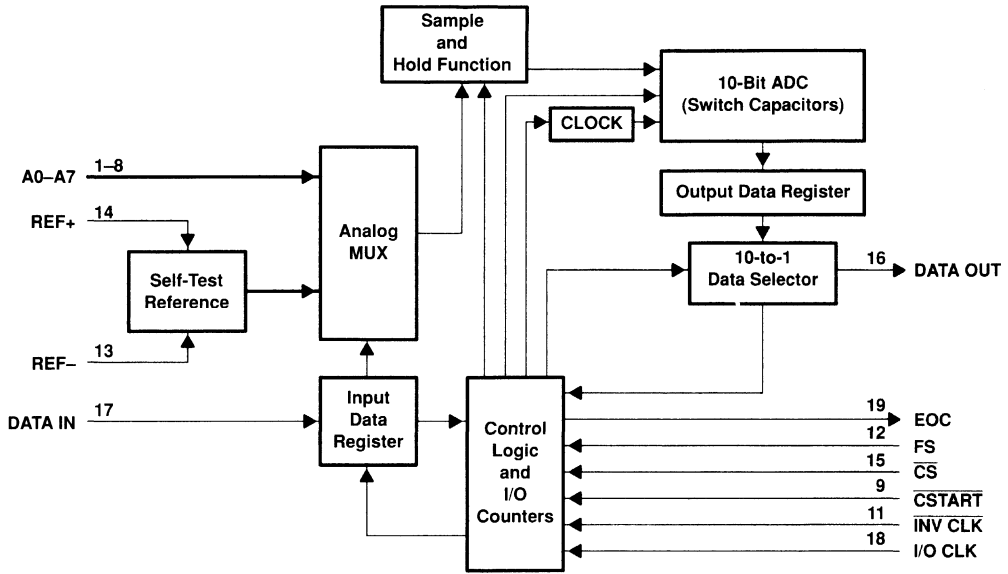
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TLV1548M
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTER
WITH SERIAL CONTROL AND 8 ANALOG INPUTS

SGLS104 – DECEMBER 1997

functional block diagram



Terminals shown are for the J package.

AVAILABLE OPTIONS

T _A	PACKAGES	
	(J)	(FK)
-55°C to 125°C	TLV1548MJB	TLV1548MFKB

PRODUCT PREVIEW



TLV1548M
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTER
WITH SERIAL CONTROL AND 8 ANALOG INPUTS

SGLS104 – DECEMBER 1997

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
A0–A3 A4–A7	1–4 5–8	I	Analog inputs. The analog inputs are internally multiplexed. (For a source impedance greater than 1 k Ω , the asynchronous start should be used to increase the sampling time.)
\overline{CS}	15	I	Chip select. A high-to-low transition on \overline{CS} resets the internal counters and controls and enables DATA IN, DATA OUT, and I/O CLK within the maximum setup time. A low-to-high transition disables DATA IN, DATA OUT, and I/O CLK within the setup time.
CSTART	9	I	Sampling/conversion start control. CSTART controls the start of the sampling of an analog input from a selected multiplex channel. A high-to-low transition starts the sampling of the analog input signal. A low-to-high transition puts the sample-and-hold function in hold mode and starts the conversion. CSTART is independent from I/O CLK and works when \overline{CS} is high. The low CSTART duration controls the duration of the sampling cycle for the switched capacitor array. CSTART is tied to V _{CC} if not used.
DATA IN	17	I	Serial data input. The 4-bit serial data selects the desired analog input and test voltage to be converted next in a normal cycle. These bits can also set the conversion rate and enable the power-down mode. When operating in the microprocessor mode, the input data is presented MSB first and is shifted in on the first four rising ($\overline{INV CLK} = V_{CC}$) or falling ($\overline{INV CLK} = GND$) edges of I/O CLK (after $\overline{CS}\downarrow$). When operating in the DSP mode, the input data is presented MSB first and is shifted in on the first four falling ($\overline{INV CLK} = V_{CC}$) or rising ($\overline{INV CLK} = GND$) edges of I/O CLK (after FS \downarrow). After the four input data bits have been read into the input data register, DATA IN is ignored for the remainder of the current conversion period.
DATA OUT	16	O	Three-state serial output of the A/D conversion result. DATA OUT is in the high-impedance state when \overline{CS} is high and active when \overline{CS} is low. With a valid CS signal, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB or LSB value of the previous conversion result. DATA OUT changes on the falling (microprocessor mode) or rising (DSP mode) edge of I/O CLK.
EOC	19	O	End of conversion. EOC goes from a high to a low logic level on the tenth rising (microprocessor mode) or tenth falling (DSP mode) edge of I/O CLK and remains low until the conversion is complete and data is ready for transfer. EOC can also indicate that the converter is busy.
FS	12	I	DSP frame synchronization input. FS indicates the start of a serial data frame into or out of the device. FS is tied to V _{CC} when interfacing the device with a microprocessor.
GND	10		Ground return for internal circuitry. All voltage measurements are with respect to GND, unless otherwise noted.
$\overline{INV CLK}$	11	I	Inverted clock input. $\overline{INV CLK}$ is tied to GND when an inverted I/O CLK is used as the source of the input clock. This affects both microprocessor and DSP interfaces. $\overline{INV CLK}$ is tied to V _{CC} if I/O CLK is not inverted. $\overline{INV CLK}$ can also invoke a built-in test mode.

PRODUCT PREVIEW



TLV1548M
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTER
WITH SERIAL CONTROL AND 8 ANALOG INPUTS
 SGLS104 – DECEMBER 1997

Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
I/O CLK	18	I	<p>Input/output clock. I/O CLK receives the serial I/O clock input in the two modes and performs the following four functions in each mode:</p> <p>Microprocessor mode</p> <ul style="list-style-type: none"> When $\overline{\text{INVCLK}} = V_{\text{CC}}$, I/O CLK clocks the four input data bits into the input data register on the first four rising edges of I/O CLK after $\overline{\text{CS}}\downarrow$ with the multiplexer address available after the fourth rising edges. When $\overline{\text{INV CLK}} = \text{GND}$, input data bits are clocked in on the first four falling edges instead. On the fourth falling edge of I/O CLK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth rising edge of I/O CLK except in the extended sampling cycle where the duration of $\overline{\text{CSTART}}$ determines when to end the sampling cycle. Output data bits change on the first ten falling I/O clock edges regardless of the condition of $\overline{\text{INV CLK}}$. I/O CLK transfers control of the conversion to the internal state machine on the tenth rising edge of I/O CLK regardless of the condition of $\overline{\text{INV CLK}}$. <p>Digital signal processor (DSP) mode</p> <ul style="list-style-type: none"> When $\overline{\text{INV CLK}} = V_{\text{CC}}$, I/O CLK clocks the four input data bits into the input data register on the first four falling edges of I/O CLK after $\overline{\text{FS}}\downarrow$ with the multiplexer address available after the fourth falling edges. When $\overline{\text{INV CLK}} = \text{GND}$, input data bits are clocked in on the first four rising edges instead. On the fourth rising edge of I/O CLK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLK except in the extended sampling cycle where the duration of $\overline{\text{CSTART}}$ determines when to end the sampling cycle. Output data bits change on the first ten rising I/O CLK edges regardless of the condition of $\overline{\text{INV CLK}}$. I/O CLK transfers control of the conversion to the internal state machine on the tenth falling edge of I/O CLK regardless of the condition of $\overline{\text{INV CLK}}$.
REF+	14	I	Upper reference voltage (nominally V_{CC}). The maximum input voltage range is determined by the difference between the voltages applied to REF+ and REF-.
REF-	13	I	Lower reference voltage (nominally ground)
V _{CC}	20	I	Positive supply voltage

PRODUCT PREVIEW



TLV1548M
LOW-VOLTAGE 10-BIT ANALOG-TO-DIGITAL CONVERTER
WITH SERIAL CONTROL AND 8 ANALOG INPUTS

SGLS104 – DECEMBER 1997

APPLICATION INFORMATION

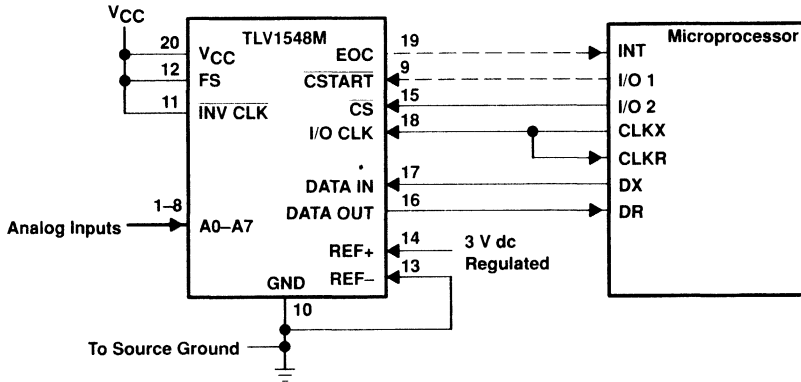


Figure 1. Typical Interface to a Microprocessor

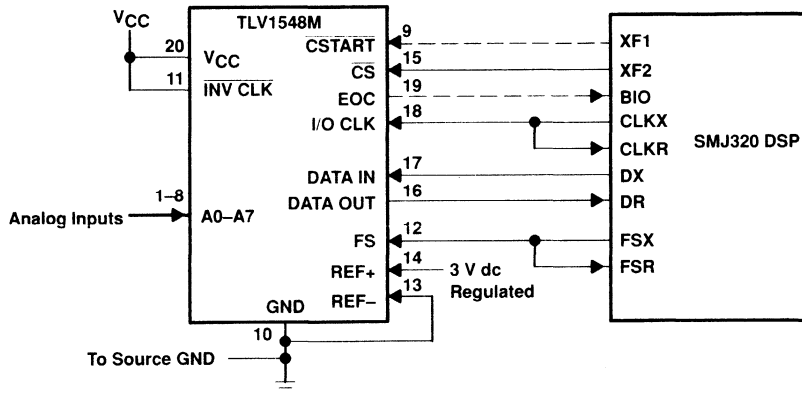


Figure 2. Typical Interface to a SMJ320 DSP

PRODUCT PREVIEW

TLV1549C, TLV1549I, TLV1549M 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS071C – JANUARY 1993 – REVISED MARCH 1995

- 3.3-V Supply Operation
- 10-Bit-Resolution Analog-to-Digital Converter (ADC)
- Inherent Sample and Hold Function
- Total Unadjusted Error . . . ± 1 LSB Max
- On-Chip System Clock
- Terminal Compatible With TLC1549 and TLC1549x
- Application Report Available†
- CMOS Technology

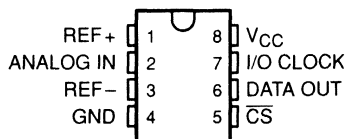
description

The TLV1549C, TLV1549I, and TLV1549M are 10-bit, switched-capacitor, successive-approximation, analog-to-digital converters. The devices have two digital inputs and a 3-state output [chip select (\overline{CS}), input-output clock (I/O CLOCK), and data output (DATA OUT)] that provide a three-wire interface to the serial port of a host processor.

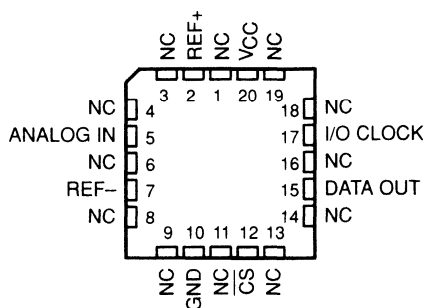
The sample-and-hold function is automatic. The converter incorporated in the device features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

The TLV1549C is characterized for operation from 0°C to 70°C. The TLV1549I is characterized for operation from -40°C to 85°C. The TLV1549M is characterized for operation over the full military temperature range of -55°C to 125°C.

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

AVAILABLE OPTIONS

T _A	PACKAGE			
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	TLV1549CD	—	—	TLV1549CP
-40°C to 85°C	TLV1549ID	—	—	TLV1549IP
-55°C to 125°C	—	TLV1549MFK	TLV1549MJG	—

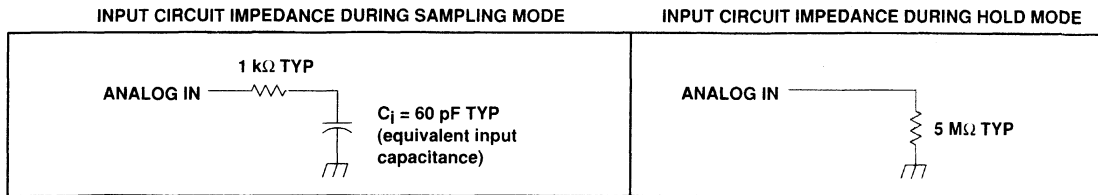
† Interfacing the TLV1549 10-Bit Serial-Out ADC to Popular 3.3-V Microcontrollers (SLAA005)

TLV1549C, TLV1549I, TLV1549M

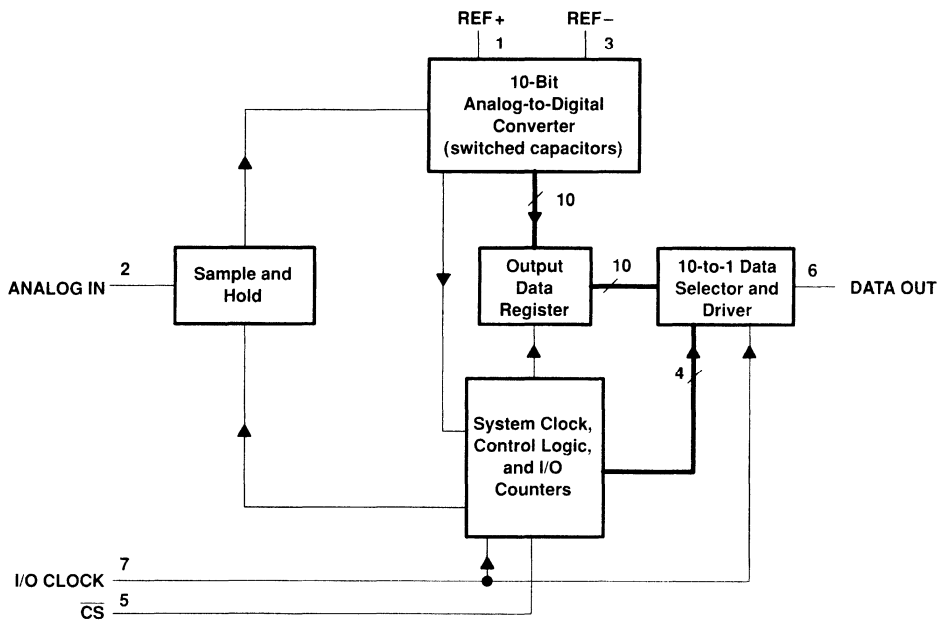
10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS071C - JANUARY 1993 - REVISED MARCH 1995

typical equivalent inputs



functional block diagram



Terminal numbers shown are for the D, JG, and P packages only.

TLV1549C, TLV1549I, TLV1549M
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

SLAS071C – JANUARY 1993 – REVISED MARCH 1995

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ANALOG IN	2	I	Analog input. The driving source impedance should be $\leq 1\text{ k}\Omega$. The external driving source to ANALOG IN should have a current capability $\geq 10\text{ mA}$.
$\overline{\text{CS}}$	5	I	Chip select. A high-to-low transition on $\overline{\text{CS}}$ resets the internal counters and controls and enables DATA OUT and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OUT	6	O	This 3-state serial output for the A/D conversion result is in the high-impedance state when $\overline{\text{CS}}$ is high and active when $\overline{\text{CS}}$ is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next most significant bit, and the remaining bits are shifted out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs.
GND	4	I	The ground return for internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	7	I	The input/output clock receives the serial I/O CLOCK input and performs the following three functions: 1) On the third falling edge of I/O CLOCK, the analog input voltage begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 2) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 3) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF +	1	I	The upper reference voltage value (nominally V_{CC}) is applied to REF +. The maximum input voltage range is determined by the difference between the voltage applied to REF + and the voltage applied to REF –.
REF –	3	I	The lower reference voltage value (nominally ground) is applied to this REF –.
VCC	8	I	Positive supply voltage

detailed description

With chip select ($\overline{\text{CS}}$) inactive (high), the I/O CLOCK input is initially disabled and DATA OUT is in the high-impedance state. When the serial interface takes $\overline{\text{CS}}$ active (low), the conversion sequence begins with the enabling of I/O CLOCK and the removal of DATA OUT from the high-impedance state. The serial interface then provides the I/O CLOCK sequence to I/O CLOCK and receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host serial interface. The first ten I/O clocks provide the control timing for sampling the analog input.

There are six basic serial interface timing modes that can be used with the TLV1549. These modes are determined by the speed of I/O CLOCK and the operation of $\overline{\text{CS}}$ as shown in Table 1. These modes are: (1) a fast mode with a 10-clock transfer and $\overline{\text{CS}}$ inactive (high) between transfers, (2) a fast mode with a 10-clock transfer and $\overline{\text{CS}}$ active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and $\overline{\text{CS}}$ inactive (high) between transfers, (4) a fast mode with a 16-bit transfer and $\overline{\text{CS}}$ active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and $\overline{\text{CS}}$ inactive (high) between transfers, and (6) a slow mode with a 16-clock transfer and $\overline{\text{CS}}$ active (low) continuously.

The MSB of the previous conversion appears on DATA OUT on the falling edge of $\overline{\text{CS}}$ in mode 1, mode 3, and mode 5, within 21 μs from the falling edge of the tenth I/O CLOCK in mode 2 and mode 4, and following the 16th clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of the I/O CLOCK. Ten bits of data are transmitted to the host serial interface through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the tenth clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLOCK transfer is more than ten clocks long.

Table 1 lists the operational modes with respect to the state of $\overline{\text{CS}}$, the number of I/O serial transfer clocks that can be used, and the timing on which the MSB of the previous conversion appears at the output.



TLV1549C, TLV1549I, TLV1549M
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

SLAS071C – JANUARY 1993 – REVISED MARCH 1995

Table 1. Mode Operation

MODES		\overline{CS}	NO. OF I/O CLOCKS	MSB AT DATA OUT†	TIMING DIAGRAM
Fast Modes	Mode 1	High between conversion cycles	10	\overline{CS} falling edge	Figure 6
	Mode 2	Low continuously	10	Within 21 μ s	Figure 7
	Mode 3	High between conversion cycles	11 to 16‡	\overline{CS} falling edge	Figure 8
	Mode 4	Low continuously	16‡	Within 21 μ s	Figure 9
Slow Modes	Mode 5	High between conversion cycles	11 to 16‡	\overline{CS} falling edge	Figure 10
	Mode 6	Low continuously	16‡	16th clock falling edge	Figure 11

† This timing also initiates serial-interface communication.

‡ No more than 16 clocks should be used.

All the modes require a minimum period of 21 μ s after the falling edge of the tenth I/O CLOCK before a new transfer sequence can begin. During a serial I/O CLOCK data transfer, \overline{CS} must be active (low) so that the I/O CLOCK input is enabled. When \overline{CS} is toggled between data transfers (modes 1, 3, and 5), the transitions at \overline{CS} are recognized as valid only if the level is maintained for a minimum period of 1.425 μ s after the transition. If the transfer is more than ten I/O clocks (modes 3, 4, 5, and 6), the rising edge of the eleventh clock must occur within 9.5 μ s after the falling edge of the tenth I/O CLOCK; otherwise, the device could lose synchronization with the host serial interface and \overline{CS} has to be toggled to restore proper operation.

fast modes

The device is in a fast mode when the serial I/O CLOCK data transfer is completed within 21 μ s from the falling edge of the tenth I/O CLOCK. With a 10-clock serial transfer, the device can only run in a fast mode.

mode 1: fast mode, \overline{CS} inactive (high) between transfers, 10-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O-CLOCK transfers and each transfer is ten clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 2: fast mode, \overline{CS} active (low) continuously, 10-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O-CLOCK transfers and each transfer is ten clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions. Within 21 μ s after the falling edge of the tenth I/O CLOCK, the MSB of the previous conversion appears at DATA OUT.

mode 3: fast mode, \overline{CS} inactive (high) between transfers, 11- to 16-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O-CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 4: fast mode, \overline{CS} active (low) continuously, 16-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O-CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions. Within 21 μ s after the falling edge of the tenth I/O CLOCK, the MSB of the previous conversion appears at DATA OUT.

slow modes

In a slow mode, the serial I/O CLOCK data transfer is completed after 21 μ s from the falling edge of the tenth I/O CLOCK.



TLV1549C, TLV1549I, TLV1549M
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

SLAS071C – JANUARY 1993 – REVISED MARCH 1995

mode 5: slow mode, \overline{CS} inactive (high) between transfers, 11- to 16-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O-CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 6: slow mode, \overline{CS} active (low) continuously, 16-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O-CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions. The falling edge of the sixteenth I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16-clock transfer initiated by the serial interface.

analog input sampling

Sampling of the analog input starts on the falling edge of the third I/O CLOCK, and sampling continues for seven I/O CLOCK periods. The sample is held on the falling edge of the tenth I/O CLOCK.

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and this 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are determined.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.



TLV1549C, TLV1549I, TLV1549M

10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS071C – JANUARY 1993 – REVISED MARCH 1995

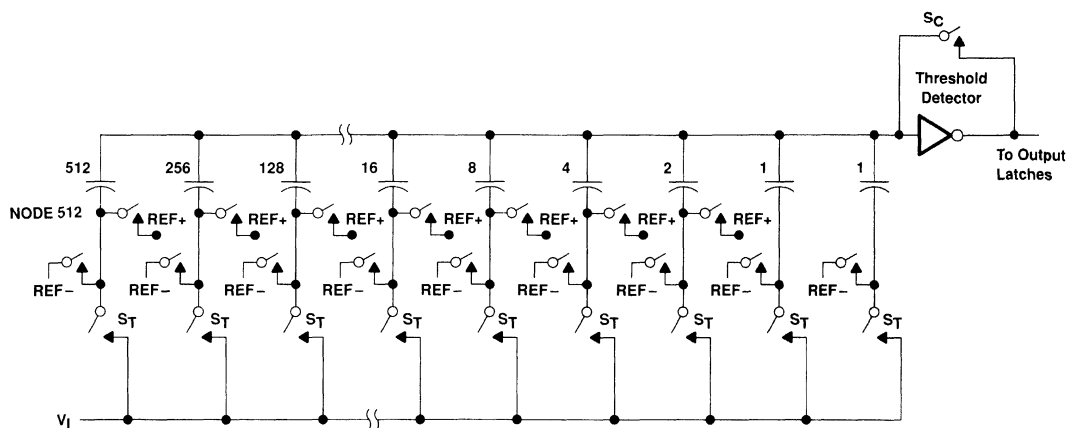


Figure 1. Simplified Model of the Successive-Approximation System

chip-select operation

The trailing edge of \overline{CS} starts all modes of operation, and \overline{CS} can abort a conversion sequence in any mode. A high-to-low transition on \overline{CS} within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Exercise care to prevent \overline{CS} from being taken low close to completion of conversion because the output data may be corrupted.

reference voltage inputs

There are two reference inputs used with the TLV1549: REF+ and REF-. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading, respectively. The values of REF+, REF-, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF-.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1):	TLV1549C	-0.5 V to 6.5 V
	TLV1549I	-0.5 V to 6.5 V
	TLV1549M	-0.5 V to 6 V
Input voltage range, V_I (any input)		-0.3 V to $V_{CC} + 0.3$ V
Output voltage range, V_O		-0.3 V to $V_{CC} + 0.3$ V
Positive reference voltage, V_{ref+}		$V_{CC} + 0.1$ V
Negative reference voltage, V_{ref-}		-0.1 V
Peak input current (any input)		± 20 mA
Peak total input current (all inputs)		± 30 mA
Operating free-air temperature range, T_A :	TLV1549C	0°C to 70°C
	TLV1549I	-40°C to 85°C
	TLV1549M	-55°C to 125°C
Storage temperature range, T_{stg}		-65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from the case for 10 seconds		260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to ground with REF- and GND wired together (unless otherwise noted).



TLV1549C, TLV1549I, TLV1549M 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS071C – JANUARY 1993 – REVISED MARCH 1995

recommended operating conditions

	MIN	NOM	MAX	UNIT	
Supply voltage, V_{CC}	3	3.3	3.6	V	
Positive reference voltage, V_{ref+} (see Note 2)	V_{CC}			V	
Negative reference voltage, V_{ref-} (see Note 2)	0			V	
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)	2.5	V_{CC}	$V_{CC} + 0.2$	V	
Analog input voltage (see Note 2)	0			V_{CC}	
High-level control input voltage, V_{IH}	$V_{CC} = 3\text{ V to }3.6\text{ V}$			V	
Low-level control input voltage, V_{IL}	$V_{CC} = 3\text{ V to }3.6\text{ V}$			V	
Clock frequency at I/O CLOCK (see Note 3)	0		2.1	MHz	
Setup time, \overline{CS} low before first I/O CLOCK \uparrow , $t_{SU}(CS)$ (see Note 4)	1.425			μs	
Hold time, \overline{CS} low after last I/O CLOCK \downarrow , $t_H(CS)$	0			ns	
Pulse duration, I/O CLOCK high, $t_{WH}(I/O)$	190			ns	
Pulse duration, I/O CLOCK low, $t_{WL}(I/O)$	190			ns	
Transition time, I/O CLOCK, $t_f(I/O)$ (see Note 5 and Figure 5)				1	
Transition time, \overline{CS} , $t_f(CS)$				10	
Operating free-air temperature, T_A	TLV1549C		0	70	$^{\circ}\text{C}$
	TLV1549I		-40	85	$^{\circ}\text{C}$
	TLV1549M		-55	125	$^{\circ}\text{C}$

- NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000). The TLV1549 is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.
3. For 11- to 16-bit transfers, after the tenth I/O CLOCK falling edge ($\leq 2\text{ V}$), at least one I/O CLOCK rising edge ($\geq 2\text{ V}$) must occur within 9.5 μs .
4. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to the I/O CLOCK. Therefore, no attempt should be made to clock out the data until the minimum \overline{CS} setup time has elapsed.
5. This is the time required for the clock input signal to fall from V_{IHmin} to V_{ILmax} or to rise from V_{ILmax} to V_{IHmin} . In the vicinity of normal room temperature, the device functions with input clock transition time as slow as 1 μs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.



TLV1549C, TLV1549I, TLV1549M
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

SLAS071C – JANUARY 1993 – REVISED MARCH 1995

electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 3\text{ V to }3.6\text{ V}$, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
V _{OH}	High-level output voltage	V _{CC} = 3 V, I _{OH} = -1.6 mA	2.4			V	
		V _{CC} = 3 V to 3.6 V, I _{OH} = -20 μA	V _{CC} - 0.1				
V _{OL}	Low-level output voltage	V _{CC} = 3 V, I _{OL} = 1.6 mA			0.4	V	
		V _{CC} = 3 V to 3.6 V, I _{OL} = 20 μA			0.1		
I _{OZ}	Off-state (high-impedance-state) output current	V _O = V _{CC} , \overline{CS} at V _{CC}			10	μA	
		V _O = 0, \overline{CS} at V _{CC}			-10		
I _{IH}	High-level input current	V _I = V _{CC}		0.005	2.5	μA	
I _{IL}	Low-level input current	V _I = 0		-0.005	-2.5	μA	
I _{CC}	Operating supply current	\overline{CS} at 0 V		0.4	2.5	mA	
Analog input leakage current		V _I = V _{CC}			1	μA	
		V _I = 0			-1		
Maximum static analog reference current into REF+		V _{ref+} = V _{CC} , V _{ref-} = GND			10	μA	
C _i	Input capacitance	TLV1549C, I (Analog)	During sample cycle		30	pF	
		TLV1549M, (Analog)	During sample cycle		30		
		TLV1549C, I (Control)			5		15
		TLV1549M, (Control)			5		

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



TLV1549C, TLV1549I, TLV1549M 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS071C – JANUARY 1993 – REVISED MARCH 1995

**operating characteristics over recommended operating free-air temperature range,
V_{CC} = V_{ref+} = 3 V to 3.6 V, I/O CLOCK frequency = 2.1 MHz**

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Linearity error (see Note 6)			±1	LSB
Zero error (see Note 7)	See Note 2		±1	LSB
Full-scale error (see Note 7)	See Note 2		±1	LSB
Total unadjusted error (see Note 8)			±1	LSB
t _{conv} Conversion time	See Figures 6–11		21	μs
t _c Total cycle time (access, sample, and conversion)	See Figures 6–11 and Note 9		21 + 10 I/O CLOCK periods	μs
t _v Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 5	10		ns
t _{d(I/O-DATA)} Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 5		240	ns
t _{PZH} , t _{PZL} Enable time, \overline{CS} ↓ to DATA OUT (MSB driven)	See Figure 3		1.3	μs
t _{PHZ} , t _{PLZ} Disable time, \overline{CS} ↑ to DATA OUT (high impedance)	See Figure 3		180	ns
t _{r(bus)} Rise time, data bus	See Figure 5		300	ns
t _{f(bus)} Fall time, data bus	See Figure 5		300	ns
t _{d(I/O-CS)} Delay time, 10th I/O CLOCK↓ to \overline{CS} ↓ to abort conversion (see Note 10)			9	μs

- NOTES: 2. Analog input voltages greater than that applied to REF + convert as all ones (1111111111), while input voltages less than that applied to REF – convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V (V_{ref+} – V_{ref-}); however, the electrical specifications are no longer applicable.
6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Zero error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
8. Total unadjusted error comprises linearity, zero, and full-scale errors.
9. I/O CLOCK period = 1/(I/O CLOCK frequency). Sampling begins on the falling edge of the third I/O CLOCK, continues for seven I/O CLOCK periods, and ends on the falling edge of the tenth I/O CLOCK (see Figure 5).
10. Any transitions of \overline{CS} are recognized as valid only if the level is maintained for a minimum of a setup time plus two falling edges of the internal clock (1.425 μs) after the transition.



TLV1549C, TLV1549I, TLV1549M
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

SLAS071C – JANUARY 1993 – REVISED MARCH 1995

PARAMETER MEASUREMENT INFORMATION

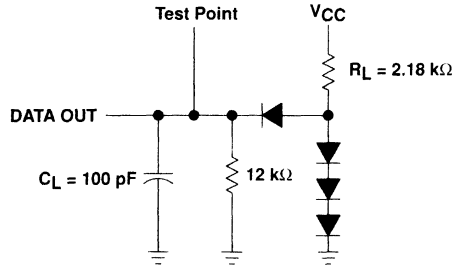


Figure 2. Load Circuit

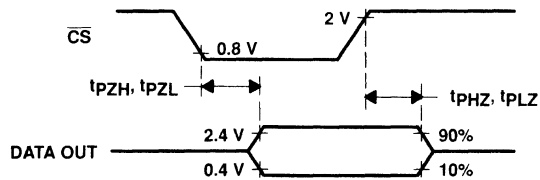


Figure 3. DATA OUT to Hi-Z Voltage Waveforms

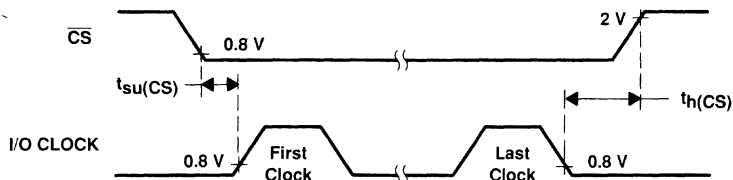


Figure 4. CS to I/O CLOCK Voltage Waveforms

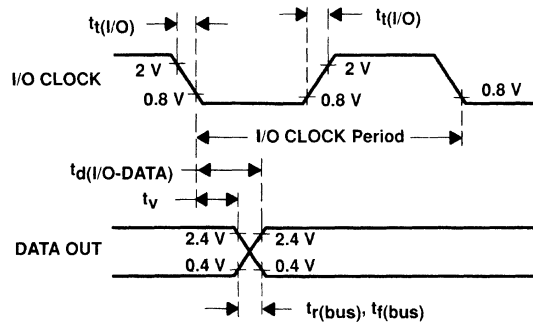


Figure 5. I/O CLOCK and DATA OUT Voltage Waveforms

TLV1549C, TLV1549I, TLV1549M
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

SLAS071C – JANUARY 1993 – REVISED MARCH 1995

PARAMETER MEASUREMENT INFORMATION

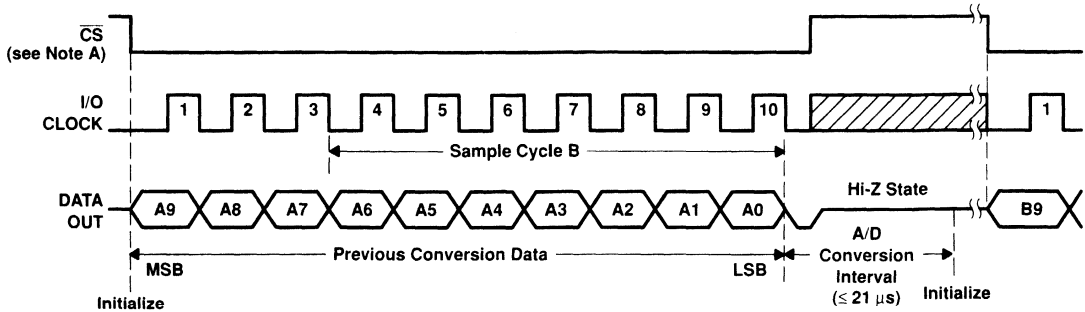


Figure 6. Timing for 10-Clock Transfer Using \overline{CS}

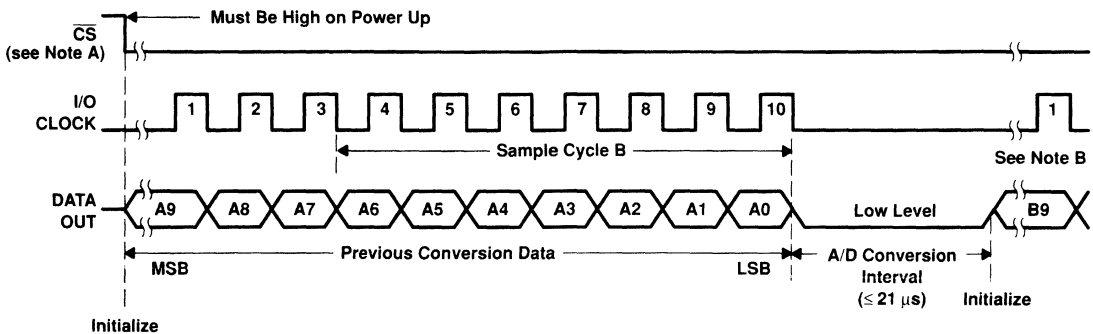


Figure 7. Timing for 10-Clock Transfer Not Using \overline{CS}

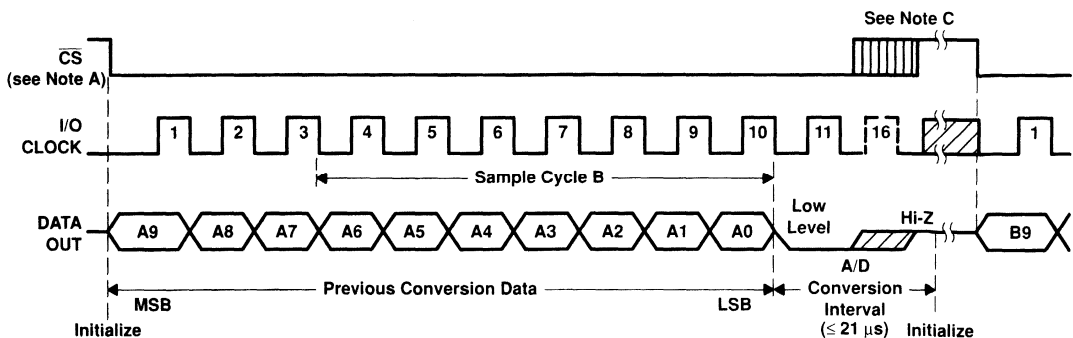


Figure 8. Timing for 11- to 16-Clock Transfer Using \overline{CS} (Serial Transfer Completed Within 21 μs)

- NOTES:
- A. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after \overline{CS} before responding to the I/O CLOCK. No attempt should be made to clock out the data until the minimum \overline{CS} setup time has elapsed.
 - B. A low-to-high transition of \overline{CS} disables I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.
 - C. The first I/O CLOCK must occur after the end of the previous conversion.

TLV1549C, TLV1549I, TLV1549M 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS071C – JANUARY 1993 – REVISED MARCH 1995

PARAMETER MEASUREMENT INFORMATION

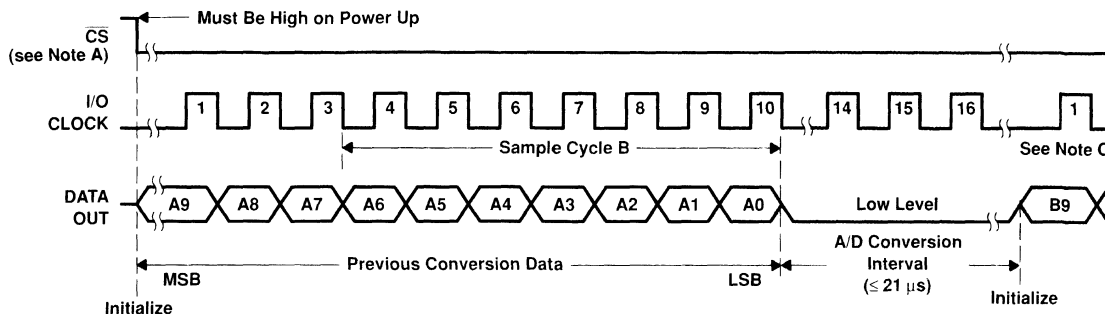


Figure 9. Timing for 16-Clock Transfer Not Using \overline{CS} (Serial Transfer Completed Within 21 μs)

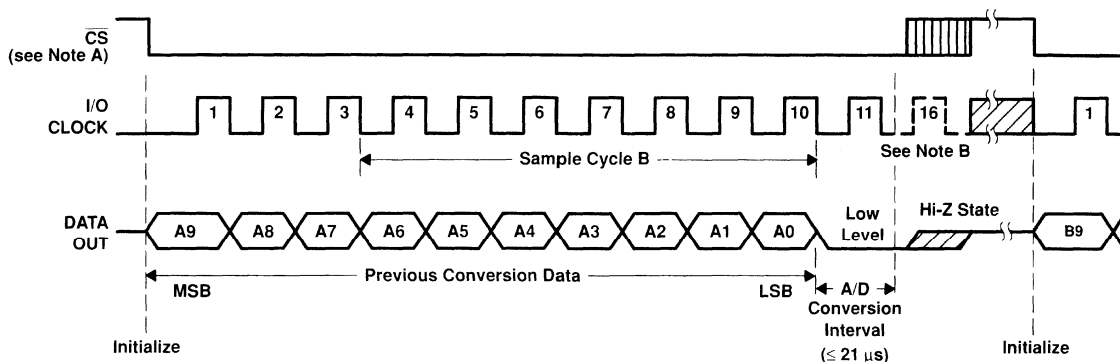


Figure 10. Timing for 11- to 16-Clock Transfer Using \overline{CS} (Serial Transfer Completed After 21 μs)

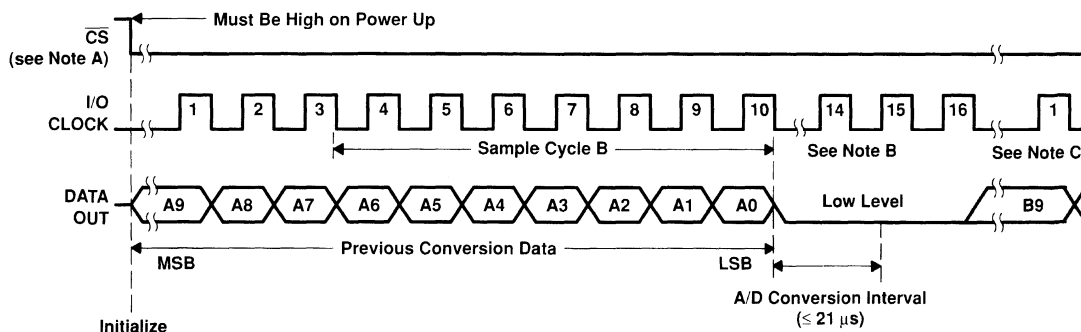


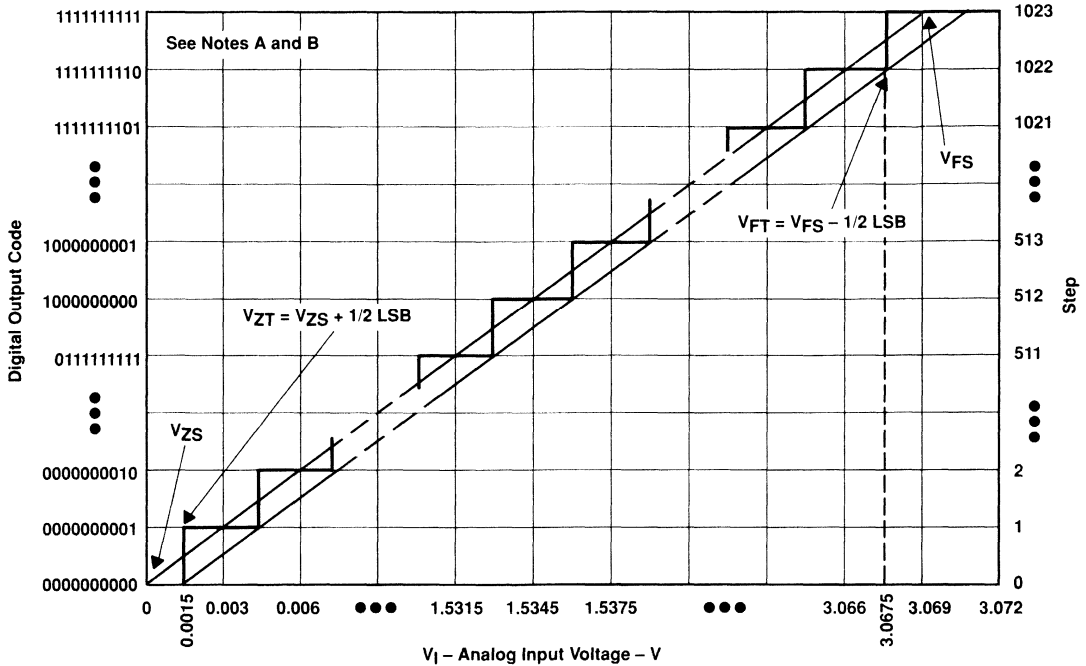
Figure 11. Timing for 16-Clock Transfer Not Using \overline{CS} (Serial Transfer Completed After 21 μs)

- NOTES:
- To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a set up time plus two falling edges of the internal system clock after \overline{CS} before responding to the I/O CLOCK. No attempt should be made to clock out the data until the minimum \overline{CS} setup time has elapsed.
 - A low-to-high transition of \overline{CS} disables I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.
 - The first I/O CLOCK must occur after the end of the previous conversion.

TLV1549C, TLV1549I, TLV1549M
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

SLAS071C – JANUARY 1993 – REVISED MARCH 1995

APPLICATION INFORMATION



- NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0015 V and the transition to full scale (V_{FT}) is 3.0675 V. 1 LSB = 3 mV.
 B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 12. Ideal Conversion Characteristics

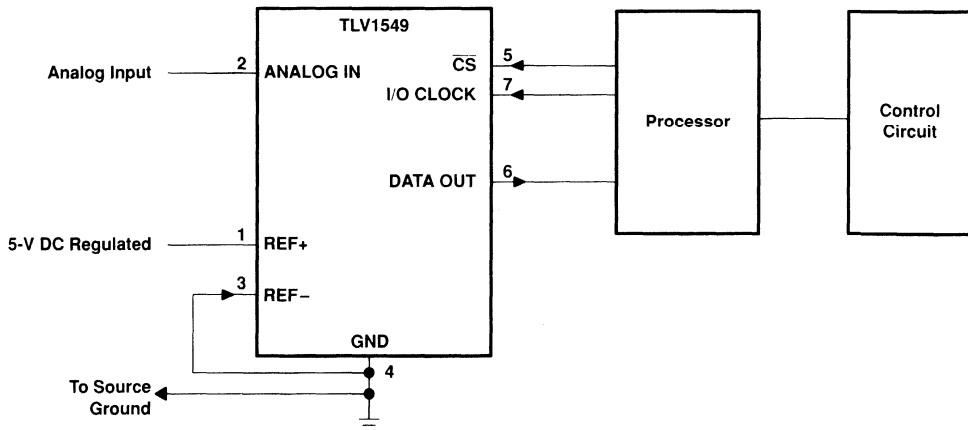


Figure 13. Typical Serial Interface

TLV1549C, TLV1549I, TLV1549M
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

SLAS071C – JANUARY 1993 – REVISED MARCH 1995

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 14, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c / R_t C_i} \right) \quad (1)$$

where

$$R_t = R_S + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S / 2048) \quad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S / 2048) = V_S \left(1 - e^{-t_c / R_t C_i} \right) \quad (3)$$

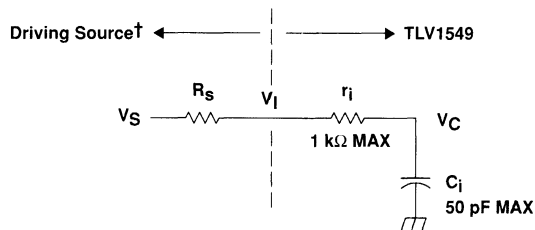
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(2048) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_S + 1 \text{ k}\Omega) \times 60 \text{ pF} \times \ln(2048) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at ANALOG IN
 V_S = External Driving Source Voltage
 R_S = Source Resistance
 r_i = Input Resistance
 C_i = Equivalent Input Capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 14. Equivalent Input Circuit Including the Driving Source

TLV1570
3-V 8-CHANNEL 10-BIT 1.25-MSPS
SERIAL ANALOG-TO-DIGITAL CONVERTER
 SLAS169 – DECEMBER 1997

- **Fast Throughput Rate: 1.25 MSPS**
- **Eight Analog Input Channels**
- **Channel Auto-Scan**
- **Differential Nonlinearity Error: $< \pm 1$ LSB**
- **Integral Nonlinearity Error: $< \pm 1$ LSB**
- **Signal-to-Noise and Distortion Ratio: 57 dB, $f_1 = 500$ kHz**
- **Single 3-V Supply Operation**
- **Low Power . . . 21 mW**
- **Auto-Power Down: 10 μ A Max**
- **Glueless Serial Interface to TMS320 DSPs and (Q)SPI Compatible Microcontrollers**
- **Internal Reference Voltage**

applications

- **Mass Storage and Hard Disk Drive**
- **Industrial Process Control**
- **Communications**
- **Automotive**
- **High-Speed Digital Signal Processing**

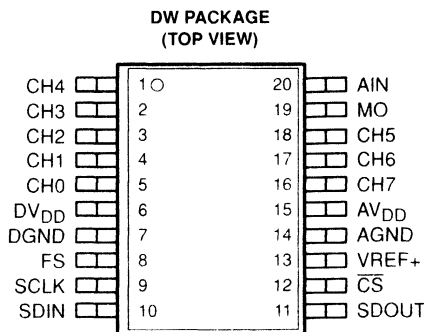
description

The TLV1570 is a 10-bit data acquisition system that combines an 8-channel input multiplexer (MUX), a high-speed 10-bit ADC, an on-chip reference, and a high-speed serial interface. The part contains an on-chip control register allowing control of channel selection, channel auto-scan, and power down via the serial port. The MUX is independently accessible. This allows the user to insert a signal conditioning circuit such as an anti-aliasing filter or an amplifier, if required, between the MUX and the ADC. This means that one signal conditioning circuit can be used for all eight channels.

The TLV1570 operates from a single 3 V power supply. It accepts an analog input range from 0 V to AVDD and digitizes the input at a maximum 1.25 MSPS throughput rate. The power dissipation is only 21 mW. The part features an auto-powerdown mode that automatically powers down to 10 μ A whenever the conversion is not performed.

The TLV1570 communicates with digital microprocessors via a simple 4- or 5-wire serial port that interfaces directly to the Texas Instruments' TMS320 DSPs and (Q)SPI compatible microcontrollers without using additional glue logic.

Very high throughput rate, simple serial interface, 3 V operation, and low power consumption make the TLV1570 an ideal choice for compact or remote high-speed systems.



AVAILABLE OPTIONS

T _A	PACKAGED DEVICES	
	SMALL OUTLINE (DW)	SMALL OUTLINE (PW)
0°C to 70°C	TLV1570CDW	TLV1570CPW
-40°C to 85°C	TLV1570IDW	TLV1570IPW

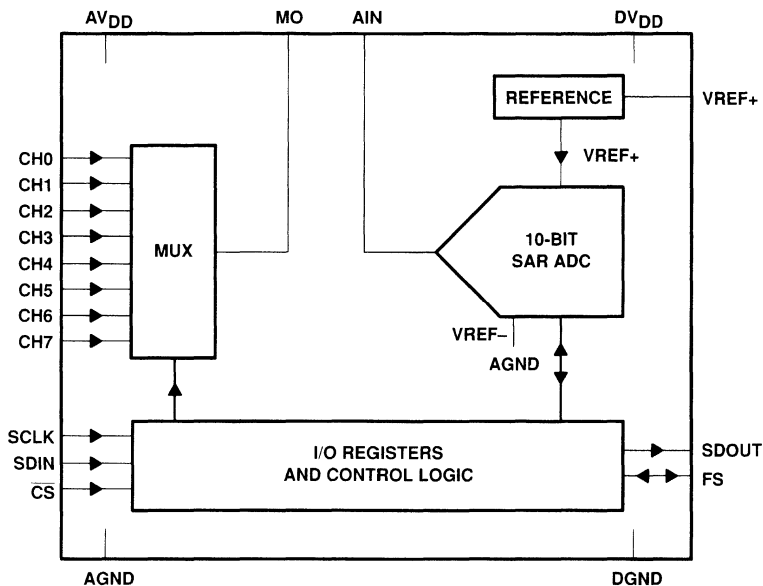
PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



TLV1570
3-V 8-CHANNEL 10-BIT 1.25-MSPS
SERIAL ANALOG-TO-DIGITAL CONVERTER
 SLAS169 – DECEMBER 1997

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	14		Analog ground
AIN	20	I	ADC analog input
AVDD	15		Analog supply voltage
CH0 – CH7	5,4,3 2,1,18 17,16	I	Analog input channels 0 – 7
CS/Powerdown	12	I	Chip Select. A logic low on this input enables the TLV1570. A logic high disables the device and disconnects the power to the TLV1570.
DGND	7		Digital ground
DVDD	6		Digital supply voltage, 3 V
FS	8	I/O	Frame sync input/output (bi-directional) in DSP mode. The falling edge of the frame sync pulse from DSP indicates the start of a serial data frame shifted out of the TLV1570. The FS terminal is pulled high when interfacing to a microcontroller.
MO	19	O	On-chip MUX analog output
SCLK	9	I	Serial clock input. This clock synchronizes the serial data transfer and is also used for internal data conversion.
SDIN	10	I	Serial data input to configure the internal control register.
SDOUT	11	O	Serial data output. A/D conversion results are provided at this output terminal.
VREF+	13	I/O	Internal reference voltage output for external coupling.

PRODUCT PREVIEW



TLV1570
**3-V 8-CHANNEL 10-BIT 1.25-MSPS
 SERIAL ANALOG-TO-DIGITAL CONVERTER**
 SLAS169 – DECEMBER 1997

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, AGND to AVDD, DGND to DVDD	–0.3 V to 6.5V
Analog input voltage range	–0.3 V to AVDD+0.3
Reference input voltage	AVDD+0.3
Digital input voltage range	–0.3 V to DVDD+0.3
Operating virtual junction temperature range, T _J	–40°C to 150°C
Operating free-air temperature range, T _A	0°C to 70°C
Storage temperature range, T _{stg}	–65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

power supplies

	MIN	NOM	MAX	UNIT
AVDD Analog supply voltage	2.7	3	3.6	V
DVDD Digital supply voltage	2.7	3	3.6	V

analog inputs

	MIN	MAX	UNIT
AIN Analog input voltage	AGND	VREF+	V

digital inputs

	MIN	NOM	MAX	UNIT	
High-level input voltage, V _{IH}	DVDD = 2.7 V to 3.6 V		2.1	2.4	V
Low-level input voltage, V _{IL}	DVDD = 2.7 V to 3.6 V			0.8	V
Input SCLK frequency	DVDD = 2.7 V to 3.6 V			20	MHZ
SCLK pulse duration, clock high, t _w (SCLKH)	DVDD = 2.7 V to 3.6 V		23		ns
SCLK pulse duration, clock low, t _w (SCLKL)	DVDD = 2.7 V to 3.6 V		23		ns

PRODUCT PREVIEW



TLV1570
3-V 8-CHANNEL 10-BIT 1.25-MSPS
SERIAL ANALOG-TO-DIGITAL CONVERTER
 SLAS169 – DECEMBER 1997

electrical characteristics, over recommended operating free-air temperature range, $AV_{DD} = DV_{DD} = 2.7\text{ V to }3.6\text{ V}$, $f_{SCLK} = 20\text{ MHz}$, $V_{REF+} = 2.4\text{ V}$ (Internal VREF Mode) (unless otherwise noted)

digital specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic inputs						
I_{IH}	High-level input current	$DV_{DD} = 3\text{ V}$	-50		50	μA
I_{IL}	Low-level input current	$DV_{DD} = 3\text{ V}$	-50		50	μA
C_I	Input capacitance			5		pF
Logic outputs						
V_{OH}	High-level output voltage	$I_{OH} = 50\ \mu\text{A} - 0.5\text{ mA}$		$DV_{DD} - 0.4$		V
V_{OL}	Low-level output voltage	$I_{OL} = 50\ \mu\text{A} - 0.5\text{ mA}$		0.4		V
I_{OZ}	High-impedance-state output current		-50		50	μA
C_O	Output capacitance			5		pF

dc specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				10		Bits
Accuracy						
INL	Integral nonlinearity	Best fit		± 0.6	± 1	LSB
DNL	Differential nonlinearity			± 0.4	± 1	LSB
	Offset error			± 0.1	± 0.15	%FSR
	Gain error			± 0.1	± 0.2	%FSR
Analog input						
	Input full scale range		GND		V_{REF+}	V
	Input capacitance			15		pF
	Input leakage current	$V_{AIN} = 0\text{ to }AV_{DD}$			± 1	μA
Voltage reference						
V_{REF+}	Internal reference voltage	Internal reference mode	2.37	2.38	2.4	V
V_{REF+}	External reference voltage	External reference mode			AV_{DD}	V
Power supply						
$I_{DD} + I_{REF}$	Operating supply current	$AV_{DD} = DV_{DD} = 3\text{ V}$, $f_{SCLK} = 20\text{ MHz}$		7		mA
I_{PD}	Supply current in powerdown mode	$I_{DD} + I_{REF}$			10	μA
	Power dissipation	$AV_{DD} = DV_{DD} = 3\text{ V}$		21		mW

PRODUCT PREVIEW



TLV1570
3-V 8-CHANNEL 10-BIT 1.25-MSPS
SERIAL ANALOG-TO-DIGITAL CONVERTER
SLAS169 – DECEMBER 1997

electrical characteristics, over recommended operating free-air temperature range, $AV_{DD} = DV_{DD} = 2.7\text{ V to }3.6\text{ V}$, $f_{SCLK} = 20\text{ MHz}$, $VREF+ = 2.4\text{ V}$ (Internal VREF Mode) (unless otherwise noted)
(continued)

ac specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Signal-to-noise ratio + distortion	$f_{(input)} = 100\text{ kHz}$	54	57		dB
THD	Total harmonic distortion	$f_{(input)} = 100\text{ kHz}$	56	60		dB
	Effective number of bits	$f_{(input)} = 100\text{ kHz}$	8.7	9.35		Bits
	Spurious-free dynamic range	$f_{(input)} = 100\text{ kHz}$	57	62		dB
Analog Input						
	Channel-to-channel cross talk			75		dB
BW	Full-power bandwidth			12		MHz
BW	Small-signal bandwidth			20		MHz

timing specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c	SCLK period	$DV_{DD} = 3\text{ V}$	50			ns
$t_{(rs)}$	Reset and sampling period			6		SLCK cycles
t_c	Conversion period			10		SLCK cycles
t_{su1}	FS setup time to SCLK falling edge in DSP mode		10			ns
t_{h1}	FS hold time to SCLK falling edge in DSP mode		4			ns
t_{su2}	FS setup time to \overline{CS} falling edge in DSP mode		5.5			ns
t_{h2}	FS hold time to \overline{CS} falling edge in DSP mode		9			ns
t_{d1}	Output delay after SCLK rising edge in DSP mode			15	25	ns
$t_{d(L)1}$	FS falling edge to next SCLK falling edge in DSP mode		6			ns
$t_{d(L)2}$	SCLK rising edge after \overline{CS} falling edge in μC mode		4			ns
t_{d2}	Output delay after SCLK rising edge in μC mode			15	25	ns
t_{su3}	Serial input data setup time to SCLK falling edge		10			ns
t_{h3}	Serial input data hold time to SCLK falling edge		4			ns

Specifications subject to change without notice.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

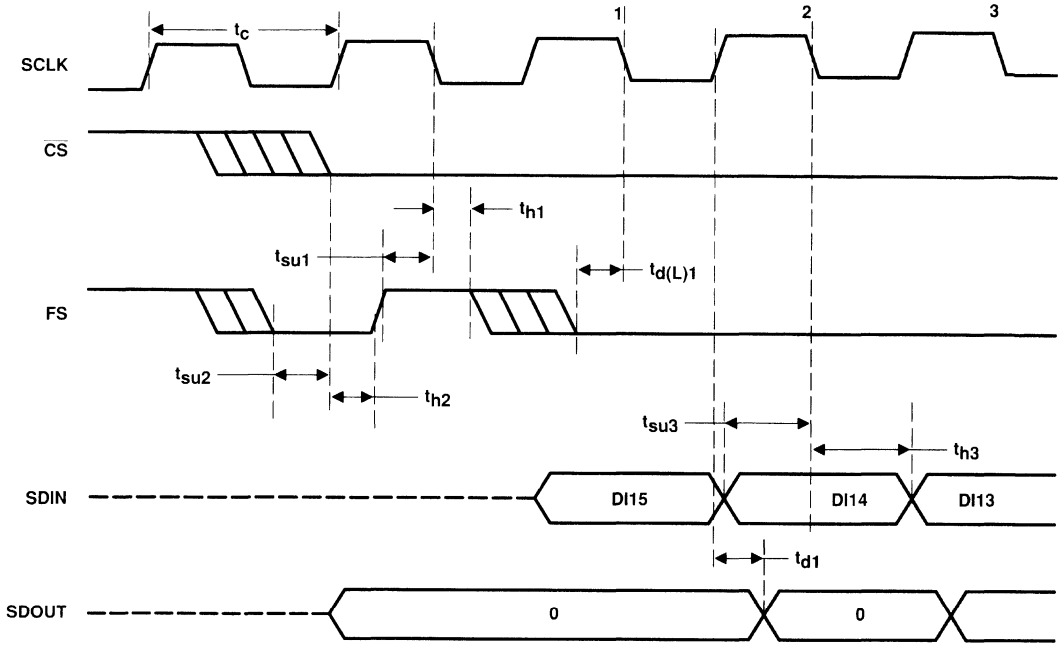


Figure 1. DSP Mode Timing Diagrams

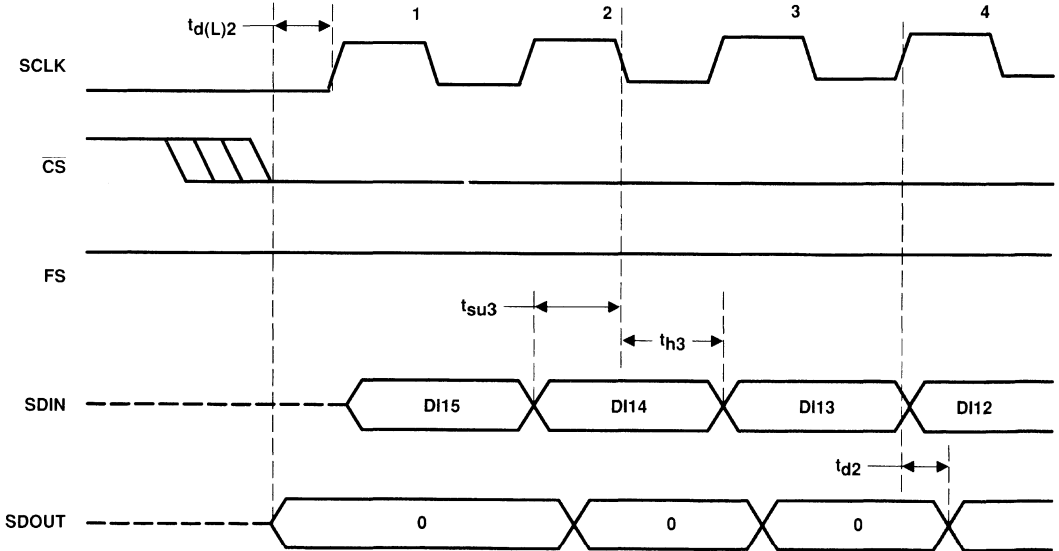


Figure 2. μ C Mode Timing Diagrams

PRODUCT PREVIEW



definitions of specifications and terminology

integral nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full scale point is defined as level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

differential nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ± 1 LSB ensures no missing codes.

zero offset

The major carry transition should occur when the analog input is at zero volts. Zero error is defined as the deviation of the actual transition from that point.

gain error

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

signal-to-noise ratio + distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

effective number of bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (\text{SINAD} - 1.76)/6.02$$

It is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

total harmonic distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

spurious free dynamic range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

TLV1570
3-V 8-CHANNEL 10-BIT 1.25-MSPS
SERIAL ANALOG-TO-DIGITAL CONVERTER
 SLAS169 – DECEMBER 1997

PRINCIPLES OF OPERATION

serial input data format

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
------	------	------	------	------	------	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----

internal register description

Bit	Description															
DI15	Software powerdown. 0 – powerup, 1 – powerdown															
DI14	Reads out values of the internal register, 1 – read. Only DI15 – DI1 will be read out.															
DI13, DI12	These two bits select the self-test voltage to be applied to the ADC input during next clock cycle: <table border="1" style="margin-left: 20px;"> <tr> <td>DI13</td><td>DI12</td><td></td></tr> <tr> <td>0</td><td>0</td><td>Allow AIN to com in normally</td></tr> <tr> <td>0</td><td>1</td><td>Apply AGND to AIN.</td></tr> <tr> <td>1</td><td>0</td><td>Apply VREF to AIN.</td></tr> <tr> <td>1</td><td>1</td><td>Apply VREF/2 to AIN</td></tr> </table>	DI13	DI12		0	0	Allow AIN to com in normally	0	1	Apply AGND to AIN.	1	0	Apply VREF to AIN.	1	1	Apply VREF/2 to AIN
DI13	DI12															
0	0	Allow AIN to com in normally														
0	1	Apply AGND to AIN.														
1	0	Apply VREF to AIN.														
1	1	Apply VREF/2 to AIN														
DI11	Low power mode. If CLKC < 10 MHz, then DI11 can be set to 0 and power consumption is reduced 20%.															
DI10	This bit controls channel auto-scan function. 0 – auto-scan disabled, 1 – auto-scan enabled.															
DI9, DI8	These two bits select the channel auto-scan modes (when DI10 is 1). <table border="1" style="margin-left: 20px;"> <tr> <td>DI9</td><td>DI8</td><td></td></tr> <tr> <td>0</td><td>0</td><td>CH1, CH2, CH3,, CH8</td></tr> <tr> <td>0</td><td>1</td><td>CH1, CH3, CH5, CH7</td></tr> <tr> <td>1</td><td>0</td><td>CH2, CH4, CH6, CH8</td></tr> <tr> <td>1</td><td>1</td><td>CH 8, CH7, CH6,, CH1</td></tr> </table>	DI9	DI8		0	0	CH1, CH2, CH3,, CH8	0	1	CH1, CH3, CH5, CH7	1	0	CH2, CH4, CH6, CH8	1	1	CH 8, CH7, CH6,, CH1
DI9	DI8															
0	0	CH1, CH2, CH3,, CH8														
0	1	CH1, CH3, CH5, CH7														
1	0	CH2, CH4, CH6, CH8														
1	1	CH 8, CH7, CH6,, CH1														
DI7	Auto-scan reset, 1 – reset. To use auto-scan feature, this bit must be set to 1 in the first cycle after power up.															
DI9, DI8, DI7	These three bits select which of the eight channels is to be used for sampling when the auto-scan is disabled (DI10 is 0). See channel selection format tables for details.															
DI6	Internal or external reference. If DI6 = 1 then the internal reference is enabled. If DI6 = 0 then the external reference is enabled.															
DI5	Reserved (always set to 0)															
DI4	Enables/Disables auto-powerdown function, 0 – Enable, 1 – Disable.															
DI3	Reserved (always set to 1)															
DI2	Reserved (always set to 0)															
DI1	Reserved (always set to 0)															
DI0	Don't care															

PRODUCT PREVIEW

channel selection format

DI9	DI8	DI7	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+							
0	0	1		+						
0	1	0			+					
0	1	1				+				
1	0	0					+			
1	0	1						+		
1	1	0							+	
1	1	1								+



APPLICATION INFORMATION

The TLV1570 is a 10-bit 8-analog input channel analog-to-digital converter with the throughput up to 1.25 MSPS. To run at its fastest conversion rate, it must be clocked at 20 MHz. The TLV1570 can be easily interfaced to microcontrollers, ASICs, DSPs, or shift registers. Its serial interface is designed to be fully compatible with Serial Peripheral Interface(SPI) and the TMS320 DSP serial ports. It requires no hardware to interface between the TLV1570 and the microcontrollers (μ Cs) with the SPI serial port or the TMS320 DSPs. However, the speed will be limited by the SCLK rate of the μ C or the DSP.

The TLV1570 interfaces to the DSPs over five lines: \overline{CS} , SCLK, SDOUT, SDIN, and FS, and interfaces to μ Cs over four lines: \overline{CS} , SCLK, SDOUT, and SDIN. The FS input should be pulled high in μ C mode. The chip is in tristate and powerdown mode when the \overline{CS} is high. After the \overline{CS} falls, the TLV1570 checks the FS input at the \overline{CS} 's falling edge to determine the operation mode. If the FS is low, the DSP mode is set, else the μ C mode is set.

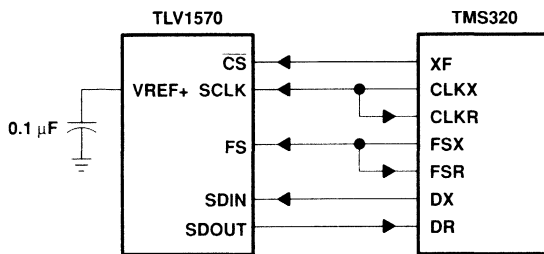


Figure 3. DSP to TLV1570 Interface

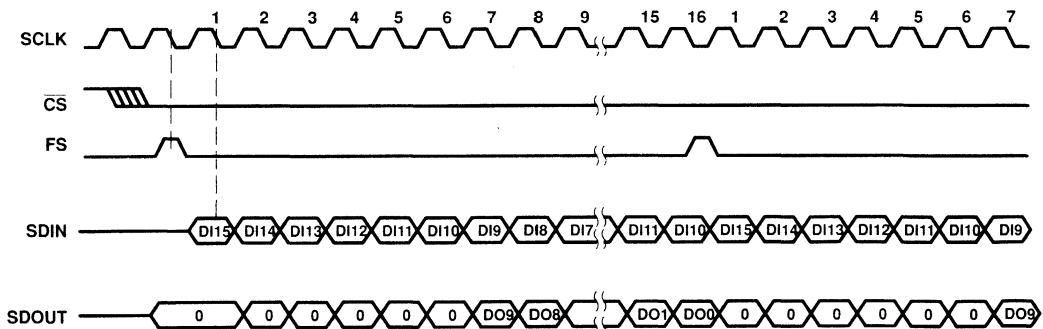


Figure 4. Typical Timing Diagram for DSP Application

PRODUCT PREVIEW

TLV1570
3-V 8-CHANNEL 10-BIT 1.25-MSPS
SERIAL ANALOG-TO-DIGITAL CONVERTER
 SLAS169 – DECEMBER 1997

APPLICATION INFORMATION

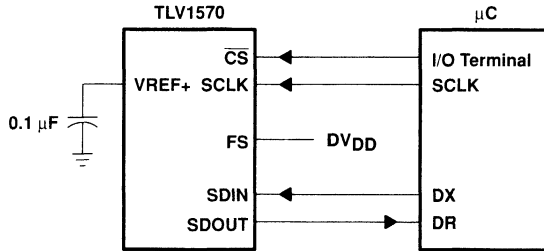


Figure 5. μ C to TLV1570 Interface

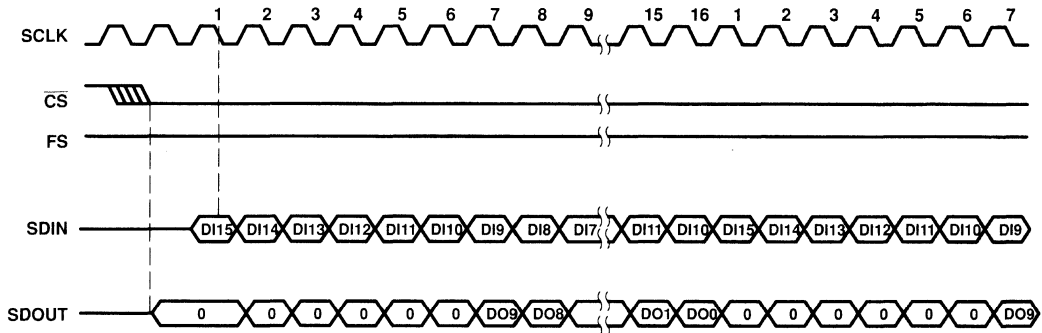


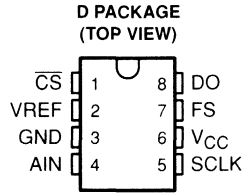
Figure 6. Typical Timing Diagram for μ C Application

PRODUCT PREVIEW



TLV1572
2.7 V TO 5.5 V, 10-BIT, 1.25 MSPS
SERIAL ADC WITH AUTO-POWERDOWN
SLAS171 – DECEMBER 1997

- **Fast Throughput Rate: 1.25 MSPS**
- **8-pin SOIC Package**
- **Differential Nonlinearity Error: $< \pm 1$ LSB**
- **Integral Nonlinearity Error: $< \pm 1$ LSB**
- **Signal-to-Noise and Distortion Ratio: 59 dB, $f_{(input)} = 500$ kHz**
- **Single 3-V to 5-V Supply Operation**
- **Very Low Power: 8 mW at 3V; 25mW at 5 V**
- **Auto-Powerdown: 10 μ A Maximum**
- **Glueless Serial Interface to TMS320 DSPs and (Q)SPI Compatible Micro-controllers**
- **Inherent Internal Sample and Hold Operation**



Applications

- **Mass Storage and HDD**
- **Automotive**
- **Digital Servos**
- **Process Control**
- **General Purpose DSP**
- **Contact Image Sensor Processing**

description

The TLV1572 is a high-speed 10-bit successive-approximation analog-to-digital converter (ADC) which operates from a single 2.7-V to 5.5-V power supply and is housed in a small 8-pin SOIC package.

The TLV1572 accepts an analog input range from 0 to V_{CC} and digitizes the input at a maximum 1.25MSPS throughput rate. The power dissipation is only 8 mW with 3-V supply or 25 mW with 5-V supply. The part features an auto-powerdown mode that automatically powers down to 10 μ A whenever the conversion is not performed.

The TLV1572 communicates with digital microprocessors via a simple 3- or 4-wire serial port that interfaces directly to the Texas Instruments' TMS320 DSPs and (Q)SPI compatible microcontrollers without using additional glue logic.

Very high throughput rate, simple serial interface, SO-8 package, 3-V operation, and low power consumption make the TLV1572 an ideal choice for compact or remote high-speed systems.

AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (D)
0°C to 70°C	TLV1572CD
-40°C to 85°C	TLV1572ID

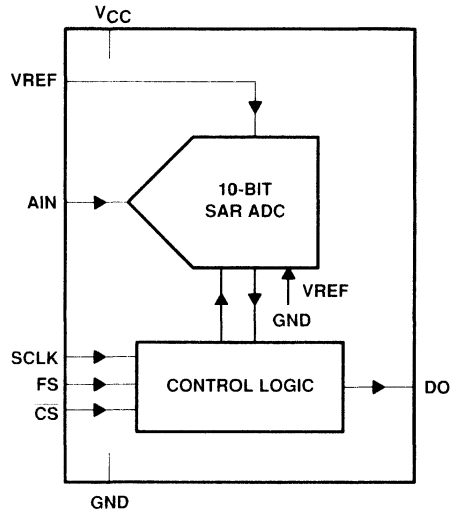
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



TLV1572
2.7 V TO 5.5 V, 10-BIT, 1.25 MSPS
SERIAL ADC WITH AUTO-POWERDOWN

SLAS171 – DECEMBER 1997

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CS/Powerdown	1	I	Chip Select. A logic low on this input enables the TLV1572. A logic high disables the device and disconnects the power to the TLV1572.
AIN	2	i	Analog input
VREF	3	I	Reference voltage input. The voltage applied to this pin defines the input span of the TLV1572.
GND	4		Ground
DO	5	O	Serial data output. A/D conversion results are provided at this output pin.
FS	6	I	Frame sync input in DSP mode. The falling edge of the frame sync pulse from DSP indicates the start of a serial data frame shifted out of the TLV1572. The FS input is tied to VCC when interfacing to a micro-controller.
SCLK	7	I	Serial clock input. This clock synchronizes the serial data transfer and is also used for internal data conversion.
VCC	8		Power supply, recommend connection to analog supply

TLV1572
2.7 V TO 5.5 V, 10-BIT, 1.25 MSPS
SERIAL ADC WITH AUTO-POWERDOWN
 SLAS171 – DECEMBER 1997

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, GND to V_{CC}	–0.3 V to 6.5V
Analog input voltage range	–0.3 V to $V_{CC} + 0.3$
Reference input voltage	$V_{CC} + 0.3$
Digital input voltage range	–0.3 V to $V_{CC} + 0.3$
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

power supply

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	2.7		5.5	V

analog inputs

	MIN	MAX	UNIT
V_{AIN} Analog input voltage	GND	V_{REF}	V
V_{REF} Reference input voltage	2.7	V_{CC}	V

digital inputs

	MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	$V_{CC} = 3\text{ V to }5.5\text{ V}$	2.1	2.4	V
Low-level input voltage, V_{IL}	$V_{CC} = 3\text{ V to }5.5\text{ V}$		0.8	V
Input SCLK frequency	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		20	MHZ
SCLK pulse duration, clock high, $t_w(\text{SCLKH})$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	23		ns
SCLK pulse duration, clock low, $t_w(\text{SCLKL})$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	23		ns
Input SCLK frequency	$V_{CC} = 3\text{ V}$		10	MHZ
SCLK pulse duration, clock high, $t_w(\text{SCLKH})$	$V_{CC} = 3\text{ V}$	45		ns
SCLK pulse duration, clock low, $t_w(\text{SCLKL})$	$V_{CC} = 3\text{ V}$	45		ns



TLV1572
2.7 V TO 5.5 V, 10-BIT, 1.25 MSPS
SERIAL ADC WITH AUTO-POWERDOWN
 SLAS171 – DECEMBER 1997

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V}$, $V_{REF} = 5\text{ V}$, $f_{SCLK} = 20\text{ MHz}$ (unless otherwise noted)

digital specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic inputs						
I_{IH}	High-level input current	$V_{CC} = 5\text{ V}$	-50		50	μA
I_{IL}	Low-level input current	$V_{CC} = 5\text{ V}$	-50		50	μA
C_i	input capacitance			5		pF
Logic outputs						
V_{OH}	High-level output voltage	$I_{OH} = 50\mu\text{A} - 0.5\text{mA}$	$V_{CC} - 0.4$			V
V_{OL}	Low-level output voltage	$I_{OL} = 50\mu\text{A} - 0.5\text{mA}$	0.4			V
I_{OZ}	High-impedance-state output current		-50		50	μA
C_O	Output capacitance			5		pF

dc specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				10		Bits
Accuracy						
INL	Integral nonlinearity	Best fit		± 0.5	± 1	LSB
DNL	Differential nonlinearity			± 0.3	± 1	LSB
Offset error				± 0.1	± 0.15	%FSR
Gain error				± 0.1	± 0.2	%FSR
Analog input						
Input full scale range			GND		V_{CC}	V
Input capacitance				15		pF
input leakage current		$V_{AIN} = 0 \text{ to } V_{CC}$			50	μA
Voltage reference input						
V_{REF+}	Positive reference voltage		3		V_{CC}	V
V_{REF-}	Negative reference voltage	Internally connects to GND		GND		V
Input resistance				2		$\text{K}\Omega$
Input capacitance				300		pF
Power supply						
$I_{CC} + I_{REF}$	Operating supply current	$V_{CC} = 5.5\text{ V}$, $f_{SCLK} = 20\text{ MHz}$		5.5	8.5	mA
		$V_{CC} = 3\text{ V}$, $f_{SCLK} = 10\text{ MHz}$		2.7		
I_{PD}	Supply current in powerdown mode	V_{CC}			10	μA
Power dissipation		$V_{CC} = 5\text{ V}$		25		mW
Power dissipation		$V_{CC} = 3\text{ V}$		8		mW



TLV1572
2.7 V TO 5.5 V, 10-BIT, 1.25 MSPS
SERIAL ADC WITH AUTO-POWERDOWN

SLAS171 – DECEMBER 1997

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V}$, $V_{REF} = 5\text{ V}$, $f_{SCLK} = 20\text{ MHz}$ (unless otherwise noted) (continued)

ac specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Signal-to-noise ratio + distortion	$f_{(input)} = 200\text{ kHz}$	54	58		dB
THD	Total harmonic distortion	$f_{(input)} = 200\text{ kHz}$	56	60		dB
	Effective number of bits	$f_{(input)} = 200\text{ kHz}$	8.7	9.35		Bits
	Spurious-free dynamic range	$f_{(input)} = 200\text{ kHz}$	57	62		dB
Analog Input						
BW	Full-power bandwidth	Source impedance = 1 k Ω		12		MHz
BW	Small-signal bandwidth	Source impedance = 1 k Ω		20		Mhz

timing specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c	SCLK period	$V_{CC} = 4.5\text{ V} - 5.5\text{ V}$	50			ns
t_c	SCLK period	$V_{CC} = 2.7\text{ V} - 3.3\text{ V}$	100			ns
t_{rs}	Reset and sampling period			6		SLCK cycles
t_c	Conversion period			10		SLCK cycles
t_{su1}	FS setup time to SCLK falling edge in DSP mode		10			ns
t_{h1}	FS hold time to SCLK falling edge in DSP mode		4			ns
t_{su2}	FS setup time to \overline{CS} falling edge in DSP mode		6			ns
t_{h2}	FS hold time to \overline{CS} falling edge in DSP mode		9			ns
t_{d1}	Output delay after SCLK rising edge in DSP mode			15	25	ns
$t_{d(L)1}$	FS falling edge to next SCLK falling edge in DSP mode		6			ns
$t_{Ld(L)2}$	SCLK rising edge after \overline{CS} falling edge in μC mode		4			ns
t_{d2}	Output delay after SCLK rising edge in μC mode			15	25	ns

Specifications subject to change without notice.



PARAMETER MEASUREMENT INFORMATION

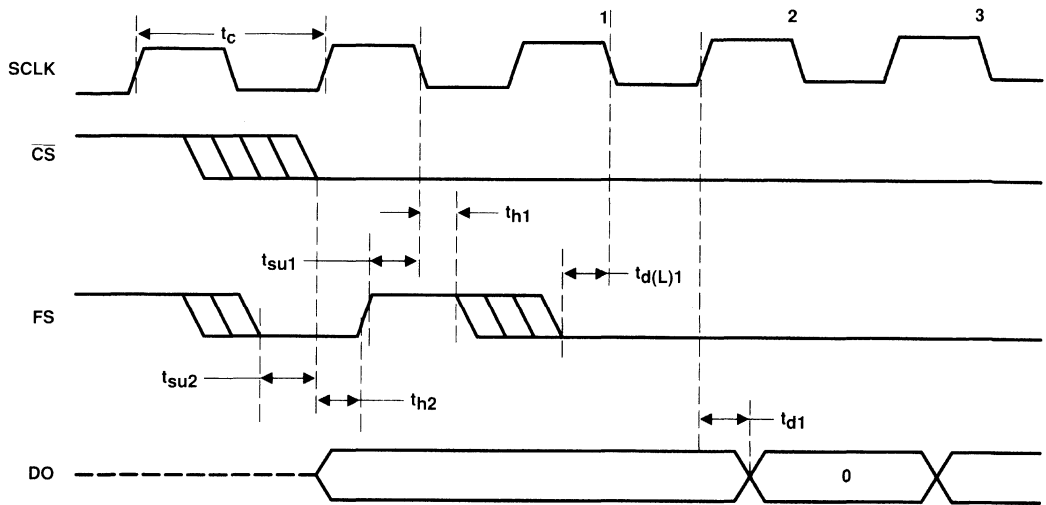


Figure 1. DSP Mode Timing Diagrams

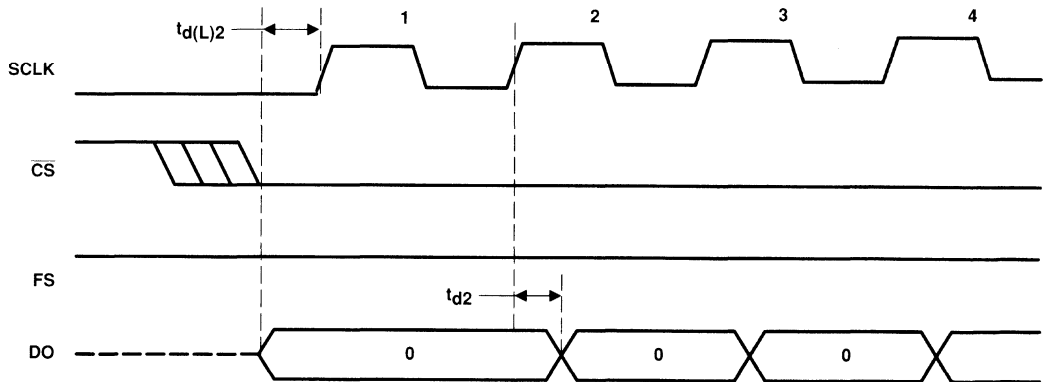


Figure 2. μ C Mode Timing Diagrams

definitions of specifications and terminology

integral nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full scale point is defined as level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

differential nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ± 1 LSB ensures no missing codes.

zero offset

The first code transition should ideally occur at an analog value 1/2 LSB above V_{REF-} . The zero offset error is defined as the error between the ideal first transition point and the actual first transition. This error effectively shifts left or right an ADC transfer function

gain error

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

signal-to-noise ratio + distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

effective number of bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (\text{SINAD} - 1.76)/6.02$$

it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

total harmonic distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

spurious free dynamic range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the largest peak spurious signal.

TLV1572
2.7 V TO 5.5 V, 10-BIT, 1.25 MSPS
SERIAL ADC WITH AUTO-POWERDOWN
 SLAS171 – DECEMBER 1997

APPLICATION INFORMATION

The TLV1572 is a 600ns, 10-bit analog-to-digital converter with the throughput up to 1.25MSPS at 5V and up to 625KSPS at 3V respectively. To run at its fastest conversion rate, it must be clocked at 20MHz at 5V or 10MHz at 3V. The TLV1572 can be easily interfaced to microcontrollers, ASICs, DSPs, or shift registers. Its serial interface is designed to be fully compatible with Serial Peripheral Interface(SPI) and the TMS320 DSP serial ports. It requires no hardware to interface between the TLV1572 and the microcontrollers (μ Cs) with the SPI serial port or the TMS320 DSPs. However, the speed will be limited by the SCLK rate of the μ C or the DSP.

The TLV1572 interfaces to the DSPs over four lines: \overline{CS} , SCLK, DO, and FS, and interfaces to μ Cs over three lines: \overline{CS} , SCLK, and DO. The FS input should be pulled high in μ C mode. The chip is in tristate and powerdown mode when the \overline{CS} is high. After the \overline{CS} falls, the TLV1572 checks the FS input at the \overline{CS} 's falling edge to determine the operation mode. If the FS is low, the DSP mode is set, else the μ C mode is set.

Interfacing TLV1572 to TMS320 DSPs

The TLV1572 is compatible with Texas Instruments TMS320 DSP serial ports. Figures 3 and 4 show the pin connections to interface the TLV1572 to the TMS320 DSPs.

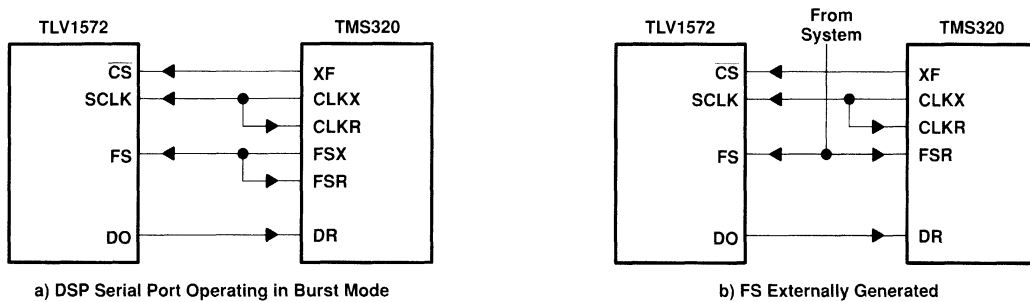


Figure 3. DSP to TLV1570 Interface

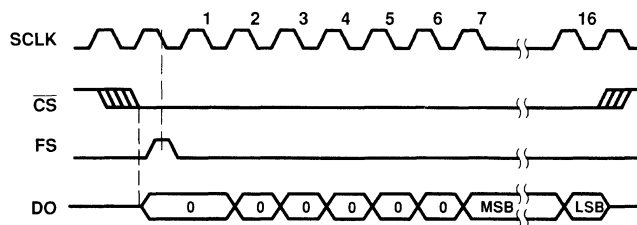


Figure 4. Typical Timing Diagram for DSP Application

In the DSP mode, the FS input should be low when the \overline{CS} goes low. There is a hold time before FS input can go high after the \overline{CS} 's falling edge to ensure proper mode latching. With the \overline{CS} going low, the DO comes out of tristate but the chip is still in powerdown until the FS (Frame Sync signal from DSP) comes.

The TLV1572 checks for the FS at the falling edges of SCLK. Once the FS is detected high, the sampling of input is started. As soon as the FS goes low, the chip starts shifting the data out on the DO line. After six null bits, the A/D conversion data becomes available on the SCLK rising edges and is latched by DSP on the falling edges. Figure 5 shows the DSP mode timing diagram.



APPLICATION INFORMATION

Interfacing TLV1572 to TMS320 DSPs(continued)

The TLV1572 goes into auto-powerdown after the LSB is shifted out. The next FS pulls it out of auto-powerdown as shown in Fig. 6. If the FS comes on the 16th bit, next conversion cycle starts from next rising edge of the SCLK allowing back to back conversions as shown in Figure 7. An FS in the middle of a conversion cycle resets the chip and starts a new conversion cycle. Therefore variable-bit transfer is supported if the FS appears earlier.

The \overline{CS} can be pulled high asynchronously to put chip into tristate and powerdown. The \overline{CS} can also be pulled low asynchronously to start checking for the FS on the falling edges of clock.

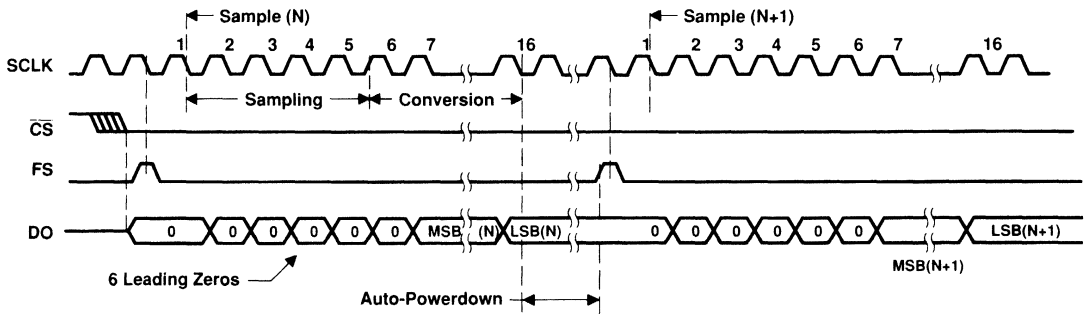


Figure 5. DSP Application Timing (Intermittent Conversion)

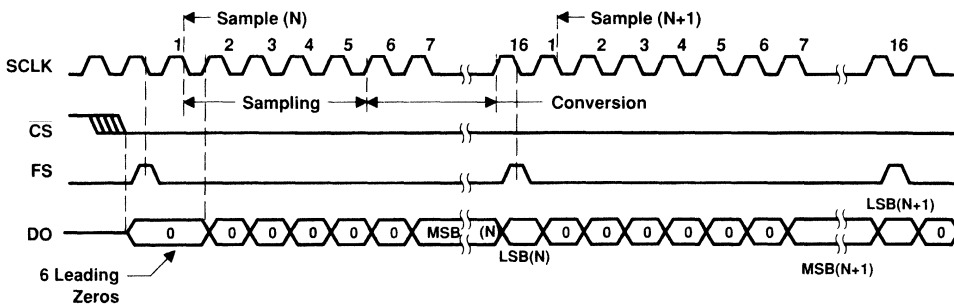


Figure 6. DSP Application Timing (Continuous Conversion)

key points

1. When \overline{CS} goes low, if FS is low, it is DSP mode. FS is sampled twice by \overline{CS} falling edge and again by internally delayed \overline{CS} falling edge. Even if a glitch appears and one latch latches 1 and another latches 0, chip goes into DSP mode (μC mode requires both latches to latch 1). There is a hold time before FS can go high again after \overline{CS} falling edge to ensure proper mode latching as detailed above. With \overline{CS} going low, DO is in tristate and the chip is in powerdown until FS rising edge.
2. 1572 checks for FS at every falling edge of SCLK. If FS is detected high, chip goes into reset. When FS goes low, 1572 waits for DSP to latch the first bit 0.
3. Sampling occurs from first falling edge of SCLK after FS going low till the rising edge when 6th bit 0 is given out. There after decisions are taken on rising edges and data is given out on rising edges a bit delayed. DSP samples on falling edge of SCLK. Data is padded with 6 leading zeros.

APPLICATION INFORMATION

key points (continued)

4. Note that chip goes into autowerdown on the 17th falling edge of SCLK (just after LSB). FS rising edge pulls it out of autowerdown. If FS comes on the 16th bit itself, next conversion cycle starts from next rising edge allowing back to back conversions. An FS in the middle of a conversion cycle starts a new conversion cycle. Thus variable-bit transfer is supported if FS appears earlier.
5. DO goes into tristate on the 17th rising edge and comes out on FS rising edge.
6. \overline{CS} can be pulled high asynchronously to put chip into tristate and powerdown. \overline{CS} may also be pulled low asynchronously to start checking for FS on falling edges of clock

For applications where the analog input must be sampled at a precise instant in time, the data conversion can be initiated by an external conversion start pulse which is completely asynchronous to the SCLK as shown in Figure 4. When a conversion start pulse is received, the pulse is used as a Frame Sync (FS) signal to initiate the data conversion and transfer. The corresponding timing diagram is shown in Figure 6.

Interfacing TLV1572 to SPI/QSPI compatible microcontrollers(μ Cs)

The TLV1572 is compatible with SPI and QSPI serial interface standards (Note: the TLV1572 supports the following SPI clock options: CLOCK_POLARITY= 0, i.e. SCLK idles low, and CLOCK_PHASE = 1). Figure 8 shows the pin connections to interface the TLV1572 to the SPI/QSPI compatible microcontrollers.

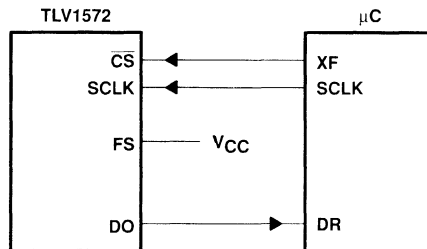


Figure 7. μ C to TLV1572 Interface

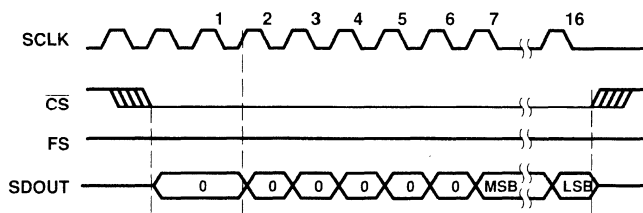


Figure 8. Typical Timing Diagram for μ C Application

To use the TLV1572 in a non-DSP application, the FS input should be pulled high as shown in Figure 8.

A total of 16 clocks are normally supplied for each conversion. If μ C cannot take in 16 bits at a time, it may take 8 bits with 8 clocks and next 8 bits with another 8 clocks. The \overline{CS} should be kept low throughout the conversion. The delay between these two 8-clock periods should not be longer than 100 μ s.

APPLICATION INFORMATION

Interfacing TLV1572 to SPI/QSPI compatible microcontrollers(μ Cs)(continued)

Unlike the DSP mode in which the conversion is initiated by the FS input signal from the DSP, the conversion is initiated by the incoming SCLK after the \overline{CS} falls. The sampling of input is started on the first rising edge of the SCLK after the \overline{CS} goes down. After six null bits, the A/D conversion data becomes available on the SCLK rising edges and is latched by μ C on the falling edges. The \overline{CS} can be pulled high during the conversion before the LSB is shifted out to use the chip as a lower resolution ADC. Figure 9 shows the μ C mode timing diagram.

The chip goes into autpowerdown after the LSB is shifted out and is brought out of the powerdown by next clock's rising edge as shown in Figure 10.

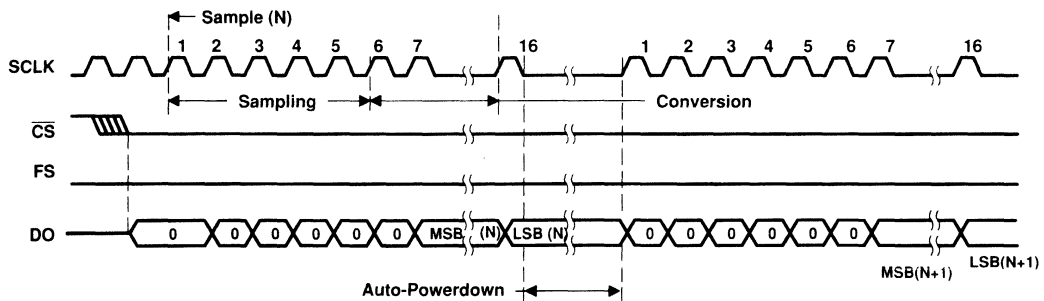


Figure 9. μ C Application

key points

1. When \overline{CS} goes low, if FS is high, it is μ C (Q)SPI mode. Thus, FS should be tied to VDD. FS is latched twice, on \overline{CS} falling edge and again on internally delayed \overline{CS} falling edge. Only if both latches latch 1, the μ C mode is set else DSP mode is set. Only polarity = 0 is supported i.e. SCLK idles low. Only clock_phase = 1 is supported as shown in timing diagrams.
2. 16 clocks have to be supplied for each conversion. If μ C cannot take in 16 bits at a time, it may take 8 bits with 8 clocks and next 8 bits with another 8 clocks keeping \overline{CS} low throughout the conversion. The delay between these two 8-clock periods should not be higher than 100 ns.
3. Sampling starts on first falling edge of SCLK and ends on the edge when 6th bit 0 is given out. Decisions are made on the rising edge and data is output on the same edge but a bit delayed to avoid noise.

TLV1572

2.7 V TO 5.5 V, 10-BIT, 1.25 MSPS

SERIAL ADC WITH AUTO-POWERDOWN

SLAS171 – DECEMBER 1997

4. Chip goes into autopowerdown on the 16th clock's falling edge and is brought out of it by next 1st(17th) clock's rising edge.
5. If (Q)SP wants less than 16-bit transfer, \overline{CS} must go high after each transfer. The falling edge of \overline{CS} will reset the 1572 for the next conversion. Thus one may do a 14-bit transfer to use the chip as an 8-bit A/D.
6. \overline{CS} going high puts chip in tristate and complete powerdown. \overline{CS} going low merely sets the mode and pulls DO out of tristate.

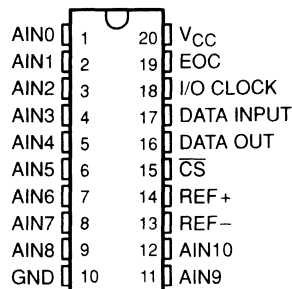
TLV2543C, TLV2543I

12-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

- 12-Bit-Resolution A/D Converter
- 10- μ s Conversion Time Over Operating Temperature Range
- 11 Analog Input Channels
- 3 Built-In Self-Test Modes
- Inherent Sample and Hold Function
- Linearity Error . . . ± 1 LSB Max
- On-Chip System Clock
- End-of-Conversion (EOC) Output
- Unipolar or Bipolar Output Operation (Signed Binary With Respect to Half of the Applied Referenced Voltage)
- Programmable MSB or LSB First
- Programmable Power Down
- Programmable Output Data Length
- CMOS Technology

DB, DW, OR N PACKAGE
(TOP VIEW)



description

The TLV2543C and TLV2543I are 12-bit, switched-capacitor, successive-approximation, analog-to-digital converters (ADCs). Each device has three control inputs [chip select (\overline{CS}), the input-output clock (I/O CLOCK), and the address input (DATA INPUT)] and is designed for communication with the serial port of a host processor or peripheral through a serial 3-state output. The device allows high-speed data transfers from the host.

In addition to the high-speed converter and versatile control capability, the device has an on-chip 14-channel multiplexer that can select any one of 11 inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the device features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating temperature range.

The TLV2543 is available in the DW, DB, and N packages. The TLV2543C is characterized for operation from 0°C to 70°C, and the TLV2543I is characterized for operation from -40°C to 85°C.

AVAILABLE OPTIONS

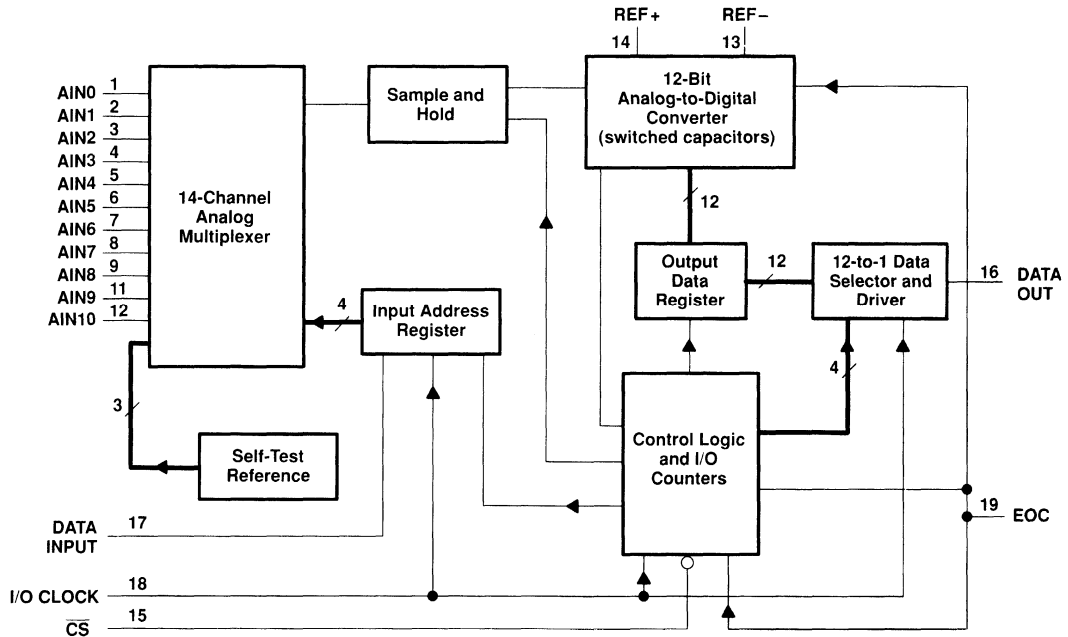
T _A	PACKAGE		
	SMALL OUTLINE		PLASTIC DIP
	DW†	DB†	N
0°C to 70°C	TLV2543CDW	TLV2543CDB	TLV2543CN
-40°C to 85°C	TLV2543IDW	—	TLV2543IN

† Available in tape and reel and ordered as the TLV2543CDWR, TLV2543CDBLE, or TLV2543IDWR.

TLV2543C, TLV2543I
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

functional block diagram



TLV2543C, TLV2543I
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS
SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AIN0 – AIN10	1–9, 11, 12	I	Analog input. These 11 analog-signal inputs are internally multiplexed. The driving source impedance should be less than or equal to 50 Ω for 4.1-MHz I/O CLOCK operation and capable of slewing the analog input voltage into a capacitance of 60 pF.
CS	15	I	Chip select. A high-to-low transition on CS resets the internal counters and controls and enables DATA OUT, DATA INPUT, and I/O CLOCK. A low-to-high transition disables DATA INPUT and I/O CLOCK within a setup time.
DATA INPUT	17	I	Serial-data input. A 4-bit serial address selects the desired analog input or test voltage to be converted. The serial data is presented with the MSB first and is shifted in on the first four rising edges of I/O CLOCK. After the four address bits are read into the address register, I/O CLOCK clocks the remaining bits in order.
DATA OUT	16	O	Serial data output. This is the 3-state serial output for the A/D conversion result. DATA OUT is in the high-impedance state when CS is high and active when CS is low. With a valid CS, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB/LSB value of the previous conversion result. The next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next MSB/LSB, and the remaining bits are shifted out in order.
EOC	19	O	End of conversion. EOC goes from a high to a low logic level after the falling edge of the last I/O CLOCK and remains low until the conversion is complete and data are ready for transfer.
GND	10		Ground. This is the ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	18	I	Input/output clock. I/O CLOCK receives the serial input and performs the following four functions: 1. It clocks the eight input data bits into the input data register on the first eight rising edges of I/O CLOCK with the multiplexer address available after the fourth rising edge. 2. On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplexer input begins charging the capacitor array and continues to do so until the last falling edge of I/O CLOCK. 3. It shifts the 11 remaining bits of the previous conversion data out on DATA OUT. Data changes on the falling edge of I/O CLOCK. 4. It transfers control of the conversion to the internal state controller on the falling edge of the last I/O CLOCK.
REF +	14	I	Reference +. The upper reference voltage value (nominally V_{CC}) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF– terminal.
REF –	13	I	Reference –. The lower reference voltage value (nominally ground) is applied to REF–.
VCC	20		Positive supply voltage.

detailed description

Initially, with chip select (\overline{CS}) high, I/O CLOCK and DATA INPUT are disabled and DATA OUT is in the high-impedance state. \overline{CS} , going low, begins the conversion sequence by enabling I/O CLOCK and DATA INPUT and removes DATA OUT from the high-impedance state.

The input data is an 8-bit data stream consisting of a 4-bit analog channel address (D7–D4), a 2-bit data length select (D3–D2), an output MSB or LSB first bit (D1), and a unipolar or bipolar output select bit (D0) that are applied to DATA INPUT. The I/O CLOCK sequence applied to the I/O CLOCK terminal transfers this data to the input data register.

During this transfer, the I/O CLOCK sequence also shifts the previous conversion result from the output data register to DATA OUT. I/O CLOCK receives the input sequence of 8, 12, or 16 clocks long depending on the data-length selection in the input data register. Sampling of the analog input begins on the fourth falling edge of the input I/O CLOCK sequence and is held after the last falling edge of the I/O CLOCK sequence. The last falling edge of the I/O CLOCK sequence also takes EOC low and begins the conversion.



TLV2543C, TLV2543I
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS
 SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

converter operation

The operation of the converter is organized as a succession of two distinct cycles: 1) the I/O cycle, and 2) the actual conversion cycle. The I/O cycle is defined by the externally provided I/O CLOCK and lasts 8, 12, or 16 clock periods depending on the selected output data length.

1. I/O cycle

During the I/O cycle, two operations take place simultaneously.

- a. An 8-bit data stream consisting of address and control information is provided to DATA INPUT. This data is shifted into the device on the rising edge of the first eight I/O CLOCKS. DATA INPUT is ignored after the first eight clocks during 12- or 16-clock I/O transfers.
- b. The data output with a length of 8, 12, or 16 bits is provided serially on DATA OUT. When \overline{CS} is held low, the first output data bit occurs on the rising edge of \overline{EOC} . When \overline{CS} is negated between conversions, the first output data bit occurs on the falling edge of \overline{CS} . This data is the result of the previous conversion period, and after the first output data bit each succeeding bit is clocked out on the falling edge of each succeeding I/O CLOCK.

2. Conversion cycle

The conversion cycle is transparent to the user, and it is controlled by an internal clock synchronized to the I/O CLOCK. During the conversion period, the device performs a successive-approximation conversion on the analog input voltage. The EOC output goes low at the start of the conversion cycle and goes high when conversion is complete and the output data register is latched. A conversion cycle is started only after the I/O cycle is completed, which minimizes the influence of external digital noise on the accuracy of the conversion.

power up and initialization

After power up, \overline{CS} must be taken from high to low to begin an I/O cycle. EOC is initially high, and the input data register is set to all zeros. The contents of the output data register are random, and the first conversion result should be ignored. To initialize during operation, \overline{CS} is taken high and returned low to begin the next I/O cycle. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

operational terminology

Previous (N-1) conversion cycle	The conversion cycle prior to the current I/O cycle.
Current (N) I/O cycle	The entire I/O CLOCK sequence that transfers address and control data into the data register and clocks the digital result from the previous conversion cycle from DATA OUT. The last falling edge of the clock in the I/O CLOCK sequence signifies the end of the current I/O cycle.
Current (N) conversion cycle	Immediately after the current I/O cycle, the current conversion cycle starts. When the current conversion cycle is complete, the current conversion result is loaded into the output register.
Current (N) conversion result	The result of the current conversion cycle that is serially shifted out during the next I/O cycle.
Next (N+1) I/O cycle	The I/O cycle after the current conversion cycle.

Example: In the 12-bit mode, the result of the current conversion cycle is a 12-bit serial-data stream clocked out during the next I/O cycle. The current I/O cycle must be exactly 12 bits long to maintain synchronization, even when this corrupts the output data from the previous conversion. The current conversion begins immediately after the twelfth falling edge of the current I/O cycle.

data input

The data input is internally connected to an 8-bit serial-input address and control register. The register defines the operation of the converter and the output data length. The host provides the data word with the MSB first. Each data bit is clocked in on the rising edge of the I/O CLOCK sequence (see Table 1 for the data register format).

data input (continued)

Table 1. Input-Register Format

FUNCTION SELECT	INPUT DATA BYTE							
	ADDRESS BITS				L1	L0	LSBF	BIP
	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
Select input channel								
AIN0 _____	0	0	0	0				
AIN1 _____	0	0	0	1				
AIN2 _____	0	0	1	0				
AIN3 _____	0	0	1	1				
AIN4 _____	0	1	0	0				
AIN5 _____	0	1	0	1				
AIN6 _____	0	1	1	0				
AIN7 _____	0	1	1	1				
AIN8 _____	1	0	0	0				
AIN9 _____	1	0	0	1				
AIN10 _____	1	0	1	0				
Select test voltage								
$(V_{ref+} - V_{ref-})/2$ _____	1	0	1	1				
V_{ref-} _____	1	1	0	0				
V_{ref+} _____	1	1	0	1				
Software power down _____	1	1	1	0				
Output data length								
8 bits _____					0	1		
12 bits _____					X	0		
16 bits _____					1	1		
Output data format								
MSB first _____							0	
LSB first _____							1	
Unipolar (binary) _____								0
Bipolar (BIP, 2s complement) _____								1

data input address bits

The four MSBs (D7 – D4) of the data register address one of the 11 input channels, a reference-test voltage, or the power-down mode. The address bits affect the current conversion, which is the conversion that immediately follows the current I/O cycle. The reference voltage is nominally equal to $V_{ref+} - V_{ref-}$.

data output length

The next two bits (D3 and D2) of the data register select the output data length. The data-length selection is valid for the current I/O cycle (the cycle in which the data is read). The data-length selection, which is valid for the current I/O cycle, allows device start-up without losing I/O synchronization. A data length of 8, 12, or 16 bits can be selected. Since the converter has 12-bit resolution, a data length of 12 bits is suggested.

With D3 and D2 set to 00 or 10, the device is in the 12-bit data-length mode and the result of the current conversion is output as a 12-bit serial-data stream during the next I/O cycle. The current I/O cycle must be exactly 12 bits long for proper synchronization, even when this means corrupting the output data from a previous conversion. The current conversion is started immediately after the twelfth falling edge of the current I/O cycle.

With bits D3 and D2 set to 11, the 16-bit data-length mode is selected, which allows convenient communication with 16-bit serial interfaces. In the 16-bit mode, the result of the current conversion is output as a 16-bit serial-data stream during the next I/O cycle with the four LSBs always set to 0 (pad bits). The current I/O cycle must be exactly 16 bits long to maintain synchronization even when this means corrupting the output data from the previous conversion. The current conversion is started immediately after the sixteenth falling edge of the current I/O cycle.

TLV2543C, TLV2543I

12-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

data output length (continued)

With bits D3 and D2 set to 01, the 8-bit data-length mode is selected, which allows fast communication with 8-bit serial interfaces. In the 8-bit mode, the result of the current conversion is output as an 8-bit serial-data stream during the next I/O cycle. The current I/O cycle must be exactly 8 bits long to maintain synchronization, even when this means corrupting the output data from the previous conversion. The four LSBs of the conversion result are truncated and discarded. The current conversion is immediately started after the eighth falling edge of the current I/O cycle.

Since D3 and D2 take effect on the current I/O cycle when the data length is programmed, there can be a conflict with the previous cycle when the data-word length is changed from one cycle to the next. This may occur when the data format is selected to be least significant bit first, since at the time the data length change becomes effective (six rising edges of I/O CLOCK), the previous conversion result has already started shifting out.

In actual operation, when different data lengths are required within an application and the data length is changed between two conversions, no more than one conversion result can be corrupted and only when it is shifted out in LSB first format.

sampling period

During the sampling period, one of the analog inputs is internally connected to the capacitor array of the converter to store the analog input signal. The converter starts sampling the selected input immediately after the four address bits have been clocked into the input data register. Sampling starts on the fourth falling edge of I/O CLOCK. The converter remains in the sampling mode until the eighth, twelfth, or sixteenth falling edge of the I/O CLOCK depending on the data-length selection. After the EOC delay time from the last I/O CLOCK falling edge, the EOC output goes low indicating that the sampling period is over and the conversion period has begun. After EOC goes low, the analog input can be changed without affecting the conversion result. Since the delay from the falling edge of the last I/O CLOCK to EOC low is fixed, time-varying analog input signals can be digitized at a fixed rate without introducing systematic harmonic distortion or noise due to timing uncertainty.

After the 8-bit data stream has been clocked in, DATA INPUT should be held at a fixed digital level until EOC goes high (indicating that the conversion is complete) to maximize the sampling accuracy and minimize the influence of external digital noise.

data register, LSB first

D1 in the input data register (LSB first) controls the direction of the output binary data transfer. When D1 is set to 0, the conversion result shifts out MSB first. When set to 1, the data shifts out LSB first. Selection of MSB first or LSB first always affects the next I/O cycle and not the current I/O cycle. When changing from one data direction to another, the current I/O cycle is never disrupted.

data register, bipolar format

D0 in the input data register controls the binary data format used to represent the conversion result. When D0 is set to 0, the conversion result is represented as unipolar (unsigned binary) data. Nominally, the conversion result of an input voltage equal to V_{ref-} is a code of all zeros (000 . . . 0), the conversion result of an input voltage equal to V_{ref+} is a code of all ones (111 . . . 1), and the conversion result of $(V_{ref+} + V_{ref-})/2$ is a code of a one followed by zeros (100 . . . 0).

When D0 is set to 1, the conversion result is represented as bipolar data (signed binary). Nominally, conversion of an input voltage equal to V_{ref-} is a code of a 1 followed by zeros (100 . . . 0), conversion of an input voltage equal to V_{ref+} is a code of a 0 followed by all ones (011 . . . 1), and the conversion of $(V_{ref+} + V_{ref-})/2$ is a code of all zeros (000 . . . 0). The MSB is interpreted as the sign bit. The bipolar data format is related to the unipolar format in that the MSBs are always each other's complement.

Selection of the unipolar or bipolar format always affects the current conversion cycle, and the result is output during the next I/O cycle. When changing between unipolar and bipolar formats, the data output during the current I/O cycle is not affected.



TLV2543C, TLV2543I
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

EOC output

The EOC signal indicates the beginning and the end of conversion. In the reset state, EOC is always high. During the sampling period (beginning after the fourth falling edge of the I/O CLOCK sequence), EOC remains high until the internal sampling switch of the converter is safely opened. The opening of the sampling switch occurs after the eighth, twelfth, or sixteenth I/O CLOCK falling edge, depending on the data-length selection in the input data register. After the EOC signal goes low, the analog input signal can be changed without affecting the conversion result.

The EOC signal goes high again after the conversion completes and the conversion result is latched into the output data register. The rising edge of EOC returns the converter to a reset state and a new I/O cycle begins. On the rising edge of EOC, the first bit of the current conversion result is on DATA OUT when \overline{CS} is low. When \overline{CS} is negated between conversions, the first bit of the current conversion result occurs at DATA OUT on the falling edge of \overline{CS} .

data format and pad bits

D3 and D2 of the input data register determine the number of significant bits in the digital output that represent the conversion result. The LSB-first bit determines the direction of the data transfer while the BIP bit determines the arithmetic conversion. The numerical data is always justified toward the MSB in any output format.

The internal conversion result is always 12 bits long. When an 8-bit data transfer is selected, the four LSBs of the internal result are discarded to provide a faster one-byte transfer. When a 12-bit transfer is used, all bits are transferred. When a 16-bit transfer is used, four LSB pad bits are always appended to the internal conversion result. In the LSB-first mode, four leading zeros are output. In the MSB-first mode, the last four bits output are zeros.

When \overline{CS} is held low continuously, the first data bit of the just completed conversion occurs on DATA OUT on the rising edge of EOC. When a new conversion is started after the last falling edge of I/O CLOCK, EOC goes low and the serial output is forced to a logic zero until EOC goes high again.

When \overline{CS} is negated between conversions, the first data bit occurs on DATA OUT on the falling edge of \overline{CS} . On each subsequent falling edge of I/O CLOCK after the first data bit appears, the data is changed to the next bit in the serial conversion result until the required number of bits has been output.

chip-select input (\overline{CS})

The chip-select input (\overline{CS}) enables and disables the device. During normal operation, \overline{CS} should be low. Although the use of \overline{CS} is not necessary to synchronize a data transfer, it can be brought high between conversions to coordinate the data transfer of several devices sharing the same bus.

When \overline{CS} is brought high, the serial-data output is immediately brought to the high-impedance state, releasing its output data line to other devices that may share it. After an internally generated debounce time, the I/O CLOCK is inhibited, thus preventing any further change in the internal state.

When \overline{CS} is subsequently brought low again, the device is reset. \overline{CS} must be held low for an internal debounce time before the reset operation takes effect. After \overline{CS} is debounced low, I/O CLOCK must remain inactive (low) for a minimum time before a new I/O cycle can start.

\overline{CS} can be used to interrupt any ongoing data transfer or any ongoing conversion. When \overline{CS} is debounced low long enough before the end of the current conversion cycle, the previous conversion result is saved in the internal output buffer and then shifted out during the next I/O cycle.



TLV2543C, TLV2543I

12-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

power-down features

When a binary address of 1110 is clocked into the input data register during the first four I/O CLOCK cycles, the power-down mode is selected. Power down is activated on the falling edge of the fourth I/O CLOCK pulse.

During power down, all internal circuitry is put in a low-current standby mode. No conversions are performed, and the internal output buffer keeps the previous conversion cycle data results, provided that all digital inputs are held above $V_{CC} - 0.3$ V or below 0.3 V. The I/O logic remains active so the current I/O cycle must be completed even when the power-down mode is selected. Upon power-on reset and before the first I/O cycle, the converter normally begins in the power-down mode. The device remains in the power-down mode until a valid (other than 1110) input address clocks in. Upon completion of that I/O cycle, a normal conversion is performed with the results being shifted out during the next I/O cycle.

analog input, test, and power-down mode

The 11 analog inputs, three internal voltages, and power-down mode are selected by the input multiplexer according to the input addresses shown in Tables 2, 3, and 4. The input multiplexer is a break-before-make type to reduce input-to-input noise rejection resulting from channel switching. Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK and continues for the remaining I/O CLOCK pulses. The sample is held on the falling edge of the last I/O CLOCK pulse. The three internal test inputs are applied to the multiplexer, sampled, and converted in the same manner as the external analog inputs. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

Table 2. Analog-Channel-Select Address

ANALOG INPUT SELECTED	VALUE SHIFTED INTO DATA INPUT	
	BINARY	HEX
AIN0	0000	0
AIN1	0001	1
AIN2	0010	2
AIN3	0011	3
AIN4	0100	4
AIN5	0101	5
AIN6	0110	6
AIN7	0111	7
AIN8	1000	8
AIN9	1001	9
AIN10	1010	A

Table 3. Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED†	VALUE SHIFTED INTO DATA INPUT		UNIPOLAR OUTPUT RESULT (HEX)‡
	BINARY	HEX	
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	B	200
V_{ref-}	1100	C	000
V_{ref+}	1101	D	3FF

† V_{ref+} is the voltage applied to REF+, and V_{ref-} is the voltage applied to REF-.

‡ The output results shown are the ideal values and may vary with the reference stability and with internal offsets.



analog input, test, and power-down mode (continued)

Table 4. Power-Down-Select Address

INPUT COMMAND	VALUE SHIFTED INTO DATA INPUT		RESULT
	BINARY	HEX	
Power down	1110	E	$I_{CC} \leq 25 \mu A$

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF-) voltage. In the switching sequence, 12 capacitors are examined separately until all 12 bits are identified and the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 4096). Node 4096 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF-. When the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a bit 0 is placed in the output register and the 4096-weight capacitor is switched to REF-. When the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and the 4096-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 2048-weight capacitor, the 1024-weight capacitor, and so forth down the line until all bits are determined. With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.

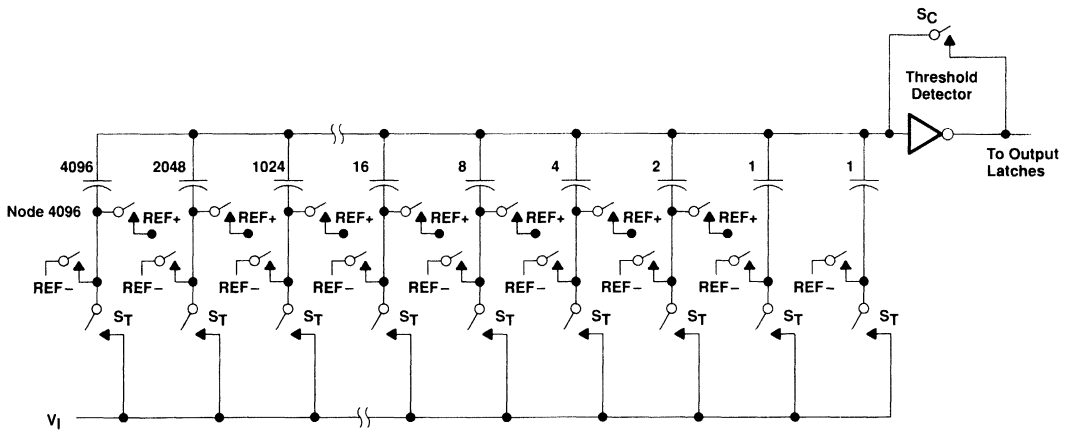


Figure 1. Simplified Model of the Successive-Approximation System

TLV2543C, TLV2543I
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS
 SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

reference voltage inputs

There are two reference voltage inputs on the device, REF+ and REF-. The voltage values on these terminals establish the upper and lower limits of the analog input to produce a full-scale and zero-scale reading respectively. These voltages and the analog input should not exceed the positive supply or be lower than ground consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ terminal voltage and at zero when the input signal is equal to or lower than REF- terminal voltage.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	-0.5 V to 6.5 V
Input voltage range, V_I (any input)	-0.3 V to $V_{CC} + 0.3$ V
Output voltage range, V_O	-0.3 V to $V_{CC} + 0.3$ V
Positive reference voltage, V_{ref+}	$V_{CC} + 0.1$ V
Negative reference voltage, V_{ref-}	-0.1 V
Peak input current, I_I (any input)	± 20 mA
Peak total input current (all inputs)	± 30 mA
Operating free-air temperature range, T_A :	TLV2543C	0°C to 70°C
	TLV2543I	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from the case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminal with REF- and GND wired together (unless otherwise noted).



TLV2543C, TLV2543I
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS
SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Positive reference voltage, V_{ref+} (see Note 2)		V_{CC}			V
Negative reference voltage, V_{ref-} (see Note 2)		0			V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)		2.5	V_{CC}	$V_{CC} + 0.1$	V
Analog input voltage (see Note 2)		0			V_{CC}
High-level control input voltage, V_{IH}	$V_{CC} = 3\text{ V to }3.6\text{ V}$	2.1			V
Low-level control input voltage, V_{IL}	$V_{CC} = 3\text{ V to }3.6\text{ V}$	0.6			V
Clock frequency at I/O CLOCK		0	3	4.1	MHz
Setup time, address bits at DATA INPUT before I/O CLOCK \uparrow , $t_{su}(A)$ (see Figure 5)		100			ns
Hold time, address bits at DATA INPUT after I/O CLOCK \uparrow , $t_h(A)$ (see Figure 5)		0			ns
Hold time, \overline{CS} low after last I/O CLOCK \downarrow , $t_h(\overline{CS})$ (see Figure 6)		0			ns
Setup time, \overline{CS} low before clocking in first address bit, $t_{su}(\overline{CS})$ (see Note 3 and Figure 6)		1.425			μs
Pulse duration, I/O CLOCK high, $t_{wH}(I/O)$		190			ns
Pulse duration, I/O CLOCK low, $t_{wL}(I/O)$		190			ns
Transition time, I/O CLOCK, $t_t(I/O)$ (see Note 4 and Figure 7)		1			μs
Transition time, DATA INPUT and \overline{CS} , $t_t(\overline{CS})$		10			μs
Operating free-air temperature, T_A	TLV2543C	0			°C
	TLV2543I	-40			
		70			
		85			

- NOTES: 2. Analog input voltages greater than the voltage applied to REF+ convert as all ones (111111111111), while input voltages less than the voltage applied to REF- convert as all zeros (000000000000).
3. To minimize errors caused by noise at the \overline{CS} input, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in an address until the minimum \overline{CS} setup time elapses.
4. This is the time required for the clock input signal to fall from V_{IHmin} to V_{ILmax} or to rise from V_{ILmax} to V_{IHmin} . In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 μs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

TLV2543C, TLV2543I
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 3\text{ V to }3.6\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage	V _{CC} = 3 V, I _{OH} = -0.2 mA	2.4			V
		V _{CC} = 3 V to 3.6 V, I _{OH} = -20 μA		V _{CC} -0.1		
V _{OL}	Low-level output voltage	V _{CC} = 3 V, I _{OL} = 0.8 mA			0.4	V
		V _{CC} = 3 V to 3.6 V, I _{OL} = 20 μA		0.1		
I _{OZ}	Off-state (high-impedance-state) output current	V _O = V _{CC} , CS at V _{CC}		1	2.5	μA
		V _O = 0, CS at V _{CC}		1	-2.5	
I _{IH}	High-level input current	V _I = V _{CC}		1	2.5	μA
I _{IL}	Low-level input current	V _I = 0		1	-2.5	μA
I _{CC}	Operating supply current	CS at 0 V		1	2.5	mA
I _{CC(PD)}	Power-down current	For all digital inputs, 0 ≤ V _I ≤ 0.3 V or V _I ≥ V _{CC} - 0.3 V		4	25	μA
I _{lkg}	Selected channel leakage current	Selected channel at V _{CC} , Unselected channel at 0 V			1	μA
		Selected channel at 0 V, Unselected channel at V _{CC}			-1	
	Maximum static analog reference current into REF+	V _{ref+} = V _{CC} , V _{ref-} = GND		1	2.5	μA
C _i	Input capacitance	Analog inputs		30	60	pF
		Control inputs		5	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.



TLV2543C, TLV2543I
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

**operating characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 3\text{ V to }3.6\text{ V}$, I/O CLOCK frequency = 4.1 MHz, (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error (see Note 6)	See Figure 2			± 1	LSB
E_D	Differential linearity error	See Figure 2			± 1	LSB
E_O	Offset error (see Note 7)	See Note 2 and Figure 2			± 1.5	LSB
E_G	Gain error (see Note 7)	See Note 2 and Figure 2			± 1	LSB
E_T	Total unadjusted error (see Note 8)				± 1.75	LSB
	Self-test output code (see Table 3 and Note 9)	DATA INPUT = 1011	2038	2048	2058	
		DATA INPUT = 1100		0	10	
		DATA INPUT = 1101	4075	4095		
t_{conv}	Conversion time	See Figures 10–15		8	10	µs
t_c	Total cycle time (access, sample, and conversion)	See Figures 10–15 and Note 10			10 + total I/O CLOCK periods + $t_d(I/O\text{-}EOC)$	µs
t_{acq}	Channel acquisition time (sample)	See Figures 10–15 and Note 10	4		12	I/O CLOCK periods
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 7	10			ns
$t_d(I/O\text{-}DATA)$	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 7			250	ns
$t_d(I/O\text{-}EOC)$	Delay time, last I/O CLOCK↓ to EOC↓	See Figure 8		1.5	2.2	µs
$t_d(EOC\text{-}DATA)$	Delay time, EOC↑ to DATA OUT (MSB/LSB)	See Figure 9			200	ns
t_{PZH}, t_{PZL}	Enable time, \overline{CS} ↓ to DATA OUT (MSB/LSB driven)	See Figure 4		0.7	1.3	µs
t_{PHZ}, t_{PLZ}	Disable time, \overline{CS} ↑ to DATA OUT (high impedance)	See Figure 4		70	150	ns
$t_r(EOC)$	Rise time, EOC	See Figure 9		15	50	ns
$t_f(EOC)$	Fall time, EOC	See Figure 8		15	50	ns
$t_r(\text{bus})$	Rise time, data bus	See Figure 7		15	50	ns
$t_f(\text{bus})$	Fall time, data bus	See Figure 7		15	50	ns
$t_d(I/O\text{-}CS)$	Delay time, last I/O CLOCK↓ to \overline{CS} ↓ to abort conversion (see Note 11)				5	µs

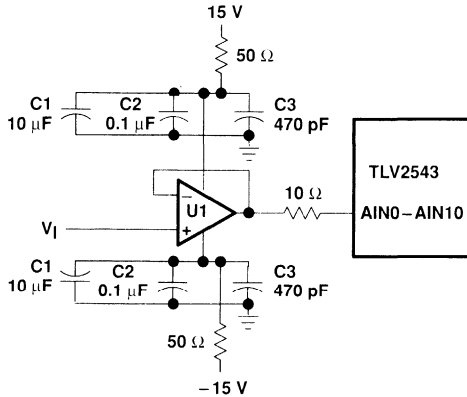
† All typical values are at $T_A = 25^\circ\text{C}$.

- NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (11111111111), while input voltages less than that applied to REF– convert as all zeros (00000000000).
6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Gain error is the difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. Offset error is the difference between the actual midstep value and the nominal midstep value at the offset point.
8. Total unadjusted error comprises linearity, zero-scale, and full-scale errors.
9. Both the input address and the output codes are expressed in positive logic.
10. I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 7).
11. Any transitions of \overline{CS} are recognized as valid only when the level is maintained for a setup time. \overline{CS} must be taken low at $\leq 5\ \mu\text{s}$ of the tenth I/O CLOCK falling edge to ensure that a conversion is aborted. Between 5 µs and 10 µs, the result is uncertain as to whether the conversion is aborted or the conversion results are valid.



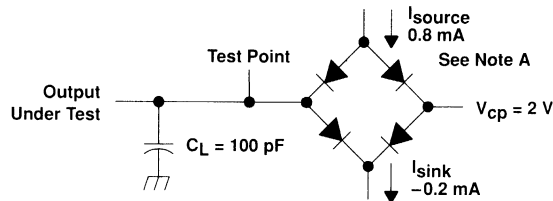
TLV2543C, TLV2543I
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS
 SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

PARAMETER MEASUREMENT INFORMATION



LOCATION	DESCRIPTION	PART NUMBER
U1	OP27	—
C1	10- μ F 35-V tantalum capacitor	—
C2	0.1- μ F ceramic NPO SMD capacitor	AVX 12105C104KA105 or equivalent
C3	470-pF porcelain high-Q SMD capacitor	Johanson 201S420471JG4L or equivalent

Figure 2. Analog Input Buffer to Analog Inputs AIN0–AIN10



NOTE A: Equivalent load circuit of the Teradyne A580 tester for timing parameter measurement.

Figure 3. Timing Load Circuits

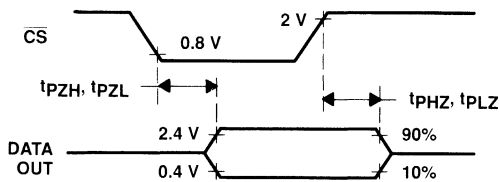


Figure 4. DATA OUT to Hi-Z Voltage Waveforms

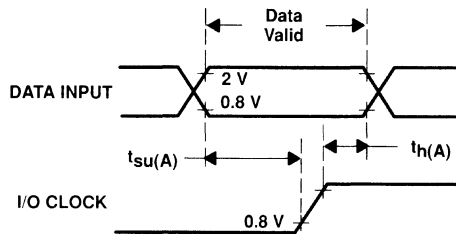


Figure 5. DATA INPUT and I/O CLOCK Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

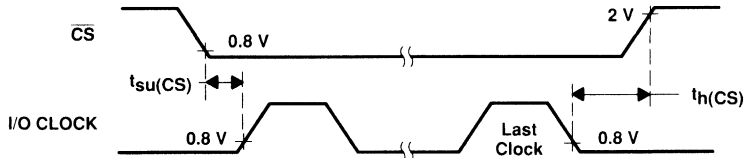


Figure 6. \overline{CS} and I/O CLOCK Voltage Waveforms†

† To ensure full conversion accuracy, it is recommended that no input signal change occurs while a conversion is ongoing.

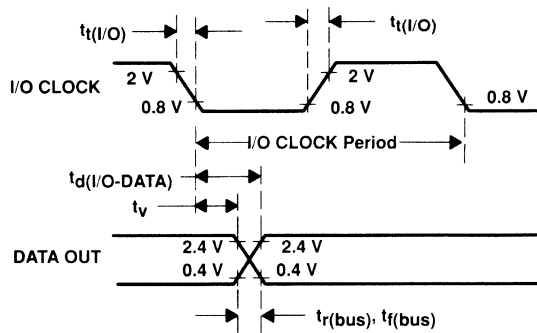


Figure 7. I/O CLOCK and DATA OUT Voltage Waveforms

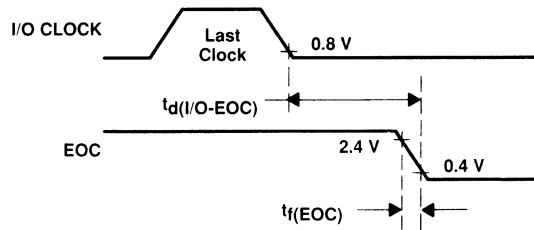


Figure 8. I/O CLOCK and EOC Voltage Waveforms

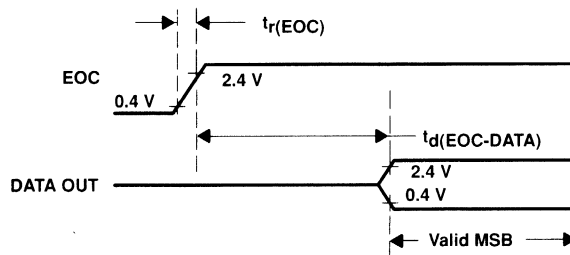


Figure 9. EOC and DATA OUT Voltage Waveforms

TLV2543C, TLV2543I
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS
 SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

PARAMETER MEASUREMENT INFORMATION

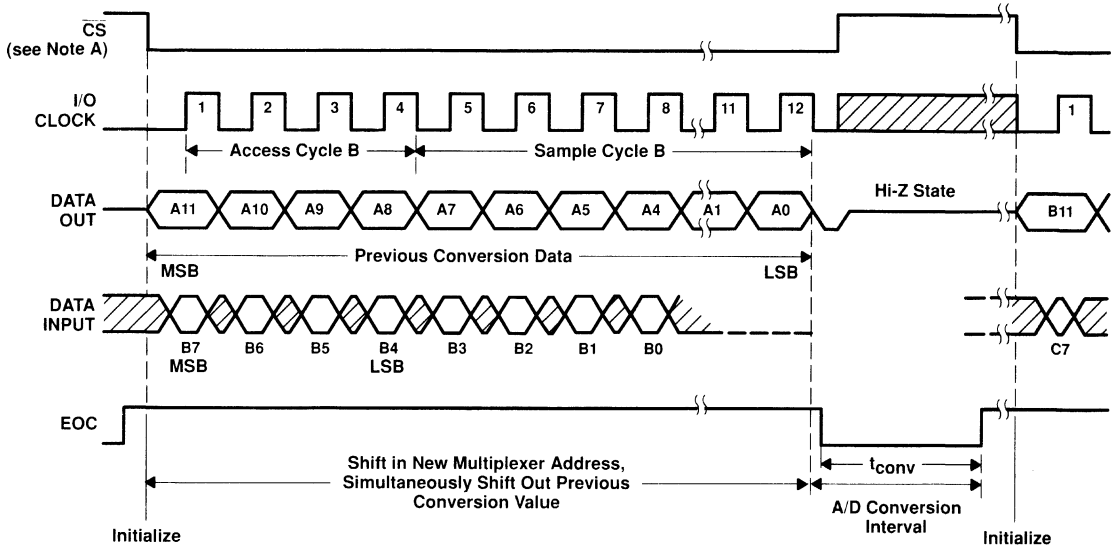


Figure 10. Timing for 12-Clock Transfer Using \overline{CS} With MSB First

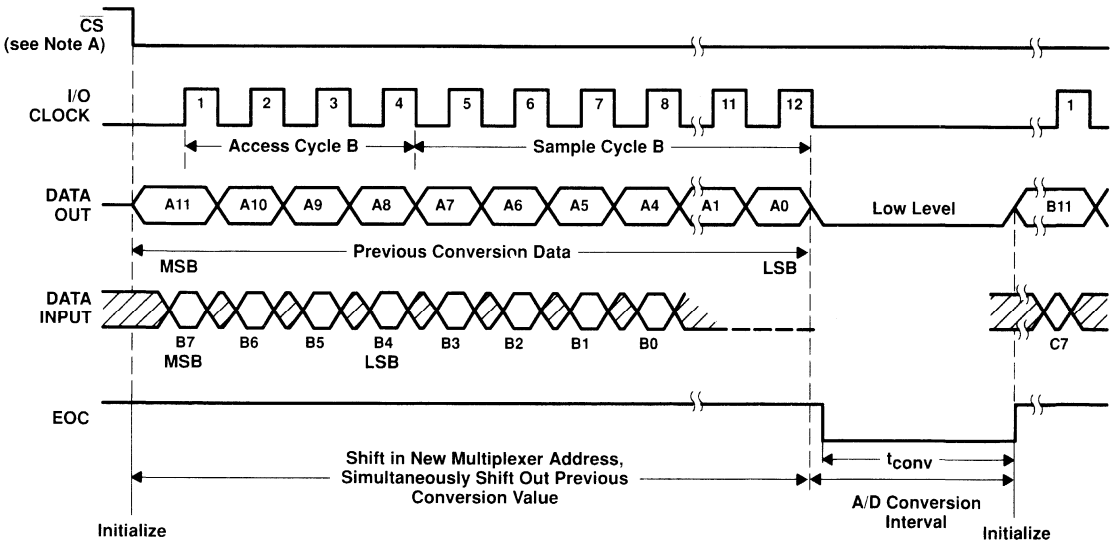


Figure 11. Timing for 12-Clock Transfer Not Using \overline{CS} With MSB First

NOTE A: To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time after \overline{CS} before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.



TLV2543C, TLV2543I
**12-BIT ANALOG-TO-DIGITAL CONVERTERS
 WITH SERIAL CONTROL AND 11 ANALOG INPUTS**
 SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

PARAMETER MEASUREMENT INFORMATION

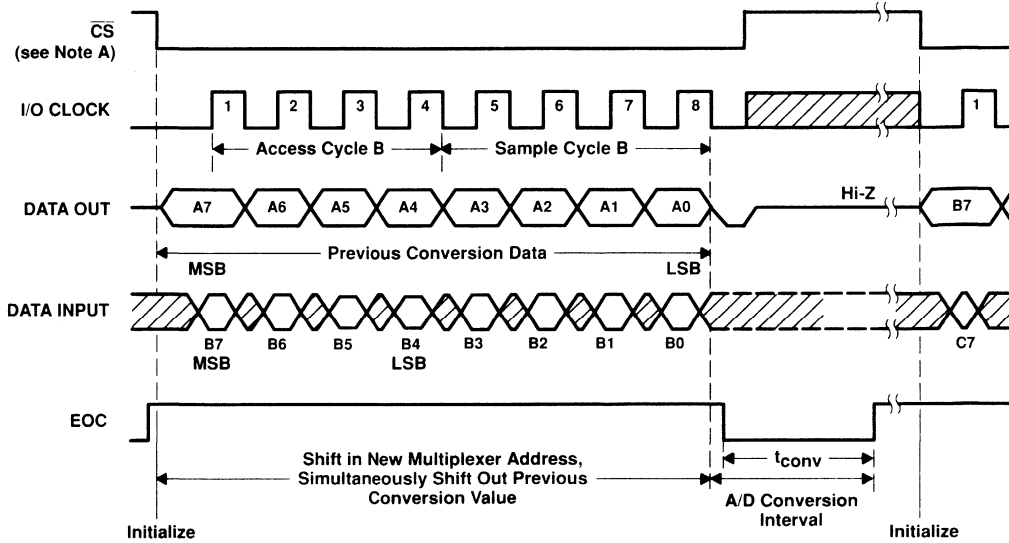


Figure 12. Timing for 8-Clock Transfer Using \overline{CS} With MSB First

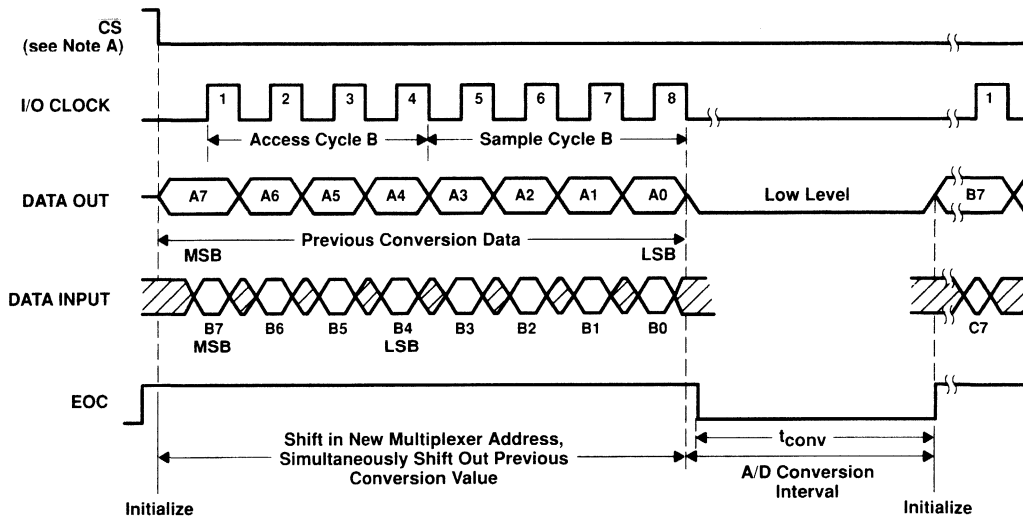


Figure 13. Timing for 8-Clock Transfer Not Using \overline{CS} With MSB First

NOTE A: To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.

TLV2543C, TLV2543I
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

PARAMETER MEASUREMENT INFORMATION

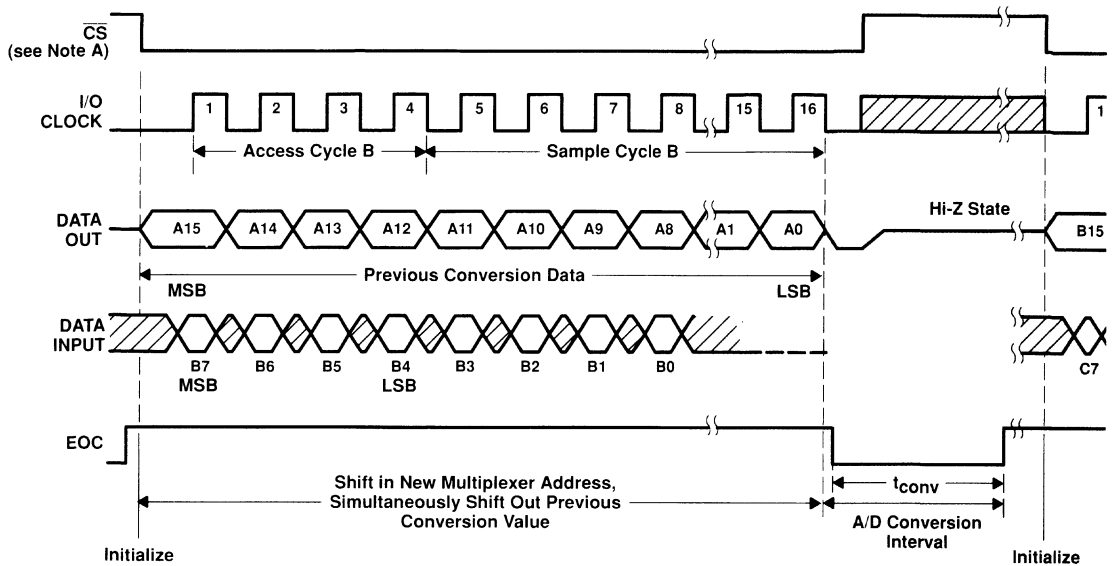


Figure 14. Timing for 16-Clock Transfer Using \overline{CS} With MSB First

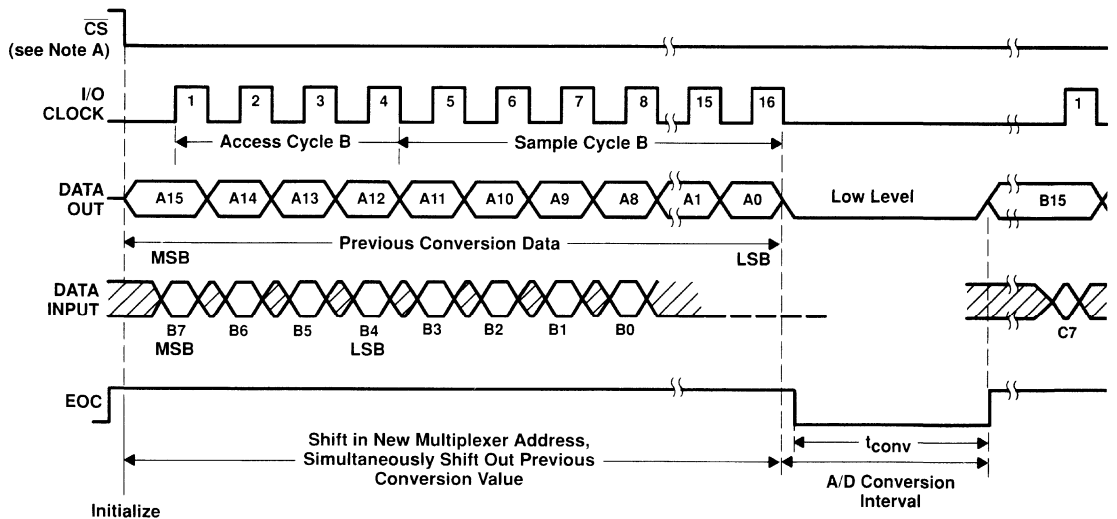
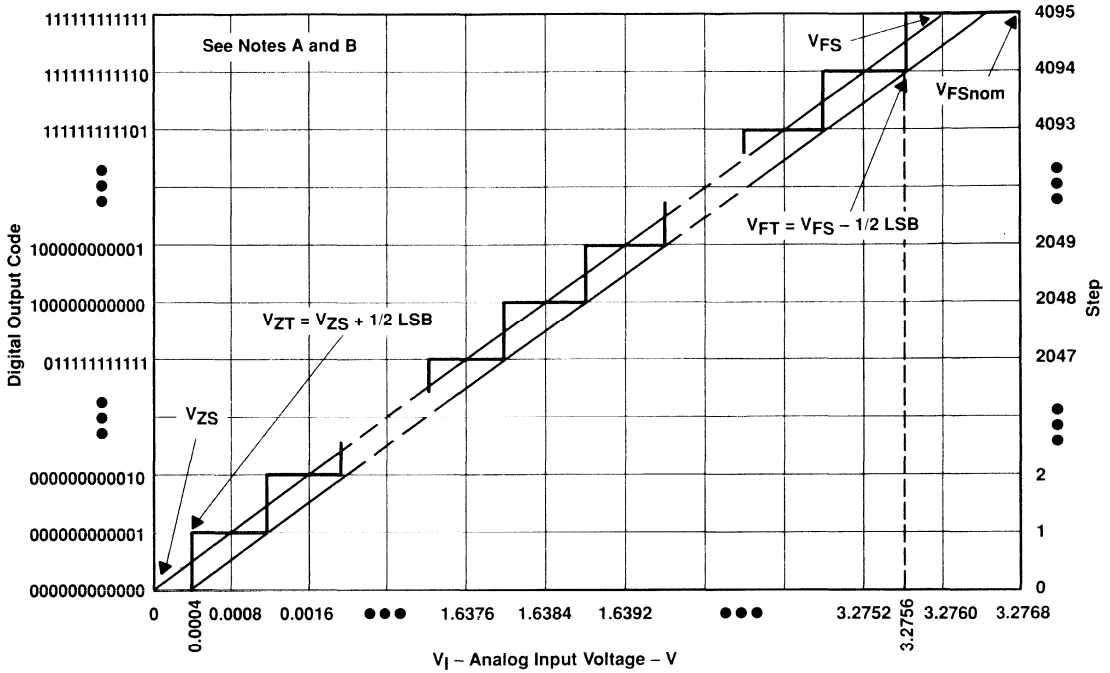


Figure 15. Timing for 16-Clock Transfer Not Using \overline{CS} With MSB First

NOTE A: To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time after \overline{CS} ↓ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.

TLV2543C, TLV2543I
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS
SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

APPLICATION INFORMATION



- NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0004 V and the transition to full scale (V_{FT}) is 3.2756 V. 1 LSB = 0.8 mV.
- B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 16. Ideal Conversion Characteristics

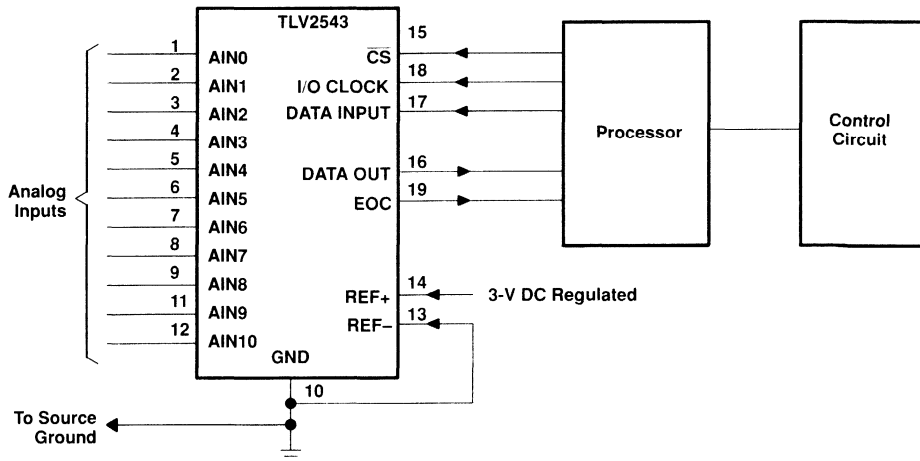


Figure 17. Serial Interface

TLV2543C, TLV2543I
12-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL AND 11 ANALOG INPUTS

SLAS096B – MARCH 1995 – REVISED OCTOBER 1995

APPLICATIONS INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 18, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c / R_t C_i} \right) \quad (1)$$

where

$$R_t = R_S + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S / 8192) \quad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S / 8192) = V_S \left(1 - e^{-t_c / R_t C_i} \right) \quad (3)$$

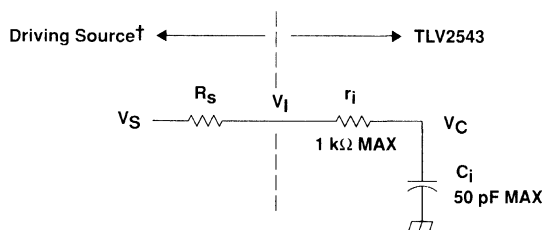
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(8192) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_S + 1 \text{ k}\Omega) \times 60 \text{ pF} \times \ln(8192) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at AIN
 V_S = External Driving Source Voltage
 R_S = Source Resistance
 r_i = Input Resistance
 C_i = Input Capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 18. Equivalent Input Circuit Including the Driving Source

TLV5510

3-V 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS124 – DECEMBER 1997

- **8-Bit Resolution**
- **Linearity Error**
 - ±0.75 LSB Max (25°C)
 - ±1 LSB Max (-20°C to 75°C)
- **Differential Linearity Error**
 - ± 0.5 LSB (25°C)
 - ±0.75 LSB Max (-20°C to 75°C)
- **Maximum Conversion Rate**
10 Mega-Samples per Second (MSPS) Min
- **3-V Single-Supply Operation**
- **Low Power Consumption . . . 40 mW Typ**
- **Low Voltage Replacement for CXD1175**

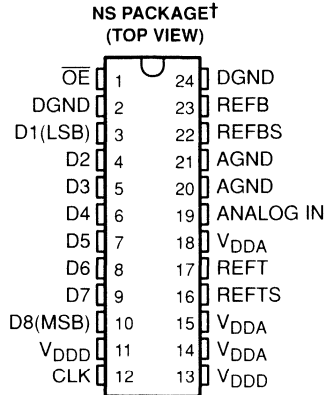
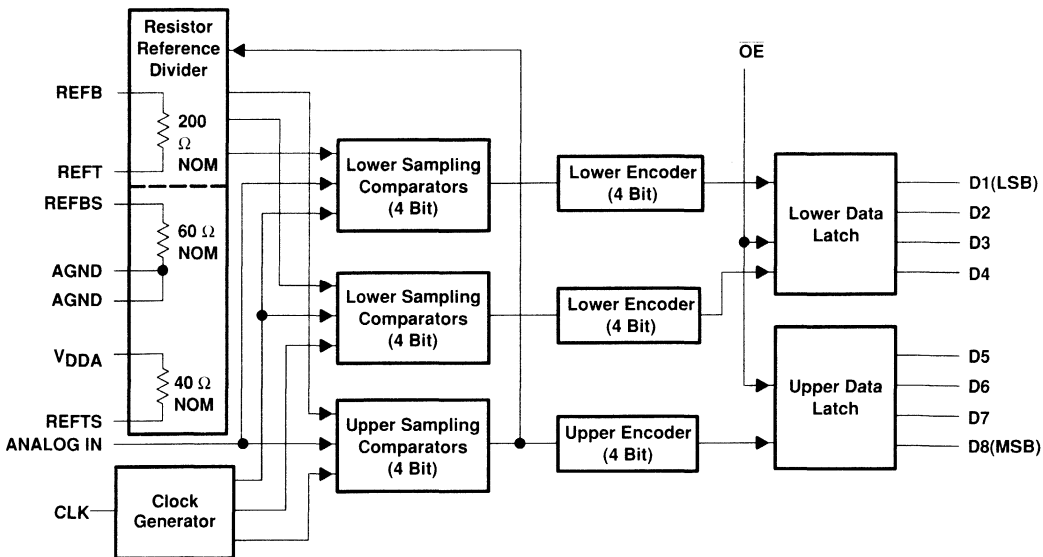
Applications

- **Communications**
- **Digital Imaging**
- **Video Conferencing**
- **High-Speed Data Conversion**

description

The TLV5510 is a CMOS 8-bit resolution semiflash analog-to-digital converter (ADC) with a 2.7-V to 3.6-V single power supply and an internal reference voltage source. It converts a wide band analog signal (such as a video signal) to a digital signal at a sampling rate of dc to 10 MHz.

functional block diagram



† Available in tape and reel only and ordered as the TLV5510INSLE.

AVAILABLE OPTIONS

T _A	NS PACKAGE (TAPE AND REEL ONLY)
-20°C to 75°C	TLV5510INSLE

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

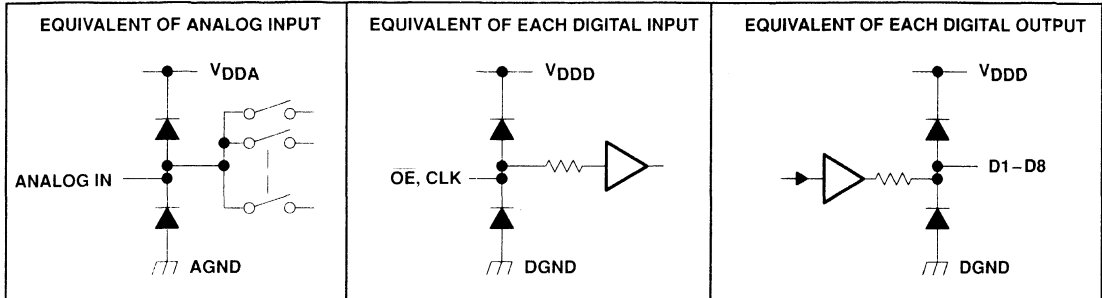


TLV5510

3-V 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS124 – DECEMBER 1997

schematics of inputs and outputs



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	20, 21		Analog ground
ANALOG IN	19	I	Analog input
CLK	12	I	Clock in
DGND	2, 24		Digital ground
D1-D8	3-10	O	Digital data out. D1:LSB, D8:MSB
\overline{OE}	1	I	Output enable. When $\overline{OE} = L$, data is enabled. When $\overline{OE} = H$, D1 - D8 is high impedance.
V_{DDA}	14, 15, 18		Analog supply voltage
V_{DDD}	11, 13		Digital supply voltage
REFB	23	I	Reference voltage in (bottom)
REFBS	22		Reference voltage (bottom). When using the internal voltage divider to generate a nominal 2-V reference, this terminal is shorted to the REFB terminal and the REFTS terminal is shorted to the REFT terminal (see Figure 3).
REFT	17	I	Reference voltage in (top)
REFTS	16		Reference voltage (top). When using the internal voltage divider to generate a nominal 2-V reference, this terminal is shorted to the REFT terminal and the REFB terminal is shorted to the REFB terminal (see Figure 3).

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DDA} , V_{DDD}	7 V
Reference voltage input range, $V_{ref(T)}$, $V_{ref(B)}$, $V_{ref(BS)}$, $V_{ref(TS)}$	AGND to V_{DDA}
Analog input voltage range, $V_{I(ANLG)}$	AGND to V_{DDA}
Digital input voltage range, $V_{I(DGTL)}$	DGND to V_{DDD}
Digital output voltage range, $V_{O(DGTL)}$	DGND to V_{DDD}
Operating free-air temperature range, T_A	-20°C to 75°C
Storage temperature range, T_{stg}	-55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

TLV5510

3-V 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS124 – DECEMBER 1997

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V _{DDA} –AGND	2.7	3.3	3.6	V
	V _{DDD} –DGND	2.7	3.3	3.6	
	AGND–DGND	–100	0	100	mV
Reference input voltage (top), V _{ref(T)}		V _{ref(B)} +2	V _{ref(B)} +2	V _{CC} –0.3	V
Reference input voltage (bottom), V _{ref(B)}		0	0.6	V _{ref(T)} –2	V
Analog input voltage range, V _{I(ANLG)} (see Note 1)		V _{ref(B)}		V _{ref(T)}	V
High-level input voltage, V _{IH}		2.5			V
Low-level input voltage, V _{IL}		0.5			V
Pulse duration, clock high, t _{w(H)}		50			ns
Pulse duration, clock low, t _{w(L)}		50			ns

NOTE 1: REFT – REFB ≤ 2.4 V maximum

electrical characteristics at V_{DD} = 3 V, V_{ref(T)} = 2.6 V, V_{ref(B)} = 0.6 V, f_{conv} = 10 MSPS, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
E _L	Linearity error	f _{conv} = 10 MSPS, V _I = 0.6 V to 2.6 V	T _A = 25°C		±0.4	±0.75	LSB
			T _A = –20°C to 75°C			±1	
E _D	Linearity error, differential		T _A = 25°C		±0.3	±0.5	
			T _A = –20°C to 75°C			±0.75	
Self bias (1)		Short REFB to REFBS, Short REFT to REFTS		0.57	0.61	0.65	V
Self bias (2)				1.9	2.02	2.15	
Self bias (3)		Short REFB to AGND, Short REFT to REFTS		2.18	2.29	2.4	
I _{ref}	Reference current	V _{ref(T)} – V _{ref(B)} = 2 V		6	10	14	mA
R _{ref}	Reference voltage resistor	Between REFT and REFB terminals		140	200	260	Ω
C _i	Analog input capacitance	V _{I(ANLG)} = 1.5 V + 0.07 V _{rms}		16			pF
E _{ZS}	Zero-scale error	V _{ref} = REFT – REFB = 2 V		–18	–43	–68	mV
E _{FS}	Full-scale error			–20	0	20	
I _{IH}	High-level input current	V _{DD} = MAX,	V _{IH} = V _{DD}			5	μA
I _{IL}	Low-level input current	V _{DD} = MAX,	V _{IL} = 0			5	
I _{OH}	High-level output current	OE = GND,	V _{DD} = MIN, V _{OH} = V _{DD} – 0.5 V	–1.5			mA
I _{OL}	Low-level output current	OE = GND,	V _{DD} = MIN, V _{OL} = 0.4 V	2.5			
I _{IOZH}	High-level high-impedance-state output leakage current	OE = V _{DD} ,	V _{DD} = MAX, V _{OH} = V _{DD}			16	μA
I _{IOZL}	Low-level high-impedance-state output leakage current	OE = V _{DD} ,	V _{DD} = MIN, V _{OL} = 0			16	
I _{DD}	Supply current	f _S = 10 MSPS,	NTSC ramp wave input	13		20	mA

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

PRODUCT PREVIEW



TLV5510

3-V 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS124 – DECEMBER 1997

operating characteristics at $V_{DD} = 3\text{ V}$, $V_{ref(T)} = 2.6\text{ V}$, $V_{ref(B)} = 0.6\text{ V}$, $f_{CLK} = 10\text{ MHz}$, $T_A = 25^\circ\text{C}$
(unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{conv} Maximum conversion rate	$V_{I(ANLG)} = 0.5\text{ V} - 2.5\text{ V}$, $f_I = 1\text{-kHz ramp wave form}$	10			MSPS
BW Analog input bandwidth	At -1 dB		14		MHz
t_{pd} Digital output delay time	$C_L \leq 10\text{ pF}$ (see Note 2)		18	30	ns
t_{AJ} Aperture jitter time			30		ps
t_{pS} Sampling delay time			4		ns

NOTE 2: C_L includes probe and jig capacitance

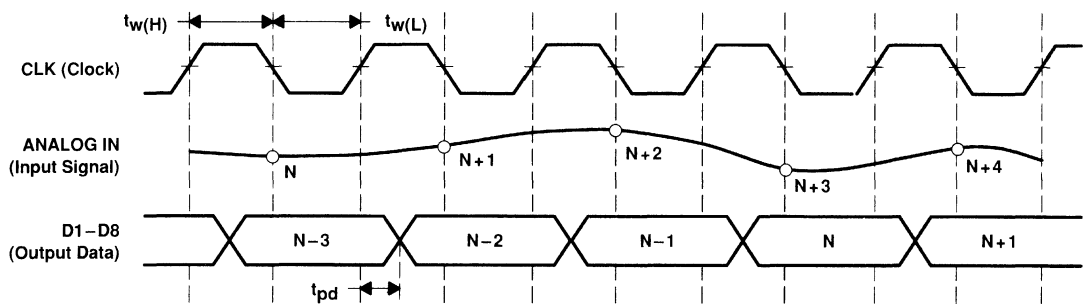


Figure 1. I/O Timing Diagram

PRODUCT PREVIEW



TLV5510

3-V 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS124 – DECEMBER 1997

PRINCIPLES OF OPERATION

functional description

The TLV5510 is a semiflash ADC featuring two lower comparator blocks of four bits each.

As shown in Figure 2, input voltage $V_I(1)$ is sampled with the falling edge of CLK1 to the upper comparators block and the lower comparators block(A), S(1). The upper comparators block finalizes the upper data UD(1) with the rising edge of CLK2, and simultaneously, the lower reference voltage generates the voltage RV(1) corresponding to the upper data. The lower comparators block (A) finalizes the lower data LD(1) with the rising edge of CLK3. UD(1) and LD(1) are combined and output as OUT(1) with the rising edge of CLK4. According to the above internal operation described, output data is delayed 2.5 clocks from the analog input voltage sampling point.

Input voltage $V_I(2)$ is sampled with the falling edge of CLK2. UD(2) is finalized with the rising edge of CLK3, and LD(2) is finalized with the rising edge of CLK4 at the lower comparators block(B). OUT(2) is output with the rising edge of CLK5.

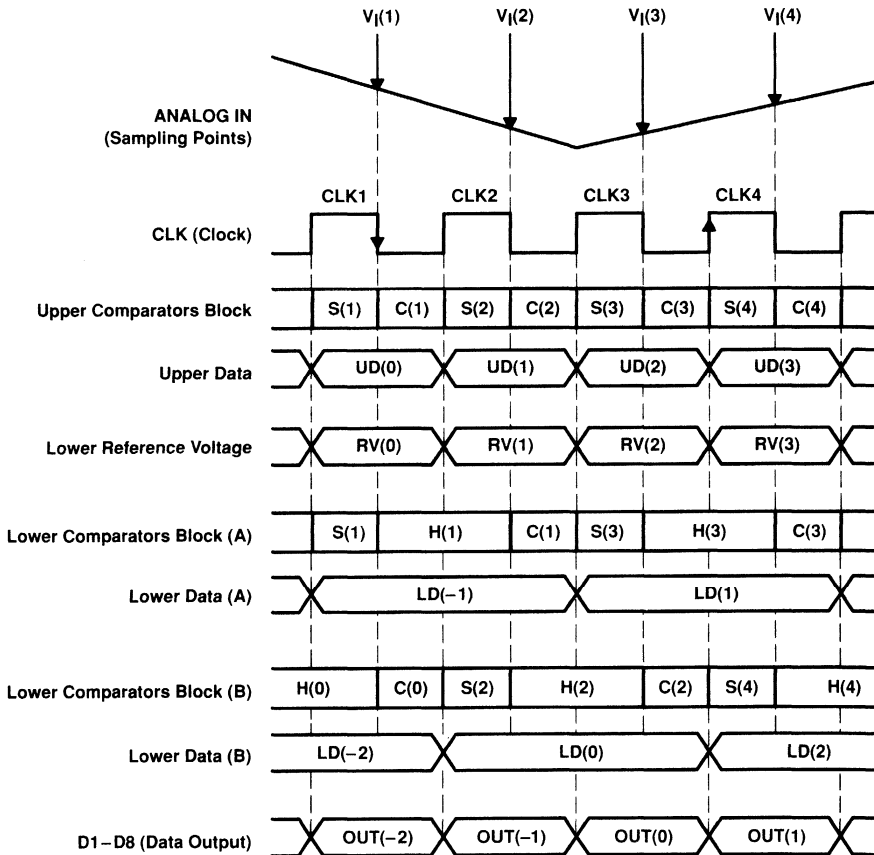


Figure 2. Internal Functional Timing Diagram

PRODUCT PREVIEW



TLV5510

3-V 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS124 – DECEMBER 1997

PRINCIPLES OF OPERATION

internal referencing

Three internal resistors are provided such that the device can generate an internal reference voltage. These resistors are brought out on terminals V_{DDA} , REFTS, REFT, REFB, REFBS, and AGND.

To use the internally generated reference voltage, terminal connections should be made as shown in Figure 3. This connection provides the standard video 2-V reference for the nominal digital output.

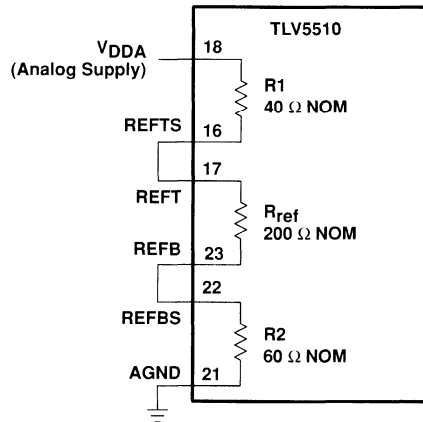


Figure 3. External Connections for Using the Internal Reference Resistor Divider

functional operation

The TLV5510 functions as shown in the Table 1.

Table 1. Functional Operation

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE								
		MSB								LSB
$V_{ref(T)}$	255	1	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	128	1	0	0	0	0	0	0	0	0
•	127	0	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
$V_{ref(B)}$	0	0	0	0	0	0	0	0	0	0

PRODUCT PREVIEW



TLV5510

3-V 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS124 – DECEMBER 1997

APPLICATION INFORMATION

The following notes are design recommendations that should be used with the TLV5510.

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or printed-circuit-board (PCB) techniques should be used throughout the evaluation and production process. Breadboards should be copper clad for bench evaluation.
- Since AGND and DGND are connected internally, the ground lead in must be kept as noise free as possible. A good method to use is twisted-pair cables for the supply lines to minimize noise pickup. An analog and digital ground plane should be used on PCB layouts when additional logic devices are used. The AGND and DGND terminals of the device should be tied to the analog ground plane.
- V_{DDA} to AGND and V_{DDD} to DGND should be decoupled with 1- μ F and 0.01- μ F capacitors, respectively, placed as close as possible to the appropriate device terminals. A ceramic chip capacitor is recommended for the 0.01- μ F capacitor. Care should be exercised to assure a solid noise-free ground connection for the analog and digital grounds.
- V_{DDA} , AGND, and ANALOG IN terminals should be shielded from the higher frequency terminals, CLK and D0–D7. If possible, AGND traces should be placed on both sides of the ANALOG IN traces on the PCB for shielding.
- In testing or application of the device, the resistance of the driving source connected to the analog input should be 10 Ω or less within the analog frequency range of interest.

PRODUCT PREVIEW

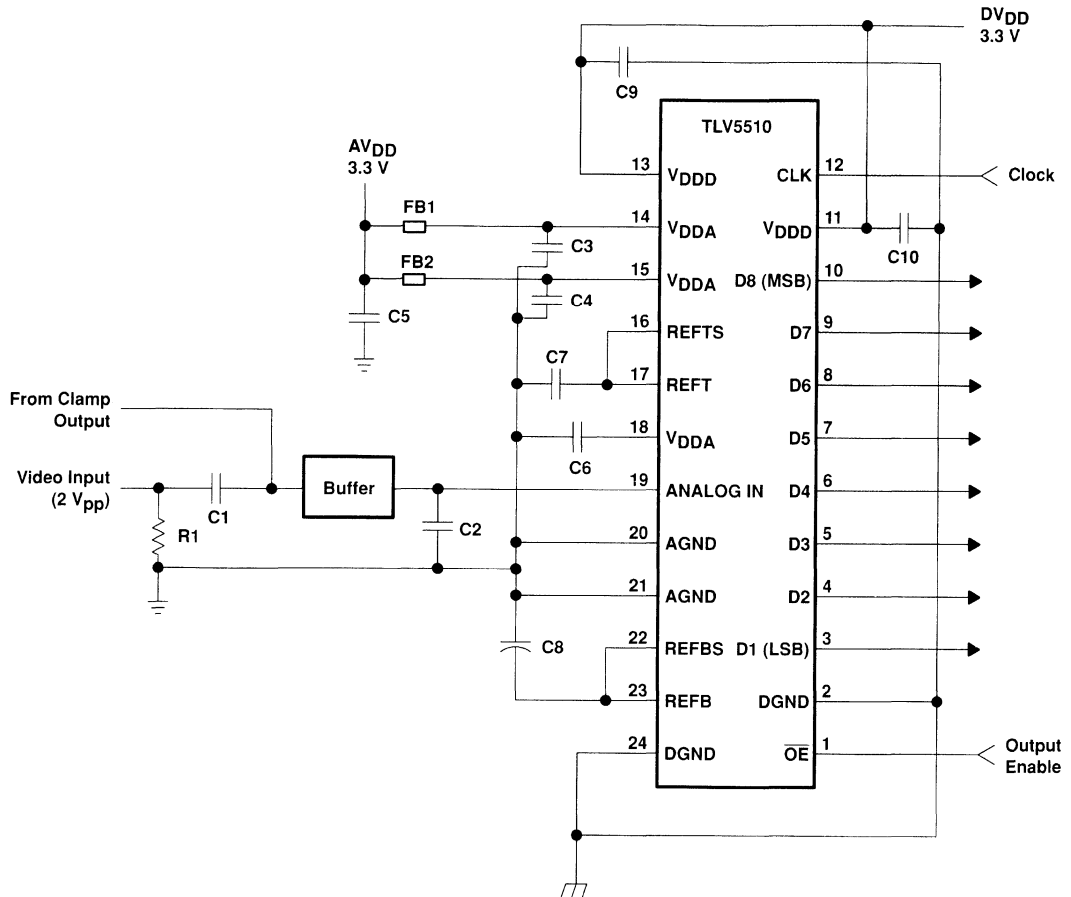


TLV5510 3-V 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

SLAS124 – DECEMBER 1997

APPLICATION INFORMATION

PRODUCT PREVIEW



LOCATION	DESCRIPTION
C1, C3, C4, C6–C10	0.1 μ F Capacitor
C2	10 pF Capacitor
C5	47 μ F Capacitor
FB1, FB2	Ferrite Bead
R1	75 Ω resistor

Figure 4. Application and Test Schematic



General Information	1
General Purpose ADCs	2
General Purpose DACs	3
DSP AICs and CODECs	4
Special Functions	5
Video Interface Palettes	6
Digital Imaging Sensor Products	7
Mechanical Information	8

Contents

	Page
AD7524M :	3-3
TL5632 :	3-11
TLC5602 :	3-19
TLC5604 :	3-27
TLC5614 :	3-29
TLC5615 :	3-31
TLC5616 :	3-47
TLC5617 :	3-55
TLC5618 :	3-75
TLC5618M :	3-95
TLC5620 :	3-97
TLC5628 :	3-107
TLC7225 :	3-117
TLC7226 :	3-137
TLC7524 :	3-153
TLC7528 :	3-163
TLC7628 :	3-177
TLV5613 :	3-187
TLV5619 :	3-195
TLV5620 :	3-203
TLV5621 :	3-215
TLV5628 :	3-231
TMS57014A :	3-243

AD7524M

Advanced LinCMOS™ 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SGLS028A - SEPTEMBER 1989 - REVISED MARCH 1995

- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easily interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonicity Over Entire A/D Conversion Range**
- **Segmented High-Order Bits Ensure Low-Glitch Output**
- **Designed to Be interchangeable With Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface With SMJ320**

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	1/2 LSB Max
Power dissipation at $V_{DD} = 5\text{ V}$	5 mW Max
Settling time	100 ns Max
Propagation delay	80 ns Max

description

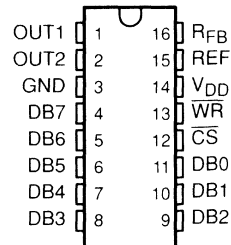
The AD7524M is an Advanced LinCMOS™ 8-bit digital-to-analog converter (DAC) designed for easy interface to most popular microprocessors.

The AD7524M is an 8-bit multiplying DAC with input latches and with a load cycle similar to the write cycle of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most-significant bits, which produce the highest glitch impulse. The AD7524M provides accuracy to 1/2 LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 mW typically.

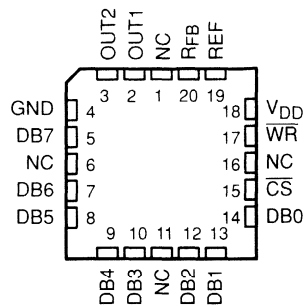
Featuring operation from a 5-V to 15-V single supply, the AD7524M interfaces easily to most microprocessor buses or output ports. Excellent multiplying (2 or 4 quadrant) makes the AD7524M an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The AD7524M is characterized for operation from -55°C to 125°C .

**J PACKAGE
(TOP VIEW)**



**FK PACKAGE
(TOP VIEW)**



NC—No internal connection

AVAILABLE OPTIONS

T_A	PACKAGE	
	CERAMIC CHIP CARRIER (FK)	CERAMIC DIP (J)
-55°C to 125°C	AD7524MFK	AD7524MJ

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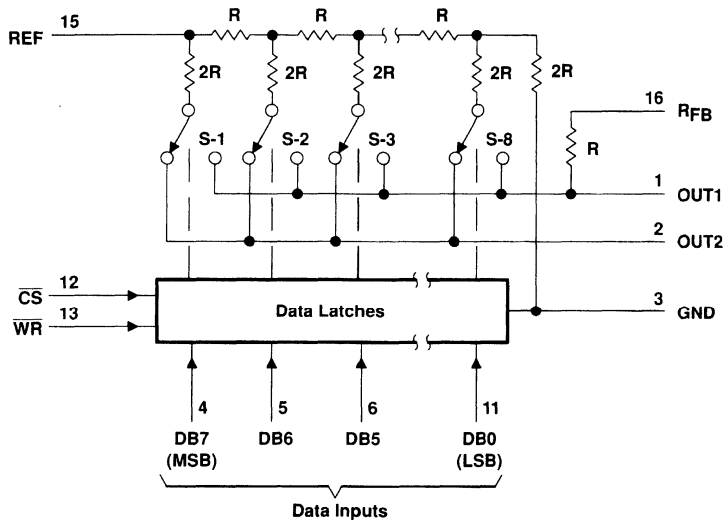
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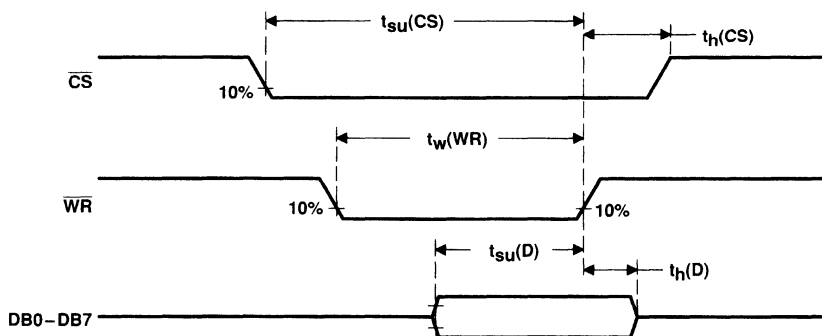
AD7524M
Advanced LinCMOS™ 8-BIT MULTIPLYING
DIGITAL-TO-ANALOG CONVERTER

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functional block diagram



operating sequence



AD7524M
Advanced LinCMOS™ 8-BIT MULTIPLYING
DIGITAL-TO-ANALOG CONVERTER
 SGLS028A – SEPTEMBER 1989 – REVISED MARCH 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD}	–0.3 V to 17 V
Voltage between R_{FB} and GND	±25 V
Digital input voltage range, V_I	–0.3 V to $V_{DD}+0.3$ V
Reference voltage range, V_{ref}	±25 V
Peak digital input current, I_I	10 μ A
Operating free-air temperature range, T_A	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Case temperature for 60 seconds, T_C : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	$V_{DD} = 5$ V			$V_{DD} = 15$ V			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}	±10			±10			V
High-level input voltage, V_{IH}	2.4			13.5			V
Low-level input voltage, V_{IL}	0.8			1.5			V
\overline{CS} setup time, $t_{su}(CS)$	40			40			ns
\overline{CS} hold time, $t_h(CS)$	0			0			ns
Data bus input setup time, $t_{su}(D)$	25			25			ns
Data bus input hold time, $t_h(D)$	10			10			ns
Pulse duration, \overline{WR} low, $t_w(WR)$	40			40			ns
Operating free-air temperature, T_A	–55		125	–55		125	°C



AD7524M

Advanced LinCMOS™ 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SGLS028A – SEPTEMBER 1989 – REVISED MARCH 1995

electrical characteristics over recommended operating free-air temperature range, $V_{ref} = 10\text{ V}$, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{DD} = 5\text{ V}$			$V_{DD} = 15\text{ V}$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH} High-level input current	$V_I = V_{DD}$	Full-range		10		10	μA	
		25°C		1		1		
I_{IL} Low-level input current	$V_I = 0$	Full-range		-10		-10	μA	
		25°C		-1		-1		
I_{pkg} Output leakage current	OUT1	DB0–DB7 at 0, \overline{WR} and \overline{CS} at 0 V	Full-range	± 400	± 200	nA		
		$V_{ref} = \pm 10\text{ V}$	25°C	± 50	± 50			
	OUT2	DB0–DB7 at V_{DD} , \overline{WR} and \overline{CS} at 0	Full-range	± 400	± 200			
		$V_{ref} = \pm 10\text{ V}$	25°C	± 50	± 50			
I_{DD} Supply current	Quiescent	DB0–DB7 at V_{IHmin} or V_{ILmax}		2	2	mA		
	Standby	DB0–DB7 at 0 V or V_{DD}	Full-range	500	500	μA		
			25°C	100	100			
k_{SVS} Supply voltage sensitivity, $\Delta\text{gain}/\Delta V_{DD}$	$\Delta V_{DD} = 10\%$	Full-range		0.16	0.04	%/%		
		25°C	0.002	0.02	0.001	0.02	pF	
C_i Input capacitance, DB0–DB7, \overline{WR} , \overline{CS}	$V_I = 0$			5	5	pF		
C_o Output capacitance	OUT1	DB0–DB7 at 0, \overline{WR} and \overline{CS} at 0 V		30	30	pF		
	OUT2			120	120			
	OUT1	DB0–DB7 at V_{DD} , \overline{WR} and \overline{CS} at 0 V		120	120			
	OUT2			30	30			
Reference input impedance (REF to GND)			5	20	5	20	k Ω	

operating characteristics over recommended operating free-air temperature range, $V_{ref} = 10\text{ V}$, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC} = 5\text{ V}$		$V_{DD} = 15\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	
Linearity error			± 0.2		± 0.2	%FSR
Gain error	See Note 1	Full range	± 1.4	± 0.6	%FSR	
		25°C	± 1	± 0.5		
Settling time (to 1/2 LSB)	See Note 2		100	100	ns	
Propagation delay from digital input to 90% of final analog output current	See Note 2		80	80	ns	
Feedthrough at OUT1 or OUT2	$V_{ref} = \pm 10\text{ V}$ (100 kHz sinewave), \overline{WR} and \overline{CS} at 0, DB0–DB7 at 0	Full range	0.5	0.5	%FSR	
		25°C	0.25	0.25		
Temperature coefficient of gain	$T_A = 25\text{ C}$ to t_{min} or t_{max}		± 0.004	± 0.001	%FSR/ $^{\circ}\text{C}$	

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal Full Scale Range (FSR) = $V_{ref} - 1\text{ LSB}$.
2. OUT1 load = 100 Ω , $C_{ext} = 13\text{ pF}$, \overline{WR} at 0 V, \overline{CS} at 0 V, DB0–DB7 at 0 V to V_{DD} or V_{DD} to 0 V.



PRINCIPLES OF OPERATION

The AD7524M is an 8-bit multiplying D/A converter consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded and these decoded bits, through a modification in the R-2R ladder, control three equally weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 1. With all digital inputs low, the entire reference current, I_{ref} , is switched to OUT2. The current source $1/256$ represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 1. Analysis of the circuit for all digital inputs high is similar to Figure 1; however, in this case, I_{ref} would be switched to OUT1.

Interfacing the AD7524M D/A converter to a microprocessor is accomplished via the data bus and the \overline{CS} and \overline{WR} control signals. When \overline{CS} and \overline{WR} are both low, the AD7524M analog output responds to the data activity on the DB0–DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the CS signal or WR signal goes high, the data on the DB0–DB7 inputs are latched until the \overline{CS} and \overline{WR} signals go low again. When \overline{CS} is high, the data inputs are disabled regardless of the state of the \overline{WR} signal.

The AD7524M is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

AD7524M
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DIGITAL-TO-ANALOG CONVERTER
 SGLS028A – SEPTEMBER 1989 – REVISED MARCH 1995

PRINCIPLES OF OPERATION

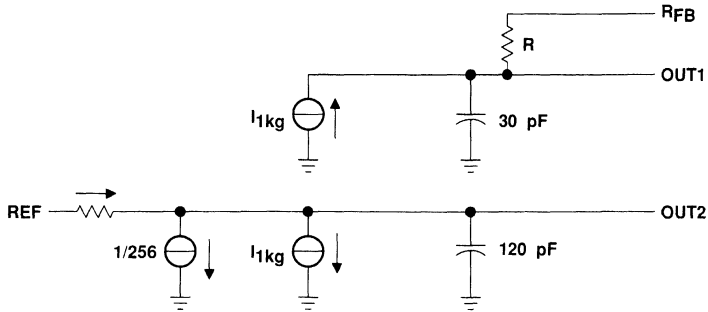


Figure 1. AD7524M Equivalent Circuit With All Digital Inputs Low

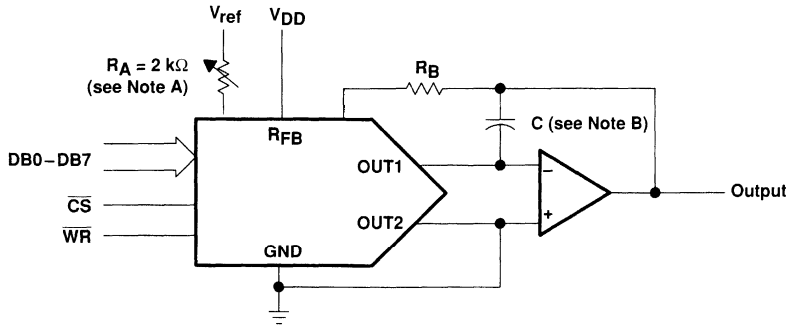


Figure 2. Unipolar Operation (2-Quadant Multiplication)

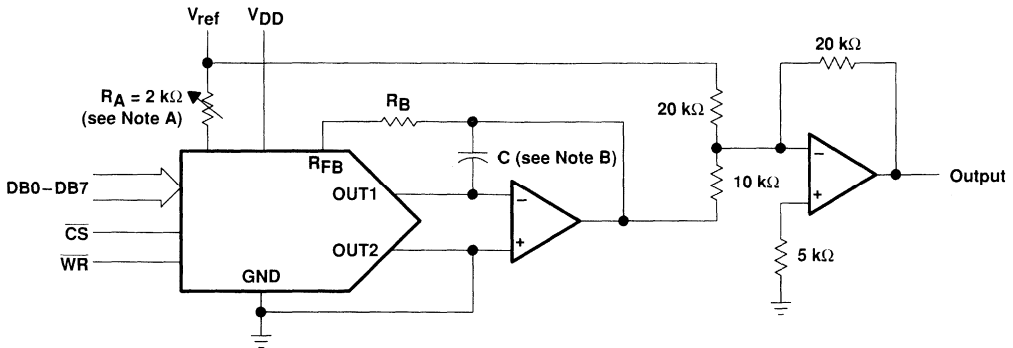


Figure 3. Bipolar Operation (4-Quadant Operation)

NOTES: A. R_A and R_B used only if gain adjustment is required.
 B. C phase compensation (10 – 15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

PRINCIPLES OF OPERATION

Table 1. Unipolar Binary Code

DIGITAL INPUT (see NOTE 3)		ANALOG OUTPUT
MSB	LSB	
11111111		$-V_{ref} (255/256)$
10000001		$-V_{ref} (129/256)$
10000000		$-V_{ref} (128/256) = -V_{ref} / 2$
01111111		$-V_{ref} (127/256)$
00000001		$-V_{ref} (1/256)$
00000000		0

NOTES: 3. $LSB = 1/256 (V_{ref})$.

Table 2. Bipolar (Offset Binary) Code

DIGITAL INPUT (see NOTE 4)		ANALOG OUTPUT
MSB	LSB	
11111111		$V_{ref} (127/128)$
10000001		$V_{ref} (128)$
10000000		0
01111111		$-V_{ref} (128)$
00000001		$-V_{ref} (127/128)$
00000000		$-V_{ref}$

NOTES: 4. $LSB = 1/128 (V_{ref})$.

microprocessor interfaces

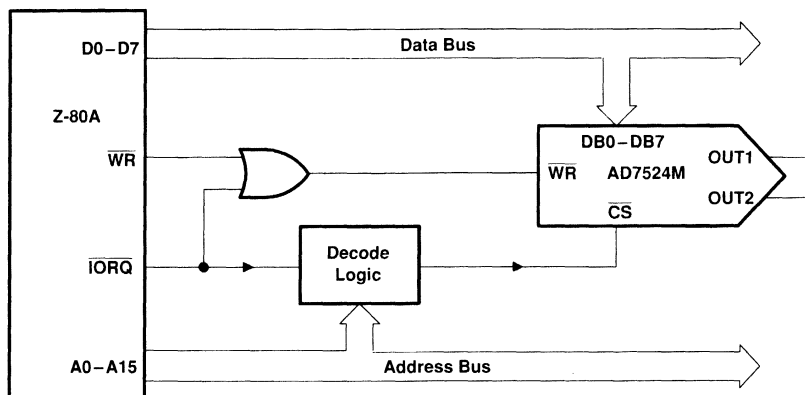


Figure 4. AD7524M–Z-80A Interface

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PRINCIPLES OF OPERATION

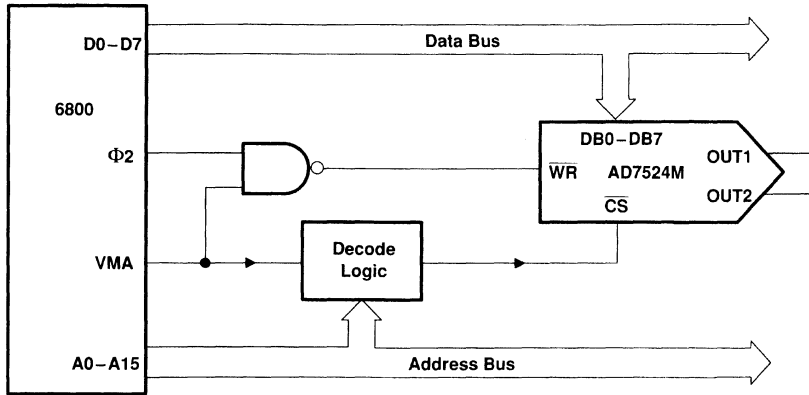


Figure 5. AD7524M-6800 Interface

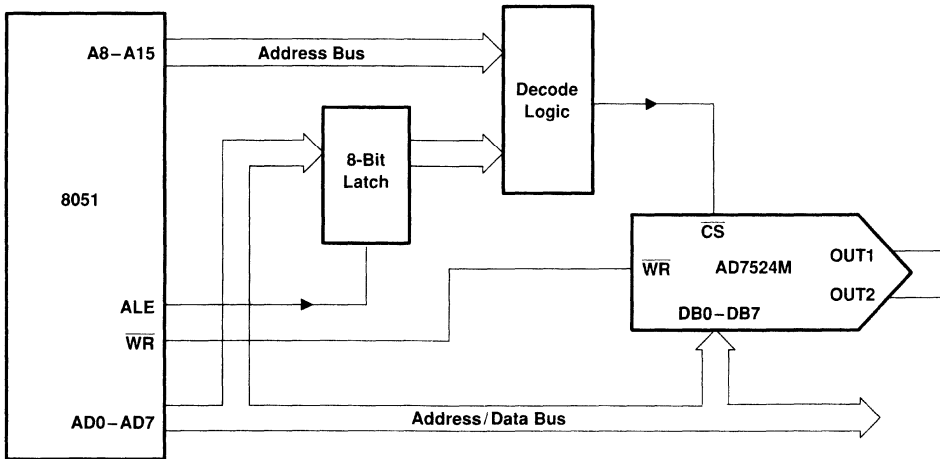


Figure 6. AD7524M-8051 Interface

TL5632C

8-BIT 3-CHANNEL HIGH-SPEED DIGITAL-TO-ANALOG CONVERTER

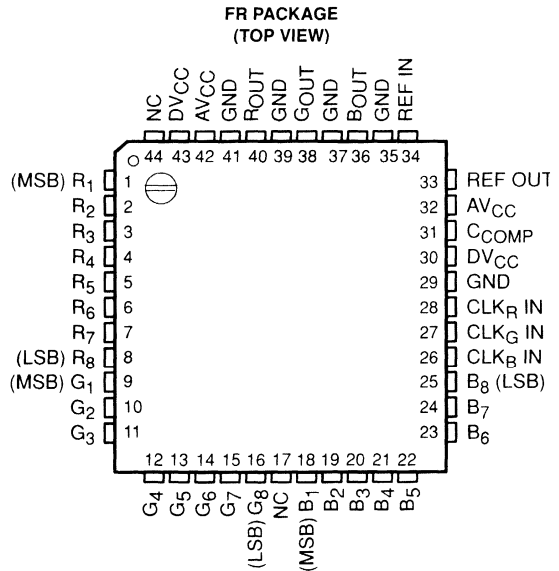
SLAS091 – DECEMBER 1994

- 8-Bit Resolution
- Linearity . . . $\pm 1/2$ LSB Maximum
- Differential Nonlinearity . . . $\pm 1/2$ LSB Maximum
- Conversion Rate . . . 60 MHz Min
- Nominal Output Signal Operating Range
V_{CC} to V_{CC} – 1 V
- TTL Digital Input Voltage
- 5-V Single Power Supply Operation
- Low Power Consumption . . . 350 mW Typ

description

The TL5632C is a low-power ultra-high-speed video digital-to-analog converter that uses the Advanced Low-Power Schottky (ALS) process. The device has a three channel I/O; the red, the blue, and the green channel. The red, blue, and green signals are referred to collectively as the RGB signal. An internally generated reference is also provided for the standard video output voltage range. Conversion of digital signals to analog signals can be at a sampling rate of dc to 60 MHz. The high conversion rate makes the TL5632C suitable for digital television, computer digital video processing, and high-speed data conversion.

The TL5632C is characterized for operation from 0°C to 70°C.



NC – No internal connection

FUNCTION TABLE

STEP	DIGITAL INPUT	OUTPUT VOLTAGE
0	LLLLLLLLL	3.980 V
1	LLLLLLLLH	3.984 V
•	•	•
•	•	•
•	•	•
127	LHHHHHHH	4.488 V
128	HLLLLLLL	4.492 V
129	HLLLLLLH	4.996 V
•	•	•
•	•	•
•	•	•
254	HHHHHHHL	4.996 V
255	HHHHHHHH	5.000 V

AVAILABLE OPTIONS

T _A	PACKAGE
0°C to 70°C	TL5632CFR

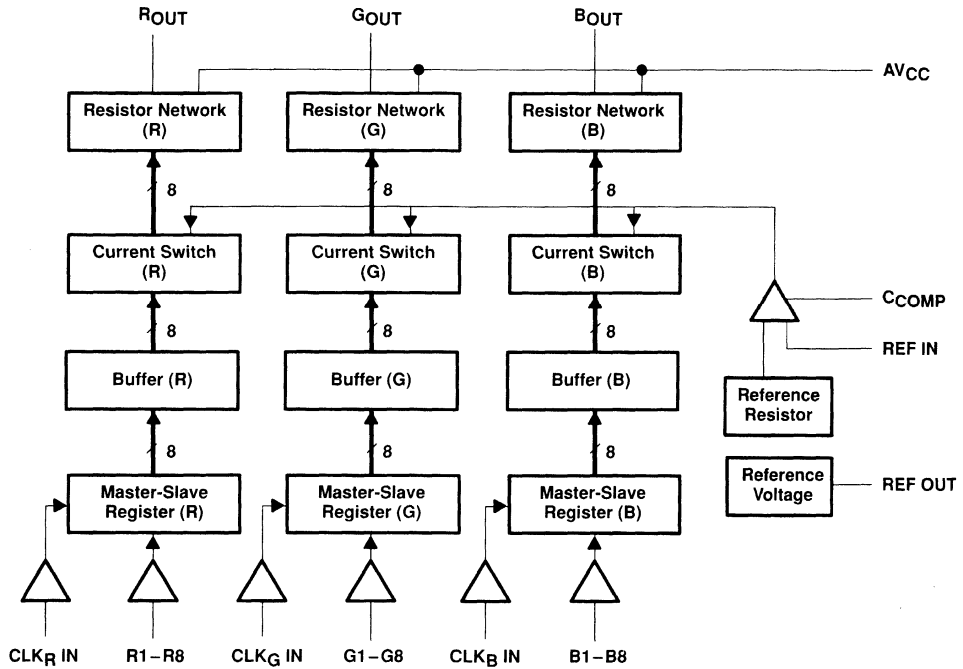
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



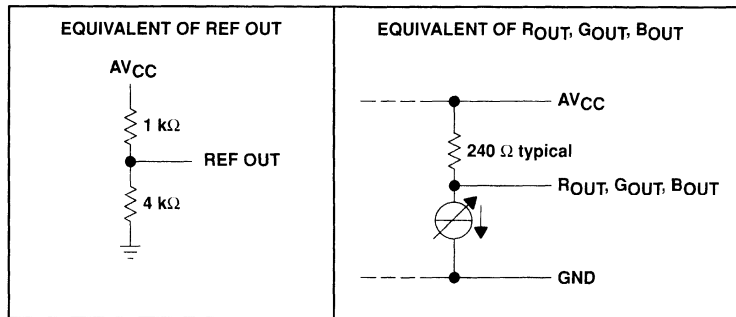
TL5632C 8-BIT 3-CHANNEL HIGH-SPEED DIGITAL-TO-ANALOG CONVERTER

SLAS091 – DECEMBER 1994

functional block diagram



schematics of outputs



TL5632C

8-BIT 3-CHANNEL HIGH-SPEED DIGITAL-TO-ANALOG CONVERTER

SLAS091 – DECEMBER 1994

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
B ₁ – B ₈	18 – 25	I	B-channel digital input (B ₁ = MSB)
B _{OUT}	36	O	B-channel analog output
C _{COMP}	31		Phase compensation capacitance. A 1 μF capacitor is connected from C _{COMP} to GND.
CLK _B IN	26	I	B-channel clock input
CLK _G IN	27	I	G-channel clock input
CLK _R IN	28	I	R-channel clock input
G ₁ – G ₈	9 – 16	I	G-Channel digital input (G ₁ = MSB)
GND	29, 35, 37, 39, 41		Ground. All GND terminals are connected internally; however, all GND terminals should be connected externally to a ground plane or equivalent low impedance ground return.
G _{OUT}	38	O	G-channel analog output
NC	17, 44		No connection internally
R ₁ – R ₈	1 – 8	I	R-channel digital input (R ₁ = MSB)
R _{OUT}	40	O	R-channel analog output
AV _{CC}	32, 42		Analog power supply voltage
DV _{CC}	30, 43		Digital power supply voltage
REF IN	34	I	Reference voltage input. REF IN accepts the reference voltage on REF OUT. An external reference can also be applied consistent with Note 1.
REF OUT	33	O	Reference voltage output. An internal voltage divider generates the voltage level (see schematics of outputs, page 2).

NOTE 1: $V_{CC} - V_{ref} \leq 1.2\text{ V}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Power supply voltage range, AV _{CC} , DV _{CC} (see Note 2)	–0.3 V to 7 V
Digital input voltage range, V _I	–0.3 V to DV _{CC}
Analog output voltage range, R _{OUT} , G _{OUT} , B _{OUT} , C _{COMP} (externally applied)	–0.3 V to AV _{CC} + 0.3 V
Reference input range, REF IN	–0.3 V to AV _{CC} + 0.3 V
Reference output range, REF OUT	–0.3 V to AV _{CC} + 0.3 V
Operating free-air temperature range, T _A	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: All voltage values are with respect to GND.



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TL5632C

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SLAS091 – DECEMBER 1994

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} , DV_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Reference voltage, V_{ref} (see Note 1)	3.8	4	4.2	V
Setup time, data before $CLK\uparrow$, t_{SU1}	10			ns
Hold time, data after $CLK\uparrow$, t_{H1}	3			ns
Pulse duration at high level, t_{W1}	8.3			ns
Pulse duration at low level, t_{W2}	8.3			ns
External phase compensation capacitance, C_{COMP}	1			μ F
Operating free-air temperature, T_A	0		70	$^{\circ}$ C

NOTE 1: $V_{CC} - V_{ref} \leq 1.2$ V

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Resolution				8	Bit
I_{IH}	High-level input current $V_{CC} = 5.25$ V, $V_{IH} = 2.7$ V			20	μ A
I_{IL}	Low-level input current $V_{CC} = 5.25$ V, $V_{IH} = 2.7$ V	-400			μ A
I_{ref}	Reference input current REF IN = 4 V			10	μ A
V_{ref}	Reference output voltage $V_{CC} = 5$ V, With internal reference	3.8	4	4.2	V
V_{FS}	Full-scale analog output voltage $V_{IH} = 2$ V, REF IN = 4 V	$AV_{CC} - 15$	AV_{CC}	$AV_{CC} + 15$	mV
V_{ZS}	Zero-scale analog output voltage $V_{IL} = 0.8$ V, REF IN = 4 V	3.9	3.98	4.05	V
	RGB full-scale ratio	0%	4%	8%	
z_o	Output impedance	200	240	280	Ω
I_{CC}	Supply current		70	90	mA

operating characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error End point, REF IN = 4 V			± 0.5	LSB
E_D	Differential linearity error REF IN = 4 V			± 0.5	LSB
f_c	Maximum conversion rate		60		MHz
t_{PLH}	Propagation delay time, low-to-high level		10		ns
t_{PHL}	Propagation delay time, high-to-low level		10		
t_r	Rise time		5		ns
t_f	Fall time		5		

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^{\circ}$ C.

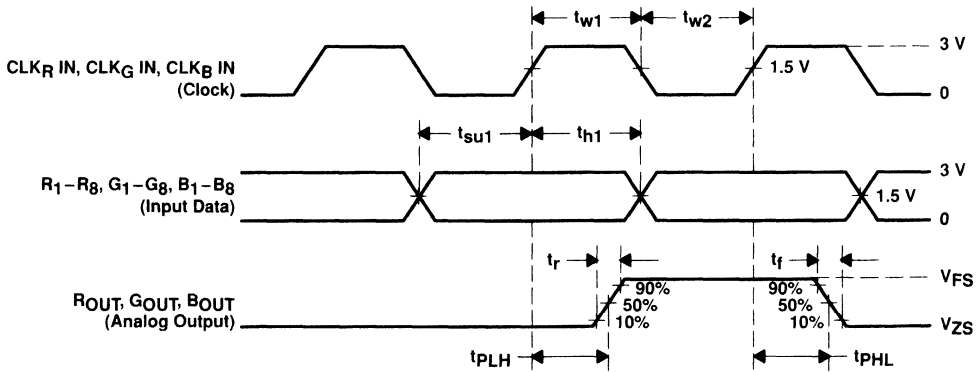
‡ C_L includes probe and jig capacitances.



TL5632C 8-BIT 3-CHANNEL HIGH-SPEED DIGITAL-TO-ANALOG CONVERTER

SLAS091 – DECEMBER 1994

PARAMETER MEASUREMENT INFORMATION



TYPICAL CHARACTERISTICS

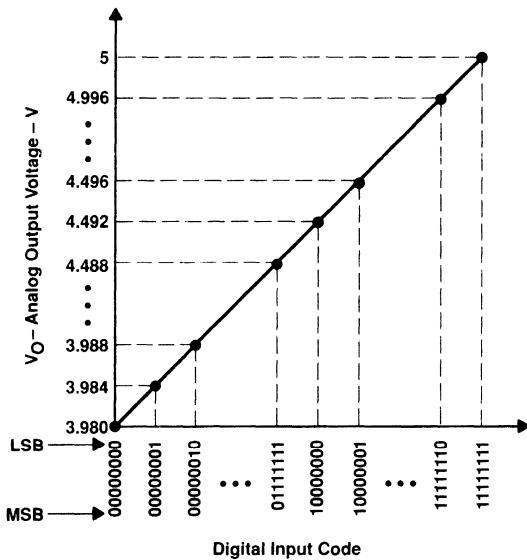


Figure 1. Ideal Conversion Characteristics

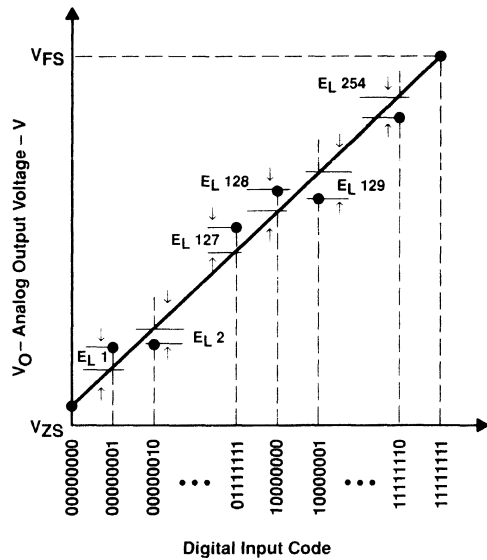


Figure 2. End-Point Linearity Error



TL5632C

8-BIT 3-CHANNEL HIGH-SPEED DIGITAL-TO-ANALOG CONVERTER

SLAS091 – DECEMBER 1994

APPLICATION INFORMATION

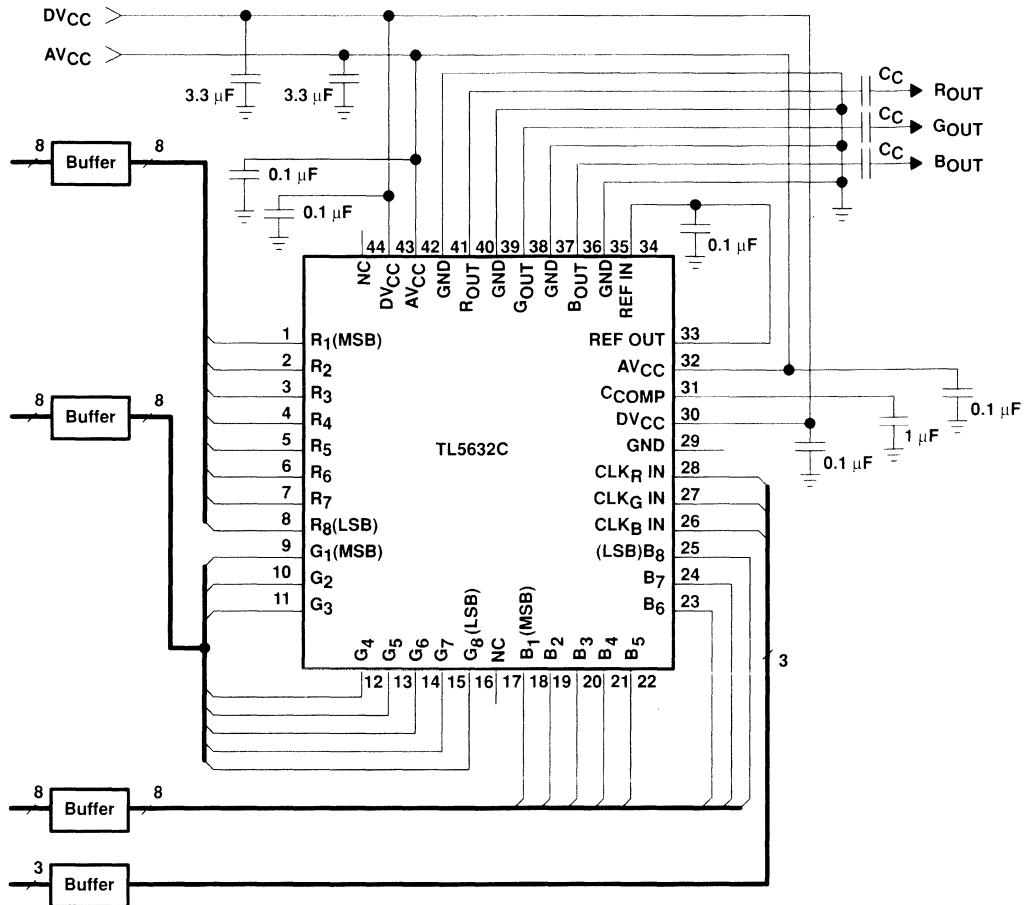
The following design procedures should be used for optimum operation.

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or RF printed-circuit-board (PCB) techniques should be used throughout the evaluation and production process.
- Wide ground leads or a ground plane should be used on the PCB layouts to minimize parasitic inductance and resistance. A ground plane is the better choice for noise reduction.
- AV_{CC} and DV_{CC} are also separate internally, so they must be connected externally. These external PCB leads should also be made as wide as possible. A ferrite bead or equivalent inductance should be placed in series with AV_{CC} and the decoupling capacitor before the AV_{CC} and DV_{CC} leads are connected together on the board. It is critical that the supply voltage applied to AV_{CC} be as noise free and ripple free as possible. Ripple and noise rejection should be a minimum of 60 dB below the full-scale output range of 1 V peak-to-peak.
- AV_{CC} to GND and DV_{CC} to GND should be decoupled with 3.3- μ F and 0.1- μ F capacitors, respectively, as close as possible to the appropriate device terminals. A ceramic chip capacitor is recommended for the 0.1- μ F capacitor.
- The phase compensation capacitor should be connected between C_{COMP} and GND with as short a lead-in as possible.
- The no-connection (NC) terminals on the small-outline package should be connected to GND.
- AV_{CC} , DV_{CC} , and R_{OUT} , G_{OUT} , and B_{OUT} should be shielded from the high-frequency terminals CLK_R IN, CLK_G IN, and CLK_B IN and the input data terminals. GND traces should be placed on both sides of the R_{OUT} , G_{OUT} , and B_{OUT} traces on the PCB to the following signal processing stage. These output traces should be as short as possible.

TL5632C 8-BIT 3-CHANNEL HIGH-SPEED DIGITAL-TO-ANALOG CONVERTER

SLAS091 – DECEMBER 1994

APPLICATION INFORMATION



- NOTES: A. Buffers are SN74AS244 or equivalent.
 B. 0.1 μF capacitors should be placed as close to the device terminals as possible.
 C. The coupling capacitor (C_C) value is application specific and selectable by the user.

Figure 3. Typical Bypass, Buffer, and Output Configuration

TLC5602C, TLC5602M VIDEO 8-BIT DIGITAL-TO-ANALOG CONVERTERS

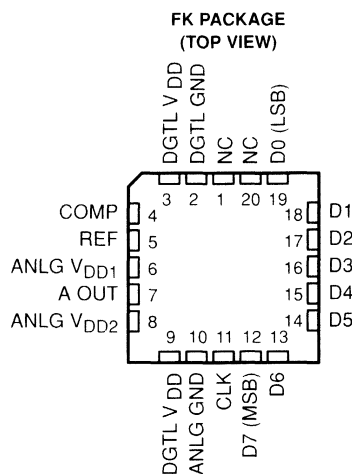
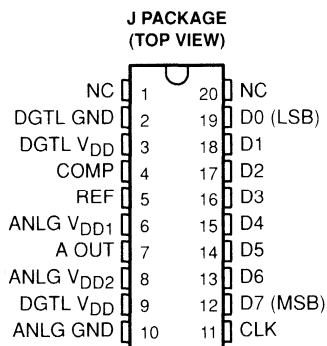
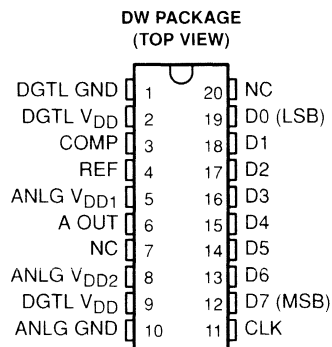
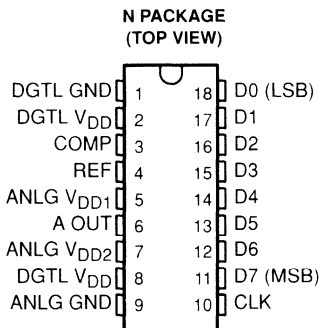
SLAS023C – FEBRUARY 1989 – REVISED MAY 1995

- 8-Bit Resolution
- $\pm 0.2\%$ Linearity
- Maximum Conversion Rate
30 MHz Typ
20 MHz Min
- Analog Output Voltage Range
 V_{DD} to $V_{DD} - 1$ V
- TTL Digital Input Voltage
- 5-V Single Power-Supply Operation
- Low Power Consumption . . . 80 mW Typ
- Interchangeable With Fujitsu MB40778

description

The TLC5602x devices are low-power, ultra-high-speed video, digital-to-analog converters that use the LinEPIC™ 1- μ m CMOS process. The TLC5602x converts digital signals to analog signals at a sampling rate of dc to 20 MHz. Because of high-speed operation, the TLC5602x devices are suitable for digital video applications such as digital television, video processing with a computer, and radar-signal processing.

The TLC5602C is characterized for operation from 0°C to 70°C. The TLC5602M is characterized over the full military temperature range of -55°C to 125°C.



NC—No internal connection

LinEPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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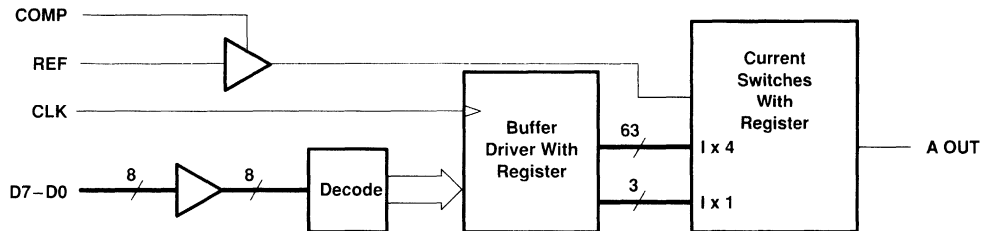
TLC5602C, TLC5602M VIDEO 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS023C – FEBRUARY 1989 – REVISED MAY 1995

AVAILABLE OPTIONS

PACKAGE				
T _A	WIDE-BODY SMALL OUTLINE (DW)	CERAMIC CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	TLC5602CDW			TLC5602CN
-55°C to 125°C		TLC5602MFK	TLC5602MJ	

functional block diagram



FUNCTION TABLE

STEP	DIGITAL INPUTS								OUTPUT VOLTAGE†
	D7	D6	D5	D4	D3	D2	D1	D0	
0	L	L	L	L	L	L	L	L	3.980 V
1	L	L	L	L	L	L	L	H	3.984 V
127	L	H	H	H	H	H	H	H	4.488 V
128	H	L	L	L	L	L	L	L	4.492 V
129	H	L	L	L	L	L	L	H	4.496 V
254	H	H	H	H	H	H	H	L	4.996 V
255	H	H	H	H	H	H	H	H	5.000 V

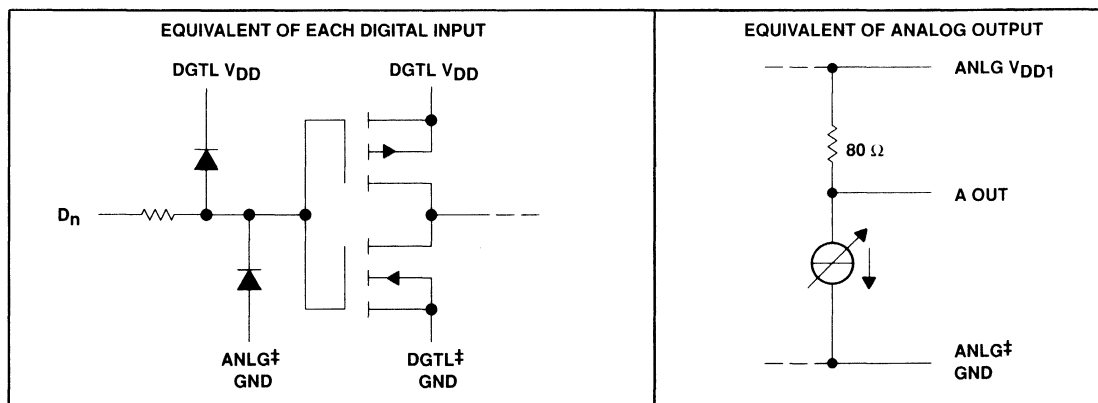
† V_{DD} = 5 V and V_{ref} = 4.02 V



TLC5602C, TLC5602M VIDEO 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS023C – FEBRUARY 1989 – REVISED MAY 1995

schematics of equivalent input and output



† ANLG GND and DGTL GND do not connect internally and should be tied together as close to the device terminals as possible.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, ANLG V_{DD} , DGTL V_{DD}	–0.5 V to 7 V
Digital input voltage range, V_I	–0.5 V to 7 V
Analog reference voltage range, V_{ref}	$V_{DD} - 1.7$ V to $V_{DD} + 0.5$ V
Operating free-air temperature range, T_A : TLC5602C	0°C to 70°C
TLC5602M	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75	5	5.25	V
Analog reference voltage, V_{ref}		3.8	4	4.2	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Pulse duration, CLK high or low, t_w		25			ns
Setup time, data before CLK \uparrow , t_{SU}		16.5			ns
Hold time, data after CLK \uparrow , t_H		12.5			ns
Phase compensation capacitance, C_{comp} (see Note 1)		1			μ F
Load resistance, R_L		75k			Ω
Operating free-air temperature, T_A	TLC5602C	0	70		°C
	TLC5602M	–55	125		

NOTE 1: The phase compensation capacitor should be connected between COMP and ANLG GND.

TLC5602C, TLC5602M

VIDEO 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS023C – FEBRUARY 1989 – REVISED MAY 1995

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [‡]	MAX	UNIT	
I_{IH}	High-level input current	Digital inputs	$V_I = 5\text{ V}$			± 1	μA	
I_{IL}	Low-level input current		$V_I = 0\text{ V}$			± 1	μA	
I_{ref}	Input reference current		$V_{ref} = 4\text{ V}$			10	μA	
V_{FS}	Full-scale analog output voltage		$V_{DD} = 5\text{ V}, V_{ref} = 4.02\text{ V}$	$V_{DD}-15$	V_{DD}	$V_{DD}+15$	mV	
V_{ZS}	Zero-scale analog output voltage		$V_{DD} = 5\text{ V}, V_{ref} = 4.02\text{ V}, T_A = \text{full range}^{\S}$	TLC5602C	3.919	3.98	4.042	V
				TLC5602M	3.919	3.98	4.042	
				TLC5602M	3.919	3.98	4.062	
r_o	Output resistance		$T_A = 25^\circ\text{C}$	TLC5602C	60	80	120	Ω
			$T_A = \text{full range}^{\S}$	TLC5602M				
C_i	Input capacitance		$f_{clock} = 1\text{ MHz}, T_A = 25^\circ\text{C}$			15	pF	
I_{DD}	Supply current		$f_{clock} = 20\text{ MHz}, V_{ref} = V_{DD}-0.95\text{ V}$			16	25	mA

[‡] All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

[§] Full range for the TLC5602C is 0°C to 70°C , and full range for the TLC5602M is -55°C to 125°C .

operating characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
$E_{L(\text{adj})}$	Linearity error, best-straight-line	$T_A = \text{full range}^{\ddagger}$	TLC5602C			$\pm 0.2\%$	
		$T_A = 25^\circ\text{C}$	TLC5602M			$\pm 0.2\%$	
		$T_A = \text{full range}^{\ddagger}$				$\pm 0.4\%$	
E_L	Linearity error, end point					$\pm 0.15\%$	
E_D	Linearity error, differential					$\pm 0.2\%$	
G_{diff}	Differential gain		NTSC 40-IRE modulated ramp, $f_{clock} = 14.3\text{ MHz}, Z_L \geq 75\text{ k}\Omega$			0.7%	
f_{diff}	Differential phase						0.4°
t_{pd}	Propagation delay time, CLK to analog output		$C_L = 10\text{ pF}$			25	ns
t_s	Settling time to within 1/2 LSB		$C_L = 10\text{ pF}$			30	ns

[†] All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

[‡] Full range for the TLC5602C is 0°C to 70°C , and full range for the TLC5602M is -55°C to 125°C .



TLC5602C, TLC5602M VIDEO 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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PARAMETER MEASUREMENT INFORMATION

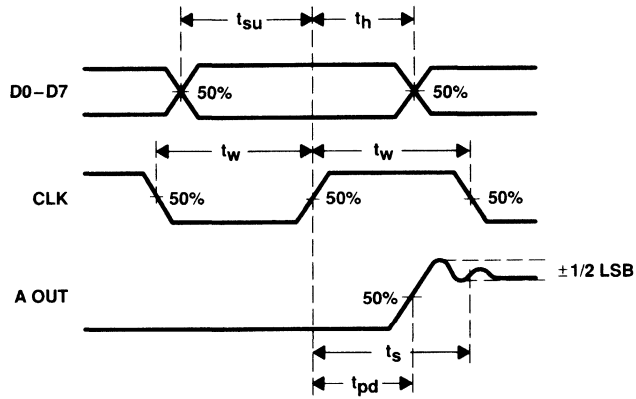


Figure 1. Voltage Waveforms

TLC5602C, TLC5602M VIDEO 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS023C – FEBRUARY 1989 – REVISED MAY 1995

TYPICAL CHARACTERISTICS

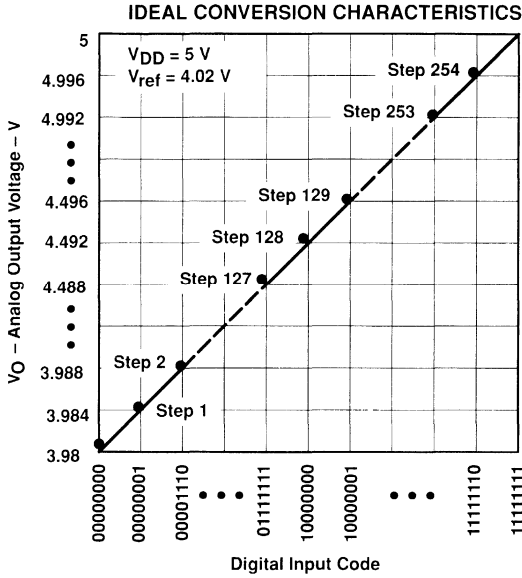


Figure 2

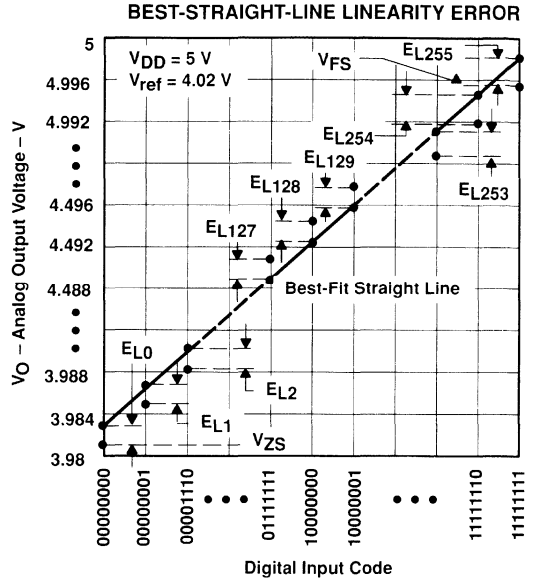


Figure 3

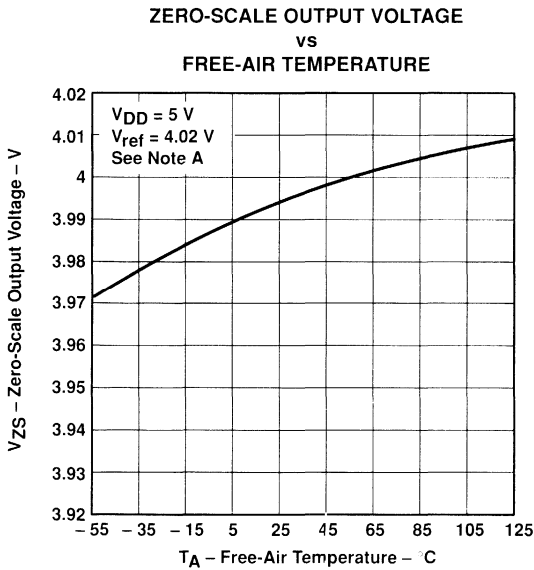


Figure 4

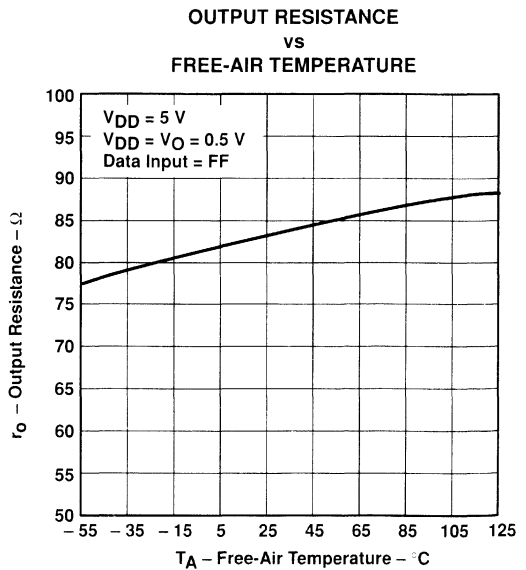


Figure 5

NOTE A: V_{ref} is relative to ANLG GND. V_{DD} is the voltage between ANLG V_{DD} and DGTL V_{DD} tied together and ANLG GND and DGTL GND tied together.



TLC5602C, TLC5602M
VIDEO 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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TYPICAL CHARACTERISTICS

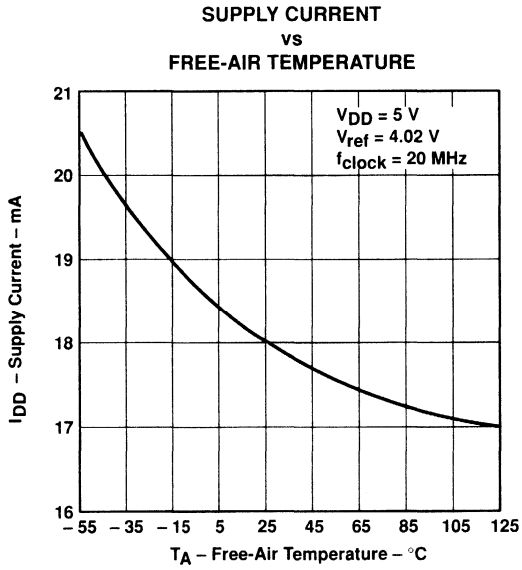
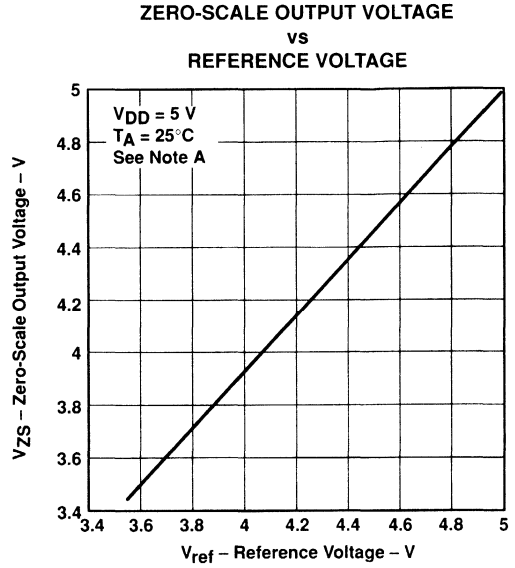


Figure 6



NOTE A: V_{ref} is relative to ANLG GND. V_{DD} is the voltage between ANLG V_{DD} and DGTL V_{DD} tied together and ANLG GND and DGTL GND tied together.

Figure 7

TLC5602C, TLC5602M

VIDEO 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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APPLICATION INFORMATION

The following design recommendations benefit the TLC5602 user:

- Physically separate and shield external analog and digital circuitry as much as possible to reduce system noise.
- Use RF breadboarding or RF printed-circuit-board (PCB) techniques throughout the evaluation and production process.
- Since ANLG GND and DGTL GND are not connected internally, these terminals need to be connected externally. With breadboards, these ground lines should connect to the power-supply ground through separate leads with proper supply bypassing. A good method is to use a separate twisted pair for the analog and digital supply lines to minimize noise pickup.

Use wide ground leads or a ground plane on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.

- ANLG V_{DD} and DGTL V_{DD} are also separated internally, so they must connect externally. These external PCB leads should also be made as wide as possible. Place a ferrite bead or equivalent inductance in series with ANLG V_{DD} and the decoupling capacitor as close to the device terminals as possible before the ANLG V_{DD} and DGTL V_{DD} leads are connected together on the board.
- Decouple ANLG V_{DD} to ANLG GND and DGTL V_{DD} to DGTL GND with a 1- μ F and 0.01- μ F capacitor, respectively, as close as possible to the appropriate device terminals. A ceramic chip capacitor is recommended for the 0.01- μ F capacitor.
- Connect the phase compensation capacitor between COMP and ANLG GND with as short a lead-in as possible.
- The no-connection (NC) terminals on the small-outline package should be connected to ANLG GND.
- Shield ANLG V_{DD} , ANLG GND, and A OUT from the high-frequency terminals CLK and D7–D0. Place ANLG GND traces on both sides of the A OUT trace on the PCB.



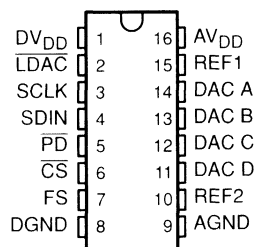
TLC5604

3-V TO 5-V 10-BIT 3- μ S QUADRUPLE DIGITAL-TO-ANALOG CONVERTER WITH POWERDOWN

SLAS176 – DECEMBER 1997

- Four 10-bit D/A Converters
- SPI and TMS320 Compatible Serial Interface
- Internal Power-on Reset
- Low Power Consumption
 - 7.25 mW for 5V Supply
 - 3.93 mW for 3V Supply
- Reference Input Buffers
- Voltage Output Range . . . 2 \times the Reference Input Voltage
- Monotonic Over Temperature

D OR PW PACKAGE
(TOP VIEW)



applications

- Battery Powered Test Instruments
- Digital Offset and Gain Adjustment
- Battery Operated/Remote Industrial Controls
- Machine and Motion Control Devices
- Cellular Telephones

description

The TLC5604 device is 3- μ s quadruple 10-bit voltage output digital-to-analog converter (DAC) with a SPI and TMS320 compatible serial interface. This interface accepts 16 bit words comprised of 4 instruction bits and 12 DAC data bits. The unique feature of this part is that it is four separate DACs in one package. TLC5604 only dissipates 7.25 mW of power with a 5 V supply and 3.93 mW of power with a 3 V supply.

There is an asynchronous LDAC pin for updating the output voltage, and a powerdown pin to ensure repeatable startup conditions.

The resistor string output voltage is buffered by a 2 \times gain rail-to-rail output buffer. The buffer operates with a Class A output stage to improve stability and reduce settling time.

AVAILABLE OPTIONS

T _A	PACKAGE	
	SOIC (D)	TSSOP (PW)
0°C to 70°C	TLC5604CD	TLC5604CPW
-40°C to 85°C	TLC5604ID	TLC5604IPW

PRODUCT PREVIEW



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

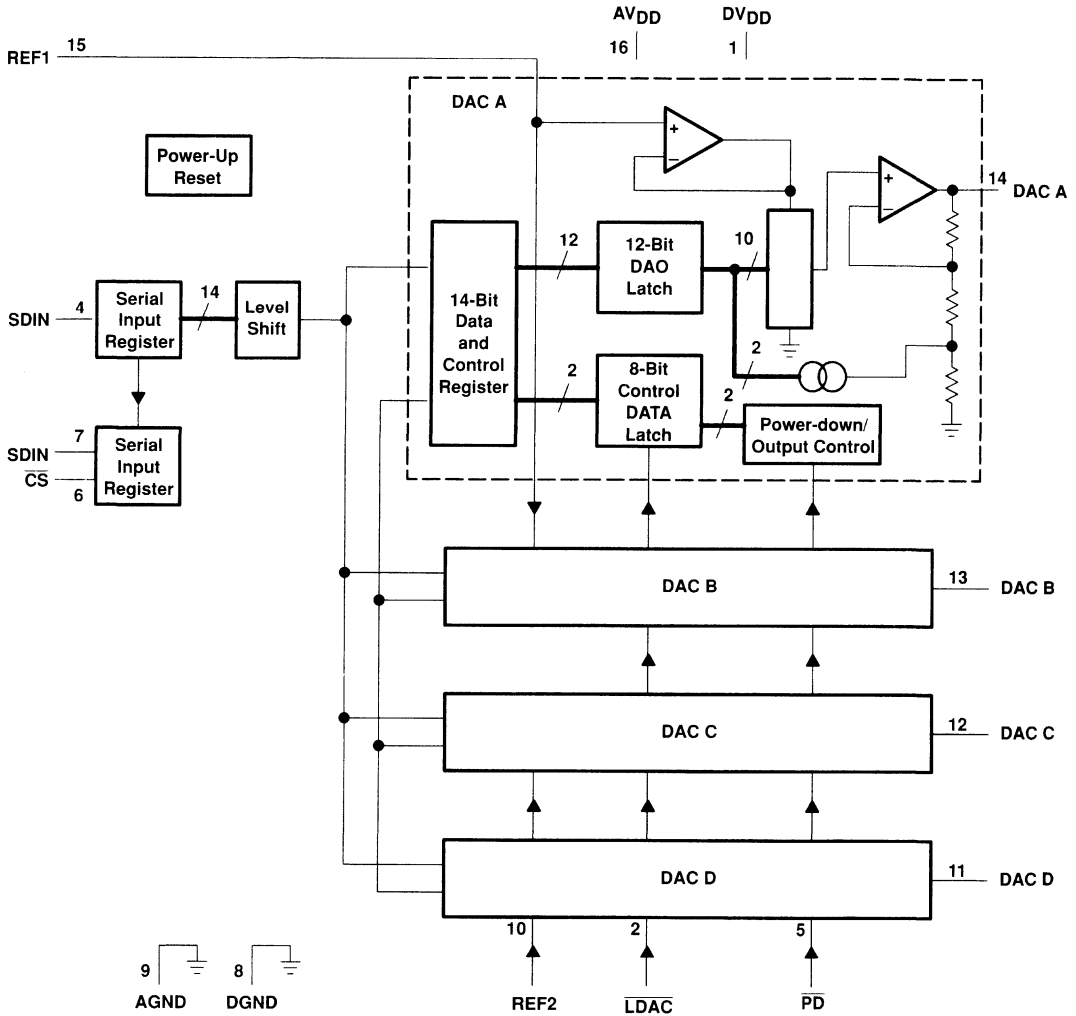


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TLC5604
3-V TO 5-V 10-BIT 3- μ S QUADRUPLE DIGITAL-TO-ANALOG CONVERTER
WITH POWERDOWN
 SLAS176 – DECEMBER 1997

functional block diagram



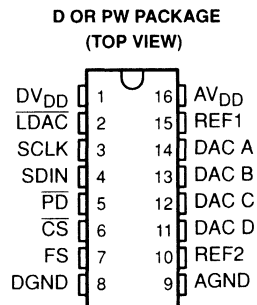
PRODUCT PREVIEW

TLC5614

3-V TO 5-V 12-BIT QUADRUPLE DIGITAL-TO-ANALOG CONVERTER WITH POWERDOWN

SLAS175 – DECEMBER 1997

- Four 12-Bit DACs
- SPI and TMS320 Compatible Serial Interface
- Hardware Powerdown
- Internal Power-on Reset
- Low Power Consumption
 - 7.25 mW for 5-V Supply
 - 3.93 mW for 3-V Supply
- Reference Input Buffers
- Voltage Output Range . . . 2× the Reference Input Voltage
- Monotonic Over Temperature



applications

- Battery Powered Test Instruments
- Digital Offset and Gain Adjustment
- Battery Operated/Remote Industrial Controls
- Machine and Motion Control Devices
- Cellular Telephones

description

The TLC5614 device is 3- μ s quadruple 12-bit voltage output digital-to-analog converter (DAC) with a SPI and TMS320 compatible serial interface. This interface accepts 16 bit words comprised of 4 instruction bits and 12 DAC data bits. The unique feature of this part is that it is four separate DACs in one package. TLC5614 only dissipates 7.25 mW of power with a 5-V supply and 3.93 mW of power with a 3-V supply.

There is an asynchronous LDAC pin for updating the output voltage, and a powerdown pin to ensure repeatable startup conditions.

The resistor string output voltage is buffered by a 2× gain rail-to-rail output buffer. The buffer operates with a Class A output stage to improve stability and reduce settling time.

AVAILABLE OPTIONS

T _A	PACKAGE	
	SOIC (D)	TSSOP (PW)
0°C to 70°C	TLC5614CD	TLC5614CPW
-40°C to 85°C	TLC5614ID	TLC5614IPW



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**TEXAS
INSTRUMENTS**

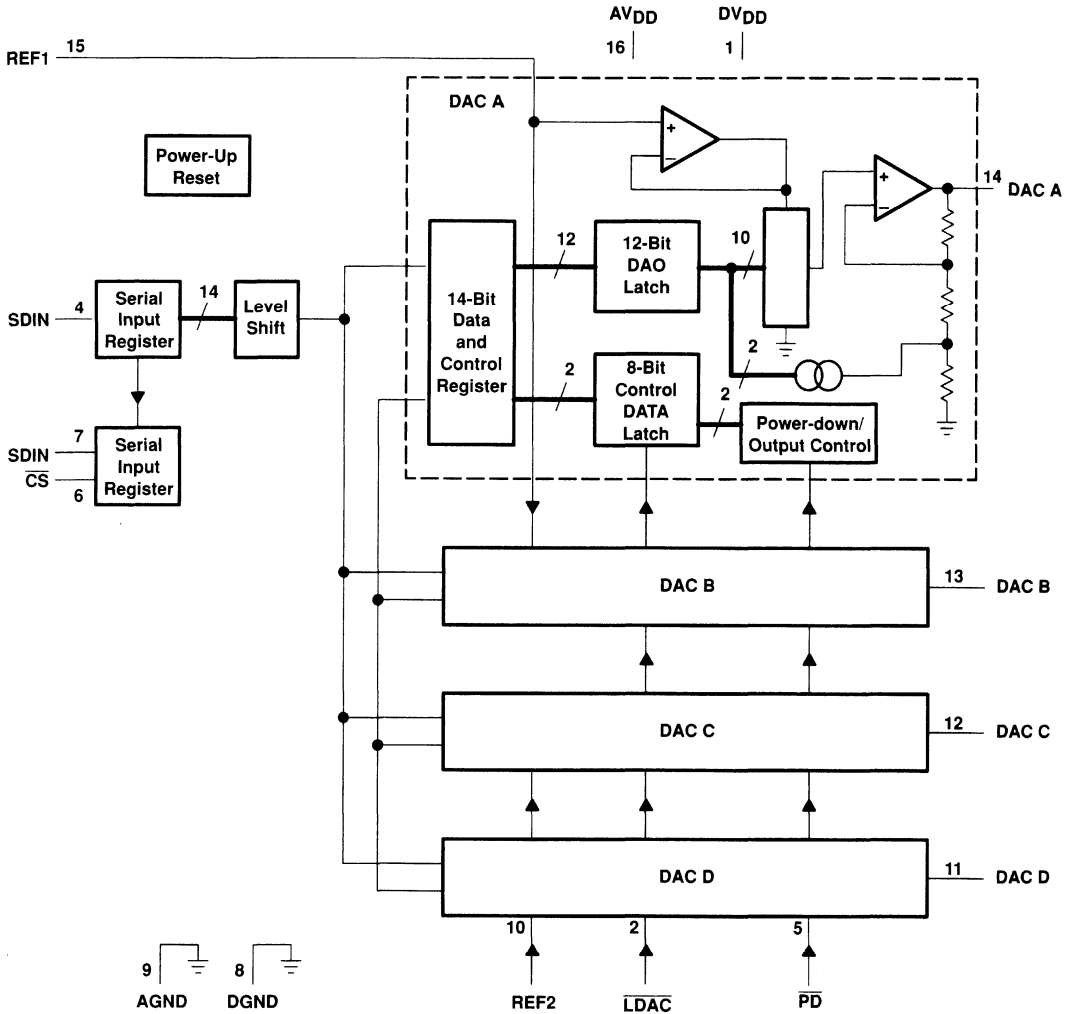
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TLC5614
3-V TO 5-V 12-BIT QUADRUPLE DIGITAL-TO-ANALOG CONVERTER
WITH POWERDOWN

SLAS175 – DECEMBER 1997

functional block diagram



PRODUCT PREVIEW

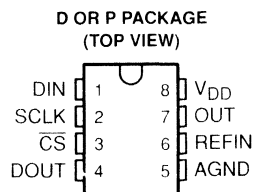


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TLC5615C, TLC5615I 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS142B – OCTOBER 1996 – REVISED MARCH 1997

- 10-Bit CMOS Voltage Output DAC in an 8-Terminal Package
- 5-V Single Supply Operation
- 3-Wire Serial Interface
- High-Impedance Reference Inputs
- Voltage Output Range . . . 2 Times the Reference Input Voltage
- Internal Power-On Reset
- Low Power Consumption . . . 1.75 mW Max
- Update Rate of 1.21 MHz
- Settling Time to 0.5 LSB . . . 12.5 μ s Typ
- Monotonic Over Temperature
- Pin Compatible with the Maxim MAX515



applications

- Battery-Powered Test Instruments
- Digital Offset and Gain Adjustment
- Battery Operated/Remote Industrial Controls
- Machine and Motion Control Devices
- Cellular Telephones

description

The TLC5615 is a 10-bit voltage output digital-to-analog converter (DAC) with a buffered reference input (high impedance). The DAC has an output voltage range that is two times the reference voltage, and the DAC is monotonic. The device is simple to use, running from a single supply of 5 V. A power-on-reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLC5615 is over a three-wire serial bus that is CMOS compatible and easily interfaced to industry standard microprocessor and microcontroller devices. The device receives a 16-bit data word to produce the analog output. The digital inputs feature Schmitt triggers for high noise immunity. Digital communication protocols include the SPI™, QSPI™, and Microwire™ standards.

The 8-terminal small-outline D package allows digital control of analog functions in space-critical applications. The TLC5615C is characterized for operation from 0 °C to 70 °C. The TLC5615I is characterized for operation from –40 °C to 85 °C.

AVAILABLE OPTIONS

PACKAGE		
T _A	SMALL OUTLINE† (D)	PLASTIC DIP (P)
0 °C to 70 °C	TLC5615CD	TLC5615CP
–40 °C to 85 °C	TLC5615ID	TLC5615IP

† Available in tape and reel as the TLC5615CDR and the TLC5615IDR

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corporation.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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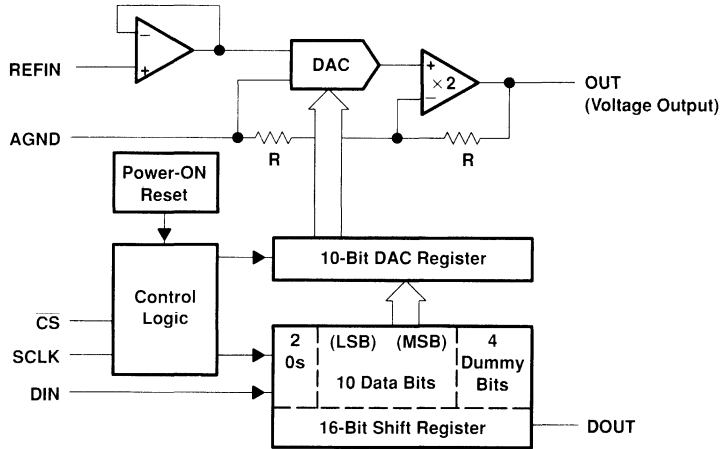
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TLC5615C, TLC5615I

10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS142B – OCTOBER 1996 – REVISED MARCH 1997

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
DIN	1	I	Serial data input
SCLK	2	I	Serial clock input
CS	3	I	Chip select, active low
DOUT	4	O	Serial data output for daisy chaining
AGND	5		Analog ground
REFIN	6	I	Reference input
OUT	7	O	DAC analog voltage output
V _{DD}	8		Positive power supply

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V _{DD} to AGND)	7 V
Digital input voltage range to AGND	-0.3 V to V _{DD} + 0.3 V
Reference input voltage range to AGND	-0.3 V to V _{DD} + 0.3 V
Output voltage at OUT from external source	V _{DD} + 0.3 V
Continuous current at any terminal	±20 mA
Operating free-air temperature range, T _A : TLC5615C	0°C to 70°C
TLC5615I	-40°C to 85°C
Storage temperature range, T _{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

TLC5615C, TLC5615I

10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS142B – OCTOBER 1996 – REVISED MARCH 1997

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	5	5.5	V
High-level digital input voltage, V_{IH}		2.4			V
Low-level digital input voltage, V_{IL}		0.8			V
Reference voltage, V_{ref} to REFIN terminal		2	2.048	$V_{DD}-2$	V
Load resistance, R_L		2			k Ω
Operating free-air temperature, T_A	TLC5615C	0		70	°C
	TLC5615I	-40		85	°C

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref} = 2.048\text{ V}$ (unless otherwise noted)

static DAC specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			10			bits
Integral nonlinearity, end point adjusted (INL)		$V_{ref} = 2.048\text{ V}$. See Note 1				± 1 LSB
Differential nonlinearity (DNL)		$V_{ref} = 2.048\text{ V}$. See Note 2	± 0.1		± 0.5	LSB
E _{ZS}	Zero-scale error (offset error at zero scale)	$V_{ref} = 2.048\text{ V}$. See Note 3				± 3 LSB
	Zero-scale-error temperature coefficient	$V_{ref} = 2.048\text{ V}$. See Note 4	3			ppm/°C
E _G	Gain error	$V_{ref} = 2.048\text{ V}$. See Note 5				± 3 LSB
	Gain-error temperature coefficient	$V_{ref} = 2.048\text{ V}$. See Note 6	1			ppm/°C
PSRR	Power-supply rejection ratio	Zero scale	80			dB
		Gain	80			
Analog full scale output		$R_L = 100\text{ k}\Omega$	$2V_{ref}(1023/1024)$			V

- NOTES:
- The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors (see text).
 - The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
 - Zero-scale error is the deviation from zero-voltage output when the digital input code is zero (see text).
 - Zero-scale-error temperature coefficient is given by: $E_{ZS} TC = [E_{ZS}(T_{max}) - E_{ZS}(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
 - Gain error is the deviation from the ideal output ($V_{ref} - 1\text{ LSB}$) with an output load of 10 k Ω excluding the effects of the zero-scale error.
 - Gain temperature coefficient is given by: $E_G TC = [E_G(T_{max}) - E_G(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
 - Zero-scale-error rejection ratio (E_{ZS}-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
 - Gain-error rejection ratio (E_G-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero-scale change.

voltage output (OUT)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _O	Voltage output range	$R_L = 10\text{ k}\Omega$	0	$V_{DD}-0.4$		V
Output load regulation accuracy		$V_{O(OUT)} = 2\text{ V}$. $R_L = 2\text{ k}\Omega$				0.5 LSB
I _{OSC}	Output short circuit current	OUT to V_{DD} or AGND	20			mA
V _{OL(low)}	Output voltage, low-level	$I_{O(OUT)} \leq 5\text{ mA}$	0.25			V
V _{OH(high)}	Output voltage, high-level	$I_{O(OUT)} \leq -5\text{ mA}$	4.75			V



TLC5615C, TLC5615I

10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS142B – OCTOBER 1996 – REVISED MARCH 1997

reference input (REFIN)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I Input voltage		0		$V_{DD}-2$	V
r_i Input resistance		10			$M\Omega$
C_i Input capacitance			5		pF

digital inputs (DIN, SCLK, \overline{CS})

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH} High-level digital input voltage		2.4			V
V_{IL} Low-level digital input voltage				0.8	V
I_{IH} High-level digital input current	$V_I = V_{DD}$			± 1	μA
I_{IL} Low-level digital input current	$V_I = 0$			± 1	μA
C_i Input capacitance			8		pF

digital output (DOUT)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} Output voltage, high-level	$I_O = -2$ mA	$V_{DD}-1$			V
V_{OL} Output voltage, low-level	$I_O = 2$ mA			0.4	V

power supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD} Supply voltage		4.5	5	5.5	V
I_{DD} Power supply current	$V_{DD} = 5.5$ V. No load. All inputs = 0 V or V_{DD}		150	250	μA
	$V_{DD} = 5.5$ V. No load. All inputs = 0 V or V_{DD}		230	350	μA

analog output dynamic performance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise + distortion, $S/(N+D)$	$V_{ref} = 1$ V _{pp} at 1 kHz + 2.048 V _{dc} . code = 11 1111 1111. See Note 9	60			dB

NOTE 9: The limiting frequency value at 1 V_{pp} is determined by the output-amplifier slew rate.

digital input timing requirements (see Figure 1)

PARAMETER	MIN	NOM	MAX	UNIT
$t_{su}(DS)$ Setup time, DIN before SCLK high	45			ns
$t_h(DH)$ Hold time, DIN valid after SCLK high	0			ns
$t_{su}(CSS)$ Setup time, \overline{CS} low to SCLK high	1			ns
$t_{su}(CS1)$ Setup time, \overline{CS} high to SCLK high	50			ns
$t_h(CSH0)$ Hold time, SCLK low to \overline{CS} low	1			ns
$t_h(CSH1)$ Hold time, SCLK low to \overline{CS} high	0			ns
$t_w(CS)$ Pulse duration, minimum chip select pulse width high	20			ns
$t_w(CL)$ Pulse duration, SCLK low	25			ns
$t_w(CH)$ Pulse duration, SCLK high	25			ns



TLC5615C, TLC5615I

10-BIT DIGITAL-TO-ANALOG CONVERTERS

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output switching characteristic

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{pd}(DOUT)$ Propagation delay time, DOUT	$C_L = 50 \text{ pF}$			50	ns

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5 \text{ V} \pm 5\%$, $V_{ref} = 2.048 \text{ V}$ (unless otherwise noted)

analog output dynamic performance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR Output slew rate	$C_L = 100 \text{ pF}$, $T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$,	0.3	0.5		V/ μs
t_s Output settling time	To 0.5 LSB, $R_L = 10 \text{ k}\Omega$, $C_L = 100 \text{ pF}$, See Note 10		12.5		μs
Glitch energy	DIN = All 0s to all 1s		5		nV*s

NOTE 10: Settling time is the time for the output signal to remain within ± 0.5 LSB of the final measured value for a digital input code change of 000 hex to 3FF hex or 3FF hex to 000 hex.

reference input (REFIN)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference feedthrough	REFIN = $1 V_{pp}$ at 1 kHz + 2.048 Vdc (see Note 11)		-80		dB
Reference input bandwidth (f-3dB)	REFIN = $0.2 V_{pp} + 2.048 \text{ Vdc}$ REFIN = $0.2 V_{pp} + 2.048 \text{ Vdc}$		30		kHz

NOTE 11: Reference feedthrough is measured at the DAC output with an input code = 000 hex and a V_{ref} input = $2.048 \text{ Vdc} + 1 V_{pp}$ at 1 kHz.

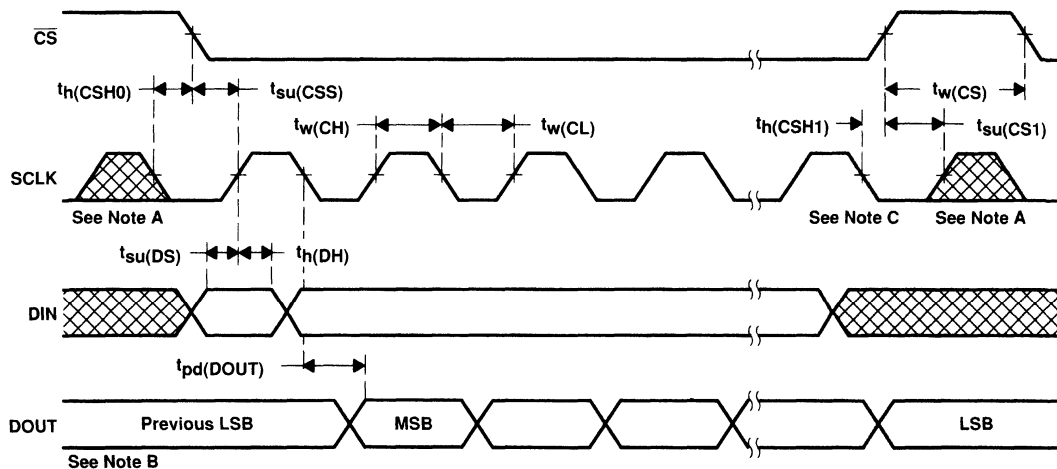


TLC5615C, TLC5615I

10-BIT DIGITAL-TO-ANALOG CONVERTERS

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input clock, applied at the SCLK terminal, should be inhibited low when \overline{CS} is high to minimize clock feedthrough.
 B. Data input from preceding conversion cycle.
 C. Sixteenth SCLK falling edge

Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

OUTPUT SINK CURRENT
vs
OUTPUT PULLDOWN VOLTAGE

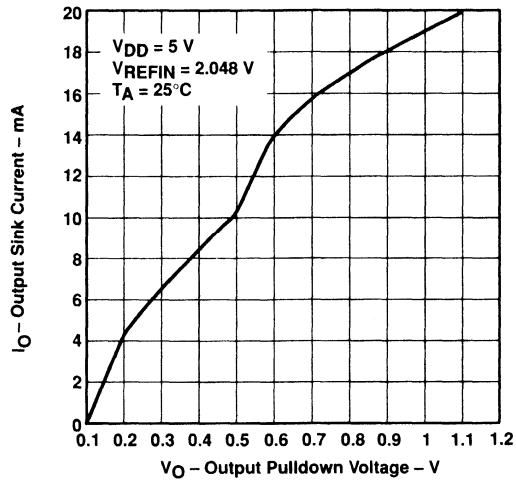


Figure 2

OUTPUT SOURCE CURRENT
vs
OUTPUT PULLUP VOLTAGE

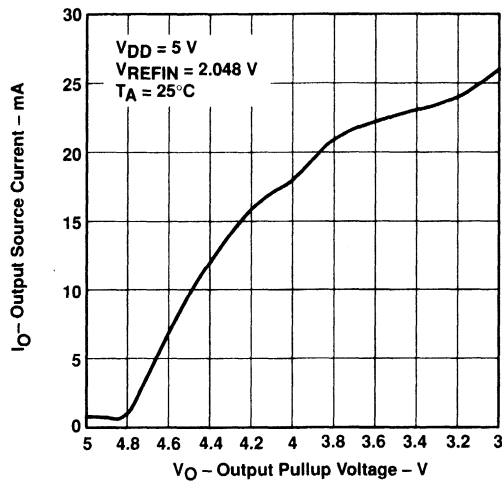


Figure 3

TLC5615C, TLC5615I 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS142B – OCTOBER 1996 – REVISED MARCH 1997

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
TEMPERATURE

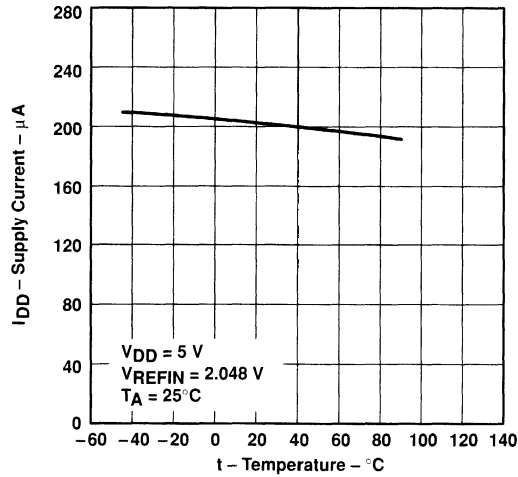


Figure 4

VREFIN TO V_(OUT)
RELATIVE GAIN
vs
INPUT FREQUENCY

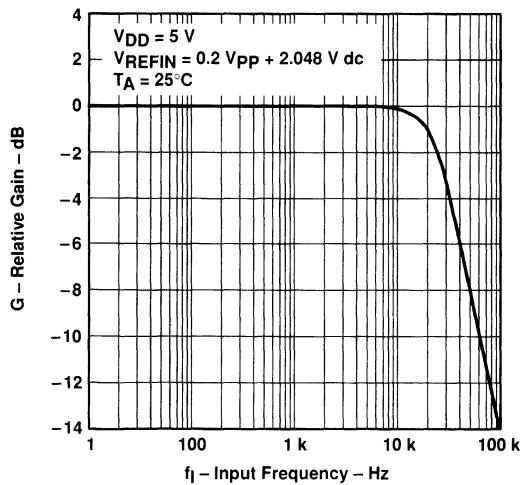


Figure 5

SIGNAL-TO-NOISE + DISTORTION
vs
INPUT FREQUENCY AT REF_{IN}

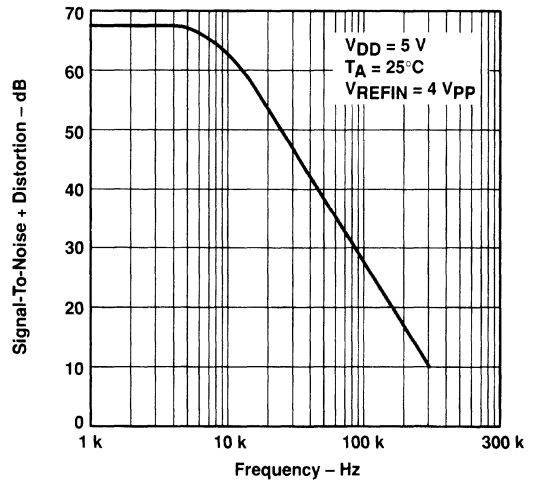


Figure 6



TYPICAL CHARACTERISTICS

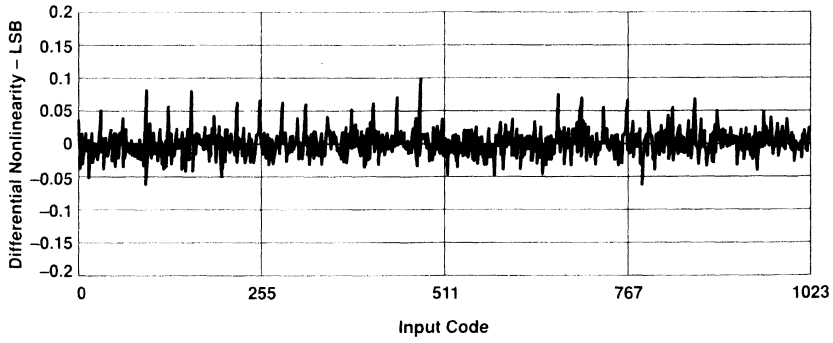


Figure 7. Differential Nonlinearity With Input Code

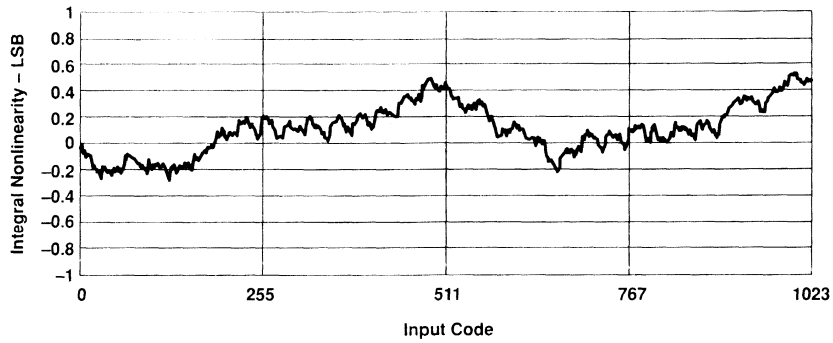


Figure 8. Integral Nonlinearity With Input Code

TLC5615C, TLC5615I

10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS142B – OCTOBER 1996 – REVISED MARCH 1997

APPLICATION INFORMATION

general function

The TLC5615 uses a resistor string network buffered with an op amp in a fixed gain of 2 to convert 10-bit digital data to analog voltage levels (see functional block diagram and Figure 9). The output of the TLC5615 is the same polarity as the reference input (see Table 1).

An internal circuit resets the DAC register to all zeros on power up.

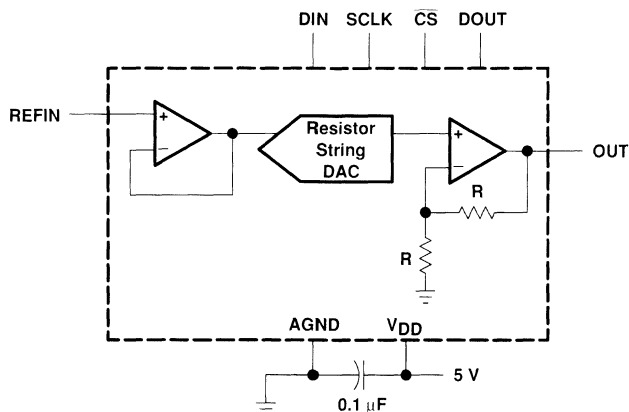


Figure 9. TLC5615 Typical Operating Circuit

Table 1. Binary Code Table (0 V to 2 V_{REFIN} Output), Gain = 2

INPUT†			OUTPUT
1111	1111	11(00)	$2(V_{REFIN}) \frac{1023}{1024}$
	:		:
1000	0000	01(00)	$2(V_{REFIN}) \frac{513}{1024}$
1000	0000	00(00)	$2(V_{REFIN}) \frac{512}{1024} = V_{REFIN}$
0111	1111	11(00)	$2(V_{REFIN}) \frac{511}{1024}$
	:		:
0000	0000	01(00)	$2(V_{REFIN}) \frac{1}{1024}$
0000	0000	00(00)	0 V

† A 10-bit data word with two bits below the LSB bit (sub-LSB) with 0 values must be written since the DAC input latch is 12 bits wide.

APPLICATION INFORMATION

buffer amplifier

The output buffer has a rail-to-rail output with short circuit protection and can drive a 2-k Ω load with a 100-pF load capacitance. Settling time is 12.5 μ s typical to within 0.5 LSB of final value.

external reference

The reference voltage input is buffered, which makes the DAC input resistance not code dependent. Therefore, the REFIN input resistance is 10 M Ω and the REFIN input capacitance is typically 5 pF independent of input code. The reference voltage determines the DAC full-scale output.

logic interface

The logic inputs function with either TTL or CMOS logic levels. However, using rail-to-rail CMOS logic achieves the lowest power dissipation. The power requirement increases by approximately 2 times when using TTL logic levels.

serial clock and update rate

Figure 1 shows the TLC5615 timing. The maximum serial clock rate is:

$$f_{(\text{SCLK})\text{max}} = \frac{1}{t_{w(\text{CH})} + t_{w(\text{CL})}}$$

or approximately 14 MHz. The digital update rate is limited by the chip-select period, which is:

$$t_{p(\text{CS})} = 16 \times (t_{w(\text{CH})} + t_{w(\text{CL})}) + t_{w(\text{CS})}$$

and is equal to 820 ns which is a 1.21 MHz update rate. However, the DAC settling time to 10 bits of 12.5 μ s limits the update rate to 80 kHz for full-scale input step transitions.

TLC5615C, TLC5615I

10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS142B – OCTOBER 1996 – REVISED MARCH 1997

APPLICATION INFORMATION

serial interface

When chip select (\overline{CS}) is low, the input data is read into a 16-bit shift register with the input data clocked in most significant bit first. The rising edge of the SCLK input shifts the data into the input register.

The rising edge of \overline{CS} then transfers the data to the DAC register. When \overline{CS} is high, input data cannot be clocked into the input register. All \overline{CS} transitions should occur when the SCLK input is low.

If the daisy chain (cascading) function (see daisy-chaining devices section) is not used, a 12-bit input data sequence with the MSB first can be used as shown in Figure 10:

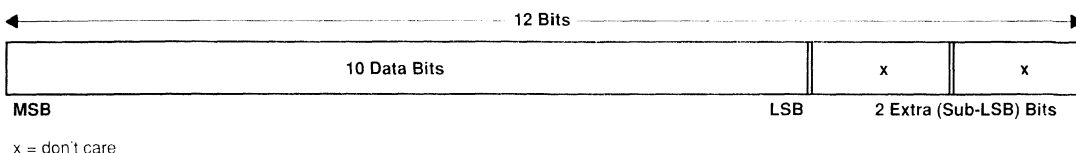


Figure 10. 12-Bit Input Data Sequence

or 16 bits of data can be transferred as shown in Figure 11 with the 4 upper dummy bits first.

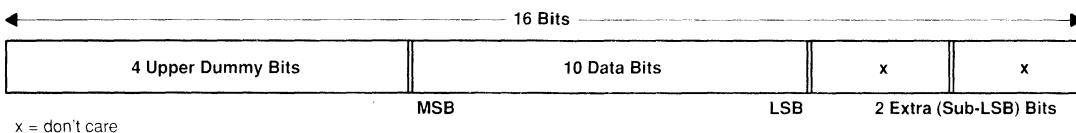


Figure 11. 16-Bit Input Data Sequence

The data from DOUT requires 16 falling edges of the input clock and, therefore, requires an extra clock width. When daisy chaining multiple TLC5615 devices, the data requires 4 upper dummy bits because the data transfer requires 16 input-clock cycles plus one additional input-clock falling edge to clock out the data at the DOUT terminal (see Figure 1).

The two extra (sub-LSB) bits are always required to provide hardware and software compatibility with 12-bit data converter transfers.

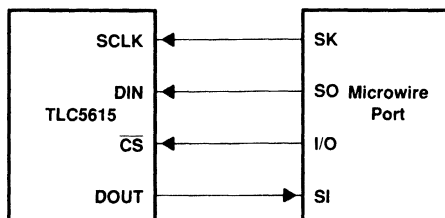
The TLC5615 three-wire interface is compatible with the SPI, QSPI†, and Microwire serial standards. The hardware connections are shown in Figure 12 and Figure 13.

The SPI and Microwire interfaces transfer data in 8-bit bytes, therefore, two write cycles are required to input data to the DAC. The QSPI interface, which has a variable input data length from 8 to 16 bits, can load the DAC input register in one write cycle.

† CPOL = 0, CPHA = 0, QSPI protocol designations

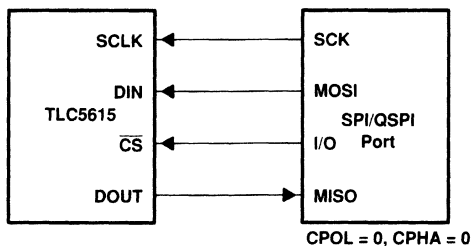
APPLICATION INFORMATION

serial interface (continued)



NOTE A: The DOUT-SI connection is not required for writing to the TLC5615 but may be used for verifying data transfer if desired.

Figure 12. Microwire Connection



NOTE A: The DOUT-MISO connection is not required for writing to the TLC5615 but may be used for verifying data transfer.

Figure 13. SPI/QSPI Connection

daisy-chaining devices

DACs can be daisy-chained by connecting the DOUT terminal of one device to the DIN of the next device in the chain, providing that the setup time, $t_{su(CSS)}$, (\overline{CS} low to SCLK high) is greater than the sum of the setup time, $t_{su(DS)}$, plus the propagation delay time, $t_{pd(DOUT)}$, for proper timing (see digital input timing requirements section). The data at DIN appears at DOUT, delayed by 16 clock cycles plus one clock width. DOUT is a totem-poled output for low power. DOUT changes on the SCLK falling edge when \overline{CS} is low. When \overline{CS} is high, DOUT remains at the value of the last data bit and does not go into a high-impedance state.

TLC5615C, TLC5615I

10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS142B – OCTOBER 1996 – REVISED MARCH 1997

APPLICATION INFORMATION

linearity, offset, and gain error using single ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 14.

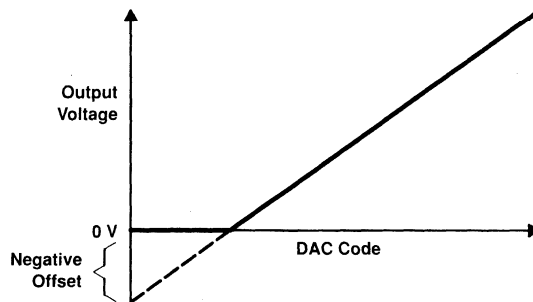


Figure 14. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. For the TLC5615, the zero-scale (offset) error is plus or minus 3 LSB maximum. The code is calculated from the maximum specification for the negative offset.

APPLICATION INFORMATION

power-supply bypassing and ground management

Printed circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane making sure that analog ground currents are well managed and there are negligible voltage drops across the ground plane.

A 0.1- μF ceramic-capacitor bypass should be connected between V_{DD} and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog supply from the digital power supply.

Figure 15 shows the ground plane layout and bypassing technique.

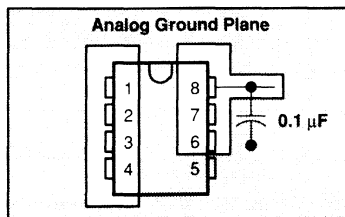


Figure 15. Power-Supply Bypassing

saving power

Setting the DAC register to all 0s minimizes power consumption by the reference resistor array and the output load when the system is not using the DAC.

ac considerations

digital feedthrough

Even with $\overline{\text{CS}}$ high, high-speed serial data at any of the digital input or output terminals may couple through the DAC package internal stray capacitance and appear at the DAC analog output as digital feedthrough. Digital feedthrough is tested by holding $\overline{\text{CS}}$ high and transmitting 0101010101 from DIN to DOUT.

analog feedthrough

Higher frequency analog input signals may couple to the output through internal stray capacitance. Analog feedthrough is tested by holding $\overline{\text{CS}}$ high, setting the DAC code to all 0s, sweeping the frequency applied to REFIN, and monitoring the DAC output.

TLC5616C, TLC5616I

2.7 V TO 5.5 V LOW POWER 12-BIT DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN

SLAS152 – DECEMBER 1997

- 12-Bit Voltage Output DAC
- Programmable Settling Time vs Power Consumption
 - 2.5 μ s in Fast Mode
 - 8.2 μ s in Slow Mode
- Compatible With TMS320 and SPI Serial Ports
- Differential Nonlinearity . . . <0.5 LSB Typ
- Ultra Low Power Consumption:
 - 600 μ W Typ in Slow Mode
 - 1.74 mW Typ in Fast Mode at 3 V
- Buffered High-Impedance Reference Input
- Voltage Output Range . . . 2 Times the Reference Input Voltage
- Monotonic Over Temperature

applications

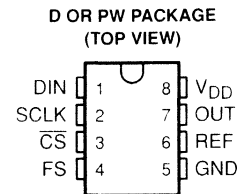
- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices

description

The TLC5616 is a 12-bit voltage output digital-to-analog converter (DAC) with a flexible 4-wire serial interface. The 4-wire serial interface allows seamless interface to TMS320 and SPI, QSPI, and Microwire serial ports. The TLC5616 is programmed by writing a 16-bit serial string into the device with four programming bits and 12 data bits. Developed for a wide range of supply voltages, the TLC5616 can operate from 2.7 V to 5.5 V.

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The buffer operates with a Class A output stage to improve stability and reduce settling time. The settling time of the DAC is programmable to allow the designer to optimize settling time versus power dissipation. The settling time of the DAC is easily toggled by programming one of the 16 bits loaded along with the data. A high-impedance buffer is integrated on the REF terminal to reduce the need to use a low source impedance drive to the terminal.

Implemented with a CMOS process, the TLC5616 is designed for single supply operation from 2.7 V to 5.5 V. The device is available in 8 terminal SOIC and TSSOP packages to reduce board space and is available in standard commercial and industrial temperature ranges. The TLC5616C is characterized for operation from 0°C to 70°C. The TLC5616I is characterized for operation from -40°C to 85°C.



PRODUCT PREVIEW

AVAILABLE OPTIONS

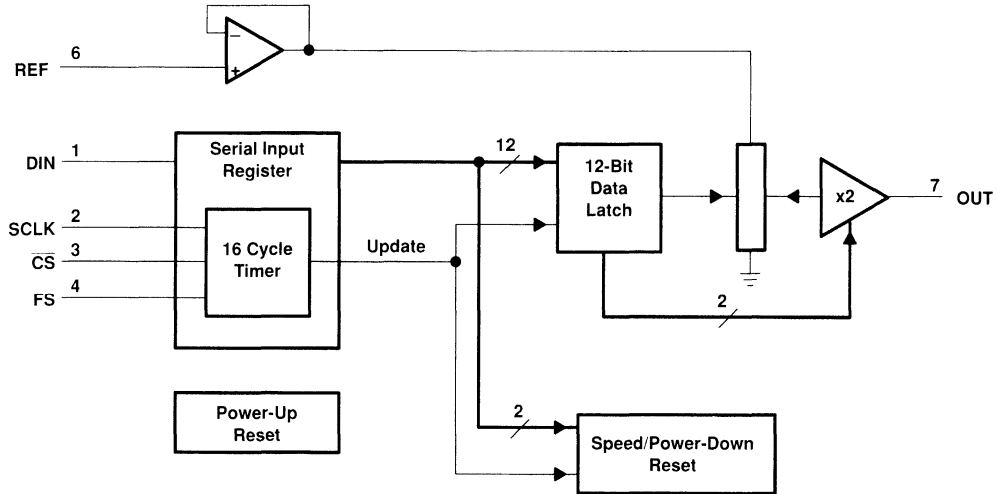
PACKAGE		
T _A	SMALL OUTLINE† (D)	SMALL OUTLINE (PW)
0°C to 70°C	TLC5616CD	TLC5616CPW
-40°C to 85°C	TLC5616ID	TLC5616IPW

† Available in tape and reel as the TLC5616CDR and the TLC5616IDR

TLC5616C, TLC5616I
2.7 V TO 5.5 V LOW POWER 12-BIT DIGITAL-TO-ANALOG
CONVERTERS WITH POWER DOWN

SLAS152 – DECEMBER 1997

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
$\overline{\text{CS}}$	3	I	Chip select. Digital output used to enable and disable inputs, active low.
DIN	1	I	Serial digital data input
FS	4	O	Frame sync. Digital input used for 4-wire serial interfaces such as the TMS320 DSP interface.
GND	5		Analog ground
OUT	7	O	DAC analog output
REF	6	I	Reference analog input voltage
SCLK	2	I	Serial digital clock input
VDD	8		Positive power supply

PRODUCT PREVIEW



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TLC5616C, TLC5616I
2.7 V TO 5.5 V LOW POWER 12-BIT DIGITAL-TO-ANALOG
CONVERTERS WITH POWER DOWN

SLAS152 – DECEMBER 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} to AGND)	7 V
Reference input voltage range	– 0.3 V to $V_{DD} + 0.3$ V
Digital input voltage range	– 0.3 V to $V_{DD} + 0.3$ V
Operating free-air temperature range, T_A : TLC5616C	0°C to 70°C
TLC5616I	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	5 V	4.5	5	5.5	V
	3 V	2.7	3	3.3	V
High-level digital input voltage, V_{IH}	V_{DD}	2			V
Low-level digital input voltage, V_{IL}	V_{DD}			0.8	V
Reference voltage, V_{ref} to REFIN terminal	5 V	GND	2.048	$V_{DD}-1.1$	V
Reference voltage, V_{ref} to REFIN terminal	3 V	GND	1.024	$V_{DD}-1.1$	V
Load resistance, R_L		2			k Ω
Load capacitance, C_L				100	pF
Operating free-air temperature, T_A	TLC5616C	0		70	°C
	TLC5616I	–40		85	°C

PRODUCT PREVIEW



TLC5616C, TLC5616I
2.7 V TO 5.5 V LOW POWER 12-BIT DIGITAL-TO-ANALOG
CONVERTERS WITH POWER DOWN

SLAS152 – DECEMBER 1997

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5 V \pm 10\%$, $V_{DD} = 3 V \pm 10\%$, $V_{ref} = 2.048 V$, $V_{ref} = 1.024 V$ (unless otherwise noted)

static DAC specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		$V_{ref} = 2.048 V, 1.024V$	12			bits
Integral nonlinearity (INL), end point adjusted		$V_{ref} = 2.048 V, 1.024V$ See Note 1			± 3	LSB
Differential nonlinearity (DNL)		$V_{ref} = 2.048 V, 1.024V$ See Note 2			± 0.5	LSB
E _{ZS}	Zero-scale error (offset error at zero scale)	$V_{ref} = 2.048 V, 1.024V$ See Note 3			± 12	LSB
Zero-scale-error temperature coefficient		$V_{ref} = 2.048 V, 1.024V$ See Note 4		3		ppm/°C
E _G	Gain error	$V_{ref} = 2.048 V, 1.024V$ See Note 5			± 0.29	% of FS voltage
Gain error temperature coefficient		$V_{ref} = 2.048 V, 1.024V$ See Note 6		1		ppm/°C
PSRR	Power supply rejection ratio	Zero scale n	5 V		-61	dB
		Full scale			-49	dB
		Zero scale	3 V		-45	dB
		Full scale			-49	dB

- NOTES:
1. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors (see text).
 2. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
 3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero (see text).
 4. Zero-scale-error temperature coefficient is given by: $E_{ZS} TC = [E_{ZS}(T_{max}) - E_{ZS}(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
 5. Gain error is the deviation from the ideal output ($V_{ref} - 1$ LSB) with an output load of 10 k Ω excluding the effects of the zero-error.
 6. Gain temperature coefficient is given by: $E_G TC = [E_G(T_{max}) - E_G(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
 7. Zero-scale-error rejection ratio (E_{ZS}-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
 8. Gain-error rejection ratio (E_G-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero scale change.

PRODUCT PREVIEW



TLC5616C, TLC5616I
2.7 V TO 5.5 V LOW POWER 12-BIT DIGITAL-TO-ANALOG
CONVERTERS WITH POWER DOWN

SLAS152 – DECEMBER 1997

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 10\%$, $V_{DD} = 3\text{ V} \pm 10\%$, $V_{ref} = 2.048\text{ V}$, $V_{ref} = 1.024\text{ V}$ (unless otherwise noted) (Continued)

output specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O Output voltage	$R_L = 2\text{ k}\Omega$		$V_{DD}-0.1$		V
Output load regulation accuracy	$V_{O(OUT)} = 4.096\text{ V}$, $R_L = 2\text{ k}\Omega$ 2.048 V				% of FS Voltage
I_{OSC} Output short circuit current				20	mA
$I_{O(sink)}$ Output sink current					mA
$I_{O(source)}$ Output source current					mA

reference input (REF)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I Input voltage		0	$V_{DD}-1.1$		V
R_i Input resistance			10		M Ω
C_i Input capacitance			5		pF
Reference input bandwidth	REFIN = $0.2 V_{pp} + 1.024\text{ V dc}$	Fast	1.3		MHz
		Slow	525		kHz
Harmonic distortion, reference input	REFIN = $1 V_{pp} + 1.024\text{ V dc}$, frequency = 10 kHz	Fast	-73		dB
	REFIN = $1 V_{pp} + 1.024\text{ V dc}$, frequency = 100 kHz	Fast	-51		dB
	REFIN = $1 V_{pp} + 1.024\text{ V dc}$, frequency = 200 kHz	Fast	-36		dB
	REFIN = $1 V_{pp} + 1.024\text{ V dc}$, frequency = 10 kHz	Slow	-78		dB
	REFIN = $1 V_{pp} + 1.024\text{ V dc}$, frequency = 50 kHz	Slow	-41		dB
Reference feedthrough	REFIN = $1 V_{pp}$ at 1 kHz + 1.024 V dc (see Note 9)		-80		dB

NOTE 9: Reference feedthrough is measured at the DAC output with an input code = 000 hex and a V_{ref} input = $1.024\text{ V dc} + 1 V_{pp}$ at 1 kHz.

digital inputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH} High-level digital input current	$V_I = V_{DD}$			± 1	μA
I_{IL} Low-level digital input current	$V_I = 0\text{ V}$			± 1	μA
C_i Input capacitance			8		pF

power supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD} Power supply current	$V_{DD} = 5\text{ V}$, No load, All inputs = 0 V or V_{DD}	Fast	0.67	1	mA
		Slow	0.28	0.4	mA
	$V_{DD} = 3\text{ V}$, No load, All inputs = 0 V or V_{DD}	Fast	0.58	0.9	mA
		Slow	0.20	0.30	mA
Power down supply current		0.18	0.30		μA

PRODUCT PREVIEW



TLC5616C, TLC5616I

2.7 V TO 5.5 V LOW POWER 12-BIT DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN

SLAS152 – DECEMBER 1997

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 10\%$, $V_{ref} = 2.048\text{ V}$, (unless otherwise noted)

analog output dynamic performance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{s(FS)}$ Output settling time, full scale	$V_{DD} = 5\text{ V}$, To 0.5 LSB, $C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, See Note 10	Fast	2.5	3.9	μs
		Slow	8.2	18.1	μs
	$V_{DD} = 3\text{ V}$, To 0.5 LSB, $C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, See Note 10	Fast	3.2	5.3	μs
		Slow	5.7	20.4	μs
$t_{s(CC)}$ Output settling time, code to code	$V_{DD} = 5\text{ V}$, To 0.5 LSB, $C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, See Note 11	Fast			μs
		Slow			μs
	$V_{DD} = 3\text{ V}$, To 0.5 LSB, $C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, See Note 11	Fast			μs
		Slow			μs
SR Output slew rate	$V_{DD} = 5\text{ V}$, To 0.5 LSB, $C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$	Fast	3		$\text{V}/\mu\text{s}$
		Slow	0.6		$\text{V}/\mu\text{s}$
	$V_{DD} = 3\text{ V}$, To 0.5 LSB, $C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$	Fast	2.8		$\text{V}/\mu\text{s}$
		Slow	0.6		$\text{V}/\mu\text{s}$
Signal to noise + distortion, $S/(N+D)$					dB

NOTES: 10. Settling time is the time for the output signal to remain within ± 0.5 LSB of the final measured value for a digital input code change of 000 hex to 3FF hex or 3FF hex to 000 hex.

11. Settling time is the time for the output signal to remain within ± 0.5 LSB of the final measured value for a digital input code change of one count.

digital input timing requirements

	MIN	NOM	MAX	UNIT
$t_{su}(CS-FS)$ Setup time, CS low before FS \downarrow	10			ns
$t_{su}(FS-CLK)$ Setup time, FS low before first negative SCLK edge	10			ns
$t_{su}(C16-FS)$ Setup time, sixteenth negative edge after FS low on which bit D0 is sampled before rising edge of FS	10			ns
$t_{su}(C16-CS)$ Setup time, sixteenth positive CLK edge (first positive after D0 is sampled) before CS rising edge. Or is FS is used instead of sixteenth positive edge to update DAC, then setup time between FS rising edge and CS rising edge.	10			ns
t_{wH} Pulse duration, SCLK high	25			ns
t_{wL} Pulse duration, SCLK low	25			ns
$t_{su}(D)$ Setup time, data ready before SCLK falling edge	8			ns
$t_{h}(D)$ Hold time, data held valid after SCLK falling edge	5			ns
$t_d(CS1)$ Delay time, positive clock edge after D0 sampled to internal latch (and shift register) control high			5	μs

PRODUCT PREVIEW



TLC5616C, TLC5616I
 2.7 V TO 5.5 V LOW POWER 12-BIT DIGITAL-TO-ANALOG
 CONVERTERS WITH POWER DOWN
SLAS152 – DECEMBER 1997

PARAMETER MEASUREMENT INFORMATION

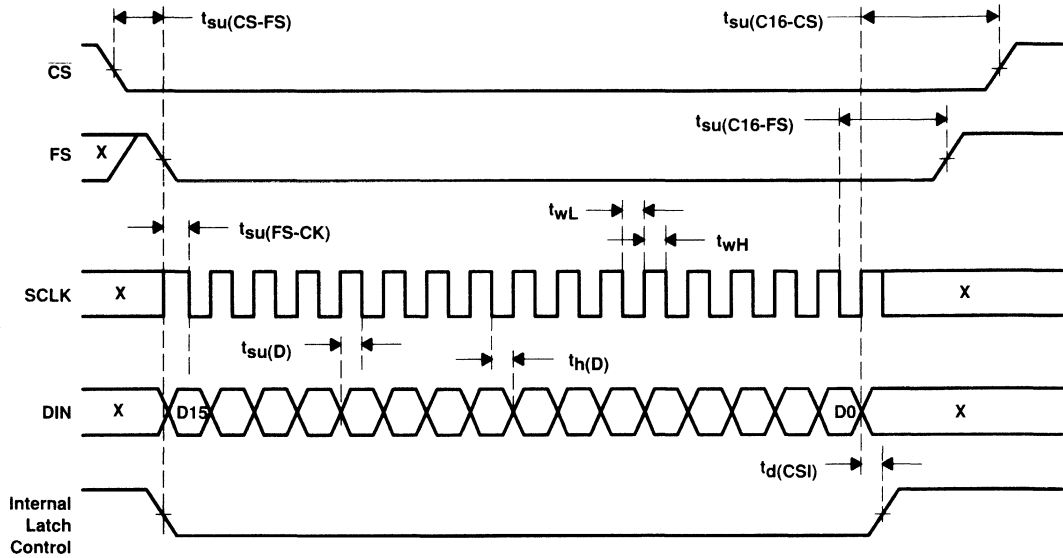


Figure 1. Timing Diagram

PRODUCT PREVIEW

PRODUCT PREVIEW

TLC5617, TLC5617A PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS151A – JULY 1997 – REVISED DECEMBER 1997

- Programmable Settling Time to 0.5 LSB
2.5 μ s or 12.5 μ s Typ
- Two 10-Bit CMOS Voltage Output DACs in
an 8 Pin Package
- Simultaneous Updates for DAC A
and DAC B
- Single Supply Operation
- 3-Wire Serial Interface
- High-Impedance Reference Inputs
- Voltage Output Range . . . 2 Times the
Reference Input Voltage
- Software Power Down Mode
- Internal Power-On Reset
- TMS320 and SPI Compatible
- Low Power Consumption:
3 mW Typ in Slow Mode
8 mW Typ in Fast Mode
- Input Data Update Rate of 1.21 MHz
- Monotonic Over Temperature

applications

- Battery Powered Test Instruments
- Digital Offset and Gain Adjustment
- Battery Operated/Remote Industrial
Controls
- Machine and Motion Control Devices
- Cellular Telephones

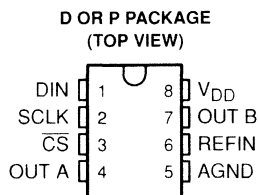
description

The TLC5617 and TLC5617A are dual 10-bit voltage output digital-to-analog converters (DAC) with buffered reference inputs (high impedance). The DACs have an output voltage range that is two times the reference voltage, and the DACs are monotonic. The device is simple to use, running from a single supply of 5 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLC5617 is over a 3-wire CMOS compatible serial bus. The device receives a 16-bit word for programming and to produce the analog output. The digital inputs feature Schmitt triggers for high noise immunity. Digital communication protocols include the SPI™, QSPI™, and Microwire™ standards.

Two versions of this device are available. The TLC5617 does not have any internal state machine and is dependent on all external timing signals. The TLC5617A has an internal state machine that will count the number of clocks from falling edge of \overline{CS} and then update and disable the device to accepting further data inputs. The TLC5617A is recommended for TMS320 and SPI processors and the TLC5617 is recommended only for use in SPI or 3-wire serial port processors. The TLC5617A is backward compatible and designed to work in TLC5617 designed systems.

The 8-terminal small-outline D package allows digital control of analog functions in space-critical applications. The TLC5617C is characterized for operation from 0°C to 70°C. The TLC5617I is characterized for operation from -40°C to 85°C.



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 **TEXAS
INSTRUMENTS**

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SLAS151A – JULY 1997 – REVISED DECEMBER 1997

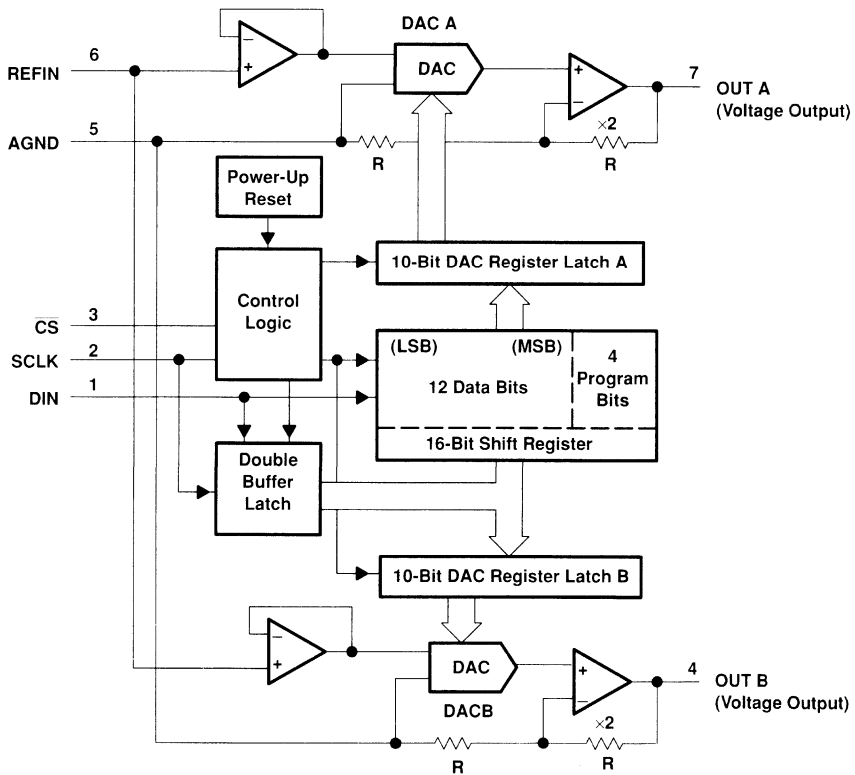
AVAILABLE OPTIONS

PACKAGE		
T _A	SMALL OUTLINE† (D)	PLASTIC DIP (P)
0°C to 70°C	TLC5617CD TLC5617ACD	TLC5617CP TLC5617ACP
-40°C to 85°C	TLC5617ID TLC5617AID	TLC5617IP TLC5617AIP

† Available in tape and reel as the TLC5617CDR and the TLC5617IDR

DEVICE	COMPATIBILITY
TLC5617	SPI, QSPI and Microwire
TLC5617A	TMS320Cxx, SPI, QSPI and Microwire

functional block diagram



TLC5617, TLC5617A PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS151A – JULY 1997 – REVISED DECEMBER 1997

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
DIN	1	I	Serial data input
SCLK	2	I	Serial clock input
CS	3	I	Chip select, active low
OUT B	4	O	DAC B analog output
AGND	5		Analog ground
REFIN	6	I	Reference voltage input
OUT A	7	O	DAC A analog output
VDD	8		Positive power supply

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} to AGND)	7 V
Digital input voltage range to AGND	-0.3 V to $V_{DD} + 0.3$ V
Reference input voltage range to AGND	-0.3 V to $V_{DD} + 0.3$ V
Output voltage at OUT from external source	$V_{DD} + 0.3$ V
Continuous current at any terminal	± 20 mA
Operating free-air temperature range, T_A : TLC5617C	0°C to 70°C
TLC5617I	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	5	5.5	V
High-level digital input voltage, V_{IH}	$V_{DD} = 5$ V	0.7 V_{DD}			V
Low-level digital input voltage, V_{IL}	$V_{DD} = 5$ V	0.3 V_{DD}			V
Reference voltage, V_{ref} to REFIN terminal		1	2.048	$V_{DD} - 1.1$	V
Load resistance, R_L		2			k Ω
Operating free-air temperature, T_A	TLC5617C	0		70	°C
	TLC5617I	-40		85	°C



TLC5617, TLC5617A PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS151A – JULY 1997 – REVISED DECEMBER 1997

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref}(\text{REFIN}) = 2.048\text{ V}$ (unless otherwise noted)

static DAC specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			10			bits
Integral nonlinearity (INL), end point adjusted		$V_{ref}(\text{REFIN}) = 2.048\text{ V}$. See Note 1			± 1	LSB
Differential nonlinearity (DNL)		$V_{ref}(\text{REFIN}) = 2.048\text{ V}$. See Note 2		± 0.1	± 0.5	LSB
E _{ZS}	Zero-scale error (offset error at zero scale)	$V_{ref}(\text{REFIN}) = 2.048\text{ V}$. See Note 3			± 3	LSB
Zero-scale-error temperature coefficient		$V_{ref}(\text{REFIN}) = 2.048\text{ V}$. See Note 4		3		ppm/°C
E _G	Gain error	$V_{ref}(\text{REFIN}) = 2.048\text{ V}$. See Note 5			± 3	LSB
Gain error temperature coefficient		$V_{ref}(\text{REFIN}) = 2.048\text{ V}$. See Note 6		1		ppm/°C
PSRR	Power-supply rejection ratio	Zero scale Gain Zero scale Gain	See Notes 7 and 8	Slow	80	dB
					80	
				Fast	80	
					80	

- NOTES:
- The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.
 - The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
 - Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
 - Zero-scale-error temperature coefficient is given by: $E_{ZS} \text{ TC} = [E_{ZS}(T_{max}) - E_{ZS}(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
 - Gain error is the deviation from the ideal output ($V_{ref} - 1\text{ LSB}$) with an output load of $10\text{ k}\Omega$ excluding the effects of the zero-error.
 - Gain temperature coefficient is given by: $E_G \text{ TC} = [E_G(T_{max}) - E_G(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
 - Zero-scale-error rejection ratio (E_{ZS}-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
 - Gain-error rejection ratio (E_G-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero scale change.

A OUT and B OUT output specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _O	Voltage output range	$R_L = 10\text{ k}\Omega$	0		$V_{DD} - 0.4$	V
Output load regulation accuracy		$V_{O}(\text{OUT}) = 2\text{ V}$, R_L from $10\text{ k}\Omega$ to $2\text{ k}\Omega$			0.5	LSB
I _{OSC}	Output short circuit current	$V_{O}(\text{A OUT})$ or $V_{O}(\text{B OUT})$ to V_{DD} or AGND		20		mA
I _{O(sink)}	Output sink current	$V_{O}(\text{OUT}) > 0.25\text{ V}$		5		mA
I _{O(source)}	Output source current	$V_{O}(\text{OUT}) < 4.75\text{ V}$		5		mA

reference input (REFIN)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _I	Input voltage range		0		$V_{DD} - 2$	V
R _I	Input resistance		10			M Ω
C _I	Input capacitance			5		pF
Reference feedthrough		REFIN = 1 V_{pp} at 1 kHz + 1.024 V dc (see Note 9)		-80		dB
Reference input bandwidth (f _{-3dB})		REFIN = 0.2 V_{pp} + 1.024 V dc	Slow	0.5		MHz
			Fast	1		

NOTE 9: Reference feedthrough is measured at the DAC output with an input code = 00 hex and a $V_{ref}(\text{REFIN})$ input = 1.024 V dc + 1 V_{pp} at 1 kHz.



TLC5617, TLC5617A

PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS151A – JULY 1997 – REVISED DECEMBER 1997

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref}(\text{REFIN}) = 2.048\text{ V}$ (unless otherwise noted) (continued)

digital inputs (DIN, SCLK, $\overline{\text{CS}}$)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH} High-level digital input current	$V_I = V_{DD}$			± 1	μA
I_{IL} Low-level digital input current	$V_I = 0\text{ V}$			± 1	μA
C_i Input capacitance			8		pF

power supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage, V_{DD}		4.5	5	5.5	V
I_{DD} Power supply current	$V_{DD} = 5.5\text{ V}$, No load, All inputs = 0 V or V_{DD}	Slow	0.6	1	mA
		Fast	1.6	2.5	
Power down supply current	D13 = 0 (see Table 3)		1		μA

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref}(\text{REFIN}) = 2.048\text{ V}$ (unless otherwise noted)

analog output dynamic performance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR Output slew rate	$C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, Code 32 to Code 1024, $V_{ref}(\text{REFIN}) = 2.048\text{ V}$, $T_A = 25^\circ\text{C}$, V_O from 10% to 90%	Slow	0.3	0.5	V/ μs
		Fast	2.4	3	
t_s Output settling time	$T_o \pm 0.5\text{ LSB}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, See Note 10	Slow	12.5		μs
		Fast	2.5		
$t_{s(c)}$ Output settling time, code to code	$T_o \pm 0.5\text{ LSB}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, See Note 11	Slow	2		μs
		Fast	2		
Glitch energy	DIN = All 0s to all 1s, $f(\text{SCLK}) = 100\text{ kHz}$, $\overline{\text{CS}} = V_{DD}$		5		nV-s
S/(N+D) Signal to noise + distortion	$V_{ref}(\text{REFIN}) = 1\text{ V}_{pp}$ at 1 kHz and 10 kHz + 1.024 V dc, Input code = 10 0000 0000	Slow	78		dB
		Fast	81		

NOTES: 10. Settling time is the time for the output signal to remain within $\pm 0.5\text{ LSB}$ of the final measured value for a digital input code change of 020 hex to 3FF hex or 3FF hex to 020 hex.

11. Settling time is the time for the output signal to remain within $\pm 0.5\text{ LSB}$ of the final measured value for a digital input code change of one count.

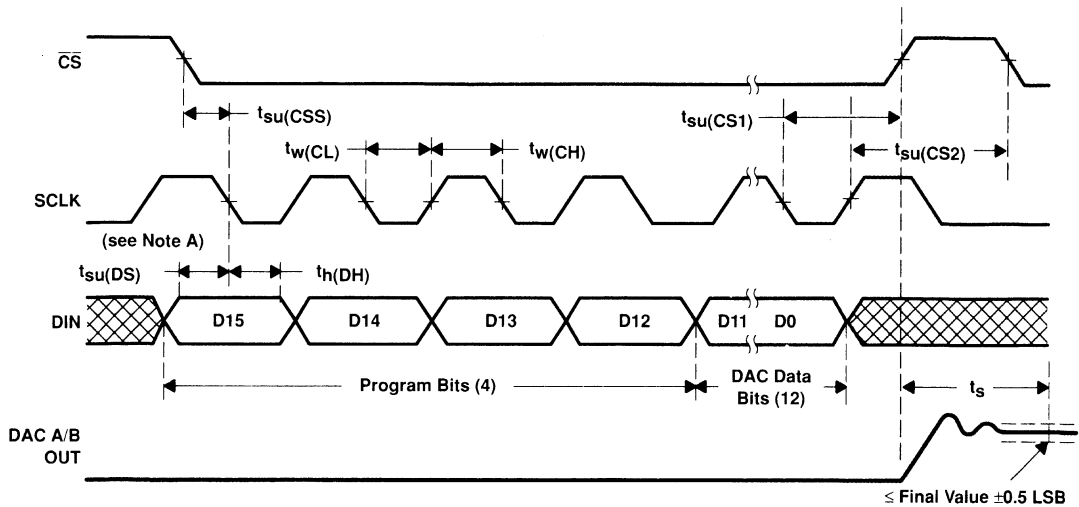
digital input timing requirements

	MIN	NOM	MAX	UNIT
$t_{su}(\text{DS})$ Setup time, DIN before SCLK low	5			ns
$t_{h}(\text{DH})$ Hold time, DIN valid after SCLK low	5			ns
$t_{su}(\text{CSS})$ Setup time, $\overline{\text{CS}}$ low to SCLK low	5			ns
$t_{su}(\text{CS1})$ Setup time, SCLK \uparrow to $\overline{\text{CS}}$ \downarrow , external end-of-write	10			ns
$t_{su}(\text{CS2})$ Setup time, SCLK \uparrow to $\overline{\text{CS}}$ \downarrow , start of next write cycle	5			ns
$t_w(\text{CL})$ Pulse duration, SCLK low	25			ns
$t_w(\text{CH})$ Pulse duration, SCLK high	25			ns
$t_d(\text{CS1})$ Delay time, CLK \uparrow to Disable (TLC5617A only)			5	ns



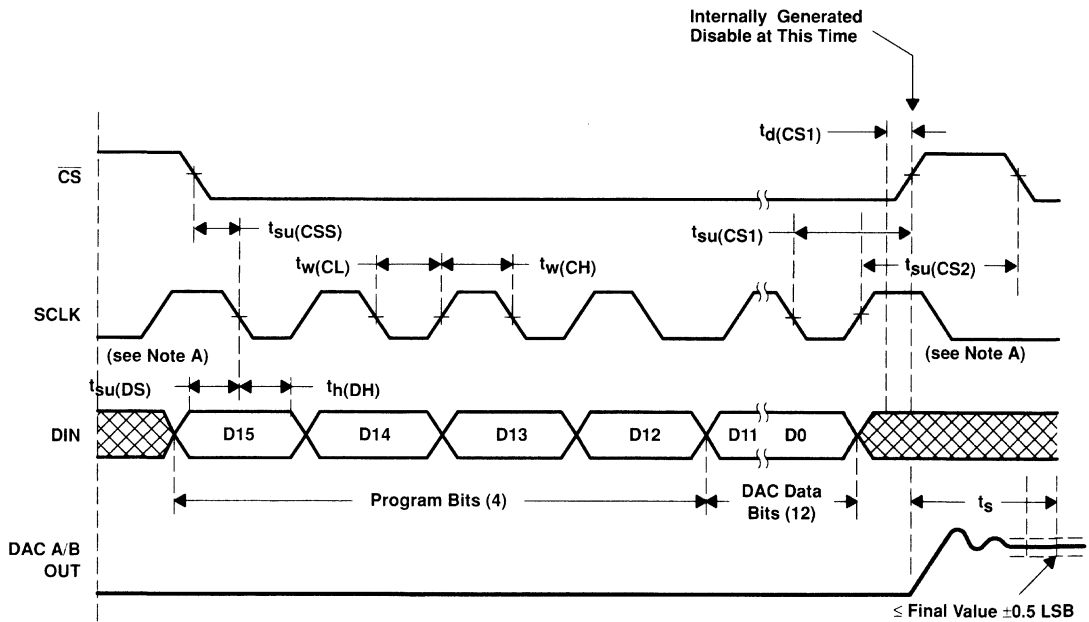
TLC5617, TLC5617A PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS151A – JULY 1997 – REVISED DECEMBER 1997



NOTE B: The input clock, applied at the SCLK terminal, should be inhibited low when \overline{CS} is high to minimize clock feedthrough.

Figure 1. Timing Diagram for the TLC5617



NOTE C: The input clock, applied at the SCLK terminal, should be inhibited low when \overline{CS} is high to minimize clock feedthrough.

Figure 2. Timing Diagram for TLC5617A only

TLC5617, TLC5617A PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS151A – JULY 1997 – REVISED DECEMBER 1997

TYPICAL CHARACTERISTICS

**OUTPUT SINK CURRENT (FAST MODE)
vs
OUTPUT LOAD VOLTAGE**

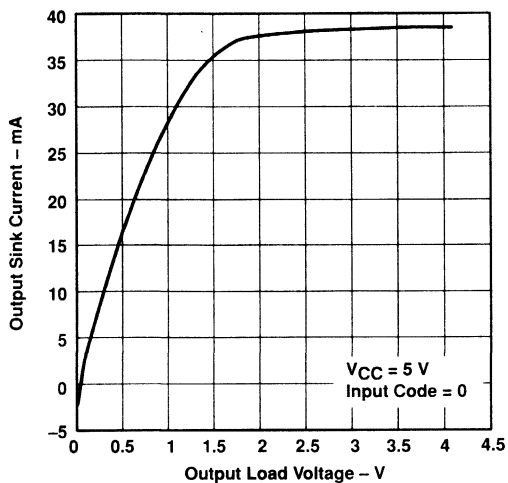


Figure 3

**OUTPUT SOURCE CURRENT (FAST MODE)
vs
OUTPUT LOAD VOLTAGE**

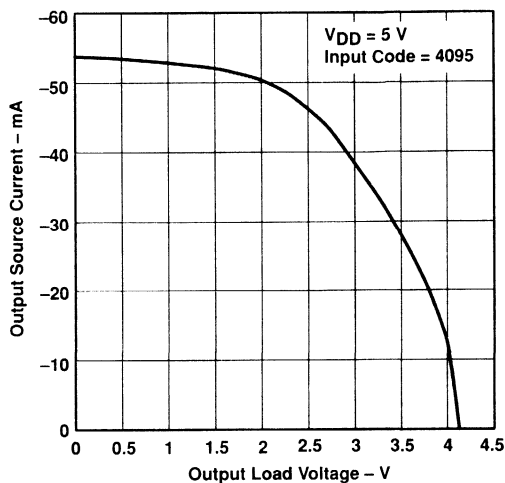


Figure 4

**OUTPUT SINK CURRENT (SLOW MODE)
vs
OUTPUT LOAD VOLTAGE**

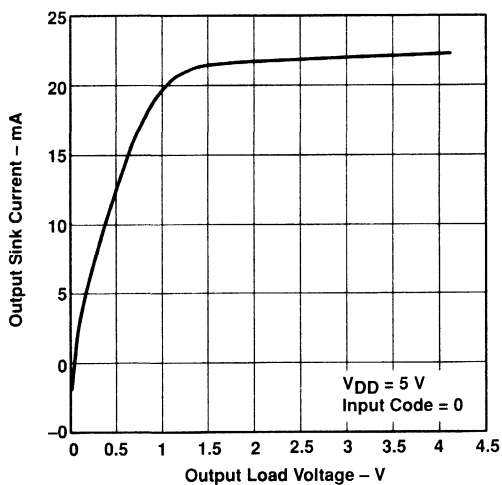


Figure 5

**OUTPUT SOURCE CURRENT (SLOW MODE)
vs
OUTPUT LOAD VOLTAGE**

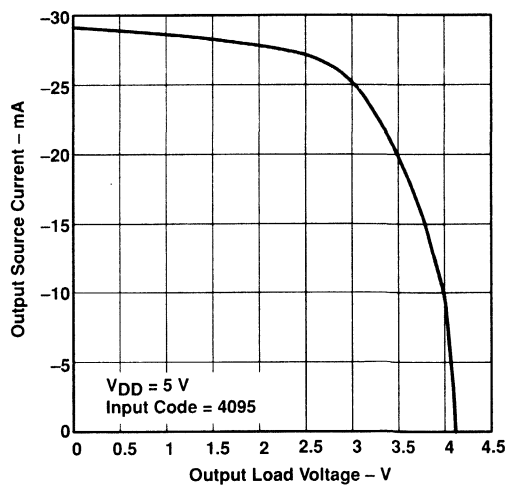


Figure 6



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SLAS151A – JULY 1997 – REVISED DECEMBER 1997

TYPICAL CHARACTERISTICS

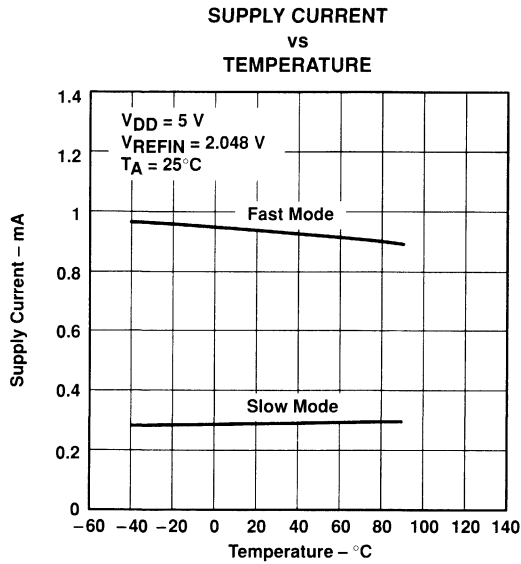


Figure 7

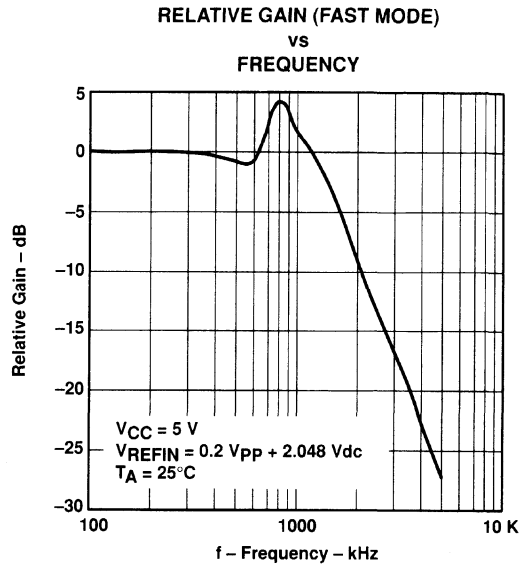


Figure 8

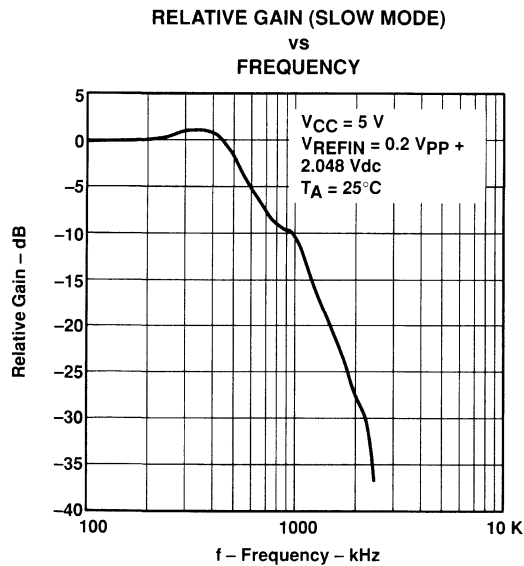


Figure 9

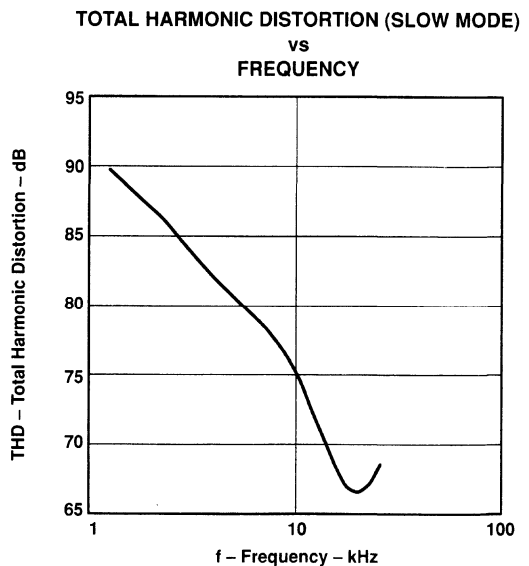


Figure 10

TLC5617, TLC5617A PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS151A – JULY 1997 – REVISED DECEMBER 1997

TYPICAL CHARACTERISTICS

**TOTAL HARMONIC DISTORTION + NOISE (SLOW MODE)
vs
FREQUENCY**

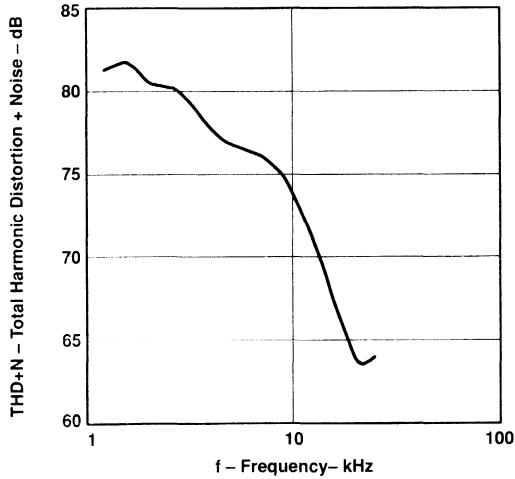


Figure 11

**SIGNAL-TO-NOISE RATIO (SLOW MODE)
vs
FREQUENCY**

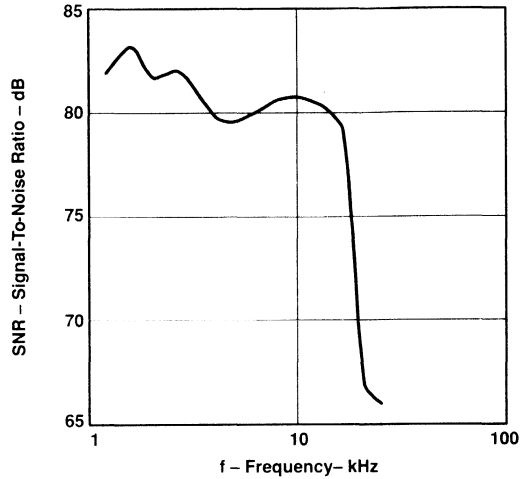


Figure 12

**TOTAL HARMONIC DISTORTION (FAST MODE)
vs
FREQUENCY**

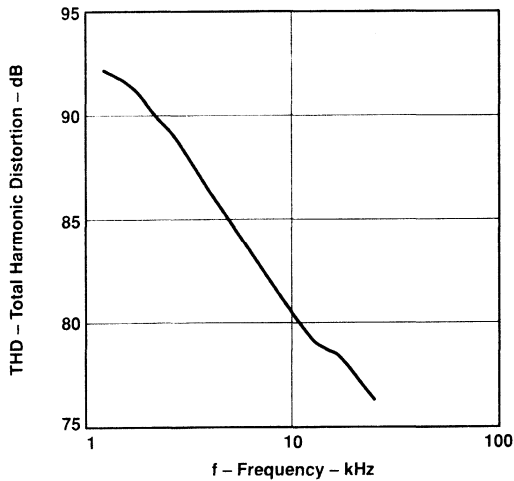


Figure 13

**TOTAL HARMONIC DISTORTION + NOISE (FAST MODE)
vs
FREQUENCY**

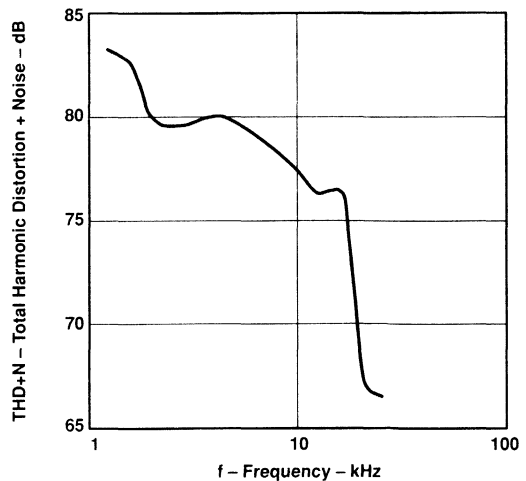


Figure 14



TLC5617, TLC5617A PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

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TYPICAL CHARACTERISTICS

SIGNAL-TO-NOISE RATIO (FAST MODE)
vs
FREQUENCY

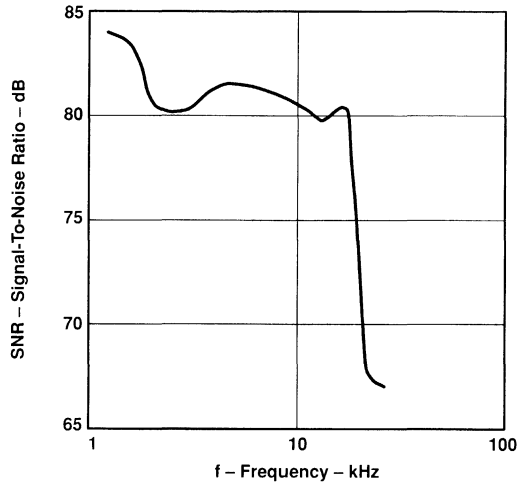


Figure 15

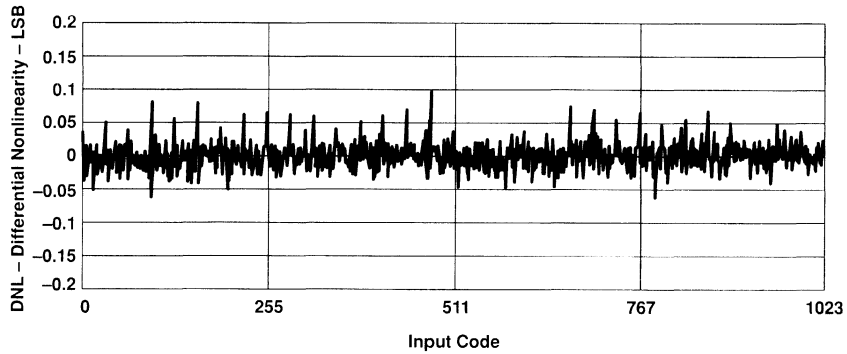


Figure 16. Differential Nonlinearity With Input Code

TLC5617, TLC5617A PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS151A – JULY 1997 – REVISED DECEMBER 1997

TYPICAL CHARACTERISTICS

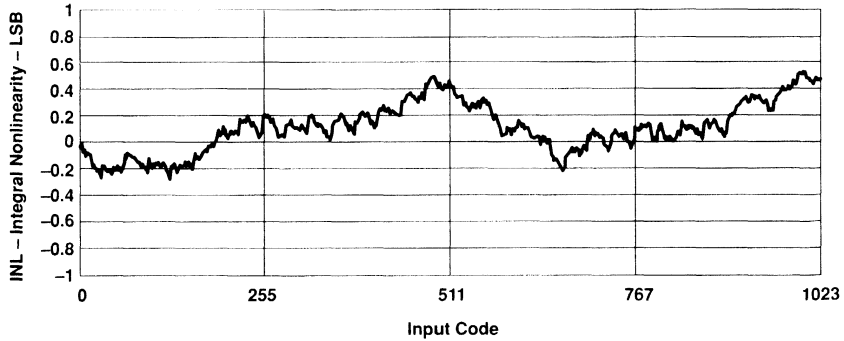


Figure 17. Integral Nonlinearity With Input Code

APPLICATION INFORMATION

general function

The TLC5617 uses a resistor string network buffered with an op amp to convert 10-bit digital data to analog voltage levels (see functional block diagram and Figure 17). The output of the TLC5617 is the same polarity as the reference input (see Table 1).

The output code is given by: $2 \left(V_{REFIN} \right) \frac{CODE}{1024}$

An internal circuit resets the DAC register to all 0s on power-up.

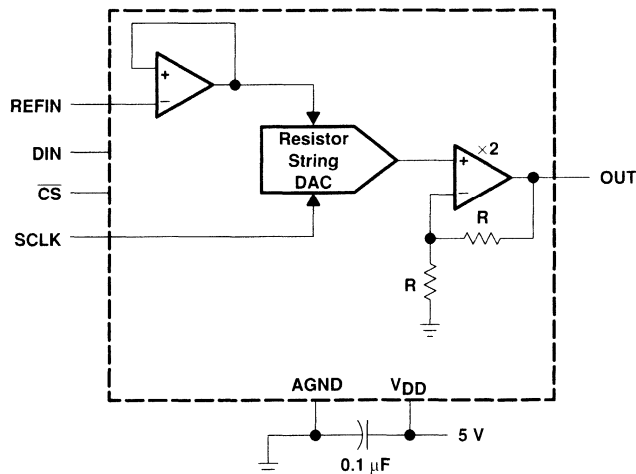


Figure 18. TLC5617 Typical Operating Circuit

TLC5617, TLC5617A PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS151A – JULY 1997 – REVISED DECEMBER 1997

APPLICATION INFORMATION

Table 1. Binary Code Table (0 V to 2 V_{REFIN} Output), Gain = 2

INPUT†			OUTPUT
1111	1111	11(00)	$2(V_{REFIN}) \frac{1023}{1024}$
	:		:
1000	0000	01(00)	$2(V_{REFIN}) \frac{513}{1024}$
1000	0000	00(00)	$2(V_{REFIN}) \frac{512}{1024} = V_{REFIN}$
0111	1111	11(00)	$2(V_{REFIN}) \frac{511}{1024}$
	:		:
0000	0000	01(00)	$2(V_{REFIN}) \frac{1}{1024}$
0000	0000	00(00)	0 V

† A 10-bit data word with two sub-LSB 0s must be written since the DAC input latch is 12 bits wide.

buffer amplifier

The output buffer has a rail-to-rail output with short circuit protection and can drive a 2-k Ω load with a 100 pF load capacitance. Settling time is a software selectable 12.5 μ s or 2.5 μ s typical to within ± 0.5 LSB of final value.

external reference

The reference voltage input is buffered which makes the DAC input resistance not code dependent. Therefore, the REF_{IN} input resistance is 10 M Ω and the REF_{IN} input capacitance is typically 5 pF, independent of input code. The reference voltage determines the DAC full-scale output.

logic interface

The logic inputs function with CMOS logic levels. Most of the standard high-speed CMOS logic families may be used.

serial clock and update rate

Figure 1 shows the TLC5617 timing. The maximum serial clock rate is

$$f_{(SCLK)max} = \frac{1}{t_{w(CH)min} + t_{w(CL)min}} = 20 \text{ MHz}$$

The digital update rate is limited by the chip-select period, which is

$$t_p(CS) = 16 \times (t_{w(CH)} + t_{w(CL)}) + t_{su}(CS1)$$

This equals 820-ns or 1.21-MHz update rate. However, the DAC settling time to 10 bits limits the update rate for full-scale input step transitions.

TLC5617, TLC5617A

PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS151A – JULY 1997 – REVISED DECEMBER 1997

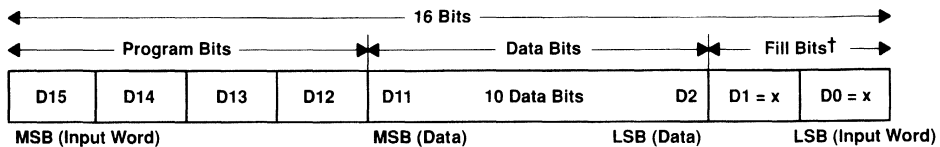
APPLICATION INFORMATION

serial interface

When chip select (\overline{CS}) is low, the input data is read into a 16-bit shift register with the input data clocked in most significant bit first. The falling edge of the SCLK input shifts the data into the input register.

The rising edge of \overline{CS} then transfers the data to the DAC register. All \overline{CS} transitions should occur when the SCLK input is low.

The 16 bits of data can be transferred with the sequence shown in Figure 18.



† Two extra (sub-LSB) bits (can be don't care)

Figure 19. Input Data Word Format

Table 2 shows the function of program bits D15 – D12.

Table 2. Program Bits D15 – D12 Function

PROGRAM BIT				DEVICE FUNCTION
D15	D14	D13	D12	
1	X	X	X	Write to latch A with serial interface register data and latch B updated with buffer latch data
0	X	X	0	Write to latch B and double buffer latch
0	X	X	1	Write to double buffer latch only
X	1	X	X	12.5 μ s settling time
X	0	X	X	2.5 μ s settling time
X	X	0	X	Powered-up operation
X	X	1	X	Powered-down mode

function of the latch control bits (D15 and D12)

Three data transfers are possible. All transfers occur immediately after \overline{CS} goes high and are described in the following sections.

latch A write, latch B update (D15 = high, D12 = X)

The serial interface register (SIR) data are written to latch A and the double buffer latch contents are written to latch B. The double buffer contents are unaffected. This control bit condition allows simultaneous output updates of both DACs.

TLC5617, TLC5617A PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS151A – JULY 1997 – REVISED DECEMBER 1997

APPLICATION INFORMATION

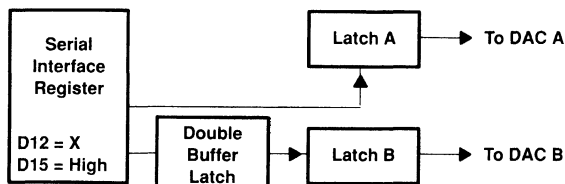


Figure 20. Latch A Write, Latch B Update

latch B and double-buffer 1 write (D15 = low, D12 = low)

The SIR data are written to both latch B and the double buffer. Latch A is unaffected.

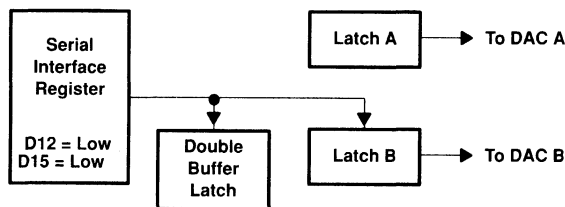


Figure 21. Latch B and Double-Buffer Write

double-buffer-only write (D15 = low, D12 = high)

The SIR data are written to the double buffer only. Latch A and B contents are unaffected.

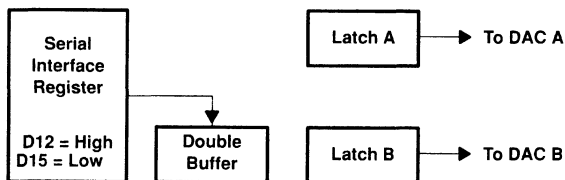


Figure 22. Double-Buffer-Only Write

purpose and use of the buffer

Normally only one DAC output can change after a write. The double buffer allows both DAC outputs to change after a single write. This is achieved by the two following steps.

1. A double-buffer-only write is executed to store the new DAC B data without changing the DAC A and B outputs.
2. Following the previous step a write to latch A is executed. This writes the SIR data to latch A and also writes the double-buffer contents to latch B. Thus both DACs receive their new data at the same time and so both DAC outputs begin to change at the same time.

Unless a double-buffer-only write is issued, the latch B and double-buffer contents are identical. Thus, following a write to latch A or B with another write to latch A does not change the latch B contents.

TLC5617, TLC5617A PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS151A – JULY 1997 – REVISED DECEMBER 1997

APPLICATION INFORMATION

operational examples

changing the latch A data from zero to full code

Assuming that latch A starts at zero code (e.g., after power-up), the latch can be filled with 1s by writing (bit D15 on the left, D0 on the right)

```
1X0X 1111 1111 11XX
```

to the serial interface. Bit D14 can be zero to select slow mode or one to select fast mode. The other Xs can be zero or one (don't care).

The latch B contents and the DAC B output are not changed by this write unless the double-buffer contents are different from the latch B contents. This can only be true if the last write was a double-buffer-only write.

changing the latch B data from zero to full code

Assuming that latch B starts at zero code (e.g., after power-up), the latch can be filled with 1s by writing (bit D15 on the left, D0 on the right).

```
0X00 1111 1111 11XX
```

to the serial interface. Bit D14 can be zero to select slow mode or one to select fast mode. The other Xs can be zero or one (don't care). The data (bits D0 to D11) are written to both the double buffer and latch B.

The latch A contents and the DAC A output are not changed by this write.

double-buffered change of both DAC outputs

Assuming that DACs A and B start at zero code (e.g., after power-up), if DAC A is to be driven to mid-scale and DAC B to full-scale, and if the outputs are to begin rising at the same time, this can be achieved as follows:

First,

```
0d01 1111 1111 11XX
```

is written (bit D15 on the left, D0 on the right) to the serial interface. This loads the full-scale code into the double buffer latch but does not change the latch B contents and the DAC B output voltage. The latch A contents and the DAC A output are also unaffected by this write operation.

Changing from fast to slow mode or slow to fast mode changes the supply current which can glitch the outputs, and so D14 (designated by d in the data word) should be set to maintain the speed mode set by the previous write. The other Xs can be ones or zeros (don't care).

Next,

```
1X0X 1000 0000 00XX
```

is written (bit D15 on the left, D0 on the right) to the serial interface. Bit D14 can be zero to select slow mode or one to select fast mode. The other Xs can be zero or one (don't care). This writes the mid-scale code (1000000000XX) to latch A and also copies the full-scale code from the double buffer to latch B. Both DAC outputs thus begin to rise after the second write.



TLC5617, TLC5617A PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS151A – JULY 1997 – REVISED DECEMBER 1997

APPLICATION INFORMATION

DSP serial interface

Utilizing a simple 3 wire serial interface, the TLC5617A can be interfaced to TMS320 compatible serial ports. The 5617A has an internal state machine that will count 16 clocks after receiving a falling edge of /CS and then disable further clocking in of data until the next falling edge is received on /CS. Therefore the /CS can be connected directly to the FS pins of the serial port and only the leading falling edge of the DSP will be used to start the write process. The TLC5617A is designed to be used with the TMS320Cxx DSP's in Burst Mode Serial Port Transmit operation.

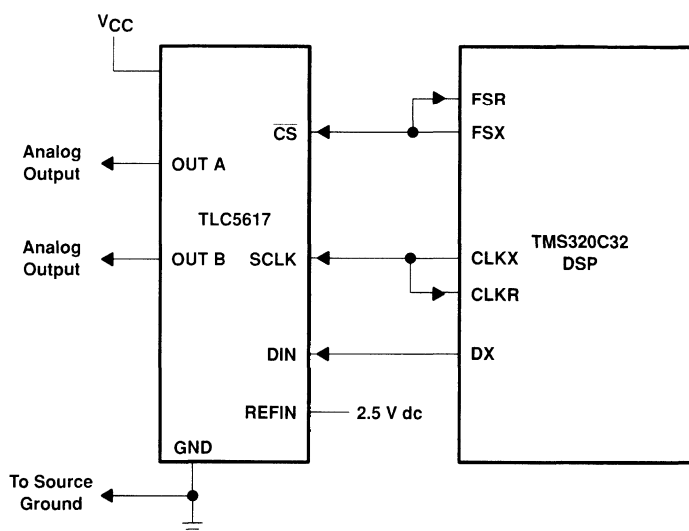


Figure 23. Interfacing The TLC5617 To TMS320C32 DSP

SPI serial interface

Both the TLC5617 and TLC5617A are compatible with SPI, QSPI or Microwire serial standards. The hardware connections are shown in Figures 23 and 24. The TLC5617A has an internal state machine that will count 16 clocks after the falling edge to /CS and then internally disable the device. The internal edge is or'd together with the /CS so that the rising edge can be provided to /CS prior to the occurrence of the internal edge to also disable the device.

general serial interface

The TLC5617 three-wire interface is compatible with the SPI, QSPI, and Microwire serial standards. The hardware connections are shown in Figure 23 and Figure 24.

The SPI and Microwire interfaces transfer data in 8-bit bytes, therefore, two write cycles are required to input data to the DAC. The QSPI interface, which has a variable input data length from 8 to 16 bits, can load the DAC input register in one write cycle.



TLC5617, TLC5617A PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS151A – JULY 1997 – REVISED DECEMBER 1997

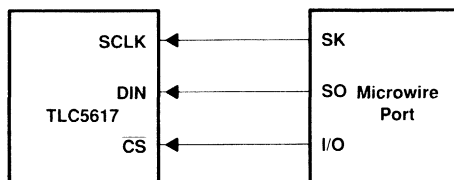


Figure 24. Microwire Connection

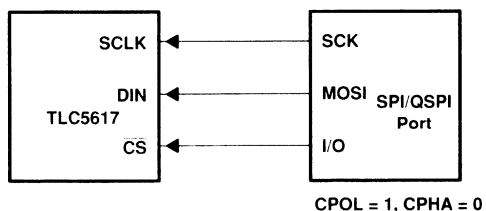


Figure 25. SPI/QSPI Connection

linearity, offset, and gain error using single end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

TLC5617, TLC5617A PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS151A – JULY 1997 – REVISED DECEMBER 1997

APPLICATION INFORMATION

linearity, offset, and gain error using single end supplies (continued)

The output voltage remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 24.

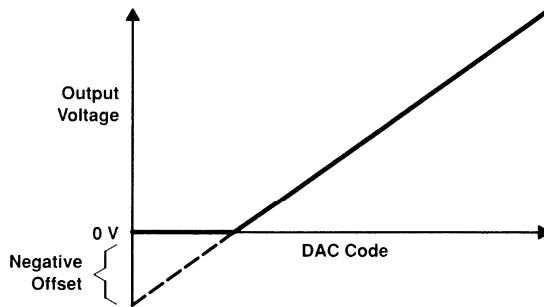


Figure 26. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero input code (all inputs 0) and full scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full scale code and the lowest code that produces a positive output voltage. For the TLC5617, the zero-scale (offset) error is plus or minus 3 LSB maximum. The code is calculated from the maximum specification for the negative offset.

power-supply bypassing and ground management

Printed circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane making sure that analog ground currents are well managed.

A 0.1 μF ceramic bypass capacitor should be connected between V_{DD} and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog and digital power supplies.

Figure 25 shows the ground plane layout and bypassing technique.

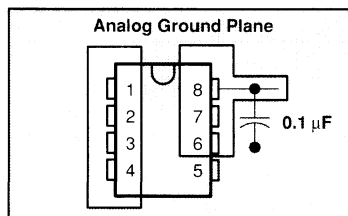


Figure 27. Power-Supply Bypassing

TLC5617, TLC5617A PROGRAMMABLE DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS151A – JULY 1997 – REVISED DECEMBER 1997

APPLICATION INFORMATION

saving power

Setting the DAC register to all 0s minimizes power consumption by the reference resistor array and the output load when the system is not using the DAC.

ac considerations/analog feedthrough

Higher frequency analog input signals may couple to the output through internal stray capacitance. Analog feedthrough is tested by holding \overline{CS} high, setting the DAC code to all 0s, sweeping the frequency applied to REFIN, and monitoring the DAC output.



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TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B – JULY 1997 – REVISED DECEMBER 1997

- Programmable Settling Time to 0.5 LSB
2.5 μ s or 12.5 μ s Typ
- Two 12-Bit CMOS Voltage Output DACs in
an 8-Pin Package
- Simultaneous Updates for DAC A
and DAC B
- Single Supply Operation
- 3-Wire Serial Interface
- High-Impedance Reference Inputs
- Voltage Output Range . . . 2 Times the
Reference Input Voltage
- Software Power Down Mode
- Internal Power-On Reset
- TMS320 and SPI Compatible
- Low Power Consumption:
3 mW Typ in Slow Mode
8 mW Typ in Fast Mode
- Input Data Update Rate of 1.21 MHz
- Monotonic Over Temperature

applications

- Battery Powered Test Instruments
- Digital Offset and Gain Adjustment
- Battery Operated/Remote Industrial
Controls
- Machine and Motion Control Devices
- Cellular Telephones

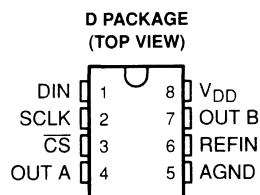
description

The TLC5618 is a dual 12-bit voltage output digital-to-analog converter (DAC) with buffered reference inputs (high impedance). The DACs have an output voltage range that is two times the reference voltage, and the DACs are monotonic. The device is simple to use, running from a single supply of 5 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLC5618 is over a 3-wire CMOS-compatible serial bus. The device receives a 16-bit word for programming and to produce the analog output. The digital inputs feature Schmitt triggers for high noise immunity. Digital communication protocols include the SPI™, QSPI™, and Microwire™ standards.

Two versions of this device are available. The TLC5618 does not have any internal state machine and is dependent on all external timing signals. The TLC5618A has an internal state machine that will count the number of clocks from falling edge of \overline{CS} and then update and disable the device to accepting further data inputs. The TLC5618A is recommended for TMS320 and SPI processors and the TLC5618 is recommended only for use in SPI or 3-wire serial port processors. The TLC5618A is backward compatible and designed to work in TLC5618 designed systems.

The 8-terminal small-outline D package allows digital control of analog functions in space-critical applications. The TLC5618C is characterized for operation from 0°C to 70°C. The TLC5618I is characterized for operation from -40°C to 85°C.



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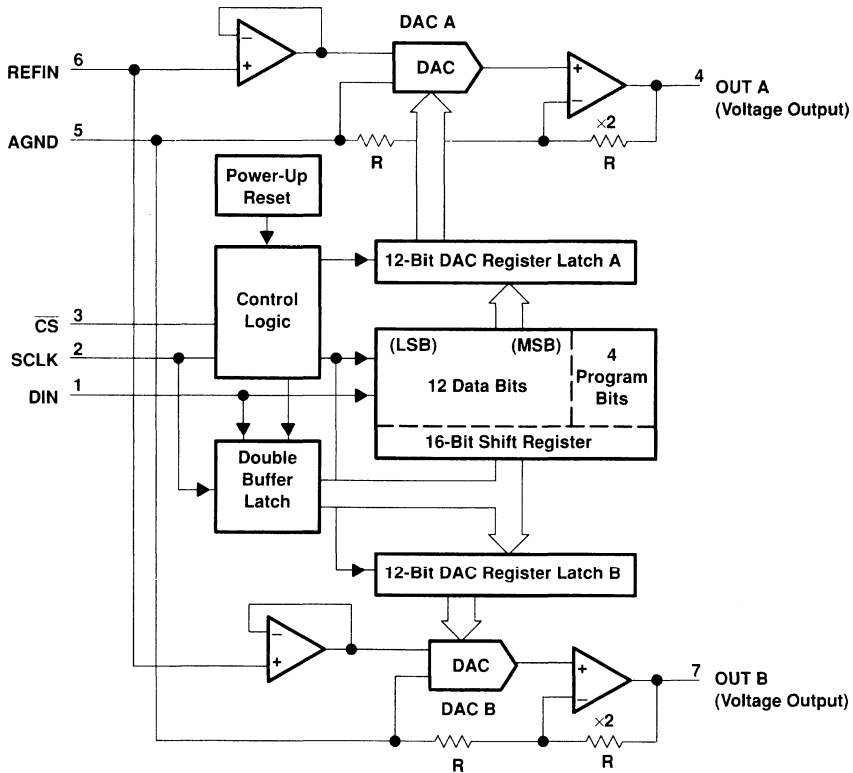
SLAS156B – JULY 1997 – REVISED DECEMBER 1997

AVAILABLE OPTIONS		
PACKAGE		
TA	SMALL OUTLINE† (D)	PLASTIC DIP (P)
0°C to 70°C	TLC5618CD TLC5618ACD	TLC5618CP TLC5618ACP
-40°C to 85°C	TLC5618ID TLC5618AID	TLC5618IP TLC5618AIP

† The D package is available in tape and reel by adding R to the part number (e.g., TLC5618CDR)

DEVICE	COMPATIBILITY
TLC5618	SPI, QSPI and Microwire
TLC5618A	TMS320Cxx, SPI, QSPI and Microwire

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
DIN	1	I	Serial data input

TLC5618, TLC5618A

PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B – JULY 1997 – REVISED DECEMBER 1997

SCLK	2	I	Serial clock input
\overline{CS}	3	I	Chip select, active low
OUT A	4	O	DAC A analog output
AGND	5		Analog ground
REFIN	6	I	Reference voltage input
OUT B	7	O	DAC B analog output
VDD	8		Positive power supply

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} to AGND)	7 V
Digital input voltage range to AGND	-0.3 V to $V_{DD} + 0.3$ V
Reference input voltage range to AGND	-0.3 V to $V_{DD} + 0.3$ V
Output voltage at OUT from external source	$V_{DD} + 0.3$ V
Continuous current at any terminal	± 20 mA
Operating free-air temperature range, T_A : TLC5618C	0°C to 70°C
TLC5618I	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	5	5.5	V
High-level digital input voltage, V_{IH}	$V_{DD} = 5$ V	0.7 V_{DD}			V
Low-level digital input voltage, V_{IL}	$V_{DD} = 5$ V	0.3 V_{DD}			V
Reference voltage, V_{ref} to REFIN terminal		2	2.048	$V_{DD} - 1.1$	V
Load resistance, R_L		2			k Ω
Operating free-air temperature, T_A	TLC5618C	0		70	°C
	TLC5618I	-40		85	°C



TLC5618, TLC5618A

PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B – JULY 1997 – REVISED DECEMBER 1997

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref}(REFIN) = 2.048\text{ V}$ (unless otherwise noted)

static DAC specifications

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Resolution				12			bits
Integral nonlinearity (INL), end point adjusted		$V_{ref}(REFIN) = 2.048\text{ V}$, See Note 1					± 4 LSB
Differential nonlinearity (DNL)		$V_{ref}(REFIN) = 2.048\text{ V}$, See Note 2		± 0.5			± 1 LSB
EZS	Zero-scale error (offset error at zero scale)	$V_{ref}(REFIN) = 2.048\text{ V}$, See Note 3					± 12 mV
Zero-scale-error temperature coefficient		$V_{ref}(REFIN) = 2.048\text{ V}$, See Note 4		3			ppm/ $^{\circ}\text{C}$
E _G	Gain error	$V_{ref}(REFIN) = 2.048\text{ V}$, See Note 5		± 0.29			% of FS voltage
Gain error temperature coefficient		$V_{ref}(REFIN) = 2.048\text{ V}$, See Note 6		1			ppm/ $^{\circ}\text{C}$
PSRR	Power-supply rejection ratio	Zero scale	See Notes 7 and 8	Slow	65		dB
		Gain			65		
		Zero scale		Fast	65		
		Gain			65		

- NOTES:
- The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.
 - The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
 - Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
 - Zero-scale-error temperature coefficient is given by: $E_{ZS\ TC} = [E_{ZS}(T_{max}) - E_{ZS}(T_{min})] / V_{ref} \times 10^6 / (T_{max} - T_{min})$.
 - Gain error is the deviation from the ideal output ($V_{ref} - 1\text{ LSB}$) with an output load of $10\text{ k}\Omega$ excluding the effects of the zero-error.
 - Gain temperature coefficient is given by: $E_{G\ TC} = [E_{G}(T_{max}) - E_{G}(T_{min})] / V_{ref} \times 10^6 / (T_{max} - T_{min})$.
 - Zero-scale-error rejection ratio (EZS-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
 - Gain-error rejection ratio (EG-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero scale change.

OUT A and OUT B output specifications

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _O	Voltage output range	$R_L = 10\text{ k}\Omega$		0		$V_{DD} - 0.4$	V
Output load regulation accuracy		$V_{O(OUT)} = 4.096\text{ V}$, $R_L = 2\text{ k}\Omega$		± 0.29			% of FS voltage
I _{OSC(sink)}	Output short circuit sink current	$V_{O(A\ OUT)} = V_{DD}$, $V_{O(B\ OUT)} = V_{DD}$, Input code zero		Fast	38		mA
				Slow	23		
I _{OSC(source)}	Output short circuit source current	$V_{O(A\ OUT)} = 0\text{ V}$, $V_{O(B\ OUT)} = 0\text{ V}$, Full-scale code		Fast	-54		mA
				Slow	-29		
I _{O(sink)}	Output sink current	$V_{O(OUT)} = 0.25\text{ V}$		5			mA
I _{O(source)}	Output source current	$V_{O(OUT)} = 4.2\text{ V}$		5			mA



TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B – JULY 1997 – REVISED DECEMBER 1997

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref}(REFIN) = 2.048\text{ V}$ (unless otherwise noted) (continued)

reference input (REFIN)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I Input voltage range		0		$V_{DD}-2$	V
R_I Input resistance			10		M Ω
C_I Input capacitance			5		pF
Reference feedthrough	REFIN = 1 V_{pp} at 1 kHz + 1.024 V dc (see Note 9)		-60		dB
Reference input bandwidth (f-3dB)	REFIN = 0.2 V_{pp} + 1.024 V dc	Slow	0.5		MHz
		Fast	1		

NOTE 9: Reference feedthrough is measured at the DAC output with an input code = 000 hex and a $V_{ref}(REFIN)$ input = 1.024 V dc + 1 V_{pp} at 1 kHz.

digital inputs (DIN, SCLK, \overline{CS})

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH} High-level digital input current	$V_I = V_{DD}$			+1	μ A
I_{IL} Low-level digital input current	$V_I = 0\text{ V}$			+1	μ A
C_I Input capacitance			8		pF

power supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD} Power supply current	$V_{DD} = 5.5\text{ V}$, No load, All inputs = 0 V or V_{DD}	Slow	0.6	1	mA
		Fast	1.6	2.5	
Power down supply current	D13 = 0 (see Table 2)		1		μ A

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref}(REFIN) = 2.048\text{ V}$ (unless otherwise noted)

analog output dynamic performance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR+ Output slew rate, positive	$C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, Code 32 to Code 4096, $V_{ref}(REFIN) = 2.048\text{ V}$, $T_A = 25\text{ C}$, V_O from 10% to 90%	Slow	0.3	0.5	V/ μ s
		Fast	2.4	3	
SR- Output slew rate, negative	$C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, Code 4096 to Code 32, $V_{ref}(REFIN) = 2.048\text{ V}$, $T_A = 25\text{ C}$, V_O from 10% to 90%	Slow	0.15	0.25	V/ μ s
		Fast	1.2	1.5	
t_s Output settling time	$T_o \pm 0.5\text{ LSB}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, See Note 10	Slow		12.5	μ s
		Fast		2.5	
$t_{s(c)}$ Output settling time, code-to-code	$T_o \pm 0.5\text{ LSB}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, See Note 11	Slow		2	μ s
		Fast		2	
Glitch energy	DIN = All 0s to all 1s, $f(SCLK) = 100\text{ kHz}$, $\overline{CS} = V_{DD}$		5		nV-s
S/(N+D) Signal to noise + distortion	$V_{ref}(REFIN) = 1\text{ V}_{pp}$ at 1 kHz and 10 kHz + 1.024 V dc, Input code = 10 0000 0000		78		dB

NOTES: 10. Settling time is the time for the output signal to remain within $\pm 0.5\text{ LSB}$ of the final measured value for a digital input code change of 020 hex to 3FF hex or 3FF hex to 020 hex.

11. Settling time is the time for the output signal to remain within $\pm 0.5\text{ LSB}$ of the final measured value for a digital input code change of one count.



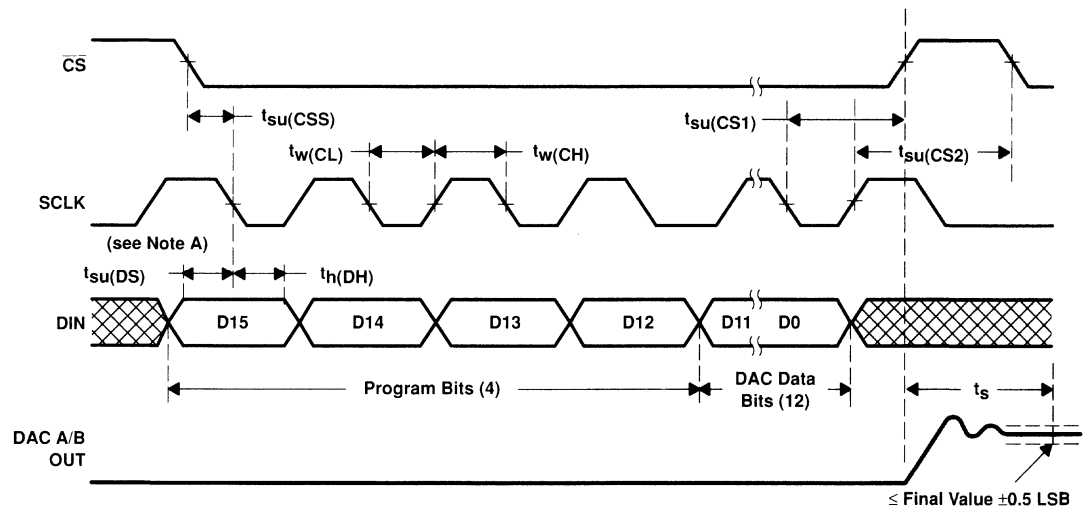
TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B – JULY 1997 – REVISED DECEMBER 1997

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5 V \pm 5\%$, $V_{ref}(REFIN) = 2.048 V$ (unless otherwise noted) (continued)

digital input timing requirements

		MIN	NOM	MAX	UNIT
$t_{su}(DS)$	Setup time, DIN before SCLK low	5			ns
$t_{h}(DH)$	Hold time, DIN valid after SCLK low	5			ns
$t_{su}(CSS)$	Setup time, \overline{CS} low to SCLK low	5			ns
$t_{su}(CS1)$	Setup time, SCLK \uparrow to \overline{CS} \downarrow , external end-of-write	10			ns
$t_{su}(CS2)$	Setup time, SCLK \uparrow to \overline{CS} \downarrow , start of next write cycle	5			ns
$t_w(CL)$	Pulse duration, SCLK low	25			ns
$t_w(CH)$	Pulse duration, SCLK high	25			ns
$t_d(CS1)$	Delay time, CLK \uparrow to Disable (TLC5618A only)			5	ns

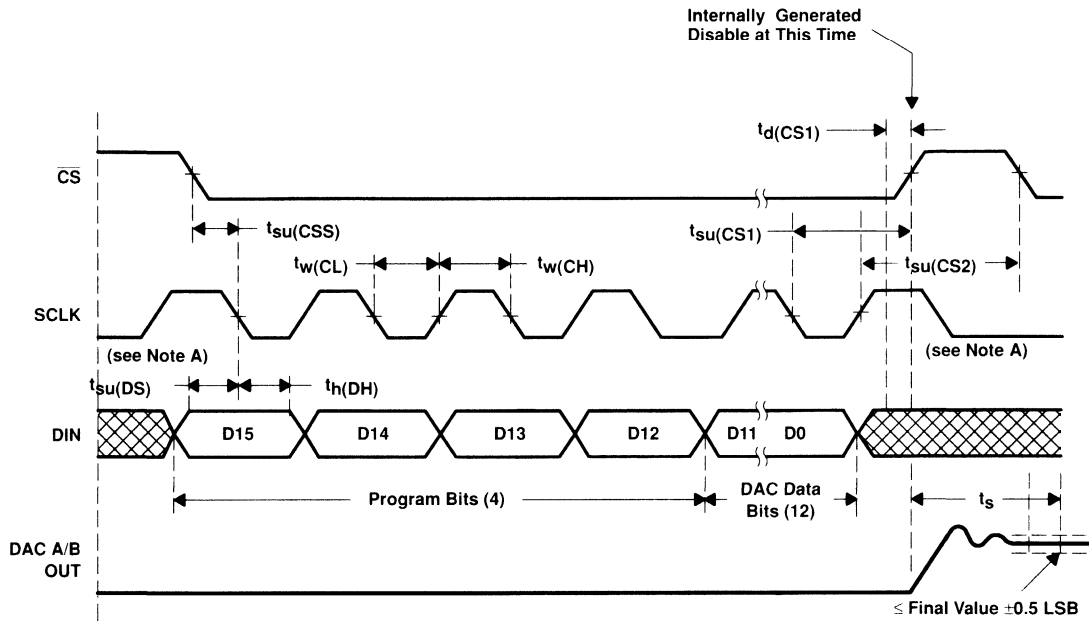


NOTE A: The input clock, applied at the SCLK terminal, should be inhibited low when \overline{CS} is high to minimize clock feedthrough.

Figure 1. Timing Diagram for the TLC5618

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B – JULY 1997 – REVISED DECEMBER 1997



NOTE B: The input clock, applied at the SCLK terminal, should be inhibited low when \overline{CS} is high to minimize clock feedthrough.

Figure 2. Timing Diagram for TLC5618A only

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B – JULY 1997 – REVISED DECEMBER 1997

TYPICAL CHARACTERISTICS

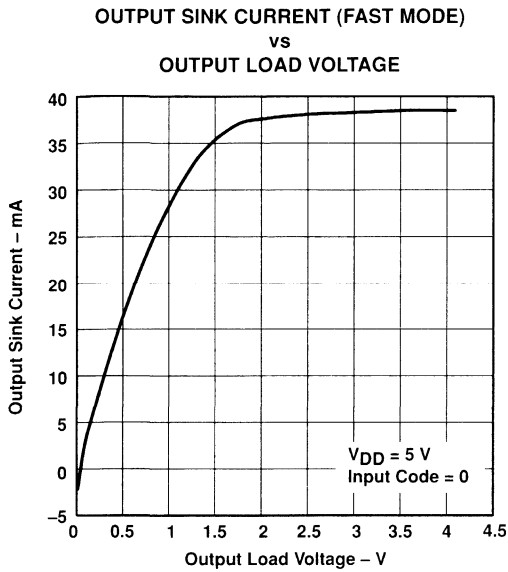


Figure 3

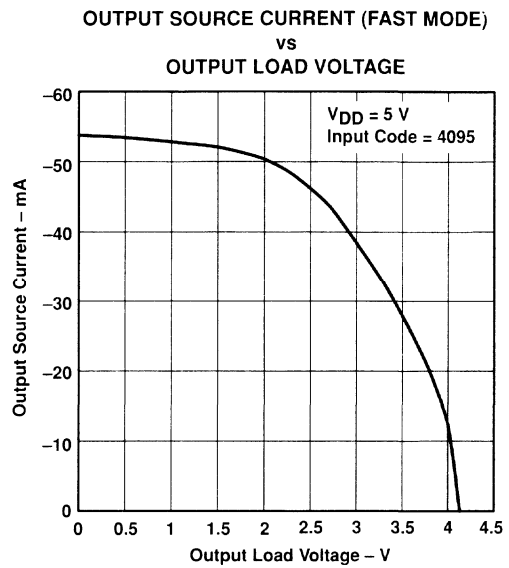


Figure 4

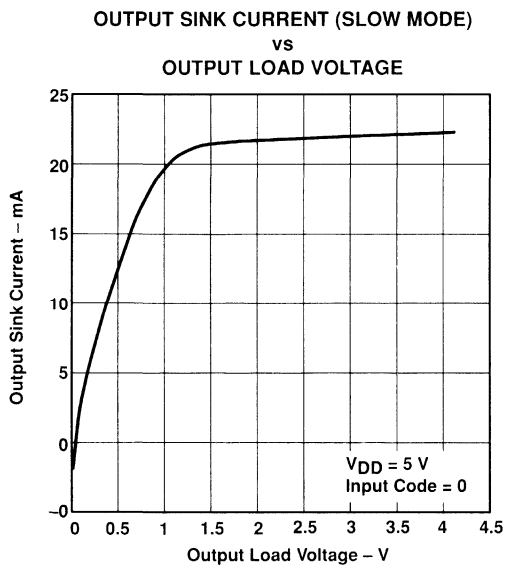


Figure 5

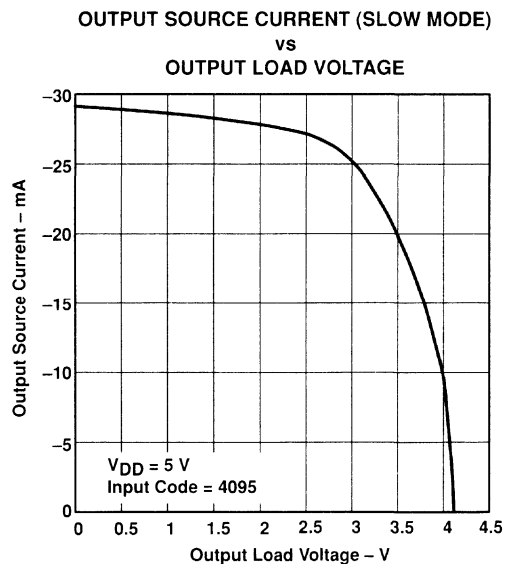


Figure 6

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B – JULY 1997 – REVISED DECEMBER 1997

TYPICAL CHARACTERISTICS

**SUPPLY CURRENT
vs
TEMPERATURE**

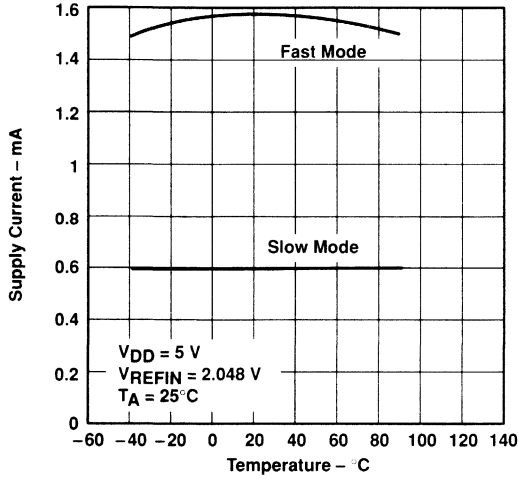


Figure 7

**RELATIVE GAIN (FAST MODE)
vs
FREQUENCY**

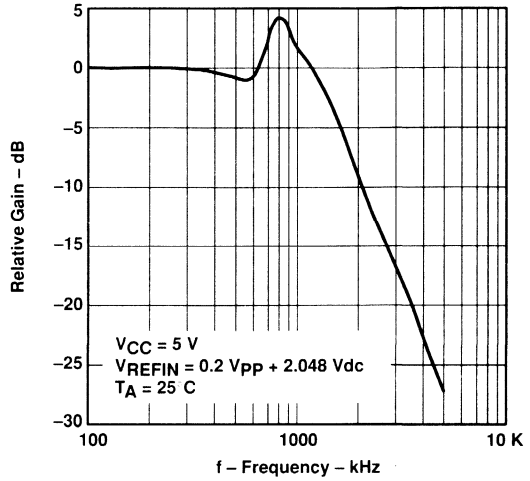


Figure 8

**RELATIVE GAIN (SLOW MODE)
vs
FREQUENCY**

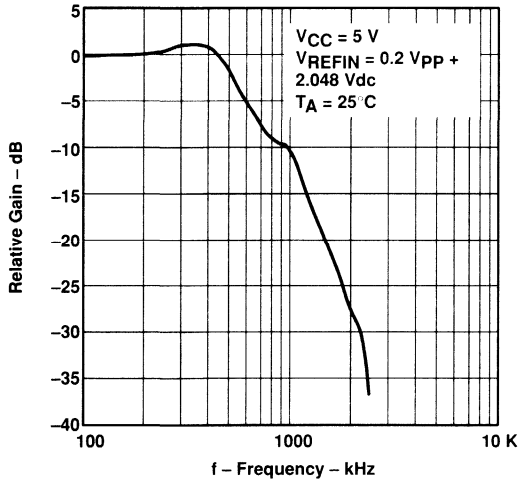


Figure 9

**TOTAL HARMONIC DISTORTION (SLOW MODE)
vs
FREQUENCY**

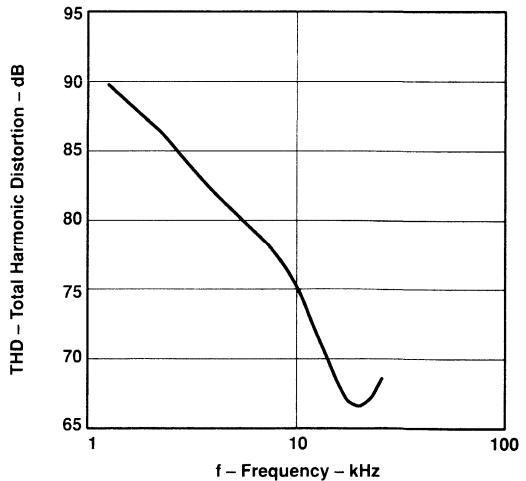


Figure 10



TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B – JULY 1997 – REVISED DECEMBER 1997

TYPICAL CHARACTERISTICS

**TOTAL HARMONIC DISTORTION + NOISE (SLOW MODE)
vs
FREQUENCY**

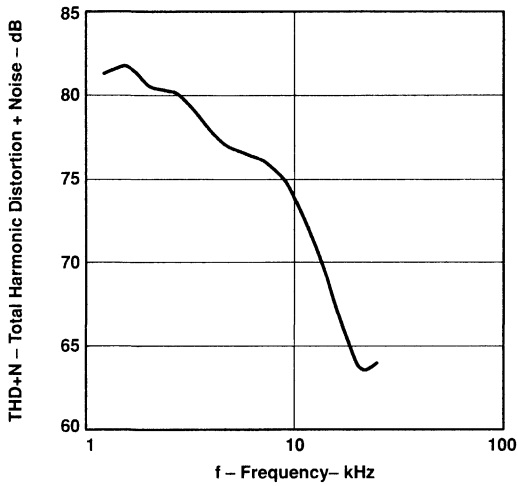


Figure 11

**SIGNAL-TO-NOISE RATIO (SLOW MODE)
vs
FREQUENCY**

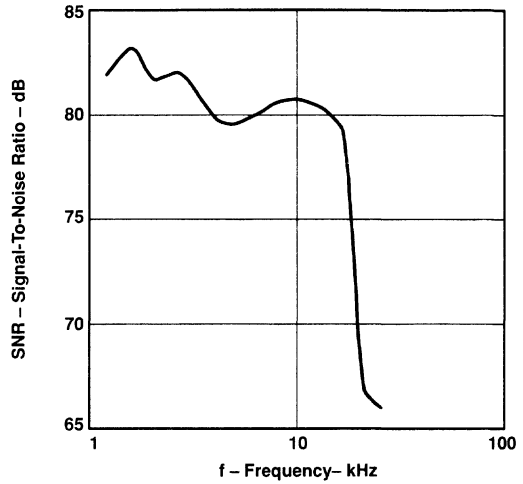


Figure 12

**TOTAL HARMONIC DISTORTION (FAST MODE)
vs
FREQUENCY**

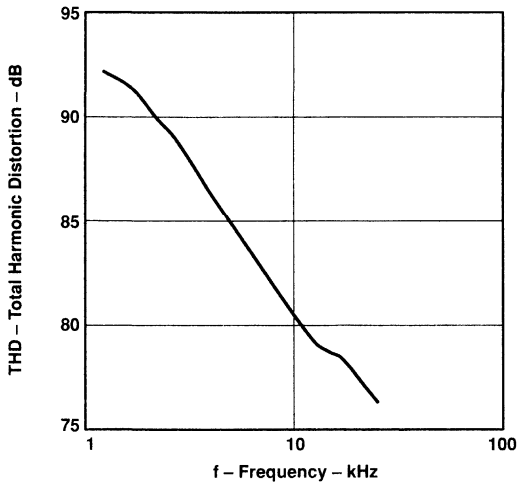


Figure 13

**TOTAL HARMONIC DISTORTION + NOISE (FAST MODE)
vs
FREQUENCY**

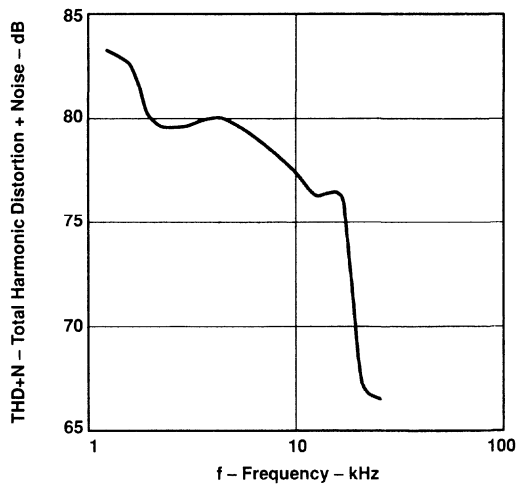


Figure 14



TLC5618, TLC5618A
PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B - JULY 1997 - REVISED DECEMBER 1997

TYPICAL CHARACTERISTICS

SIGNAL-TO-NOISE RATIO (FAST MODE)
vs
FREQUENCY

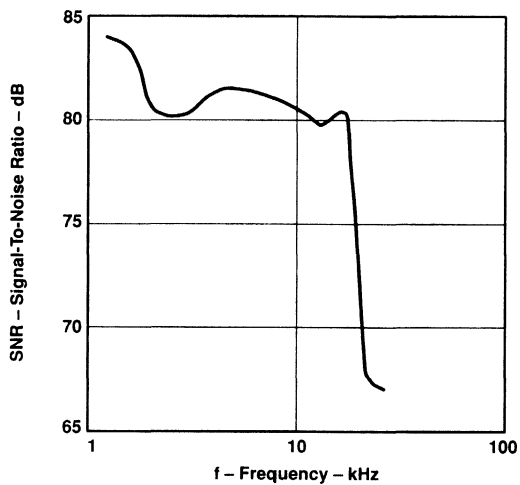


Figure 15

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

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TYPICAL CHARACTERISTICS

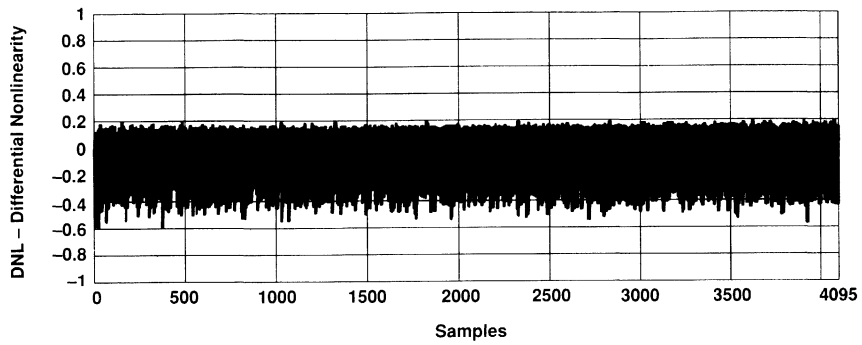


Figure 16. Differential Nonlinearity With Input Code

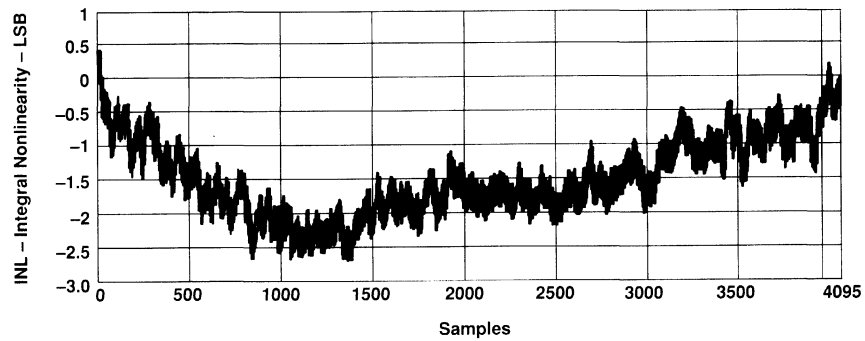


Figure 17. Integral Nonlinearity With Input Code

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B – JULY 1997 – REVISED DECEMBER 1997

APPLICATION INFORMATION

general function

The TLC5618 uses a resistor string network buffered with an op amp to convert 12-bit digital data to analog voltage levels (see functional block diagram and Figure 17). The output is the same polarity as the reference input (see Table 1).

The output code is given by: $2(V_{REFIN}) \frac{CODE}{4096}$

An internal circuit resets the DAC register to all 0s on power-up.

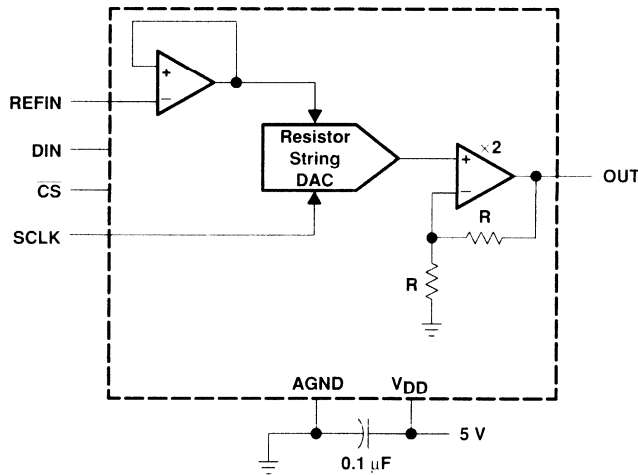


Figure 18. TLC5618 Typical Circuit

Table 1. Binary Code Table (0 V to 2 V_{REFIN} Output), Gain = 2

INPUT			OUTPUT
1111	1111	1111	$2(V_{REFIN}) \frac{4095}{4096}$
	:		:
1000	0000	0001	$2(V_{REFIN}) \frac{2049}{4096}$
1000	0000	0000	$2(V_{REFIN}) \frac{2048}{4096} = V_{REFIN}$
0111	1111	1111	$2(V_{REFIN}) \frac{2047}{4096}$
	:		:
0000	0000	0001	$2(V_{REFIN}) \frac{1}{4096}$
0000	0000	0000	0 V

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B – JULY 1997 – REVISED DECEMBER 1997

APPLICATION INFORMATION

buffer amplifier

The output buffer has a rail-to-rail output with short circuit protection and can drive a 2-k Ω load with a 100-pF load capacitance. Settling time is a software selectable 12.5 μ s or 2.5 μ s, typical to within ± 0.5 LSB of final value.

external reference

The reference voltage input is buffered which makes the DAC input resistance not code dependent. Therefore, the REFIN input resistance is 10 M Ω and the REFIN input capacitance is typically 5 pF, independent of input code. The reference voltage determines the DAC full-scale output.

logic interface

The logic inputs function with CMOS logic levels. Most of the standard high-speed CMOS logic families may be used.

serial clock and update rate

Figure 1 shows the TLC5618 timing. The maximum serial clock rate is:

$$f_{(\text{SCLK})\text{max}} = \frac{1}{t_{w(\text{CH})\text{min}} + t_{w(\text{CL})\text{min}}} = 20 \text{ MHz}$$

The digital update rate is limited by the chip-select period, which is:

$$t_p(\text{CS}) = 16 \times (t_{w(\text{CH})} + t_{w(\text{CL})}) + t_{\text{su}}(\text{CS1})$$

This equals an 820-ns or 1.21-MHz update rate. However, the DAC settling time to 12 bits limits the update rate for full-scale input step transitions.

serial interface

When chip select ($\overline{\text{CS}}$) is low, the input data is read into a 16-bit shift register with the input data clocked in most significant bit first. The falling edge of the SCLK input shifts the data into the input register.

The rising edge of $\overline{\text{CS}}$ then transfers the data to the DAC register. When $\overline{\text{CS}}$ is high, input data cannot be clocked into the input register. All $\overline{\text{CS}}$ transitions should occur when the SCLK input is low.

The 16 bits of data can be transferred with the sequence shown in Figure 18.

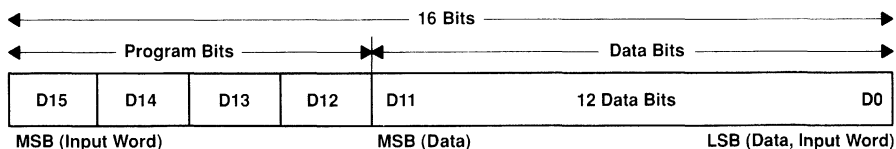


Figure 19. Input Data Word Format

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B – JULY 1997 – REVISED DECEMBER 1997

APPLICATION INFORMATION

Table 2 shows the function of program bits D15 – D12.

Table 2. Program Bits D15 – D12 Function

PROGRAM BITS				DEVICE FUNCTION
D15	D14	D13	D12	
1	X	X	X	Write to latch A with serial interface register data and latch B updated with buffer latch data
0	X	X	0	Write to latch B and double buffer latch
0	X	X	1	Write to double buffer latch only
X	1	X	X	12.5 μ s settling time
X	0	X	X	2.5 μ s settling time
X	X	0	X	Powered-up operation
X	X	1	X	Power down mode

function of the latch control bits (D15 and D12)

Three data transfers are possible. All transfers occur immediately after \overline{CS} goes high and are described in the following sections.

latch A write, latch B update (D15 = high, D12 = X)

The serial interface register (SIR) data are written to latch A and the double buffer latch contents are written to latch B. The double buffer contents are unaffected. This program bit condition allows simultaneous output updates of both DACs.

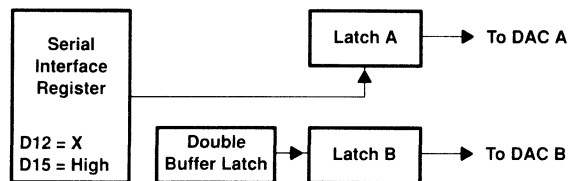


Figure 20. Latch A Write, Latch B Update

latch B and double-buffer 1 write (D15 = low, D12 = low)

The SIR data are written to both latch B and the double buffer. Latch A is unaffected.

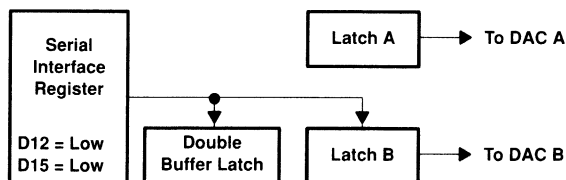


Figure 21. Latch B and Double-Buffer Write

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B – JULY 1997 – REVISED DECEMBER 1997

APPLICATION INFORMATION

double-buffer-only write (D15 = low, D12 = high)

The SIR data are written to the double buffer only. Latch A and B contents are unaffected.

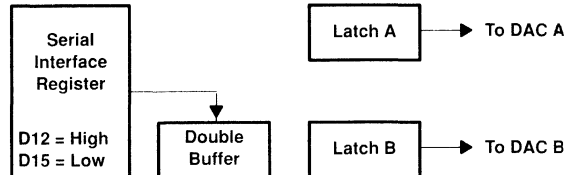


Figure 22. Double-Buffer-Only Write

purpose and use of the double buffer

Normally only one DAC output can change after a write. The double buffer allows both DAC outputs to change after a single write. This is achieved by the two following steps.

1. A double-buffer-only write is executed to store the new DAC B data without changing the DAC A and B outputs.
2. Following the previous step, a write to latch A is executed. This writes the SIR data to latch A and also writes the double-buffer contents to latch B. Thus both DACs receive their new data at the same time and so both DAC outputs begin to change at the same time.

Unless a double-buffer-only write is issued, the latch B and double-buffer contents are identical. Thus, following a write to latch A or B with another write to latch A does not change the latch B contents.

operational examples

changing the latch A data from zero to full code

Assuming that latch A starts at zero code (e.g., after power-up), the latch can be filled with 1s by writing (bit D15 on the left, D0 on the right)

```
1X0X 1111 1111 1111
```

to the serial interface. Bit D14 can be zero to select slow mode or one to select fast mode. The other X can be zero or one (don't care).

The latch B contents and the DAC B output are not changed by this write unless the double-buffer contents are different from the latch B contents. This can only be true if the last write was a double-buffer-only write.

changing the latch B data from zero to full code

Assuming that latch B starts at zero code (e.g., after power-up), the latch can be filled with 1s by writing (bit D15 on the left, D0 on the right).

```
0X00 1111 1111 1111
```

to the serial interface. Bit D14 can be zero to select slow mode or one to select fast mode. The data (bits D0 to D11) are written to both the double buffer and latch B.

The latch A contents and the DAC A output are not changed by this write.

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B – JULY 1997 – REVISED DECEMBER 1997

APPLICATION INFORMATION

double-buffered change of both DAC outputs

Assuming that DACs A and B start at zero code (e.g., after power-up), if DAC A is to be driven to mid-scale and DAC B to full-scale, and if the outputs are to begin rising at the same time, this can be achieved as follows:

First,

```
0d01 1111 1111 1111
```

is written (bit D15 on the left, D0 on the right) to the serial interface. This loads the full-scale code into the double buffer but does not change the latch B contents and the DAC B output voltage. The latch A contents and the DAC A output are also unaffected by this write operation.

Changing from fast to slow or slow to fast mode changes the supply current which can glitch the outputs, and so D14 (designated by d in the above data word) should be set to maintain the speed mode set by the previous write.

Next,

```
1X0X 1000 0000 0000
```

is written (bit D15 on the left, D0 on the right) to the serial interface. Bit D14 can be zero to select slow mode or one to select fast mode. The other X can be zero or one (do not care). This writes the mid-scale code (100000000000) to latch A and also copies the full-scale code from the double buffer to latch B. Both DAC outputs thus begin to rise after the second write.

DSP serial interface

Utilizing a simple 3 wire serial interface, the TLC5618A can be interfaced to TMS320 compatible serial ports. The 5618A has an internal state machine that will count 16 clocks after receiving a falling edge of /CS and then disable further clocking in of data until the next falling edge is received on /CS. Therefore the /CS can be connected directly to the FS pins of the serial port and only the leading falling edge of the DSP will be used to start the write process. The TLC5618A is designed to be used with the TMS320Cxx DSP's in Burst Mode Serial Port Transmit operation.



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TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B – JULY 1997 – REVISED DECEMBER 1997

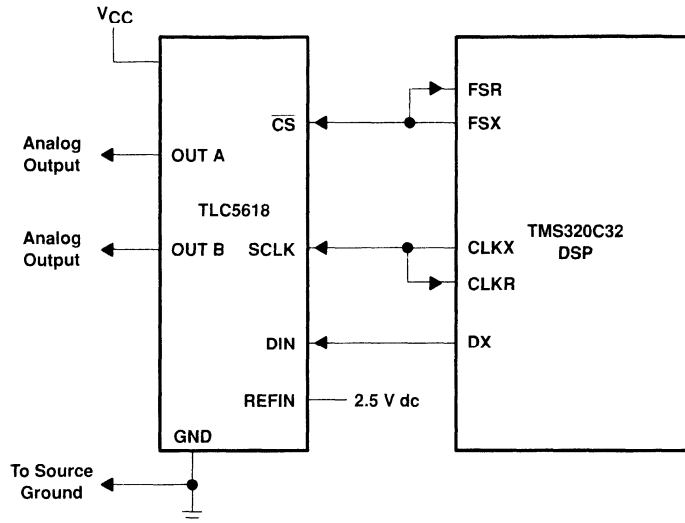


Figure 23. Interfacing The TLC5618 To TMS320C32 DSP

SPI serial interface

Both the TLC5618 and TLC5618A are compatible with SPI, QSPI or Microwire serial standards. The hardware connections are shown in Figures 23 and 24. The TLC5618A has an internal state machine that will count 16 clocks after the falling edge to /CS and then internally disable the device. The internal edge is or'd together with the /CS so that the rising edge can be provided to /CS prior to the occurrence of the internal edge to also disable the device.

general serial interface

The TLC5618 three-wire interface is compatible with the SPI, QSPI, and Microwire serial standards. The hardware connections are shown in Figure 22 and Figure 23.

The SPI and Microwire interfaces transfer data in 8-bit bytes, therefore, two write cycles are required to input data to the DAC. The QSPI interface, which has a variable input data length from 8 to 16 bits, can load the DAC input register in one write cycle.

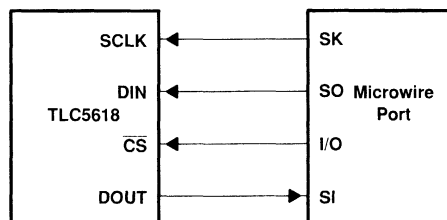


Figure 24. Microwire Connection

APPLICATION INFORMATION

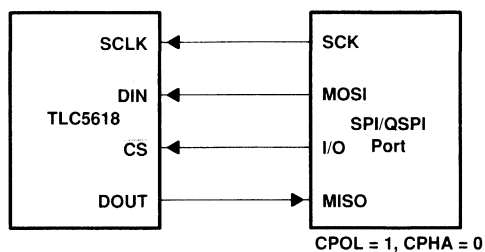


Figure 25. SPI/QSPI Connection

linearity, offset, and gain error using single end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 24.

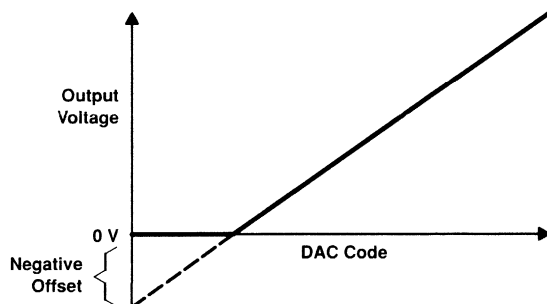


Figure 26. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. The code is calculated from the maximum specification for the negative offset.

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156B – JULY 1997 – REVISED DECEMBER 1997

APPLICATION INFORMATION

power-supply bypassing and ground management

Printed circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane making sure that analog ground currents are well managed.

A 0.1 μF ceramic bypass capacitor should be connected between V_{DD} and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog and digital power supplies.

Figure 25 shows the ground plane layout and bypassing technique.

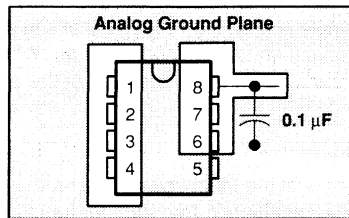


Figure 27. Power-Supply Bypassing

saving power

Setting the DAC register to all 0s minimizes power consumption by the reference resistor array and the output load when the system is not using the DAC.

ac considerations/analog feedthrough

Higher frequency analog input signals may couple to the output through internal stray capacitance. Analog feedthrough is tested by holding $\overline{\text{CS}}$ high, setting the DAC code to all 0s, sweeping the frequency applied to REFIN, and monitoring the DAC output.

TLC5618M

PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER

SGLS106 – DECEMBER 1997

- Programmable Settling Time to 0.5 LSB
3 μ s or 15 μ s Typ
- Two 12-Bit CMOS Voltage Output DACs in an 8-Pin Package
- Simultaneous Updates for DAC A and DAC B
- Single Supply Operation
- 3 Wire Serial Interface
- High-Impedance Reference Inputs
- Voltage Output Range . . . 2 Times the Reference Input Voltage
- Software Power Down Mode
- Internal Power-On Reset
- Low Power Consumption:
3 mW Typ in Slow Mode
8 mW Typ in Fast Mode
- Input Data Update Rate of 1.21 MHz
- Monotonic Over Temperature

applications

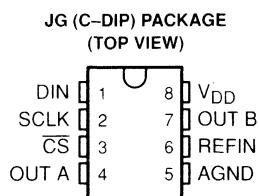
- Battery Powered Test Instruments
- Digital Offset and Gain Adjustment
- Battery Operated/Remote Military Controls
- Machine and Motion Control Devices
- Military Communications

description

The TLC5618 is a dual 12-bit voltage output digital-to-analog converter (DAC) with buffered reference inputs (high impedance). The DACs have an output voltage range that is two times the reference voltage, and the DACs are monotonic. The device is simple to use, running from a single supply of 5 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLC5618 is over a 3-wire CMOS-compatible serial bus. The device receives a 16-bit word for programming and to produce the analog output. The digital inputs feature Schmitt triggers for high noise immunity. Digital communication protocols include the SPI™, QSPI™, and Microwire™ standards.

The 8-terminal JG package allows digital control of analog functions in space-critical applications. The TLC5618M is characterized for operation over the full military temperature range of -55°C to 125°C. The target release timeframe for the TLC876M is estimated to be during the first half of 1998.



AVAILABLE OPTION

PACKAGE	
T_A	CERAMIC DIP (JG)
-55 C to 125 C	TLC5618MJG

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corporation.

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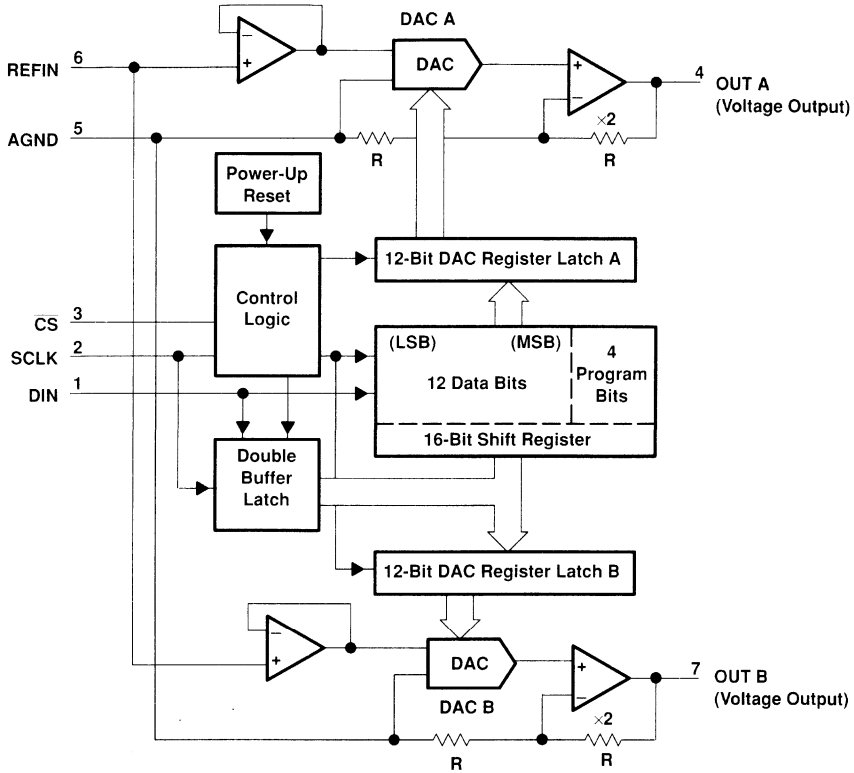
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PRODUCT PREVIEW

TLC5618M PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER

SGLS106 – DECEMBER 1997

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
DIN	1	I	Serial data input
SCLK	2	I	Serial clock input
CS	3	I	Chip select, active low
OUT A	4	O	DAC A analog output
AGND	5		Analog ground
REFIN	6	I	Reference voltage input
OUT B	7	O	DAC B analog output
V _{DD}	8		Positive power supply

PRODUCT PREVIEW

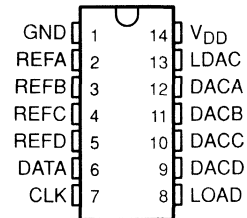


TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081D – NOVEMBER 1994 – REVISED APRIL 1997

- Four 8-Bit Voltage Output DACs
- 5-V Single-Supply Operation
- Serial Interface
- High-Impedance Reference Inputs
- Programmable 1 or 2 Times Output Range
- Simultaneous Update Facility
- Internal Power-On Reset
- Low-Power Consumption
- Half-Buffered Output

N OR D PACKAGE
(TOP VIEW)



applications

- Programmable Voltage Sources
- Digitally Controlled Amplifiers/Attenuators
- Mobile Communications
- Automatic Test Equipment
- Process Monitoring and Control
- Signal Synthesis

description

The TLC5620C and TLC5620I are quadruple 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that ranges between either one or two times the reference voltages and GND, and the DACs are monotonic. The device is simple to use, running from a single supply of 5 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLC5620C and TLC5620I are over a simple three-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 11-bit command word comprises eight bits of data, two DAC-select bits, and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs are updated simultaneously through control of LDAC. The digital inputs feature Schmitt triggers for high noise immunity.

The 14-terminal small-outline (D) package allows digital control of analog functions in space-critical applications. The TLC5620C is characterized for operation from 0°C to 70°C. The TLC5620I is characterized for operation from -40°C to 85°C. The TLC5620C and TLC5620I do not require external trimming.

AVAILABLE OPTIONS

T _A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	TLC5620CD	TLC5620CN
-40°C to 85°C	TLC5620ID	TLC5620IN

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

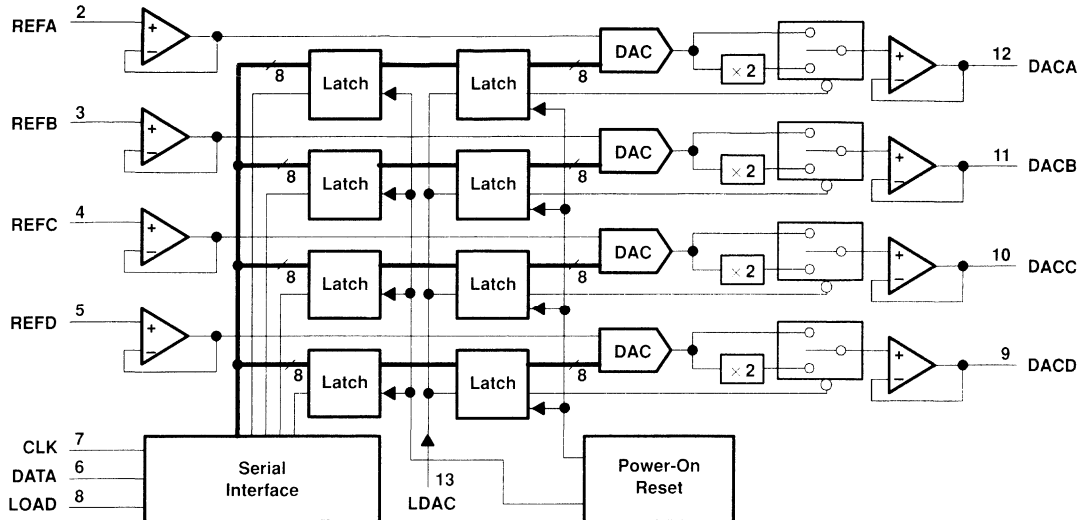
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TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081D – NOVEMBER 1994 – REVISED APRIL 1997

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CLK	7	I	Serial interface clock. The input digital data is shifted into the serial interface register on the falling edge of the clock applied to the CLK terminal.
DACA	12	O	DAC A analog output
DACB	11	O	DAC B analog output
DACC	10	O	DAC C analog output
DACD	9	O	DAC D analog output
DATA	6	I	Serial interface digital data input. The digital code for the DAC is clocked into the serial interface register serially. Each data bit is clocked into the register on the falling edge of the clock signal.
GND	1	I	Ground return and reference terminal
LDAC	13	I	Load DAC. When the LDAC signal is high, no DAC output updates occur when the input digital data is read into the serial interface. The DAC outputs are only updated when LDAC is taken from high to low.
LOAD	8	I	Serial Interface load control. When LDAC is low, the falling edge of the LOAD signal latches the digital data into the output latch and immediately produces the analog voltage at the DAC output terminal.
REFA	2	I	Reference voltage input to DAC A. This voltage defines the output analog range.
REFB	3	I	Reference voltage input to DAC B. This voltage defines the output analog range.
REFC	4	I	Reference voltage input to DAC C. This voltage defines the output analog range.
REFD	5	I	Reference voltage input to DAC D. This voltage defines the output analog range.
V _{DD}	14	I	Positive supply voltage

TLC5620C, TLC5620I

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081D – NOVEMBER 1994 – REVISED APRIL 1997

detailed description

The TLC5620 is implemented using four resistor-string DACs. The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 1. One end of each resistor string is connected to the GND terminal and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor elements and upon the performance of the output buffer. Since the inputs are buffered, the DACs always present a high-impedance load to the reference source.

Each DAC output is buffered by a configurable-gain output amplifier that can be programmed to times 1 or times 2 gain.

On power up, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(\text{DACA|B|C|D}) = \text{REF} \times \frac{\text{CODE}}{256} \times (1 + \text{RNG bit value})$$

where CODE is in the range 0 to 255 and the range (RNG) bit is 0 or 1 within the serial control word.

Table 1. Ideal Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	$(1/256) \times \text{REF} (1+\text{RNG})$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	$(127/256) \times \text{REF} (1+\text{RNG})$
1	0	0	0	0	0	0	0	$(128/256) \times \text{REF} (1+\text{RNG})$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	$(255/256) \times \text{REF} (1+\text{RNG})$

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial input register to the selected DAC as shown in Figure 1. When LDAC is low, the selected DAC output voltage is updated when LOAD goes low. When LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered most significant bit (MSB) first. Data transfers using two 8-clock cycle periods are shown in Figures 3 and 4.

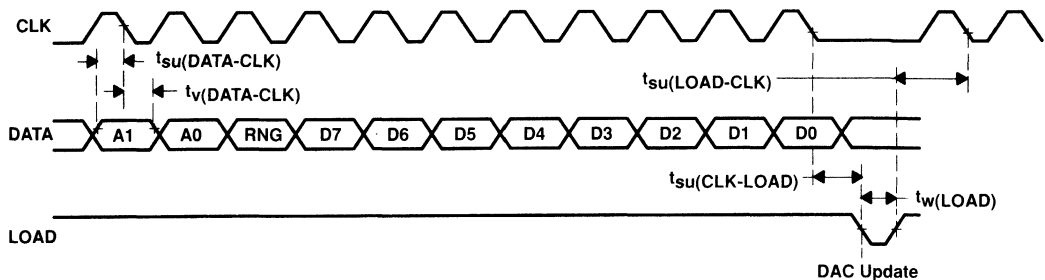


Figure 1. LOAD-Controlled Update (LDAC = Low)

TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081D – NOVEMBER 1994 – REVISED APRIL 1997

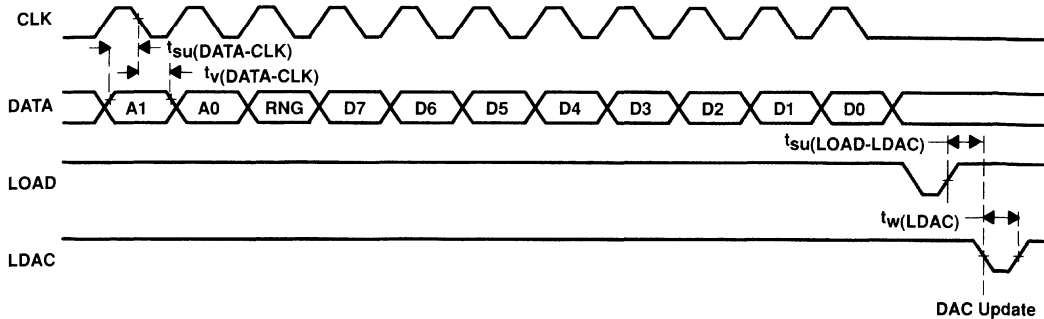


Figure 2. LDAC-Controlled Update

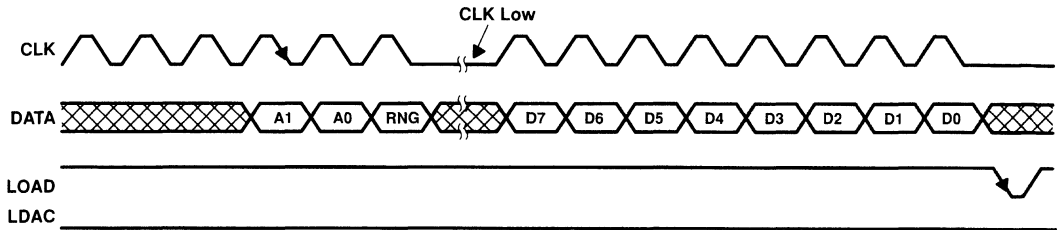


Figure 3. Load-Controlled Update Using 8-Bit Serial Word (LDAC = Low)

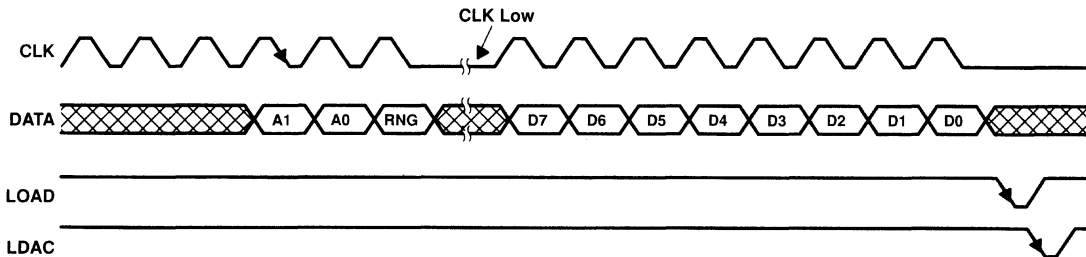


Figure 4. LDAC-Controlled Update Using 8-Bit Serial Word

Table 2 lists the A1 and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = low, the output range is between the applied reference voltage and GND, and when RNG = high, the range is between twice the applied reference voltage and GND.

Table 2. Serial Input Decode

A1	A0	DAC UPDATED
0	0	DACA
0	1	DACB
1	0	DACC
1	1	DACD

TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081D – NOVEMBER 1994 – REVISED APRIL 1997

linearity, offset, and gain error using single-end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset voltage, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 5.

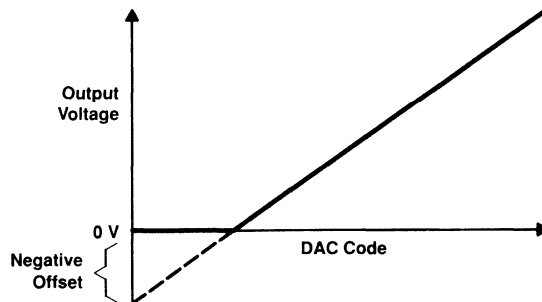


Figure 5. Effect of Negative Offset (Single Supply)

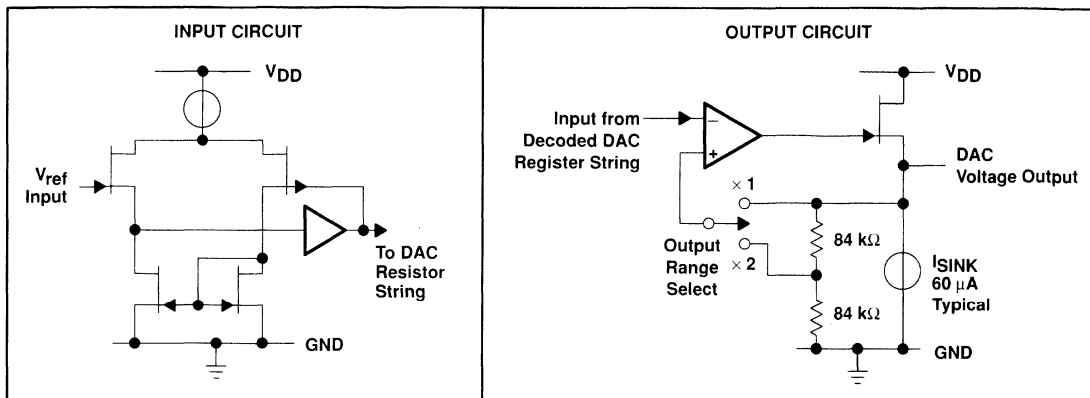
This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below ground.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single-supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. The code is calculated from the maximum specification for the negative offset voltage.

TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081D – NOVEMBER 1994 – REVISED APRIL 1997

equivalent inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage ($V_{DD} - GND$)	7 V
Digital input voltage range	$GND - 0.3 V$ to $V_{DD} + 0.3 V$
Reference input voltage range, V_{ID}	$GND - 0.3 V$ to $V_{DD} + 0.3 V$
Operating free-air temperature range, T_A : TLC5620C	$0^\circ C$ to $70^\circ C$
TLC5620I	$-40^\circ C$ to $85^\circ C$
Storage temperature range, T_{stg}	$-50^\circ C$ to $150^\circ C$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	$260^\circ C$

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.75		5.25	V
High-level input voltage, V_{IH}	$0.8 V_{DD}$			V
Low-level input voltage, V_{IL}			0.8	V
Reference voltage, V_{ref} [A B C D]			$V_{DD} - 1.5$	V
Analog full-scale output voltage, $R_L = 10 k\Omega$		3.5		V
Load resistance, R_L	10			$k\Omega$
Setup time, data input, $t_{su}(DATA-CLK)$ (see Figures 1 and 2)	50			ns
Valid time, data input valid after $CLK\downarrow$, $t_v(DATA-CLK)$ (see Figures 1 and 2)	50			ns
Setup time, CLK eleventh falling edge to $LOAD$, $t_{su}(CLK-LOAD)$ (see Figure 1)	50			ns
Setup time, $LOAD\uparrow$ to $CLK\downarrow$, $t_{su}(LOAD-CLK)$ (see Figure 1)	50			ns
Pulse duration, $LOAD$, $t_w(LOAD)$ (see Figure 1)	250			ns
Pulse duration, $LDAC$, $t_w(LDAC)$ (see Figure 2)	250			ns
Setup time, $LOAD\uparrow$ to $LDAC\downarrow$, $t_{su}(LOAD-LDAC)$ (see Figure 2)	0			ns
CLK frequency			1	MHz
Operating free-air temperature, T_A	TLC5620C	0	70	$^\circ C$
	TLC5620I	-40	85	$^\circ C$



TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081D – NOVEMBER 1994 – REVISED APRIL 1997

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref} = 2\text{ V}$, $\times 1$ gain output range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	$V_I = V_{DD}$				± 10	μA
I_{IL}	Low-level input current	$V_I = 0\text{ V}$				± 10	μA
$I_{O(sink)}$	Output sink current	Each DAC output		20			μA
$I_{O(source)}$	Output source current			2			mA
C_i	Input capacitance				15		pF
	Reference input capacitance				15		
I_{DD}	Supply current	$V_{DD} = 5\text{ V}$				2	mA
I_{ref}	Reference input current	$V_{DD} = 5\text{ V}$,	$V_{ref} = 2\text{ V}$			± 10	μA
E_L	Linearity error (end point corrected)	$V_{ref} = 2\text{ V}$,	$\times 2$ gain (see Note 1)			± 1	LSB
E_D	Differential-linearity error	$V_{ref} = 2\text{ V}$,	$\times 1$ gain (see Note 2)			± 0.9	LSB
E_{ZS}	Zero-scale error	$V_{ref} = 2\text{ V}$,	$\times 2$ gain (see Note 3)	0		30	mV
	Zero-scale-error temperature coefficient	$V_{ref} = 2\text{ V}$,	$\times 2$ gain (see Note 4)		10		$\mu\text{V}/\text{C}$
E_{FS}	Full-scale error	$V_{ref} = 2\text{ V}$,	$\times 2$ gain (see Note 5)			+60	mV
	Full-scale-error temperature coefficient	$V_{ref} = 2\text{ V}$,	$\times 2$ gain (see Note 6)		+25		$\mu\text{V}/\text{C}$
PSRR	Power-supply rejection ratio	See Notes 7 and 8				0.5	mV/V

- NOTES: 1. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
2. Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
4. Zero-scale-error temperature coefficient is given by: $ZSETC = [ZSE(T_{max}) - ZSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
5. Full-scale error is the deviation from the ideal full-scale output ($V_{ref} - 1$ LSB) with an output load of 10 k Ω .
6. Full-scale-error temperature coefficient is given by: $FSETC = [FSE(T_{max}) - FSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
7. Zero-scale-error rejection ratio (ZSE RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
8. Full-scale-error rejection ratio (FSE RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage.

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref} = 2\text{ V}$, $\times 1$ gain output range (unless otherwise noted)

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	$C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$		1		$\text{V}/\mu\text{s}$
Output settling time	$T_o \pm 0.5$ LSB, $C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$. See Note 9		10		μs
Large-signal bandwidth	Measured at -3 dB point		100		kHz
Digital crosstalk	$\text{CLK} = 1\text{-MHz}$ square wave measured at DACA-DACD		-50		dB
Reference feedthrough	See Note 10		-60		dB
Channel-to-channel isolation	See Note 11		-60		dB
Reference input bandwidth	See Note 12		100		kHz

- NOTES: 9. Settling time is the time between a LOAD falling edge and the DAC output reaching full scale voltage within ± 0.5 LSB starting from an initial output voltage equal to zero.
10. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
11. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
12. Reference bandwidth is the -3 dB bandwidth with an input at $V_{ref} = 1.25\text{ V}$ dc + 2 V_{pp} and with a full-scale digital-input code.



TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081D – NOVEMBER 1994 – REVISED APRIL 1997

PARAMETER MEASUREMENT INFORMATION

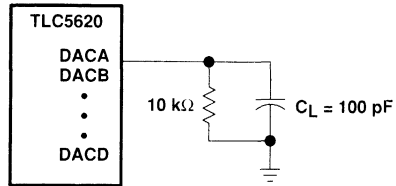


Figure 6. Slew, Settling Time, and Linearity Measurements

TYPICAL CHARACTERISTICS

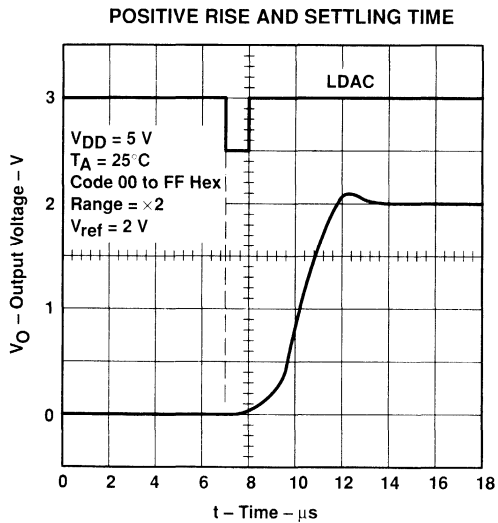


Figure 7

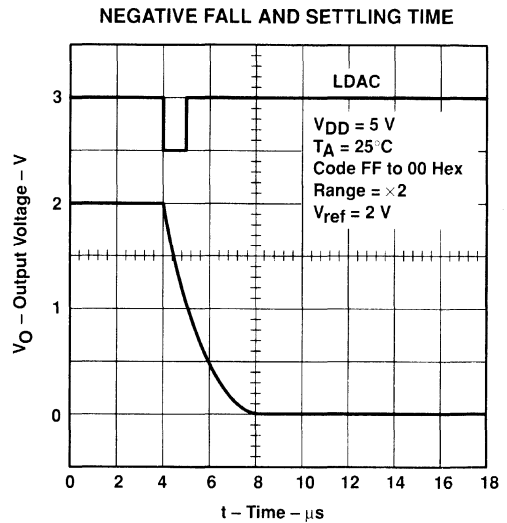


Figure 8

TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081D – NOVEMBER 1994 – REVISED APRIL 1997

TYPICAL CHARACTERISTICS

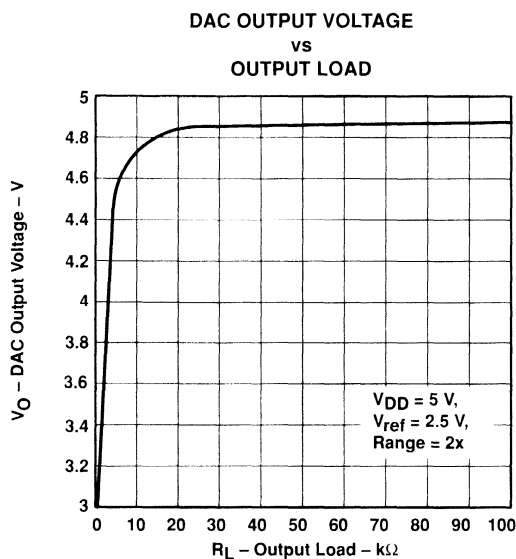


Figure 9

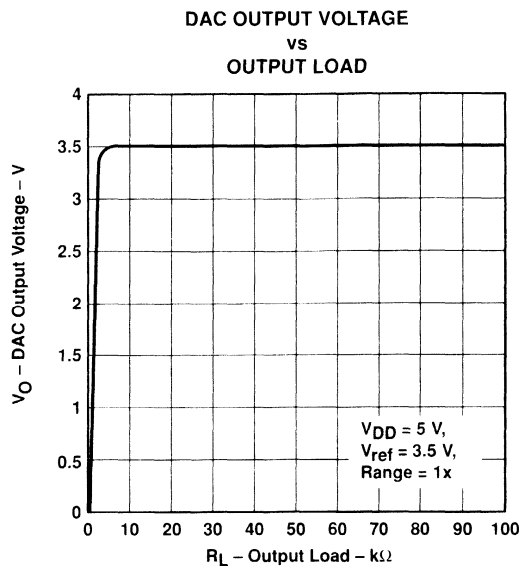


Figure 10

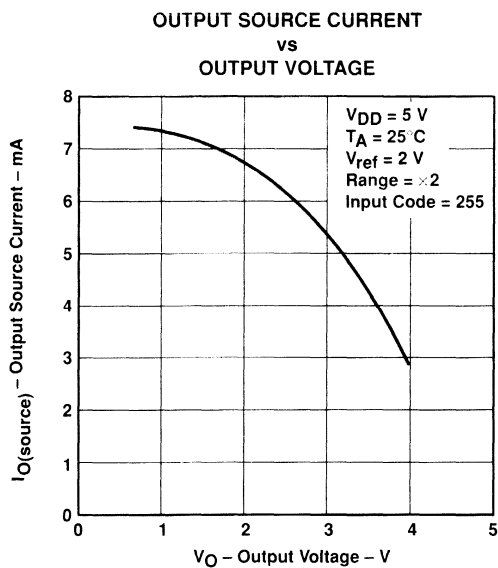


Figure 11

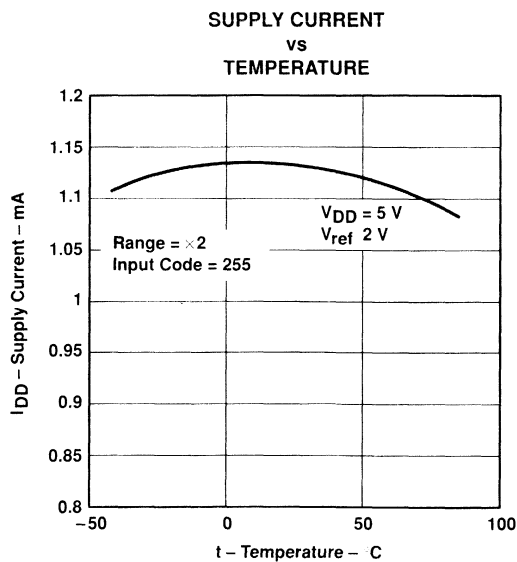


Figure 12



TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081D – NOVEMBER 1994 – REVISED APRIL 1997

TYPICAL CHARACTERISTICS

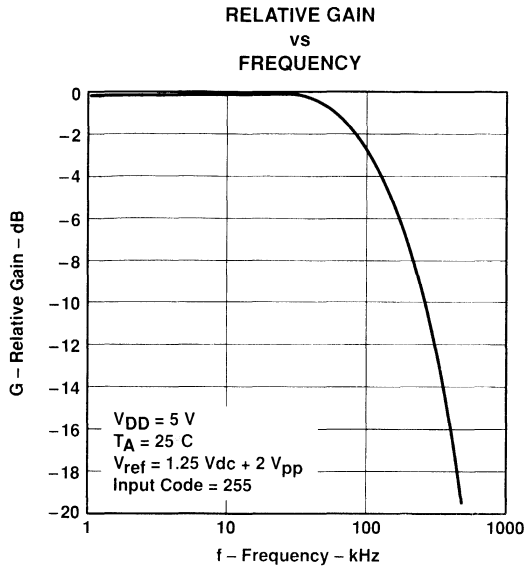


Figure 13

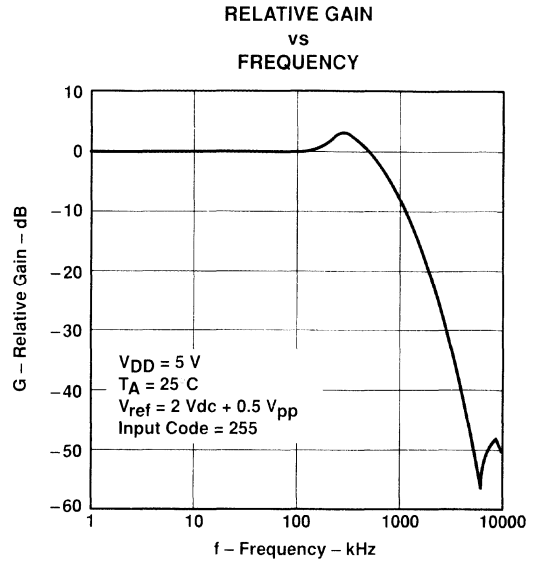
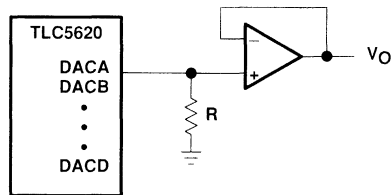


Figure 14

APPLICATION INFORMATION



NOTE A: Resistor $R \geq 10\text{ k}\Omega$

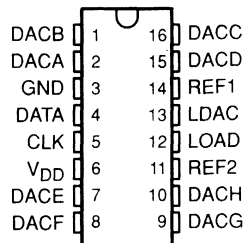
Figure 15. Output Buffering Scheme

TLC5628C, TLC5628I OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS089E – NOVEMBER 1994 – REVISED APRIL 1997

- Eight 8-Bit Voltage Output DACs
- 5-V Single-Supply Operation
- Serial Interface
- High-Impedance Reference Inputs
- Programmable 1 or 2 Times Output Range
- Simultaneous Update Facility
- Internal Power-On Reset
- Low-Power Consumption
- Half-Buffered Output

N OR DW PACKAGE
(TOP VIEW)



applications

- Programmable Voltage Sources
- Digitally Controlled Amplifiers/Attenuators
- Mobile Communications
- Automatic Test Equipment
- Process Monitoring and Control
- Signal Synthesis

description

The TLC5628C and TLC5628I are octal 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that ranges between either one or two times the reference voltages and GND and are monotonic. The device is simple to use, running from a single supply of 5 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLC5628C and TLC5628I are over a simple three-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 12-bit command word comprises eight bits of data, three DAC select bits, and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs are updated simultaneously through control of LDAC. The digital inputs feature Schmitt triggers for high-noise immunity.

The 16-terminal small-outline (D) package allows digital control of analog functions in space-critical applications. The TLC5628C is characterized for operation from 0°C to 70°C. The TLC5628I is characterized for operation from -40°C to 85°C. The TLC5628C and TLC5628I do not require external trimming.

AVAILABLE OPTIONS

PACKAGE		
T _A	SMALL OUTLINE (DW)	PLASTIC DIP (N)
0°C to 70°C	TLC5628CDW	TLC5628CN
-40°C to 85°C	TLC5628IDW	TLC5628IN

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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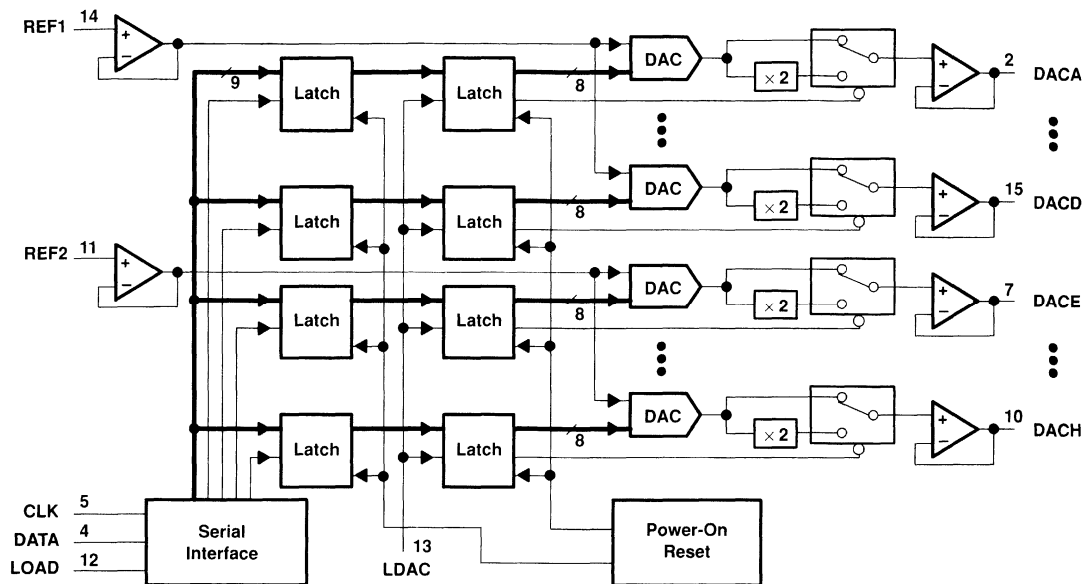
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TLC5628C, TLC5628I

OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS089E – NOVEMBER 1994 – REVISED APRIL 1997

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CLK	5	I	Serial interface clock. The input digital data is shifted into the serial interface register on the falling edge of the clock applied to the CLK terminal.
DACA	2	O	DAC A analog output
DACB	1	O	DAC B analog output
DACC	16	O	DAC C analog output
DACD	15	O	DAC D analog output
DACE	7	O	DAC E analog output
DACF	8	O	DAC F analog output
DAG	9	O	DAC G analog output
DACH	10	O	DAC H analog output
DATA	4	I	Serial interface digital data input. The digital code for the DAC is clocked into the serial interface register serially. Each data bit is clocked into the register on the falling edge of the clock signal.
GND	3	I	Ground return and reference terminal
LDAC	13	I	Load DAC. When LDAC is high, no DAC output updates occur when the input digital data is read into the serial interface. The DAC outputs are only updated when LDAC is taken from high to low.
LOAD	12	I	Serial interface load control. When LDAC is low, the falling edge of the LOAD signal latches the digital data into the output latch and immediately produces the analog voltage at the DAC output terminal.
REF1	14	I	Reference voltage input to DAC A B C D. This voltage defines the analog output range.
REF2	11	I	Reference voltage input to DAC E F G H. This voltage defines the analog output range.
VDD	6	I	Positive supply voltage



TLC5628C, TLC5628I OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS089E – NOVEMBER 1994 – REVISED APRIL 1997

detailed description

The TLC5628 is implemented using eight resistor-string DACs. The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 1. One end of each resistor string is connected to GND and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor segments and upon the performance of the output buffer. Since the inputs are buffered, the DACs always present a high-impedance load to the reference sources. There are two input reference terminals; REF1 is used for DACA through DACD and REF2 is used by DACE through DACH.

Each DAC output is buffered by a configurable-gain output amplifier, that can be programmed to times 1 or times 2 gain.

On power up, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(\text{DACA}|B|C|D|E|F|G|H}) = \text{REF} \times \frac{\text{CODE}}{256} \times (1 + \text{RNG bit value})$$

where CODE is in the range 0 to 255 and the range (RNG) bit is a 0 or 1 within the serial control word.

Table 1. Ideal Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	$(1/256) \times \text{REF} (1+\text{RNG})$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	$(127/256) \times \text{REF} (1+\text{RNG})$
1	0	0	0	0	0	0	0	$(128/256) \times \text{REF} (1+\text{RNG})$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	$(255/256) \times \text{REF} (1+\text{RNG})$

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial input register to the selected DAC as shown in Figure 1. When LDAC is low, the selected DAC output voltage is updated when LOAD goes low. When LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered most significant bit (MSB) first. Data transfers using two 8-clock cycle periods are shown in Figures 3 and 4.

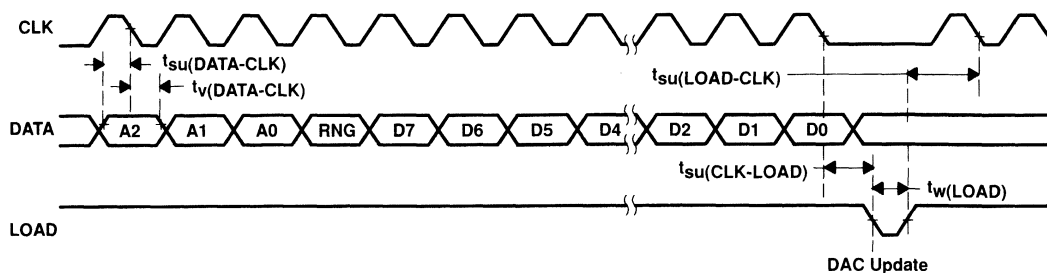


Figure 1. LOAD-Controlled Update (LDAC = Low)



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TLC5628C, TLC5628I OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS089E – NOVEMBER 1994 – REVISED APRIL 1997

data interface (continued)

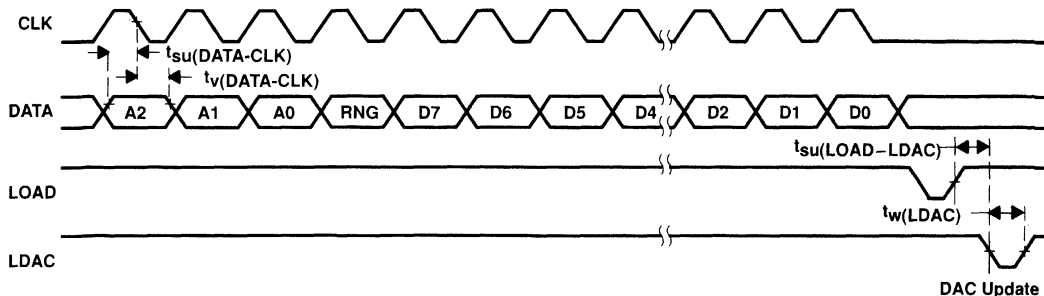


Figure 2. LDAC-Controlled Update

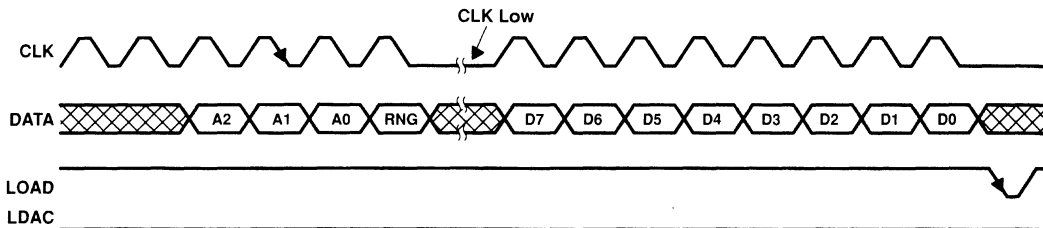


Figure 3. Load-Controlled Update Using 8-Bit Serial Word (LDAC = Low)

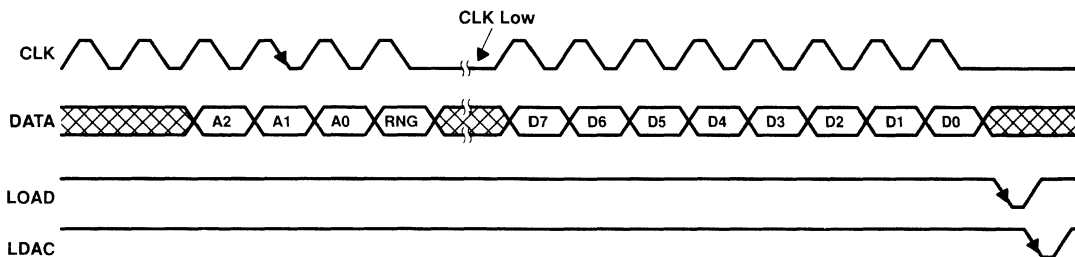


Figure 4. LDAC-Controlled Update Using 8-Bit Serial Word

Table 2 lists the A2, A1, and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = low, the output range is between the applied reference voltage and GND, and when RNG = high, the range is between twice the applied reference voltage and GND.

Table 2. Serial Input Decode

A2	A1	A0	DAC UPDATED
0	0	0	DACA
0	0	1	DACB
0	1	0	DACC
0	1	1	DACD
1	0	0	DACE
1	0	1	DACF
1	1	0	DACG
1	1	1	DACH

linearity, offset, and gain error using single-end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset voltage, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier, therefore, attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground.

The output voltage remains at 0 V until the input code value produces a sufficient output voltage to overcome the inherent negative offset voltage, resulting in the transfer function shown in Figure 5.

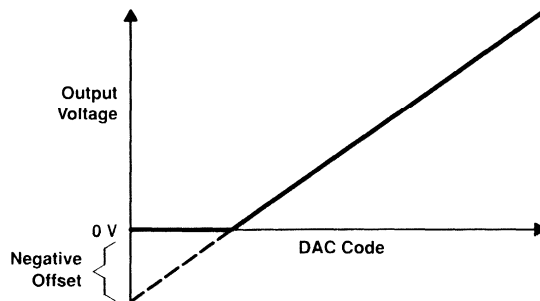


Figure 5. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces the breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below ground.

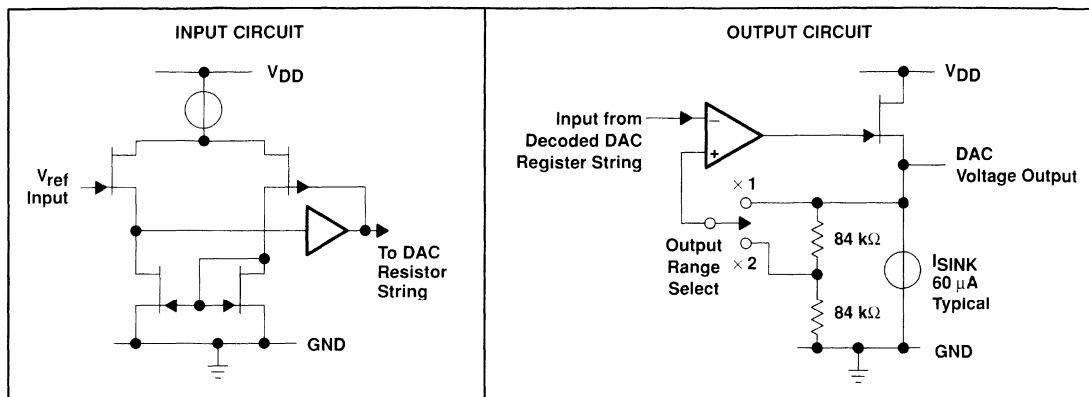
For a DAC, linearity is measured between the zero-input code (all inputs are 0) and the full-scale code (all inputs are 1) after offset and full scale are adjusted out or accounted for in some way. However, single-supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity in the unipolar mode is measured between full-scale code and the lowest code that produces a positive output voltage.

The code is calculated from the maximum specification for the negative offset voltage.

TLC5628C, TLC5628I OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS089E – NOVEMBER 1994 – REVISED APRIL 1997

equivalent of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage ($V_{DD} - GND$)	7 V
Digital input voltage range, V_{ID}	$GND - 0.3 V$ to $V_{DD} + 0.3 V$
Reference input voltage range	$GND - 0.3 V$ to $V_{DD} + 0.3 V$
Operating free-air temperature range, T_A : TLC5628C	$0^\circ C$ to $70^\circ C$
TLC5628I	$-40^\circ C$ to $85^\circ C$
Storage temperature range, T_{stg}	$-50^\circ C$ to $150^\circ C$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	$260^\circ C$

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.75		5.25	V
High-level voltage, V_{IH}	$0.8 V_{DD}$			V
Low-level voltage, V_{IL}			0.8	V
Reference voltage, V_{ref} [A B C D E F G H]			$V_{DD} - 1.5$	V
Analog full-scale output voltage, $R_L = 10 k\Omega$		3.5		V
Load resistance, R_L	10			$k\Omega$
Setup time, data input, $t_{su}(DATA-CLK)$ (see Figures 1 and 2)	50			ns
Valid time, data input valid after $CLK\downarrow$, $t_v(DATA-CLK)$ (see Figures 1 and 2)	50			ns
Setup time, CLK eleventh falling edge to LOAD, $t_{su}(CLK-LOAD)$ (see Figure 1)	50			ns
Setup time, $LOAD\uparrow$ to $CLK\downarrow$, $t_{su}(LOAD-CLK)$ (see Figure 1)	50			ns
Pulse duration, LOAD, $t_w(LOAD)$ (see Figure 1)	250			ns
Pulse duration, LDAC, $t_w(LDAC)$ (see Figure 2)	250			ns
Setup time, $LOAD\uparrow$ to $LDAC\downarrow$, $t_{su}(LOAD-LDAC)$ (see Figure 2)	0			ns
CLK frequency			1	MHz
Operating free-air temperature, T_A	TLC5628C	0	70	$^\circ C$
	TLC5628I	-40	85	$^\circ C$



TLC5628C, TLC5628I

OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS089E – NOVEMBER 1994 – REVISED APRIL 1997

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref} = 2\text{ V}$, $\times 1$ gain output range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	$V_I = V_{DD}$			± 10	μA
I_{IL}	Low-level input current	$V_I = 0\text{ V}$			± 10	μA
$I_{O(sink)}$	Output sink current	Each DAC output		20		μA
$I_{O(source)}$	Output source current			2		mA
C_i	Input capacitance			15		pF
	Reference input capacitance			15		
I_{DD}	Supply current	$V_{DD} = 5\text{ V}$			4	mA
I_{ref}	Reference input current	$V_{DD} = 5\text{ V}$, $V_{ref} = 2\text{ V}$			± 10	μA
E_L	Linearity error (end point corrected)	$V_{ref} = 2\text{ V}$, $\times 2$ gain (see Note 1)			± 1	LSB
E_D	Differential-linearity error	$V_{ref} = 2\text{ V}$, $\times 2$ gain (see Note 2)			± 0.9	LSB
E_{ZS}	Zero-scale error	$V_{ref} = 2\text{ V}$, $\times 2$ gain (see Note 3)	0		30	mV
	Zero-scale-error temperature coefficient	$V_{ref} = 2\text{ V}$, $\times 2$ gain (see Note 4)		10		$\mu\text{V}/\text{C}$
E_{FS}	Full-scale error	$V_{ref} = 2\text{ V}$, $\times 2$ gain (see Note 5)			± 60	mV
	Full-scale-error temperature coefficient	$V_{ref} = 2\text{ V}$, $\times 2$ gain (see Note 6)		± 25		$\mu\text{V}/\text{C}$
PSRR	Power supply rejection ratio	See Notes 7 and 8		0.5		mV/V

- NOTES: 1. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
2. Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
4. Zero-scale-error temperature coefficient is given by: $ZSETC = [ZSE(T_{max}) - ZSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
5. Full-scale error is the deviation from the ideal full-scale output ($V_{ref} - 1\text{ LSB}$) with an output load of $10\text{ k}\Omega$.
6. Full-scale error temperature coefficient is given by: $FSETC = [FSE(T_{max}) - FSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
7. Zero-scale-error rejection ratio (ZSE RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
8. Full-scale-error rejection ratio (FSE RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage.

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref} = 2\text{ V}$, $\times 1$ gain output range (unless otherwise noted)

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	$C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$		1		$\text{V}/\mu\text{s}$
Output settling time	$T_o \pm 0.5\text{ LSB}$, $C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, See Note 9		10		μs
Large signal bandwidth	Measured at -3 dB point		100		kHz
Digital crosstalk	$\text{CLK} = 1\text{-MHz}$ square wave measured at DACA-DACD		-50		dB
Reference feedthrough	See Note 10		-60		dB
Channel-to-channel isolation	See Note 11		-60		dB
Reference input bandwidth	See Note 12		100		kHz

- NOTES: 9. Settling time is the time between a LOAD falling edge and the DAC output reaching full-scale voltage within $\pm 0.5\text{ LSB}$ starting from an initial output voltage equal to zero.
10. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz .
11. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz .
12. Reference bandwidth is the -3 dB bandwidth with an input at $V_{ref} = 1.25\text{ V}$ dc + 2 V_{pp} and with a full-scale digital input code.



TLC5628C, TLC5628I OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS089E – NOVEMBER 1994 – REVISED APRIL 1997

PARAMETER MEASUREMENT INFORMATION

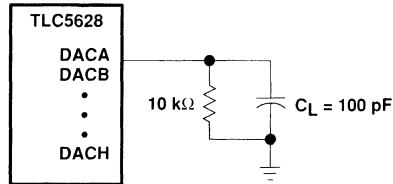


Figure 6. Slew, Settling Time, and Linearity Measurements

TYPICAL CHARACTERISTICS

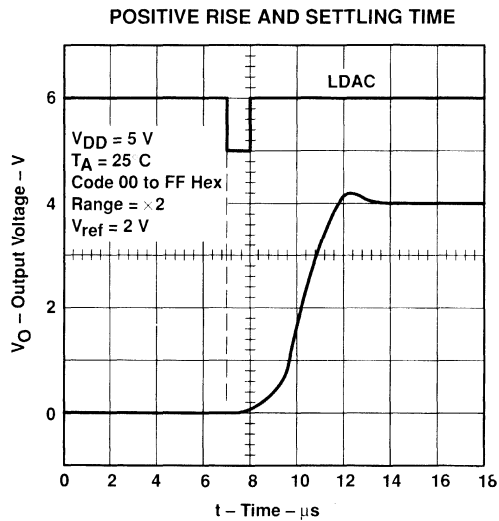


Figure 7

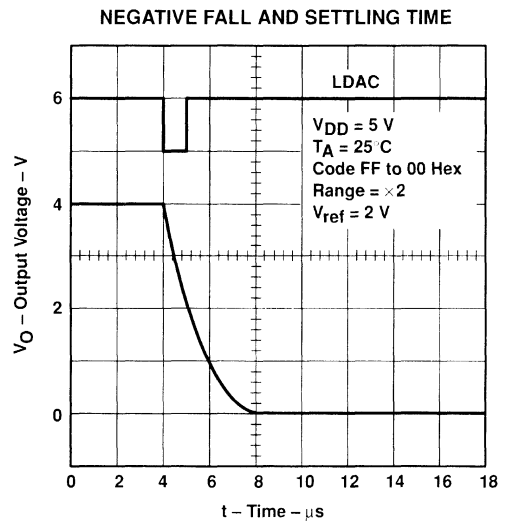


Figure 8

TLC5628C, TLC5628I OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS089E - NOVEMBER 1994 - REVISED APRIL 1997

TYPICAL CHARACTERISTICS

DAC OUTPUT VOLTAGE
vs
OUTPUT LOAD

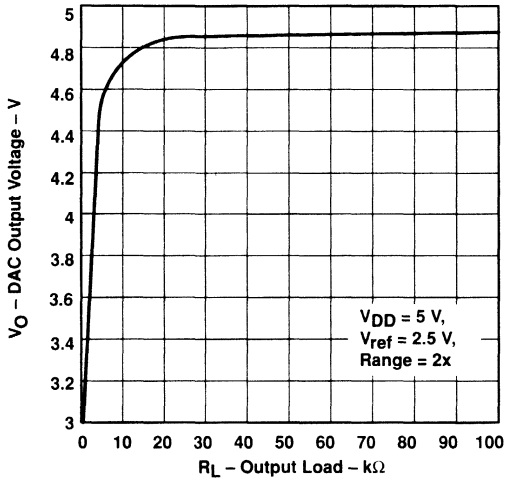


Figure 9

DAC OUTPUT VOLTAGE
vs
OUTPUT LOAD

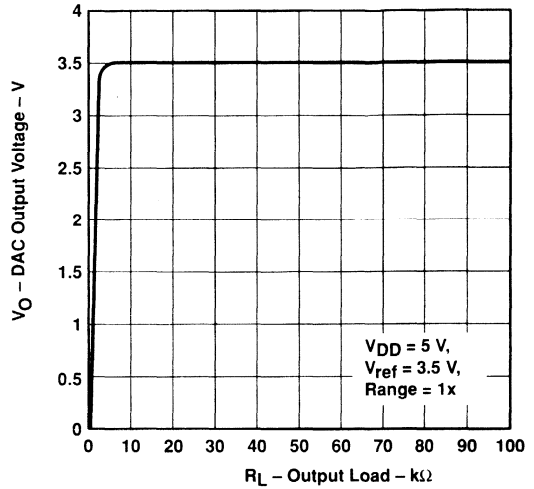


Figure 10

OUTPUT SOURCE CURRENT
vs
OUTPUT VOLTAGE

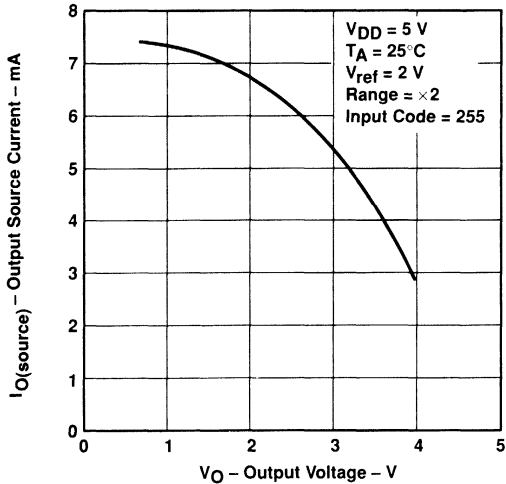


Figure 11

SUPPLY CURRENT
vs
TEMPERATURE

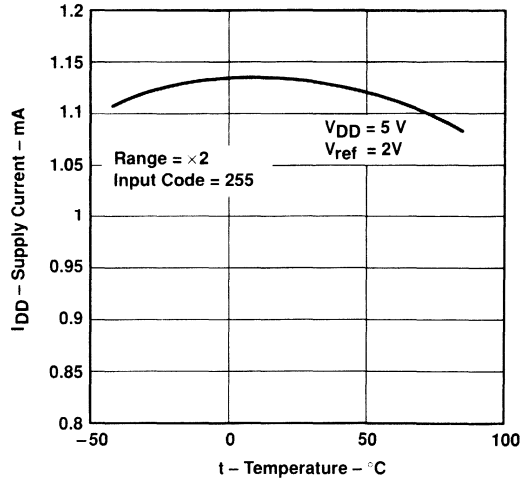


Figure 12



TLC5628C, TLC5628I OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS089E – NOVEMBER 1994 – REVISED APRIL 1997

TYPICAL CHARACTERISTICS

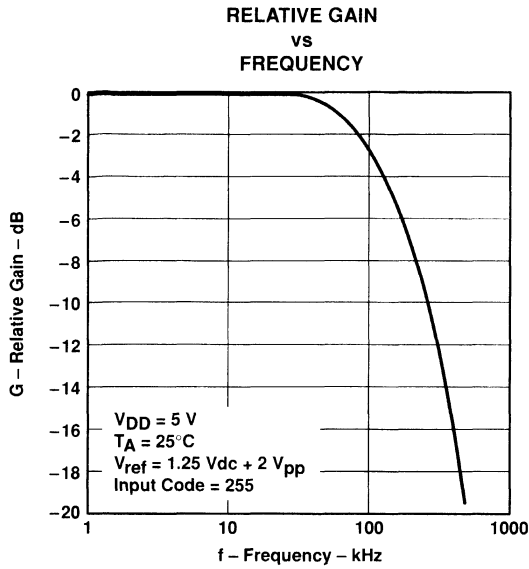


Figure 13

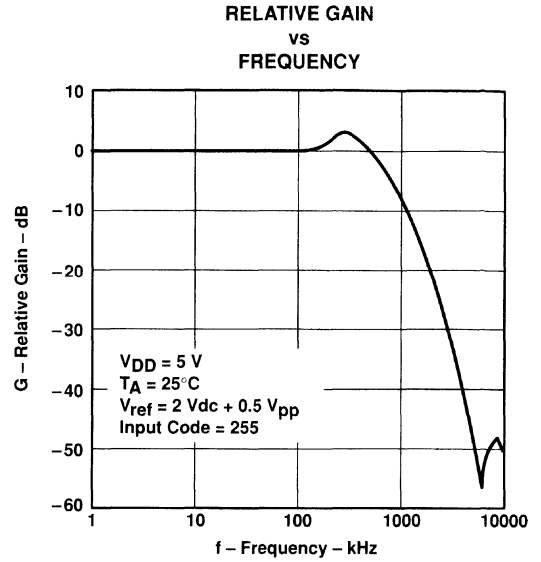
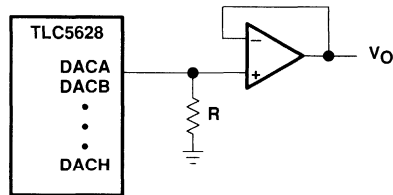


Figure 14

APPLICATION INFORMATION



NOTE A: Resistor $R \geq 10\text{ k}\Omega$

Figure 15. Output Buffering Scheme

TLC7225C, TLC7225I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS109A – OCTOBER 1996 – REVISED APRIL 1997

- Four 8-Bit D/A Converters With Individual References
- Direct Bipolar Operation Without an External Level-Shift Amplifier
- Microprocessor Compatible
- TTL/CMOS Compatible
- Single Supply Operation Possible
- Simultaneous Update Facility
- Binary Input Coding

applications

- Process Control
- Automatic Test Equipment
- Automatic Calibration of Large System Parameters e.g., Gain/Offset

description

The TLC7225 consists of four 8-bit voltage-output digital-to-analog converters (DACs), with output buffer amplifiers and interface logic with double register-buffering.

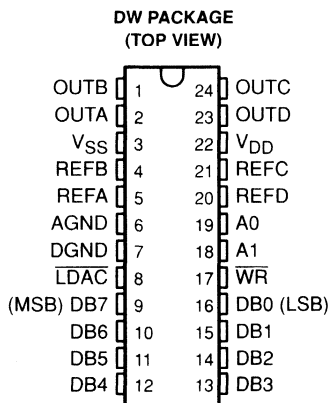
Separate on-chip latches are provided for each of the DACs. Data is transferred into one of these data latches through a common 8-bit TTL/CMOS-compatible (5 V) input port. Control inputs A0 and A1 determine which DAC is loaded when \overline{WR} goes low. Only the data held in the DAC registers determines the analog outputs of the converters. The double register buffering allows simultaneous update of all four outputs under control of \overline{LDAC} . All logic inputs are TTL- and CMOS-level compatible and the control logic is speed compatible with most 8-bit microprocessors. Each DAC includes an output buffer amplifier capable of driving up to 5 mA of output current.

The TLC7225 performance is specified for input reference voltages from 2 V to $V_{DD} - 4$ V with dual supplies. The voltage-mode configuration of the DACs allow the TLC7225 to be operated from a single power-supply rail at a reference of 10 V.

The TLC7225 is fabricated in a LinBiCMOS™ process that has been specifically developed to allow high-speed digital logic circuits and precision analog circuits to be integrated on the same chip. The TLC7225 has a common 8-bit data bus with individual DAC latches. This provides a versatile control architecture for simple interface to microprocessors. All latch-enable signals are level triggered.

Combining four DACs, four operational amplifiers, and interface logic into a small, 0.3-inch wide, 24-terminal SOIC allows significant reduction in board space requirements and offers increased reliability in systems using multiple converters. The pinout optimizes board layout with all of the analog inputs and outputs at one end of the package and all of the digital inputs at the other.

The TLC7225C is characterized for operation from 0°C to 70°C. The TLC7225I is characterized for operation from -40°C to 85°C.



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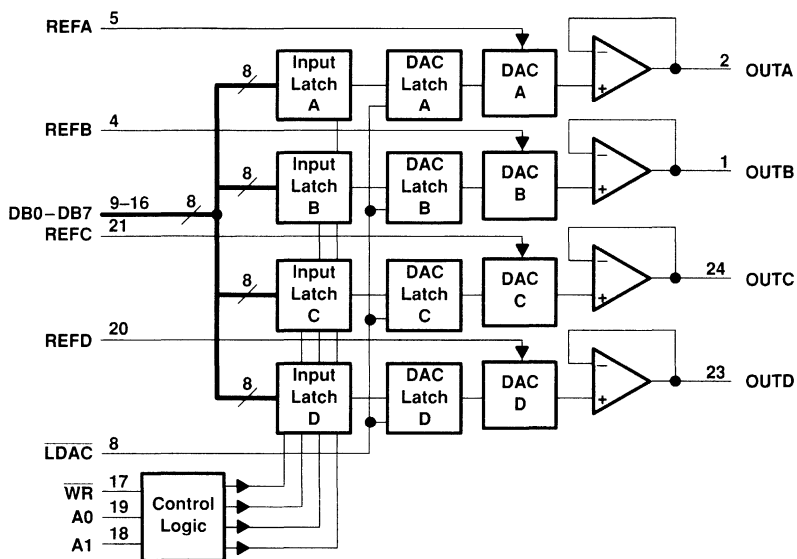
TLC7225C, TLC7225I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS109A – OCTOBER 1996 – REVISED APRIL 1997

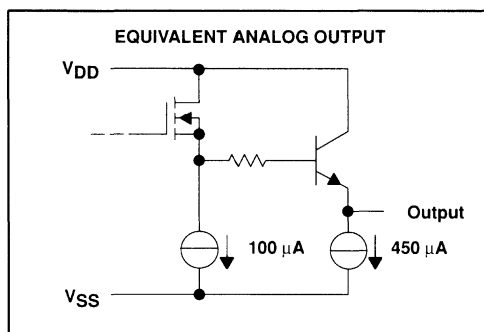
AVAILABLE OPTIONS

PACKAGED DEVICES	
T _A	SMALL OUTLINE (DW)
0°C to 70°C	TLC7225CDW
-40°C to 85°C	TLC7225IDW

functional block diagram



schematic of outputs



TLC7225C, TLC7225I

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS109A – OCTOBER 1996 – REVISED APRIL 1997

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	6		Analog ground
A0, A1	18, 19	I	DAC select inputs
DGND	7		Digital ground
DB0 – DB7	9 – 16	I	Digital DAC data inputs
LDAC	8		Load DAC. A high level simultaneously loads all four DAC registers. DAC registers are transparent when LDAC is low.
OUTA	2	O	DACA output
OUTB	1	O	DACB output
OUTC	24	O	DACC output
OUTD	23	O	DACD output
REFA	5	I	Voltage reference input to DACA
REFB	4	I	Voltage reference input to DACB
REFC	21	I	Voltage reference input to DACC
REFD	20	I	Voltage reference input to DACD
VDD	22		Positive supply voltage
VSS	3		Negative supply voltage
WR	17	I	Write input selects DAC transparency or latch mode

absolute maximum ratings over operating free-air temperature range (unless otherwise note)†

Supply voltage range, V_{DD} : to AGND or DGND	–0.3 V to 17 V
to V_{SS}	–0.3 V to 24 V
Supply voltage range, V_{SS} : to AGND or DGND	–7 V to V_{DD}
Voltage range between AGND and DGND	–0.3 V to V_{DD}
Input voltage range, V_I (to DGND)	–0.3 V to $V_{DD} + 0.3$ V
Reference voltage range, V_{ref} (to AGND)	–0.3 V to V_{DD}
Output voltage range, V_O (to AGND) (see Note 1)	V_{SS} to V_{DD}
Continuous total power dissipation at (or below) $T_A = 25^\circ\text{C}$ (see Note 2)	500 mW
Operating free-air temperature range: C suffix	0°C to 70°C
I suffix	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Output voltages may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 50 mA.

2. For operation above $T_A = 75$ C derate linearly at the rate of 2.0 mW/°C.



TLC7225C, TLC7225I

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS109A – OCTOBER 1996 – REVISED APRIL 1997

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		11.4	16.5	V
Supply voltage, V_{SS}		-5.5	0	V
High-level input voltage, V_{IH}		2		V
Low-level input voltage, V_{IL}			0.8	V
Reference voltage, V_{ref}		2	$V_{DD}-4$	V
Load resistance, R_L		2		$k\Omega$
Operating free-air temperature, T_A	C suffix	0	70	$^{\circ}C$
	I suffix	-40	85	$^{\circ}C$

timing requirements (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{su}(AW)$	Setup time, address valid before $WR\downarrow$		0		ns
$t_{su}(DW)$	Setup time, data valid before $WR\uparrow$	$V_{DD} = 11.4\text{ V to }16.5\text{ V}$, $V_{SS} = 0\text{ or }-5\text{ V}$	45		ns
$t_h(AW)$	Hold time, address valid after $WR\uparrow$	$V_{DD} = 11.4\text{ V to }16.5\text{ V}$, $V_{SS} = 0\text{ or }-5\text{ V}$	0		ns
$t_h(DW)$	Hold time, data valid after $WR\uparrow$	$V_{DD} = 11.4\text{ V to }16.5\text{ V}$, $V_{SS} = 0\text{ or }-5\text{ V}$	10		ns
t_{w1}	Pulse duration, WR low	$V_{DD} = 11.4\text{ V to }16.5\text{ V}$, $V_{SS} = 0\text{ or }-5\text{ V}$	50		ns
t_{w2}	Pulse duration, $LDAC$ low	$V_{DD} = 11.4\text{ V to }16.5\text{ V}$, $V_{SS} = 0\text{ or }-5\text{ V}$	50		ns

TLC7225C, TLC7225I

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS109A – OCTOBER 1996 – REVISED APRIL 1997

electrical characteristics over recommended operating free-air temperature range

reference inputs (all supply ranges)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
r_i	Input resistance, REFA, REFB, REFC, REFD		1.5	4		k Ω
C_i	Input capacitance, REFA, REFB, REFC, REFD	DAC loaded with all 1s			300	pF
		DAC loaded with all 0s	65			pF
Channel-to-channel isolation		$V_{ref} = 10 V_{pp}$ sine wave at 10 kHz	60			dB
ac feedthrough			70			dB

dual power supply over recommended supply and reference voltage ranges, AGND = DGND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input current, digital	$V_I = 0$ or V_{DD}			± 1	μA
I_{DD}	Supply current, V_{DD}	$V_I = V_{IL}$ or V_{IH} . No load		10	16	mA
I_{SS}	Supply current, V_{SS}	$V_I = V_{IL}$ or V_{IH} . No load		4	10	mA
Power supply sensitivity		$\Delta V_{DD} = \pm 5\%$			0.01	%/%
C_i	Input capacitance	Digital inputs			8	pF

single power supply, $V_{DD} = 14.25 V$ to $15.75 V$, $V_{SS} = AGND = DGND = 0 V$, $V_{ref} (A, B, C, D) = 10 V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input current, digital	$V_I = 0$ or V_{DD}			± 1	μA
I_{DD}	Supply current, V_{DD}	$V_I = V_{IL}$ or V_{IH} . No load		5	13	mA
Power supply sensitivity		$\Delta V_{DD} = \pm 5\%$			0.01	%/%
C_i	Input capacitance	Digital inputs			8	pF



TLC7225C, TLC7225I

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS109A – OCTOBER 1996 – REVISED APRIL 1997

operating characteristics over recommended operating free-air temperature range

dual power supply over recommended supply and reference voltage ranges, AGND = DGND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Slew rate			2.5			V/ μ s
t_s	Settling time to 1/2 LSB	$V_{ref}(A, B, C, D) = 10\text{ V}$			5	μ s
					7	
Resolution				8		Bits
Total unadjusted error		$V_{DD} = 15\text{ V} \pm 5\%$, $V_{ref}(A, B, C, D) = 10\text{ V}$			± 2	LSB
Integral nonlinearity (INL)		$V_{DD} = 15\text{ V} \pm 5\%$, $V_{ref}(A, B, C, D) = 10\text{ V}$			± 1	LSB
Differential nonlinearity (DNL)		$V_{DD} = 15\text{ V} \pm 5\%$, $V_{ref}(A, B, C, D) = 10\text{ V}$			± 1	LSB
EFS	Full-scale error	$V_{DD} = 15\text{ V} \pm 5\%$, $V_{ref}(A, B, C, D) = 10\text{ V}$			± 2	LSB
EG	Gain error	$V_{DD} = 15\text{ V} \pm 5\%$, $V_{ref}(A, B, C, D) = 10\text{ V}$		± 0.25		LSB
	Temperature coefficient of gain	$V_{DD} = 14\text{ V to } 16.5\text{ V}$, $V_{ref}(A, B, C, D) = 10\text{ V}$		± 20		ppm/ $^{\circ}$ C
				± 50		μ V/ $^{\circ}$ C
Zero-code error				± 20	± 80	mV
Digital crosstalk or feedthrough glitch impulse area		$V_{ref}(A, B, C, D) = 0$		50		nV-s

single power supply, $V_{DD} = 14.25\text{ V to } 15.75\text{ V}$, $V_{SS} = \text{AGND} = \text{DGND} = 0\text{ V}$, $V_{ref}(A, B, C, D) = 10\text{ V}$ (unless otherwise noted)

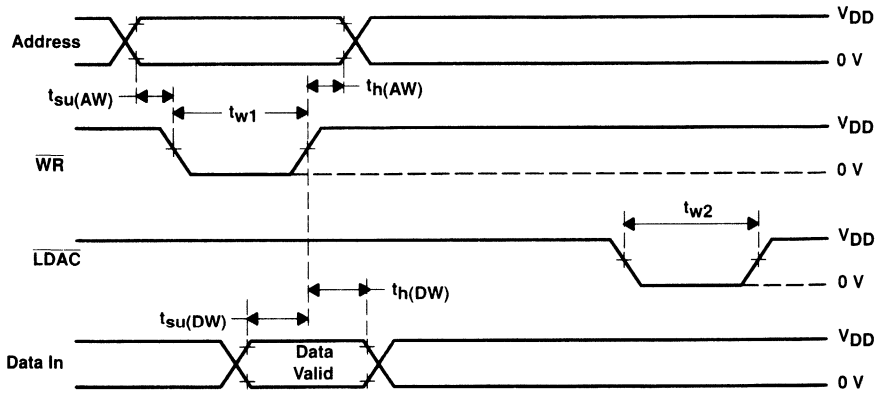
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Slew rate			2			V/ μ s
t_s	Settling time to 1/2 LSB				5	μ s
					20	
Resolution				8		Bits
Total unadjusted error					± 2	LSB
EFS	Full-scale error				± 2	LSB
	Temperature coefficient of gain	$V_{DD} = 14\text{ V to } 16.5\text{ V}$, $V_{ref}(A, B, C, D) = 10\text{ V}$		± 20		ppm/ $^{\circ}$ C
				± 50		μ V/ $^{\circ}$ C
Differential nonlinearity error (DNL)					± 1	LSB
Digital crosstalk or feedthrough glitch impulse area				50		nV-s



TLC7225C, TLC7225I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS109A – OCTOBER 1996 – REVISED APRIL 1997

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. $t_r = t_f = 20$ ns over V_{DD} range.
 B. The timing-measurement reference level is equal to $V_{IH} + V_{IL}$ divided by 2.
 C. If LDAC is activated prior to the rising edge of WR, then it must remain low for at least t_{w2} after WR goes high.

Figure 1. Write-Cycle Voltage Waveforms

TYPICAL CHARACTERISTICS

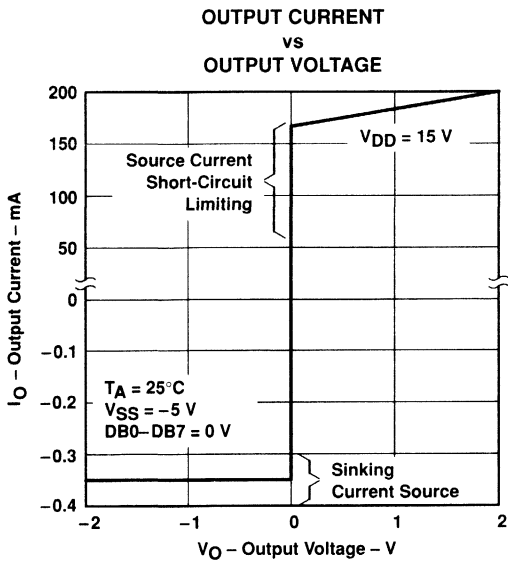


Figure 2

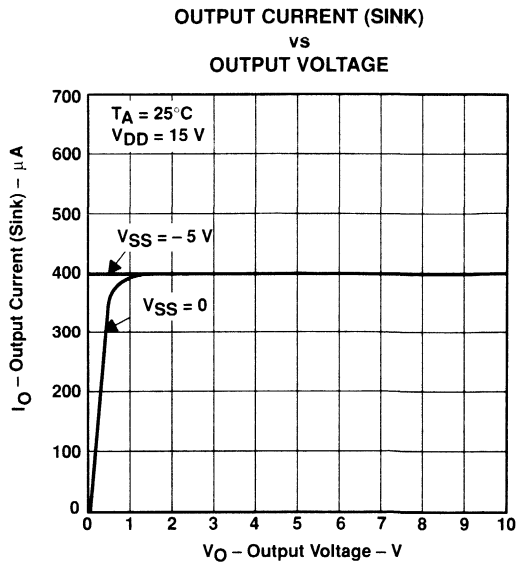


Figure 3



TLC7225C, TLC7225I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS109A – OCTOBER 1996 – REVISED APRIL 1997

APPLICATION INFORMATION

specification ranges

For the TLC7225 to operate to rated specifications, the input reference voltage must be at least 4 V below the power supply voltage at the V_{DD} terminal. This voltage differential is the overhead voltage required by the output amplifiers.

The TLC7225 is specified to operate over a V_{DD} range from $12\text{ V} \pm 5\%$ to $15\text{ V} \pm 10\%$ (i.e., from 11.4 V to 16.5 V) with a V_{SS} of $-5\text{ V} \pm 10\%$. Operation is also specified for a single supply with a V_{DD} of $15\text{ V} \pm 5\%$. Applying a V_{SS} of -5 V results in improved zero-code error, improved output sink capability with outputs near AGND, and improved negative-going settling time.

Performance is specified over the range of reference voltages from 2 V to $(V_{DD} - 4\text{ V})$ with dual supplies. This allows a range of standard reference generators to be used such as the TL1431, with an adjustable 2.5-V bandgap reference. Note that an output voltage range of 0 V to 10 V requires a nominal $15\text{ V} \pm 5\%$ power supply voltage.

DAC section

The TLC7225 contains four, identical, 8-bit voltage-mode DACs. Each converter has a separate reference input. The output voltages from the converters have the same polarity as the reference voltages, thus allowing single supply operation.

The simplified circuit diagram for channel A is shown in Figure 4. Note that AGND (terminal 6) is common to all four DACs.

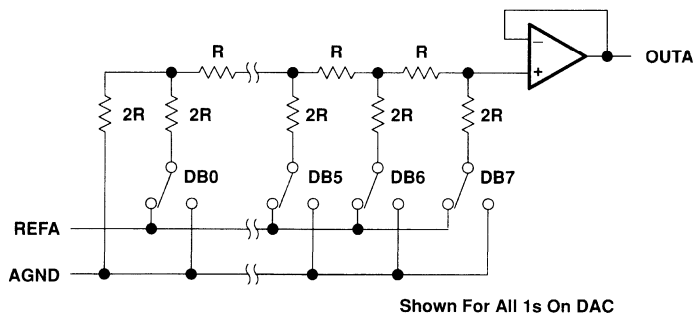


Figure 4. DAC Simplified-Circuit Diagram

The input impedance at any of the reference inputs is code dependent and can vary from 1.4 k Ω minimum to an open circuit. The lowest input impedance at any reference input occurs when that DAC is loaded with the digital code 01010101. Therefore, it is important that the reference source presents a low output impedance under changing load conditions. The nodal capacitance at the reference terminals is also code dependent and typically varies from 60 pF to 300 pF.

Each OUT_x terminal can be considered as a digitally programmable voltage source with an output voltage of:

$$V_{OUT_x} = D_x \times V_{REF_x}$$

where D_x is the fractional representation of the digital input code and can vary from 0 to 255/256.

The output impedance is that of the output buffer amplifier.

TLC7225C, TLC7225I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS109A – OCTOBER 1996 – REVISED APRIL 1997

APPLICATION INFORMATION

output buffer

Each voltage-mode DAC output is buffered by a unity-gain noninverting amplifier. This buffer amplifier is capable of developing 10 V across a 2-k Ω load and can drive capacitive loads of 3300 pF.

The TLC7225 can be operated as a single or dual supply; operating with dual supplies results in enhanced performance in some parameters which cannot be achieved with a single-supply operation. In a single supply operating ($V_{SS} = 0\text{ V} = \text{AGND}$) the sink capability of the amplifier, which is normally 400 μA , is reduced as the output voltage nears AGND. The full sink capability of 400 μA is maintained over the full output voltage range by tying V_{SS} to -5 V . This is indicated in Figure 3.

Settling time for negative-going output signals approaching AGND is similarly affected by V_{SS} . Negative-going settling time for single supply operation is longer than for dual supply operation. Positive-going settling-time is not affected by V_{SS} .

Additionally, the negative V_{SS} gives more headroom to the output amplifiers which results in better zero code performance and improved slew rate at the output than can be obtained in the single-supply mode.

digital inputs

The TLC7225 digital inputs are compatible with either TTL or 5-V CMOS levels. To minimize power supply currents, it is recommended that the digital input voltages be driven as close to the supply rails (V_{DD} and DGND) as practically possible.

interface logic information

The TLC7225 contains two registers per DAC, an input register and a DAC register. Address lines A0 and A1 select which input register accepts data from the input port. When the $\overline{\text{WR}}$ signal is low, the input latches of the selected DAC are transparent. The data is latched into the addressed input register on the rising edge of $\overline{\text{WR}}$. Table 1 shows the addressing for the input registers on the TLC7225.

Table 1. TLC7225 Addressing

CONTROL INPUTS		SELECTED INPUT REGISTER
A1	A0	
L	L	DAC A input register
L	H	DAC B input register
H	L	DAC C input register
H	H	DAC D input register

Only the data held in the DAC register determines the analog output of the converter. The $\overline{\text{LDAC}}$ signal is common to all four DACs and controls the transfer of information from the input registers to the DAC registers. Data is latched into all four DAC registers simultaneously on the rising edge of $\overline{\text{LDAC}}$. The $\overline{\text{LDAC}}$ signal is level triggered and, therefore, the DAC registers may be made transparent by tying $\overline{\text{LDAC}}$ low (the outputs of the converters responds to the data held in their respective input latches). $\overline{\text{LDAC}}$ is an asynchronous signal and is independent of $\overline{\text{WR}}$. This is useful in many applications. However, in systems where the asynchronous $\overline{\text{LDAC}}$ can occur during a write cycle (or vice versa) care must be taken to ensure that incorrect data is not latched through to the output. In other words, if $\overline{\text{LDAC}}$ is activated prior to the rising edge of $\overline{\text{WR}}$ (or $\overline{\text{WR}}$ occurs during $\overline{\text{LDAC}}$), then $\overline{\text{LDAC}}$ must stay low for a time of t_{w2} or longer after $\overline{\text{WR}}$ goes high to ensure that the correct data is latched through to the output. Table 2 shows the truth table for TLC7225 operation. Figure 5 shows the input control logic for the device and the write cycles timing diagram is shown in Figure 1.



TLC7225C, TLC7225I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS109A – OCTOBER 1996 – REVISED APRIL 1997

APPLICATION INFORMATION

Table 2. TLC7225 Truth Table

CONTROL INPUTS		FUNCTION
\overline{WR}	\overline{LDAC}	
H	H	No operation. Device not selected
L	H	Input register of selected DAC is transparent.
↑	H	Input register of selected DAC is latched.
H	L	All four DAC registers are transparent (i.e., outputs respond to data held in respective input registers) input registers are latched.
H	↑	All four DAC registers are latched.
L	L	DAC registers and selected input register are transparent. Output follows input data for selected channel.

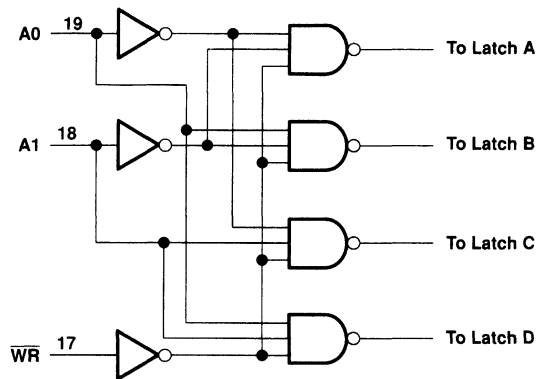


Figure 5. Input Control Logic

TLC7225C, TLC7225I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS109A – OCTOBER 1996 – REVISED APRIL 1997

APPLICATION INFORMATION

ground management and layout

The TLC7225 contains four reference inputs that can be driven from ac sources (see multiplying DAC using ac input to the REF terminals section) so careful layout and grounding is important to minimize analog crosstalk between the four channels. The dynamic performance of the four DACs depends upon the optimum choice of board layout. Figure 6 shows the relationship between input frequency and channel-to-channel isolation. Figure 7 shows a printed circuit board layout that minimizes crosstalk and feedthrough. The four input signals are screened by AGND. V_{ref} was limited between 2 V and 3.24 V to avoid slew-rate limiting effects from the output amplifier during measurements.

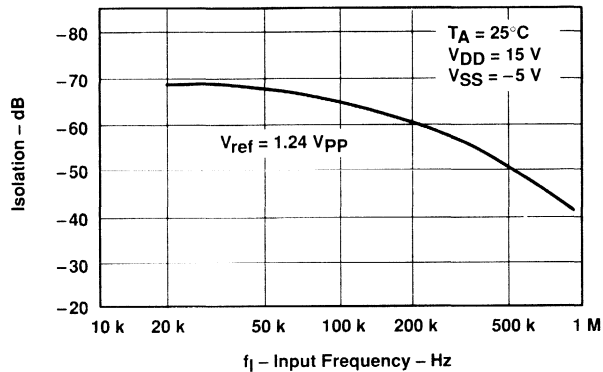


Figure 6. Channel-to-Channel Isolation

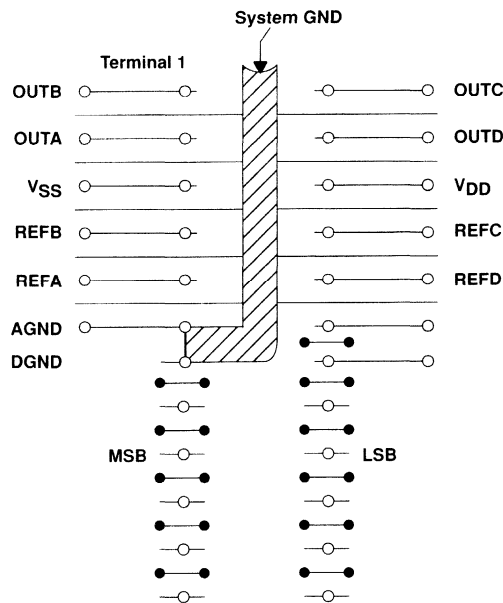


Figure 7. Suggested PCB Layout (Top View)

TLC7225C, TLC7225I

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS109A – OCTOBER 1996 – REVISED APRIL 1997

APPLICATION INFORMATION

unipolar output operation

The unipolar output operation is the basic mode of operation for each channel of the TLC7225, with the output voltages having the same positive polarity as V_{ref} . The TLC7225 can be operated with a single supply ($V_{SS} = AGND$) or with positive or negative supplies. The voltage at V_{ref} must never be negative with respect to DGND to prevent parasitic transistor turn-on. Connections for the unipolar output operation are shown in Figure 8. The transfer values are shown in Table 3.

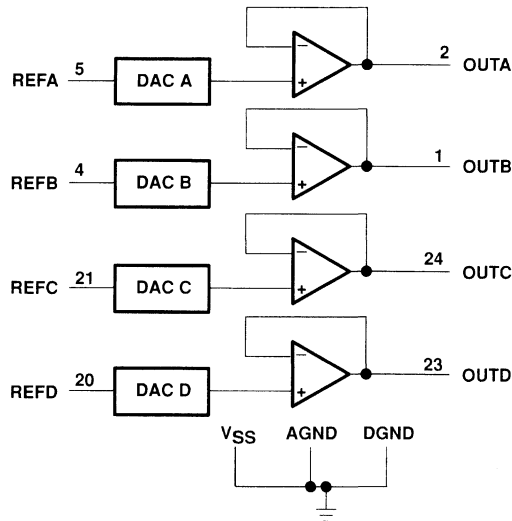


Figure 8. Unipolar Output Circuit

Table 3. Unipolar Code

DAC LATCH CONTENTS		ANALOG OUTPUT
MSB	LSB	
1111	1111	$+ V_{ref} \left(\frac{255}{256} \right)$
1000	0001	$+ V_{ref} \left(\frac{129}{256} \right)$
1000	0000	$+ V_{ref} \left(\frac{128}{256} \right) = + \frac{V_{ref}}{2}$
0111	1111	$+ V_{ref} \left(\frac{127}{256} \right)$
0000	0001	$+ V_{ref} \left(\frac{1}{256} \right)$
0000	0000	0 V

NOTE 3: $1 \text{ LSB} = (V_{ref} 2^{-8}) = V_{ref} \left(\frac{1}{256} \right)$

TLC7225C, TLC7225I

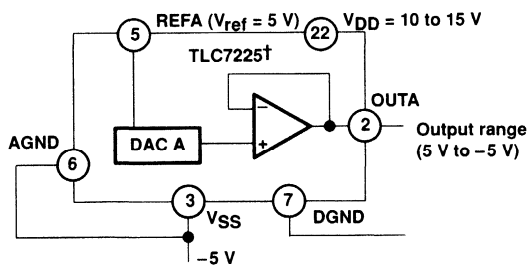
QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS109A – OCTOBER 1996 – REVISED APRIL 1997

APPLICATION INFORMATION

AGND bias for direct bipolar-output operation

The TLC7225 can be used in bipolar operation without adding additional external operational amplifiers by biasing AGND to V_{SS} as shown in Figure 9. This configuration provides an excellent method for providing a direct bipolar output with no additional components. The transfer values are shown in Table 4.



† Digital inputs omitted for clarity.

Figure 9. AGND Bias for Direct Bipolar-Output Operation

Table 4. Bipolar (Offset Binary) Code

DAC LATCH CONTENTS		ANALOG OUTPUT
MSB	LSB	
1111	1111	$+V_{ref} \left(\frac{127}{128} \right)$
1000	0001	$+V_{ref} \left(\frac{1}{128} \right)$
1000	0000	0 V
0111	1111	$-V_{ref} \left(\frac{1}{128} \right)$
0000	0001	$-V_{ref} \left(\frac{127}{128} \right)$
0000	0000	$-V_{ref} \left(\frac{128}{128} \right) = -V_{ref}$

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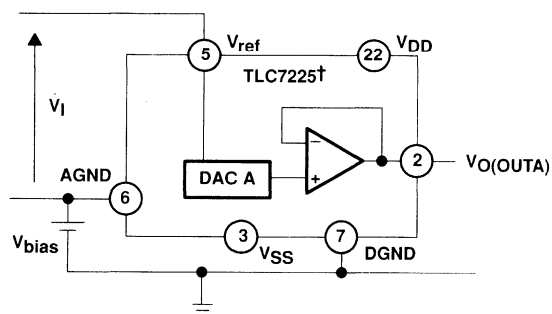
APPLICATION INFORMATION

AGND bias for positive output offset

The TLC7225 AGND terminal can be biased above or below the system ground terminal, DGND, to provide an offset-zero analog-output voltage level. Figure 10 shows a circuit configuration to achieve this for channel A of the TLC7225. The output voltage, V_O at OUTA, can be expressed as:

$$V_O = V_{\text{bias}} + D_A (V_I)$$

where D_A is a fractional representation of the digital input word ($0 \leq D \leq 255/256$).



† Digital inputs omitted for clarity.

Figure 10. AGND Bias Circuit

Increasing AGND above system ground reduces the output range. $V_{DD} - V_{\text{ref}}$ must be at least 4 V to ensure specified operation. Since the AGND terminal is common to all four DACs, this method biases up the output voltages of all the DACs in the TLC7225. Supply voltages V_{DD} and V_{SS} for the TLC7225 should be referenced to DGND.

TLC7225C, TLC7225I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS109A – OCTOBER 1996 – REVISED APRIL 1997

APPLICATION INFORMATION

bipolar-output operation using external amplifier

Each of the DACs of the TLC7225 can also be individually configured to provide bipolar output operation using an external amplifier and two resistors per channel. Figure 11 shows a circuit used to implement offset binary coding (bipolar operation) with DAC A of the TLC7225. In this case (see equation 1):

$$V_O = 1 + \frac{R_2}{R_1} (D_A V_{ref}) - \frac{R_2}{R_1} (V_{ref}) \quad (1)$$

with $R_1 = R_2$

$$V_O = (2D_A - 1) V_{ref}$$

where D_A is a fractional representation of the digital word in latch A.

Mismatch between R_1 and R_2 causes gain and offset errors. Therefore, these resistors must match and track over temperature. The TLC7225 can be operated with a single supply or from positive and negative supplies.

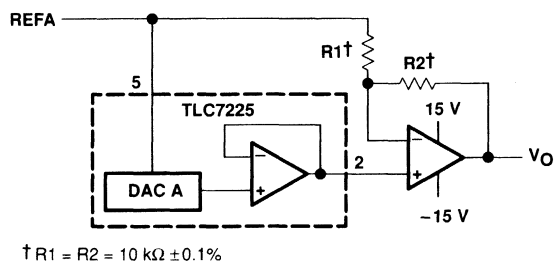


Figure 11. Bipolar-Output Circuit

multiplying DAC using ac input to the REF terminals

The TLC7225 can be used as a multiplying DAC when the reference signal is maintained between 2 V and $V_{DD} - 4$ V. When this configuration is used, V_{DD} should be 14.25 V to 15.75 V. A low output-impedance buffer should be used so that the input signal is not loaded by the resistor ladder. Figure 12 shows the general schematic.

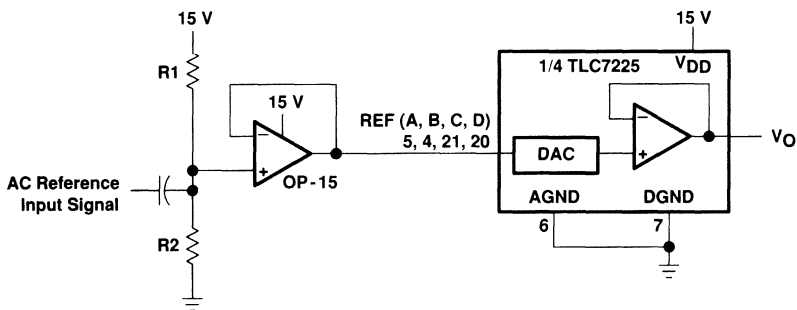


Figure 12. AC Signal-Input Scheme

TLC7225C, TLC7225I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS109A – OCTOBER 1996 – REVISED APRIL 1997

APPLICATION INFORMATION

digital word multiplication

Since each DAC of the TLC7225 has a separate reference input, the output of one DAC can be used as the reference input for another. Therefore, multiplication of digital words can be performed (with the result given in analog form). For example, when the output from DAC A is applied to REF_B then the output from DAC B, V_{OUTB} , can be expressed as given in equation 2:

$$V_{OUTB} = (D_A) (D_B) (V_{REFA}) \quad (2)$$

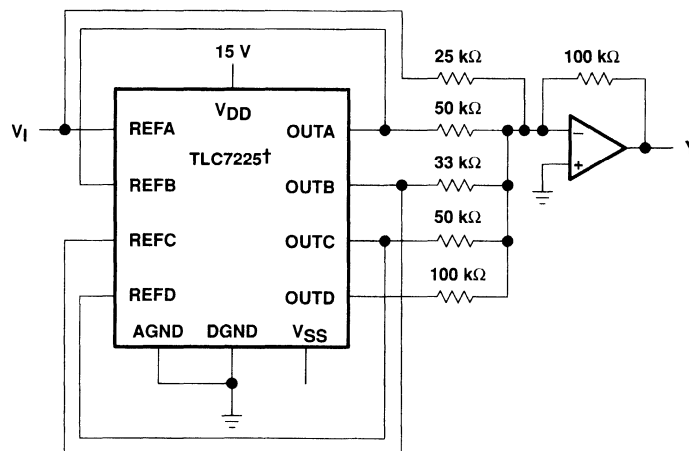
where D_A and D_B are the fractional representations of the digital words in DAC latches A and B respectively.

If $D_A = D_B = D$ then the result is $D^2 (V_{REFA})$

In this manner, the four DACs can be used on their own or in conjunction with an external summing amplifier to generate complex waveforms. Figure 13 shows one such application with the output waveform, Y , which is represented by equation 3:

$$Y = -(x^4 + 2x^3 + 3x^2 + 2x + 4) V_I \quad (3)$$

where x is the digital code that is applied to all four DAC latches.



† Digital inputs omitted for clarity

Figure 13. Complex-Waveform Generation

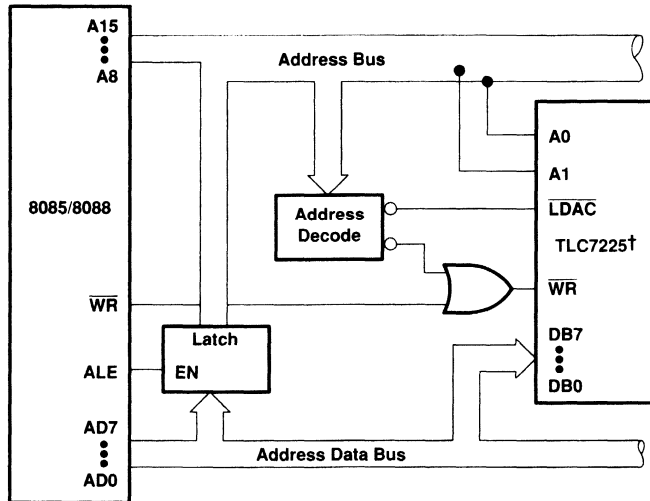
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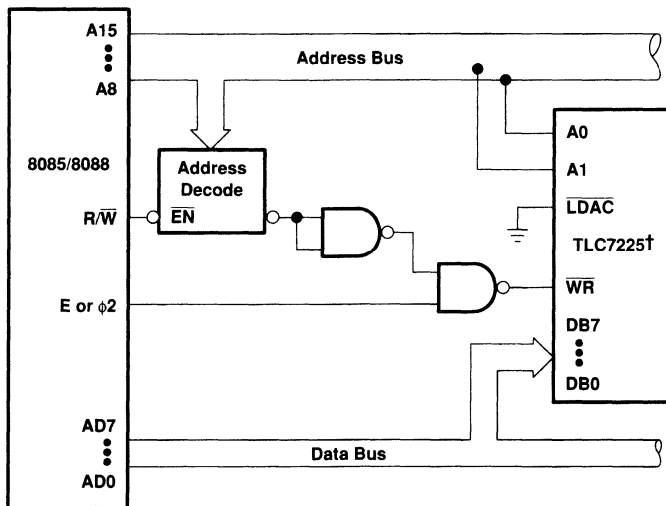
microprocessor interface

Figures 14, 15, 16, and 17 show the hardware interface to some of the standard processors.



† Linear circuitry omitted for clarity

Figure 14. TLC7225 to 8085A/8088 Interface, Double-Buffered Mode



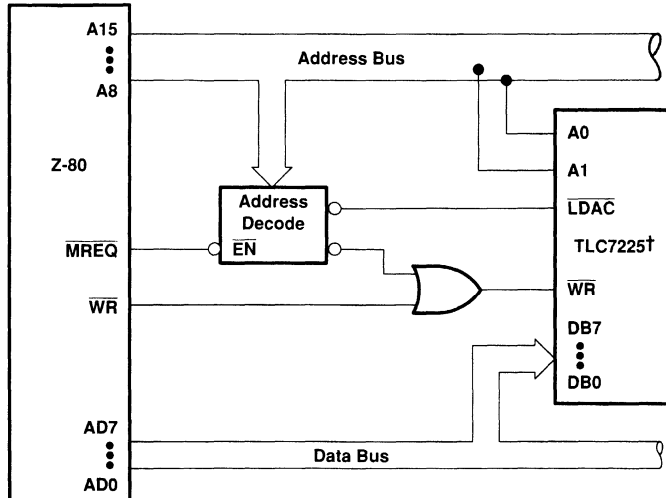
† Linear circuitry omitted for clarity

Figure 15. TLC7225 to 6809/6502 Interface, Single-Buffered Mode

TLC7225C, TLC7225I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

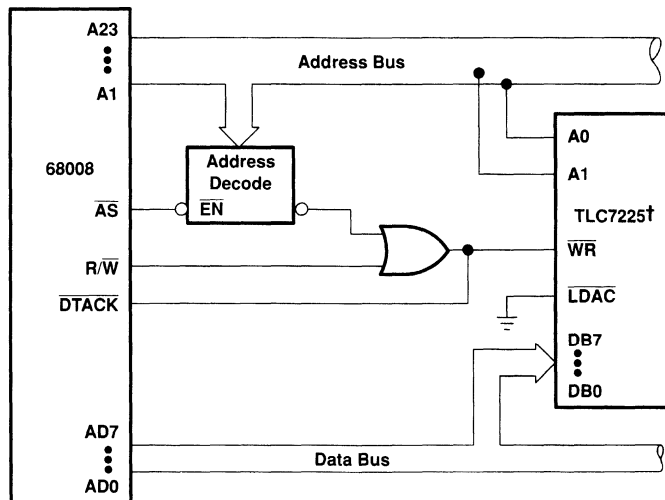
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APPLICATION INFORMATION



† Linear circuitry omitted for clarity

Figure 16. TLC7225 to Z-80 Interface, Double-Buffered Mode



† Linear circuitry omitted for clarity

Figure 17. TLC7225 to 68008 Interface, Single-Buffered Mode

APPLICATION INFORMATION

linearity, offset, and gain error using single-ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, since the most negative supply rail is ground, the output cannot drive below ground.

So with this output offset voltage, the output voltage remains at zero until the input-code value produces a sufficient output voltage to overcome the inherent offset voltage, resulting in a transfer function shown in Figure 18.

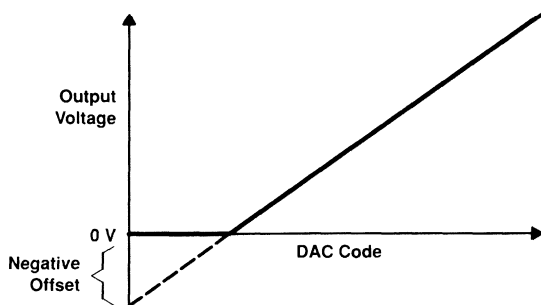


Figure 18. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below ground.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale is adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity in the unipolar mode is measured between full-scale code and the lowest code, which produces a positive output voltage.

The code is calculated from the maximum specification for the zero offset error.

TLC7226C, TLC7226E QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060B – JANUARY 1995 – REVISED AUGUST 1996

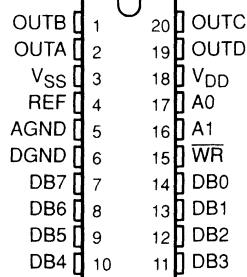
features

- Four 8-Bit D/A Converters
- Microprocessor Compatible
- TTL/CMOS Compatible
- Single Supply Operation Possible
- CMOS Technology

applications

- Process Control
- Automatic Test Equipment
- Automatic Calibration of Large System Parameters, e.g. Gain/Offset

DW OR N PACKAGE
(TOP VIEW)



description

The TLC7226C and TLC7226E consist of four 8-bit voltage-output digital-to-analog converters (DACs) with output buffer amplifiers and interface logic on a single monolithic chip.

Separate on-chip latches are provided for each of the four DACs. Data is transferred into one of these data latches through a common 8-bit TTL/CMOS-compatible 5-V input port. Control inputs A0 and A1 determine which DAC is loaded when \overline{WR} goes low. The control logic is speed compatible with most 8-bit microprocessors.

Each DAC includes an output buffer amplifier capable of sourcing up to 5 mA of output current.

The TLC7226 performance is specified for input reference voltages from 2 V to $V_{DD} - 4$ V with dual supplies. The voltage mode configuration of the DACs allows the TLC7226 to be operated from a single power supply rail at a reference of 10 V.

The TLC7226 is fabricated in a LinBiCMOS™ process that has been specifically developed to allow high-speed digital logic circuits and precision analog circuits to be integrated on the same chip. The TLC7226 has a common 8-bit data bus with individual DAC latches. This provides a versatile control architecture for simple interface to microprocessors. All latch-enable signals are level triggered.

Combining four DACs, four operational amplifiers, and interface logic into either a 0.3-inch wide, 20-terminal dual-in-line IC (DIP) or a small 20-terminal small-outline IC (SOIC) allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. The pinout is aimed at optimizing board layout with all of the analog inputs and outputs at one end of the package and all of the digital inputs at the other.

The TLC7226C is characterized for operation from 0°C to 70°C. The TLC7226E is characterized for operation from -25°C to 85°C.

AVAILABLE OPTIONS

T _A	PACKAGE	
	SMALL OUTLINE (DW)	PLASTIC DIP (N)
0°C to 70°C	TLC7226CDW	TLC7226CN
-25°C to 85°C	TLC7226EDW	TLC7226EN

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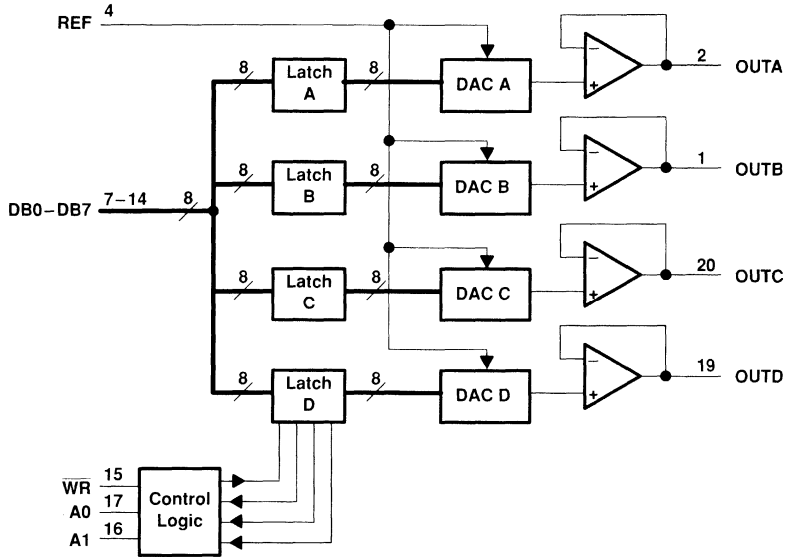
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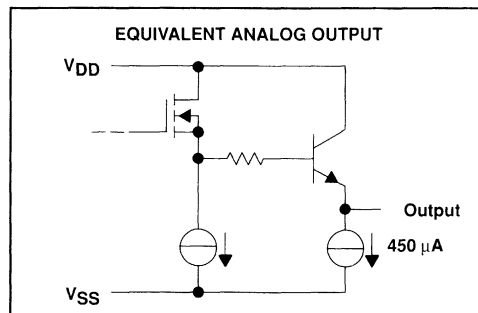
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SLAS060B – JANUARY 1995 – REVISED AUGUST 1996

functional block diagram



schematic of outputs



TLC7226C, TLC7226E QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060B – JANUARY 1995 – REVISED AUGUST 1996

Terminal Functions

TERMINAL NAME	NO.†	I/O	DESCRIPTION
AGND	5		Analog ground. AGND is the reference and return terminal for the analog signals and supply.
A0, A1	16, 17	I	DAC select inputs. The combination of high or low levels select either DACA, DACB, DACC, or DACD.
DGND	6		Digital ground. DGND is the reference and return terminal for the digital signals and supply.
DB0–DB7	7–14	I	Digital DAC data inputs. DB0–DB7 are the input digital data used for conversion.
OUTA	2	O	DACA output. OUTA is the analog output of DACA.
OUTB	1	O	DACB output. OUTB is the analog output of DACB.
OUTC	20	O	DACC output. OUTC is the analog output of DACC.
OUTD	19	O	DACD output. OUTD is the analog output of DACD.
REF	4	I	Voltage reference input. The voltage level on REF determines the full scale analog output.
VDD	18		Positive supply voltage input terminal
VSS	3		Negative supply voltage input terminal
WR	15	I	Write input. WR selects DAC transparency or latch mode. The selected input latch is transparent when WR is low.

† Terminal numbers shown are for the DW and N packages.

TLC7226C, TLC7226E

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060B – JANUARY 1995 – REVISED AUGUST 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} : AGND or DGND	–0.3 V to 17 V
$V_{SS}‡$	–0.3 V to 24 V
Supply voltage range, V_{SS} : AGND or DGND	–7 V to 0.3 V
Voltage range between AGND and DGND	–17 V to 17 V
Input voltage range, V_I (to DGND)	–0.3 V to $V_{DD} + 0.3$ V
Reference voltage range: V_{ref} (to AGND)	–0.3 V to V_{DD}
V_{ref} (to V_{SS})	–0.3 V to 20 V
Output voltage range, V_O (to AGND) (see Note 1)	V_{SS} to V_{DD}
Continuous total power dissipation at (or below) $T_A = 25^\circ\text{C}$ (see Note 2)	500 mW
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
E suffix	-25°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N packages	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ The V_{SS} terminal is connected to the substrate and must be tied to the most negative supply voltage applied to the device.

NOTES: 1. Output voltages may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 60 mA.

2. For operation above $T_A = 75^\circ\text{C}$, derate linearly at the rate of 2 mW/ $^\circ\text{C}$.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		11.4	16.5	V
Supply voltage, V_{SS}		–5.5	0	V
High-level input voltage, V_{IH}		2		V
Low-level input voltage, V_{IL}			0.8	V
Reference voltage, V_{ref}		0	$V_{DD}-4$	V
Load resistance, R_L		2		k Ω
Setup time, address valid before $\overline{WR}\downarrow$, $t_{su}(AW)$ (see Figure 6)	$V_{DD} = 11.4$ V to 16.5 V	0		ns
Setup time, data valid before $\overline{WR}\uparrow$, $t_{su}(DW)$ (see Figure 6)	$V_{DD} = 11.4$ V to 16.5 V	45		ns
Hold time, address valid before $\overline{WR}\uparrow$, $t_h(AW)$ (see Figure 6)	$V_{DD} = 11.4$ V to 16.5 V	0		ns
Hold time, data valid before $\overline{WR}\uparrow$, $t_h(DW)$ (see Figure 6)	$V_{DD} = 11.4$ V to 16.5 V	10		ns
Pulse duration, \overline{WR} low, t_w (see Figure 6)	$V_{DD} = 11.4$ V to 16.5 V	50		ns
Operating free-air temperature, T_A	C suffix	0	70	$^\circ\text{C}$
	E suffix	–25	85	$^\circ\text{C}$



TLC7226C, TLC7226E QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060B – JANUARY 1995 – REVISED AUGUST 1996

electrical characteristics over recommended operating free-air temperature range

dual power supply over recommended power supply and reference voltage ranges, AGND = DGND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input current, digital	$V_I = 0\text{ V or }V_{DD}$			±1	μA
I_{DD}	Supply current	$V_I = 0.8\text{ V or }2.4\text{ V}, V_{DD} = 16.5\text{ V}, V_{SS} = -5\text{ V},$ No load		6	16	mA
I_{SS}	Supply current	$V_I = 0.8\text{ V or }2.4\text{ V},$ No load		4	10	mA
$r_{i(\text{ref})}$	Reference input resistance		2	4		kΩ
Power supply sensitivity		$\Delta V_{DD} = \pm 5\%$			0.01	%/%
C_i	Input capacitance	REF input	All 0s loaded	65		pF
		Digital inputs	All 1s loaded		300	
					8	

operating characteristics over recommended operating free-air temperature range

dual power supply over recommended power supply and reference voltage ranges, AGND = DGND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Slew rate			2.5			V•μs	
Settling time to 1/2 LSB	Positive full scale	$V_{\text{ref}} = 10\text{ V}$			5	μs	
	Negative full scale				7		
Resolution				8		bits	
Total unadjusted error					±2	LSB	
Linearity error	Differential/integral	$V_{DD} = 15\text{ V} \pm 5\%, V_{\text{ref}} = 10\text{ V}$			±1	LSB	
Full-scale error						±2	LSB
Gain error						±0.25	LSB
Temperature coefficient of gain	Full scale	$V_{DD} = 14\text{ V to }16.5\text{ V}, V_{\text{ref}} = 10\text{ V}$			±20	ppm/°C	
	Zero-code error				±50	μV/°C	
Zero-code error					±20 ±80	mV	
Digital crosstalk glitch impulse area		$V_{\text{ref}} = 0$			50	nV•s	

single power supply, $V_{DD} = 14.25\text{ V to }15.75\text{ V}, V_{SS} = \text{AGND} = \text{DGND} = 0\text{ V}, V_{\text{ref}} = 10\text{ V}$ (unless otherwise noted)

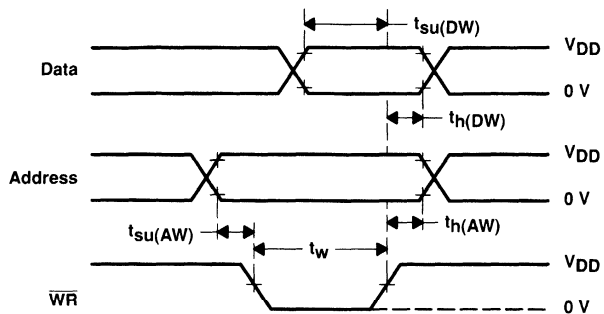
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current, I_{DD}		$V_I = 0.8\text{ V or }2.4\text{ V},$ No load		5	13	mA
Slew rate			2			V•μs
Settling time to 1/2 LSB	Positive full scale				5	μs
	Negative full scale				20	
Resolution				8		bits
Total unadjusted error					±2	LSB
Full-scale error					±2	LSB
Temperature coefficient of gain	Full scale	$V_{DD} = 14\text{ V to }16.5\text{ V}, V_{\text{ref}} = 10\text{ V}$			±20	ppm/°C
	Zero-code error				±50	μV/°C
Linearity error	Differential				±1	LSB
Digital crosstalk-glitch impulse area					50	nV•s



TLC7226C, TLC7226E QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060B – JANUARY 1995 – REVISED AUGUST 1996

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. $t_r = t_f = 20$ ns over V_{DD} range.
B. The timing measurement reference level is equal to $V_{IH} + V_{IL}$ divided by 2.
C. The selected input latch is transparent while \overline{WR} is low. Invalid data during this time can cause erroneous outputs.

Figure 1. Write-Cycle Voltage Waveforms

TLC7226C, TLC7226E QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060B – JANUARY 1995 – REVISED AUGUST 1996

TYPICAL CHARACTERISTICS

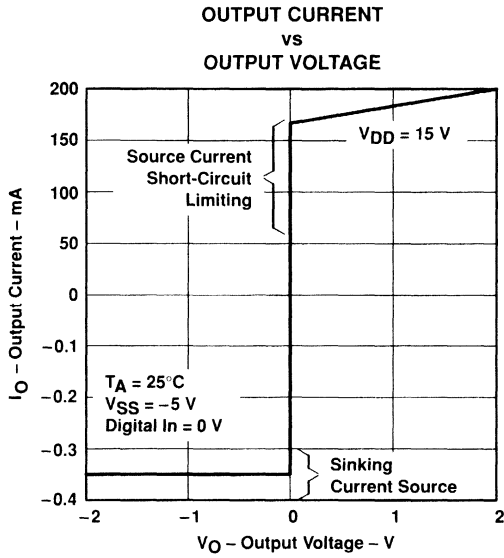


Figure 2

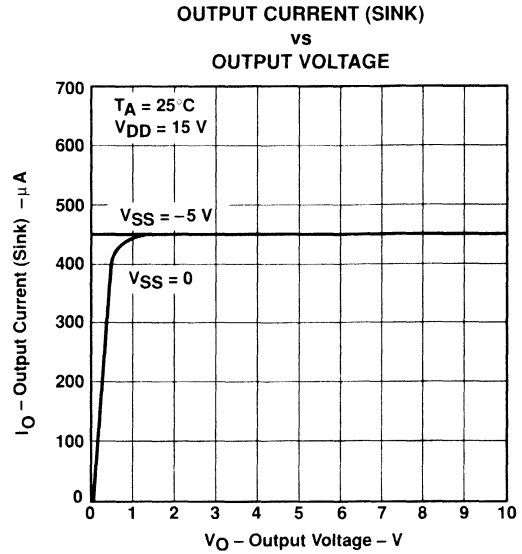


Figure 3

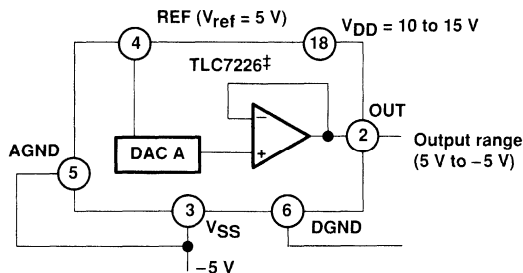
TLC7226C, TLC7226E QUADRUPLER 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060B – JANUARY 1995 – REVISED AUGUST 1996

PRINCIPLES OF OPERATION

AGND bias for direct bipolar output operation

The TLC7226 can be used in bipolar operation without adding more external operational amplifiers as shown in Figure 1 by biasing AGND to V_{SS} . This configuration provides an excellent method for providing a direct bipolar output with no additional components. The transfer values are shown in Table 1.



‡ Digital inputs omitted for clarity.

Figure 4. AGND Bias for Direct Bipolar Operation

Table 1. Bipolar (Offset Binary) Code

DAC LATCH CONTENTS		ANALOG OUTPUT
MSB	LSB	
1111	1111	$+V_{ref} \left(\frac{127}{128} \right)$
1000	0001	$+V_{ref} \left(\frac{1}{128} \right)$
1000	0000	0 V
0111	1111	$-V_{ref} \left(\frac{1}{128} \right)$
0000	0001	$-V_{ref} \left(\frac{127}{128} \right)$
0000	0000	$-V_{ref} \left(\frac{128}{128} \right) = -V_{ref}$

AGND bias for positive output offset

The TLC7226 AGND terminal can be biased above or below the system ground terminal, DGND, to provide an offset analog output voltage level. Figure 2 shows a circuit configuration to achieve this for channel A of the TLC7226. The output voltage, V_O , at OUTA can be expressed as:

$$V_O = V_{BIAS} + D_A (V_I) \quad (1)$$

where D_A is a fractional representation of the digital input word ($0 \leq D \leq 255/256$).

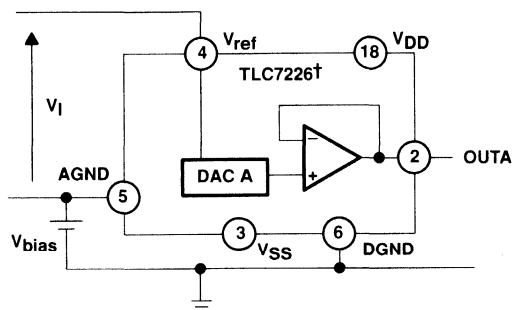
Increasing AGND above system GND reduces the output range. $V_{DD} - V_{ref}$ must be at least 4 V to ensure specified operation. Since the AGND terminal is common to all four DACs, this method biases up the output voltages of all the DACs in the TLC7226. Supply voltages V_{DD} and V_{SS} for the TLC7226 should be referenced to DGND.

TLC7226C, TLC7226E QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060B – JANUARY 1995 – REVISED AUGUST 1996

PRINCIPLES OF OPERATION

AGND bias for positive output offset (continued)



† Digital inputs omitted for clarity.

Figure 5. AGND Bias Circuit

interface logic information

Address lines A0 and A1 select which DAC accepts data from the input port. Table 2 shows the operations of the four DACs. Figure 3 shows the input control logic. When the \overline{WR} signal is low, the input latches of the selected DAC are transparent and the output responds to activity on the data bus. The data is latched into the addressed DAC latch on the rising edge of \overline{WR} . While \overline{WR} is high, the analog outputs remain at the value corresponding to the data held in their respective latches.

Table 2. Function Table

CONTROL INPUTS			OPERATION
\overline{WR}	A1	A2	
H	X	X	No operation Device not selected
L	L	L	DAC A transparent
↑	L	L	DAC A latched
L	L	H	DAC B transparent
↑	L	H	DAC B latched
L	H	L	DAC C transparent
↑	H	L	DAC C latched
L	H	H	DAC D transparent
↑	H	H	DAC D latched

L = low, H = high, X = irrelevant

TLC7226C, TLC7226E QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060B – JANUARY 1995 – REVISED AUGUST 1996

PRINCIPLES OF OPERATION

interface logic information (continued)

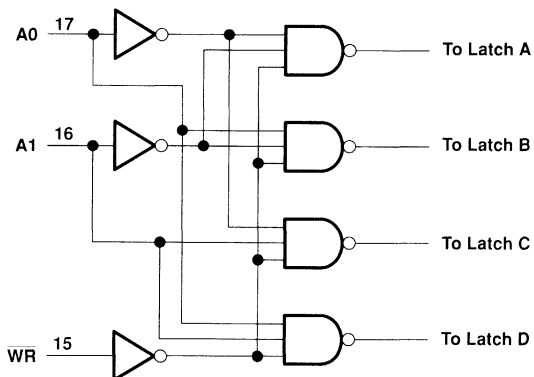


Figure 6. Input Control Logic

unipolar output operation

The unipolar output operation is the basic mode of operation for each channel of the TLC7226, with the output voltages having the same positive polarity as V_{ref} . The TLC7226 can be operated with a single power supply ($V_{SS} = AGND$) or with positive/negative power supplies. The voltage at V_{ref} must never be negative with respect to AGND to prevent parasitic transistor turn-on. Connections for the unipolar output operation are shown in Figure 4. Transfer values are shown in Table 3.

TLC7226C, TLC7226E QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060B – JANUARY 1995 – REVISED AUGUST 1996

PRINCIPLES OF OPERATION

unipolar output operation (continued)

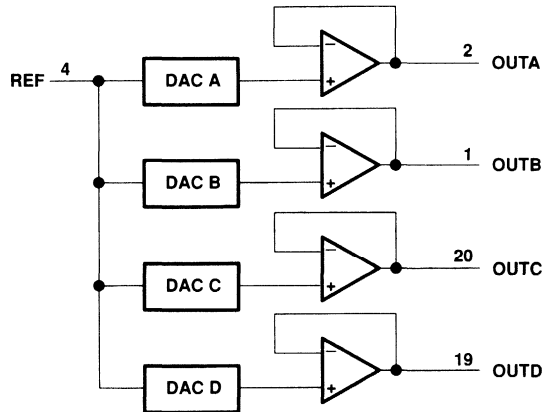


Figure 7. Unipolar Output Circuit

Table 3. Unipolar Code

DAC LATCH CONTENTS		ANALOG OUTPUT
MSB	LSB	
1111	1111	$+ V_{ref} \left(\frac{255}{256} \right)$
1000	0001	$+ V_{ref} \left(\frac{129}{256} \right)$
1000	0000	$+ V_{ref} \left(\frac{128}{256} \right) = + \frac{V_{ref}}{2}$
0111	1111	$+ V_{ref} \left(\frac{127}{256} \right)$
0000	0001	$+ V_{ref} \left(\frac{1}{256} \right)$
0000	0000	0 V

NOTE A. $1 \text{ LSB} = (V_{ref} 2^{-8}) = V_{ref} \left(\frac{1}{256} \right)$

linearity, offset, and gain error using single-ended power supplies

When an amplifier is operated from a single power supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier, with a negative voltage offset, attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot be driven to a negative voltage.

So when the output offset voltage is negative, the output voltage remains at zero volts until the input code value produces a sufficient output voltage to overcome the inherent negative offset voltage, resulting in a transfer function shown in Figure 5.

TLC7226C, TLC7226E QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060B – JANUARY 1995 – REVISED AUGUST 1996

PRINCIPLES OF OPERATION

linearity, offset, and gain error using single-ended power supplies (continued)

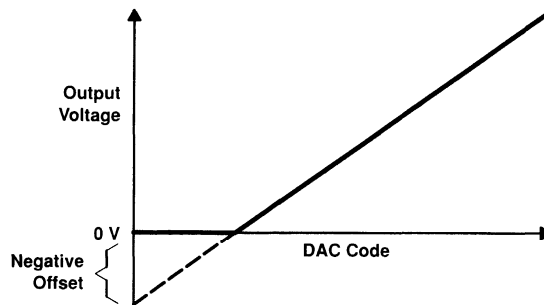


Figure 8. Effect of Negative Offset (Single Power Supply)

This negative offset error, not the linearity error, produces the breakpoint. The transfer function would have followed the dotted line if the output buffer could be driven to a negative voltage.

For a DAC, linearity is measured between zero input code (all inputs 0) and full scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single power supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity in the unipolar mode is measured between full scale code and the lowest code which produces a positive output voltage.

The code is calculated from the maximum specification for the negative offset.

TLC7226C, TLC7226E QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060B – JANUARY 1995 – REVISED AUGUST 1996

APPLICATION INFORMATION

bipolar output operation using external amplifier

Each of the DACs of the TLC7226 can also be individually configured to provide bipolar output operation, using an external amplifier and two resistors per channel. Figure 9 shows a circuit used to implement offset binary coding (bipolar operation) with DAC A of the TLC7226. In this case:

$$V_O = 1 + \frac{R_2}{R_1} \times (D_A \times V_{ref}) - \frac{R_2}{R_1} \times (V_{ref}) \quad (2)$$

with $R_1 = R_2$

$$V_O = (2D_A - 1) \times V_{ref}$$

where D_A is a fractional representation of the digital word in latch A.

Mismatch between R_1 and R_2 causes gain and offset errors. Therefore, these resistors must match and track over temperature. The TLC7226 can be operated with a single power supply or from positive and negative power supplies.

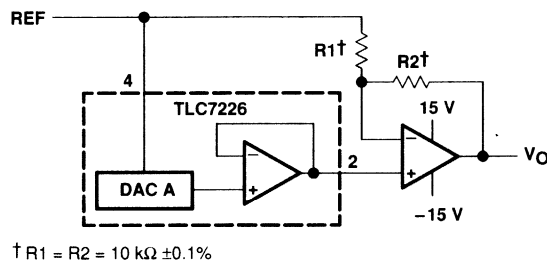


Figure 9. Bipolar Output Circuit

staircase window comparator

In many test systems, it is important to be able to determine whether some parameter lies within defined limits. The staircase window comparator shown in Figure 10 is a circuit that can be used to measure the V_{OH} and V_{OL} thresholds of a TTL device under test. Upper and lower limits on both V_{OH} and V_{OL} can be programmed using the TLC7226. Each adjacent pair of comparators forms a window of programmable size (see Figure 11). When the test voltage (V_{test}) is within a window, then the output for that window is higher. With a reference of 2.56 V applied to the REF input, the minimum window size is 10 mV.

TLC7226C, TLC7226E QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060B – JANUARY 1995 – REVISED AUGUST 1996

APPLICATION INFORMATION

staircase window comparator (continued)

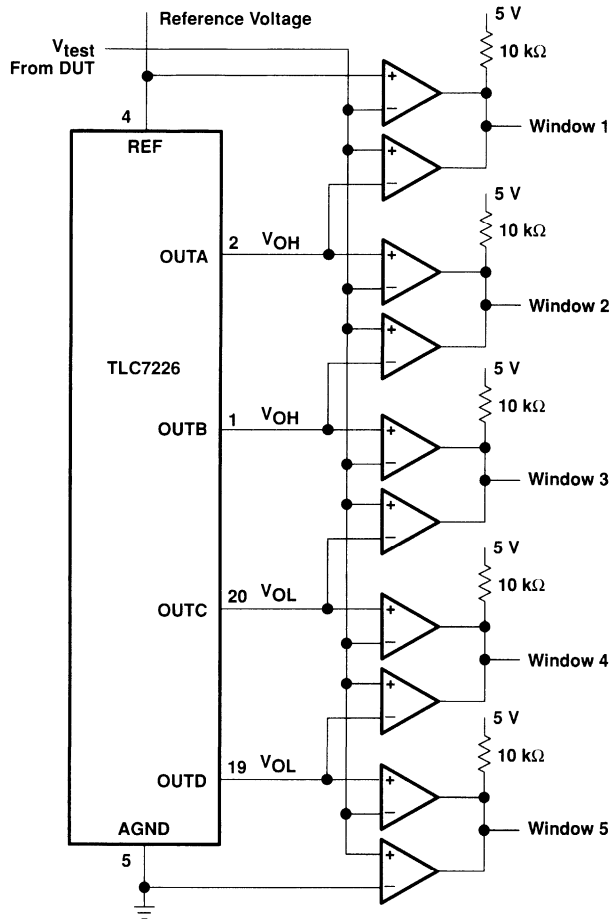


Figure 10. Logic Level Measurement

TLC7226C, TLC7226E QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060B – JANUARY 1995 – REVISED AUGUST 1996

APPLICATION INFORMATION

staircase window comparator (continued)

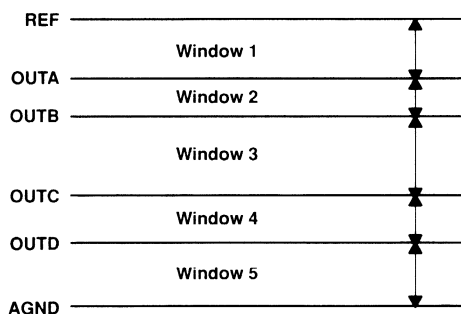


Figure 11. Adjacent Window Structure

The circuit can easily be adapted as shown in Figure 12 to allow for overlapping of windows. When the three outputs from this circuit are decoded, five different nonoverlapping programmable window possibilities can again be defined (see Figure 13).

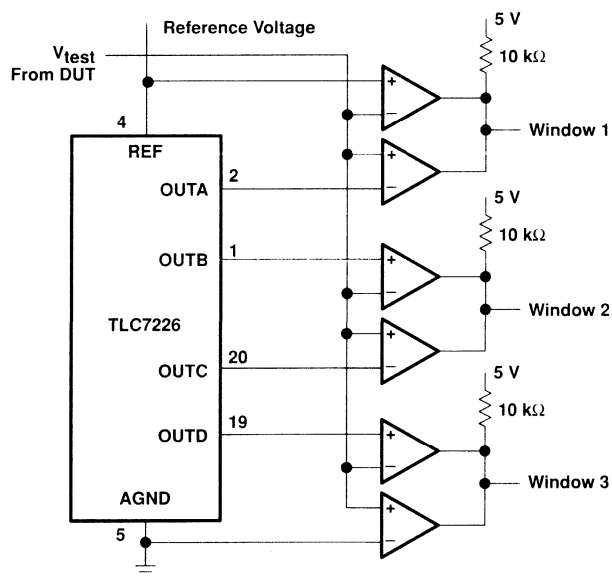


Figure 12. Overlapping Window Circuit

TLC7226C, TLC7226E QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060B – JANUARY 1995 – REVISED AUGUST 1996

APPLICATION INFORMATION

staircase window comparator (continued)

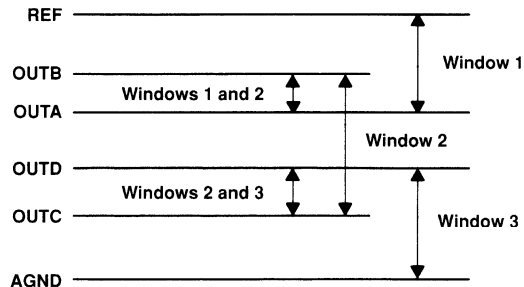


Figure 13. Overlapping Window Structure

output buffer amplifier

The unity-gain output amplifier is capable of sourcing 5 mA into a 2-k Ω load and can drive a 3300-pF capacitor. The output can be shorted to AGND indefinitely or it can be shorted to any voltage between V_{SS} and V_{DD} consistent with the maximum device power dissipation.

multiplying DAC

The TLC7226 can be used as a multiplying DAC when the reference signal is maintained between 2 V and $V_{DD} - 4$ V. When this configuration is used, V_{DD} should be 14.25 V to 15.75 V. A low output-impedance buffer should be used so that the input signal is not loaded by the resistor ladder. Figure 14 shows the general schematic.

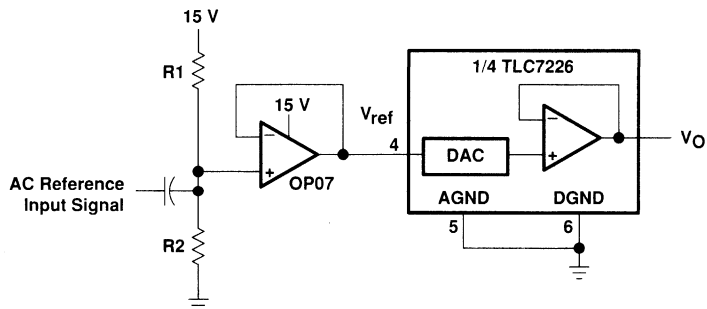


Figure 14. AC Signal Input Scheme

TLC7524C, TLC7524E, TLC7524I 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS061B – SEPTEMBER 1986 – REVISED NOVEMBER 1997

- Easily Interfaced to Microprocessors
- On-Chip Data Latches
- Monotonic Over the Entire A/D Conversion Range
- Segmented High-Order Bits Ensure Low-Glitch Output
- Interchangeable With Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524
- Fast Control Signaling for Digital Signal-Processor Applications Including Interface With TMS320
- CMOS Technology

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	1/2 LSB Max
Power dissipation at $V_{DD} = 5\text{ V}$	5 mW Max
Setting time	100 ns Max
Propagation delay time	80 ns Max

description

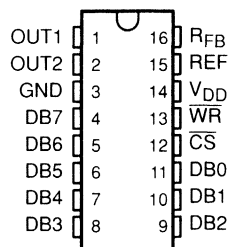
The TLC7524C, TLC7524E, and TLC7524I are CMOS, 8-bit, digital-to-analog converters (DACs) designed for easy interface to most popular microprocessors.

The devices are 8-bit, multiplying DACs with input latches and load cycles similar to the write cycles of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, which produce the highest glitch impulse. The devices provide accuracy to 1/2 LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 mW typically.

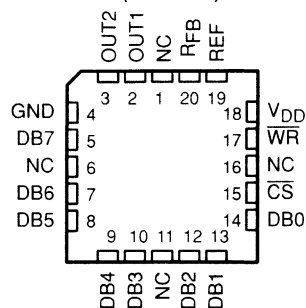
Featuring operation from a 5-V to 15-V single supply, these devices interface easily to most microprocessor buses or output ports. The 2- or 4-quadrant multiplying makes these devices an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The TLC7524C is characterized for operation from 0°C to 70°C. The TLC7524I is characterized for operation from -25°C to 85°C. The TLC7524E is characterized for operation from -40°C to 85°C.

D OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection

AVAILABLE OPTIONS

T _A	PACKAGE		
	SMALL OUTLINE PLASTIC DIP (D)	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC7524CD	TLC7524CFN	TLC7524CN
-25°C to 85°C	TLC7524ID	TLC7524IFN	TLC7524IN
-40°C to 85°C	TLC7524ED	TLC7524EFN	TLC7524EN

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



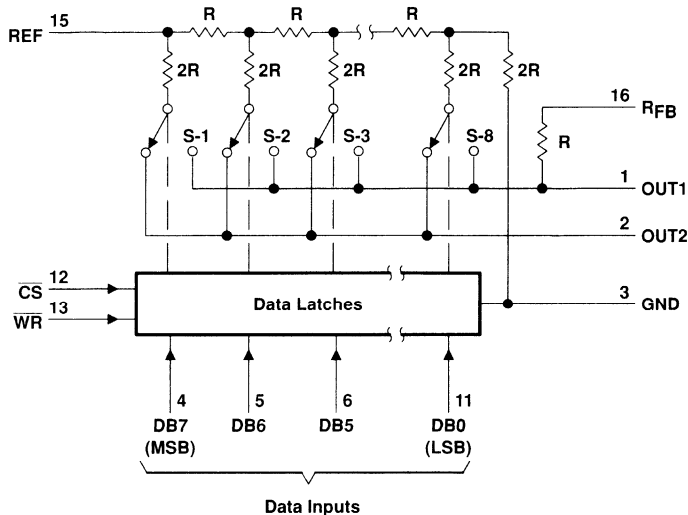
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TLC7524C, TLC7524E, TLC7524I 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS061B – SEPTEMBER 1986 – REVISED NOVEMBER 1997

functional block diagram



Terminal numbers shown are for the D or N package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{DD}	-0.3 V to 16.5 V
Digital input voltage range, V_I	-0.3 V to $V_{DD} + 0.3$ V
Reference voltage, V_{ref}	± 25 V
Peak digital input current, I_I	10 μ A
Operating free-air temperature range, T_A :	TLC7524C	0°C to 70°C
	TLC7524I	-25°C to 85°C
	TLC7524E	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Case temperature for 10 seconds, T_C : FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C

TLC7524C, TLC7524E, TLC7524I

8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS061B – SEPTEMBER 1986 – REVISED NOVEMBER 1997

recommended operating conditions

		V _{DD} = 5 V			V _{DD} = 15 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{DD}		4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V _{ref}		±10			±10			V
High-level input voltage, V _{IH}		2.4			13.5			V
Low-level input voltage, V _{IL}		0.8			1.5			V
CS setup time, t _{su} (CS)		40			40			ns
CS hold time, t _h (CS)		0			0			ns
Data bus input setup time, t _{su} (D)		25			25			ns
Data bus input hold time, t _h (D)		10			10			ns
Pulse duration, WR low, t _w (WR)		40			40			ns
Operating free-air temperature, T _A		TLC7524C		0	70	0	70	°C
		TLC7524I		-25	85	-25	85	
		TLC7524E		-40	85	-40	85	

electrical characteristics over recommended operating free-air temperature range, V_{ref} = ±10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{DD} = 5 V			V _{DD} = 15 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I _{IH}	High-level input current	V _I = V _{DD}	10			10			μA
I _{IL}	Low-level input current	V _I = 0	-10			-10			μA
I _{lkg}	Output leakage current	OUT1	DB0–DB7 at 0 V, WR, CS at 0 V, V _{ref} = ±10 V			±200			nA
		OUT2	DB0–DB7 at V _{DD} , WR, CS at 0 V, V _{ref} = ±10 V			±200			
I _{DD}	Supply current	Quiescent	DB0–DB7 at V _{IH} min or V _{IL} max			2			mA
		Standby	DB0–DB7 at 0 V or V _{DD}			500			μA
kSVS	Supply voltage sensitivity, Δgain/ΔV _{DD}	ΔV _{DD} = ±10%	0.01	0.16	0.005	0.04	%FSR/%		
C _i	Input capacitance, DB0–DB7, WR, CS	V _I = 0	5			5			pF
C _o	Output capacitance	OUT1	DB0–DB7 at 0 V, WR, CS at 0 V			30			pF
		OUT2	DB0–DB7 at 0 V, WR, CS at 0 V			120			
		OUT1	DB0–DB7 at V _{DD} , WR, CS at 0 V			120			
		OUT2	DB0–DB7 at V _{DD} , WR, CS at 0 V			30			
Reference input impedance (REF to GND)			5	20	5	20	kΩ		



TLC7524C, TLC7524E, TLC7524I

8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

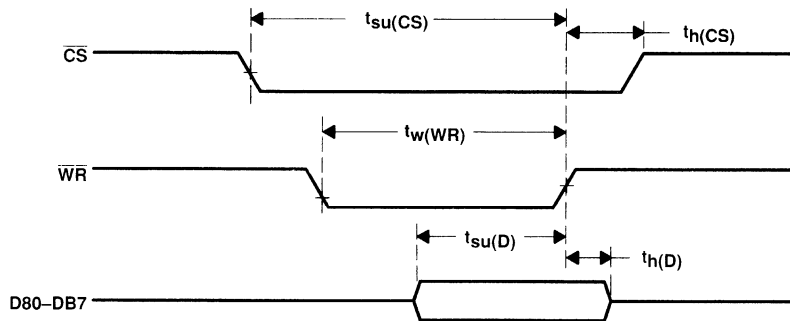
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operating characteristics over recommended operating free-air temperature range, $V_{ref} = \pm 10$ V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{DD} = 5$ V			$V_{DD} = 15$ V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Linearity error				± 0.5			± 0.5	LSB
Gain error	See Note 1			± 2.5			± 2.5	LSB
Settling time (to 1/2 LSB)	See Note 2			100			100	ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80			80	ns
Feedthrough at OUT1 or OUT2	$V_{ref} = \pm 10$ V (100-kHz sinewave) \overline{WR} and \overline{CS} at 0 V, DB0–DB7 at 0 V			0.5			0.5	%FSR
Temperature coefficient of gain	$T_A = 25^\circ\text{C}$ to MAX			± 0.004			± 0.001	%FSR/ $^\circ\text{C}$

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal full scale range (FSR) = $V_{ref} - 1$ LSB.
2. OUT1 load = 100 Ω , $C_{ext} = 13$ pF, \overline{WR} at 0 V, \overline{CS} at 0 V, DB0 – DB7 at 0 V to V_{DD} or V_{DD} to 0 V.

operating sequence



TLC7524C, TLC7524E, TLC7524I 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS061B – SEPTEMBER 1986 – REVISED NOVEMBER 1997

APPLICATION INFORMATION

voltage-mode operation

It is possible to operate the current-multiplying DAC in these devices in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output terminal. The analog output voltage is then available at the reference voltage terminal. Figure 1 is an example of a current-multiplying DAC, which is operated in voltage mode.

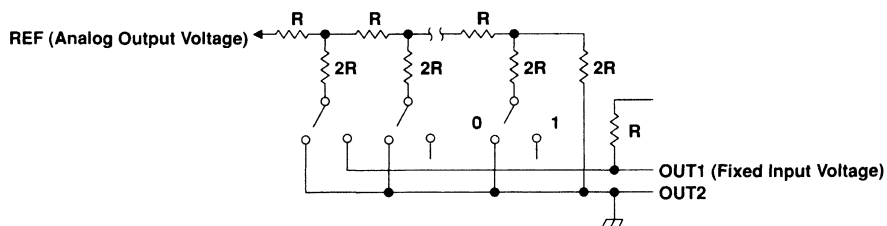


Figure 1. Voltage Mode Operation

The relationship between the fixed-input voltage and the analog-output voltage is given by the following equation:

$$V_O = V_I (D/256)$$

where

V_O = analog output voltage

V_I = fixed input voltage

D = digital input code converted to decimal

In voltage-mode operation, these devices meet the following specification:

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Linearity error at REF	$V_{DD} = 5 \text{ V}$, $OUT1 = 2.5 \text{ V}$, $OUT2$ at GND, $T_A = 25^\circ\text{C}$		1	LSB

TLC7524C, TLC7524E, TLC7524I

8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS061B – SEPTEMBER 1986 – REVISED NOVEMBER 1997

PRINCIPLES OF OPERATION

The TLC7524C, TLC7524E, and TLC7524I are 8-bit multiplying DACs consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary-weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded. These decoded bits, through a modification in the R-2R ladder, control three equally-weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 2. With all digital inputs low, the entire reference current, I_{ref} , is switched to OUT2. The current source $I/256$ represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 2. Analysis of the circuit for all digital inputs high is similar to Figure 2; however, in this case, I_{ref} would be switched to OUT1.

The DAC on these devices interfaces to a microprocessor through the data bus and the \overline{CS} and \overline{WR} control signals. When \overline{CS} and \overline{WR} are both low, analog output on these devices responds to the data activity on the DB0–DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the \overline{CS} signal or \overline{WR} signal goes high, the data on the DB0–DB7 inputs are latched until the \overline{CS} and \overline{WR} signals go low again. When \overline{CS} is high, the data inputs are disabled regardless of the state of the \overline{WR} signal.

These devices are capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 3 and 4. Tables 1 and 2 summarize input coding for unipolar and bipolar operation respectively.

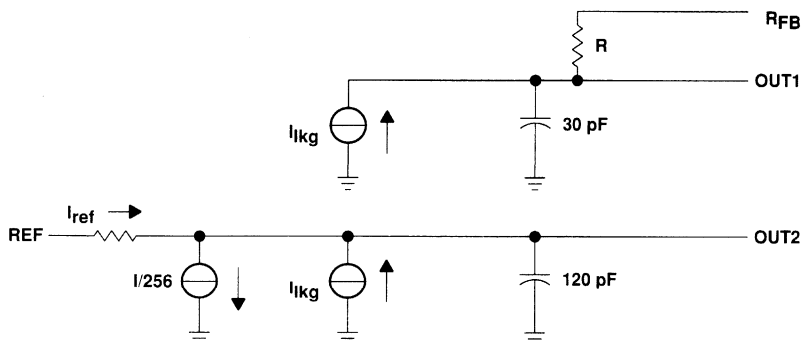


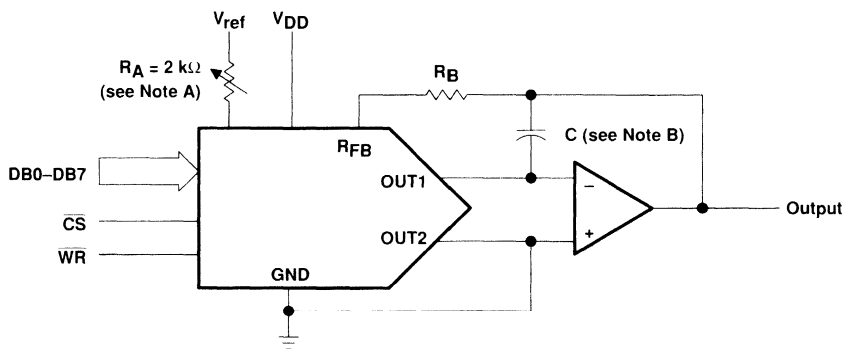
Figure 2. TLC7524 Equivalent Circuit With All Digital Inputs Low

TLC7524C, TLC7524E, TLC7524I

8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

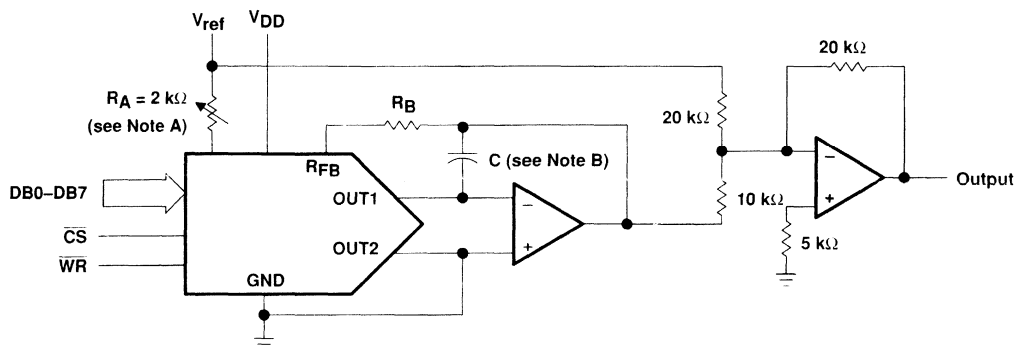
SLAS061B – SEPTEMBER 1986 – REVISED NOVEMBER 1997

PRINCIPLES OF OPERATION



NOTES: D. R_A and R_B used only if gain adjustment is required.
 E. C phase compensation (10-15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

Figure 3. Unipolar Operation (2-Quadrant Multiplication)



NOTES: A. R_A and R_B used only if gain adjustment is required.
 B. C phase compensation (10-15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

Figure 4. Bipolar Operation (4-Quadrant Operation)

Table 1. Unipolar Binary Code

DIGITAL INPUT (see Note 3)		ANALOG OUTPUT
MSB	LSB	
1	1	$-V_{ref} (255/256)$
1	0	$-V_{ref} (129/256)$
1	0	$-V_{ref} (128/256) = -V_{ref}/2$
0	1	$-V_{ref} (127/256)$
0	0	$-V_{ref} (1/256)$
0	0	0

Table 2. Bipolar (Offset Binary) Code

DIGITAL INPUT (see Note 4)		ANALOG OUTPUT
MSB	LSB	
1	1	$V_{ref} (127/128)$
1	0	$V_{ref} (1/128)$
1	0	0
0	1	$-V_{ref} (1/128)$
0	0	$-V_{ref} (127/128)$
0	0	$-V_{ref}$

NOTES: 3. LSB = $1/256 (V_{ref})$
 4. LSB = $1/128 (V_{ref})$

TLC7524C, TLC7524E, TLC7524I 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS061B - SEPTEMBER 1986 - REVISED NOVEMBER 1997

PRINCIPLES OF OPERATION

microprocessor interfaces

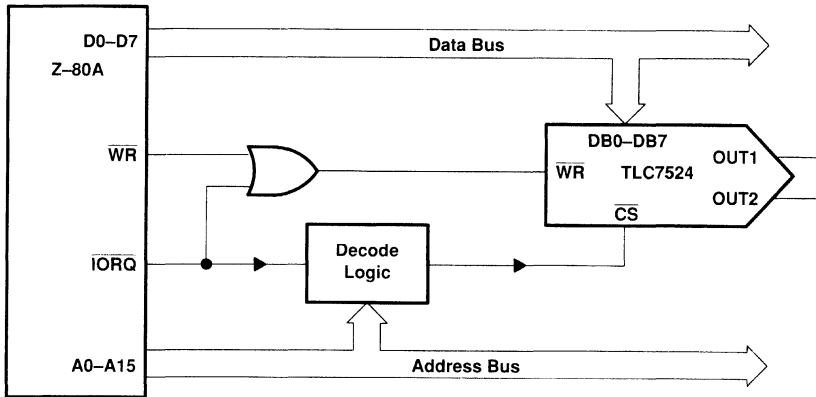


Figure 5. TLC7524 - Z-80A Interface

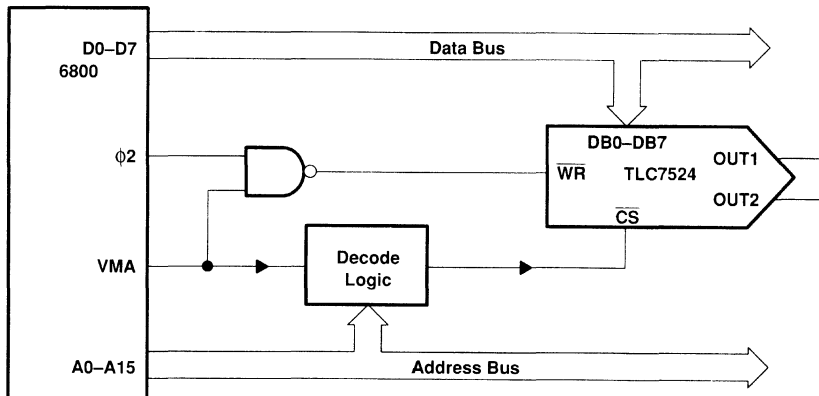


Figure 6. TLC7524 - 6800 Interface

TLC7524C, TLC7524E, TLC7524I 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS061B – SEPTEMBER 1986 – REVISED NOVEMBER 1997

PRINCIPLES OF OPERATION

microprocessor interfaces (continued)

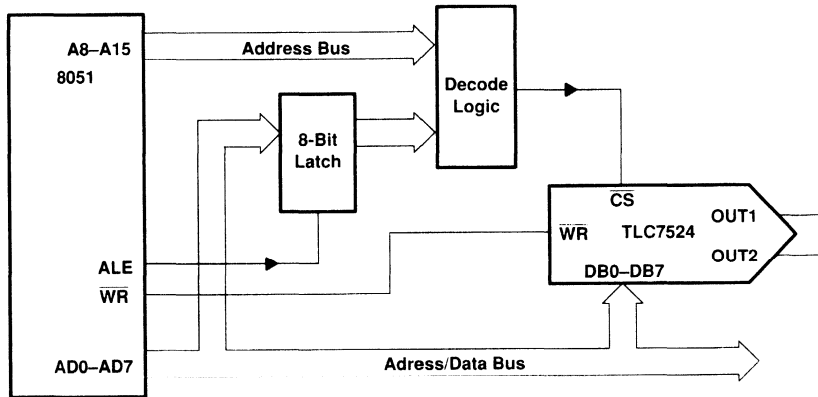


Figure 7. TLC7524 – 8051 Interface

TLC7528C, TLC7528E, TLC7528I DUAL 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS062A – JANUARY 1987 – REVISED MARCH 1995

- Easily Interfaced to Microprocessors
- On-Chip Data Latches
- Monotonic Over the Entire A/D Conversion Range
- Interchangeable With Analog Devices AD7528 and PMI PM-7528
- Fast Control Signaling for Digital Signal Processor (DSP) Applications Including Interface With TMS320
- Voltage-Mode Operation
- CMOS Technology

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation at $V_{DD} = 5\text{ V}$	20 mW
Settling Time at $V_{DD} = 5\text{ V}$	100 ns
Propagation Delay Time at $V_{DD} = 5\text{ V}$	80 ns

description

The TLC7528C, TLC7528E, and TLC7528I are dual, 8-bit, digital-to-analog converters designed with separate on-chip data latches and feature exceptionally close DAC-to-DAC matching. Data is transferred to either of the two DAC data latches through a common, 8-bit, input port. Control input $\overline{\text{DACA/DACB}}$ determines which DAC is to be loaded. The load cycle of these devices is similar to the write cycle of a random-access memory, allowing easy interface to most popular microprocessor buses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

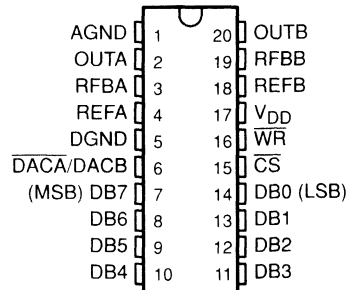
These devices operate from a 5-V to 15-V power supply and dissipates less than 15 mW (typical). The 2- or 4-quadrant multiplying makes these devices a sound choice for many microprocessor-controlled gain-setting and signal-control applications. It can be operated in voltage mode, which produces a voltage output rather than a current output. Refer to the typical application information in this data sheet.

The TLC7528C is characterized for operation from 0°C to 70°C. The TLC7528I is characterized for operation from -25°C to 85°C. The TLC7528E is characterized for operation from -40°C to 85°C.

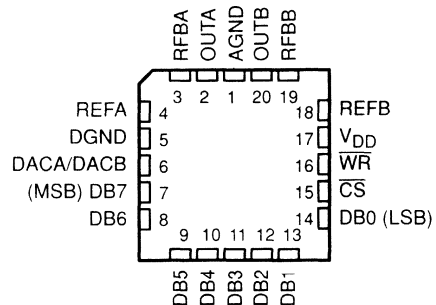
AVAILABLE OPTIONS

T _A	PACKAGE		
	SMALL OUTLINE (DW)	CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC7528CDW	TLC7528CFN	TLC7528CN
-25°C to 85°C	TLC7528IDW	TLC7528IFN	TLC7528IN
-40°C to 85°C	TLC7528EDW	TLC7528EFN	TLC7528EN

DW OR N PACKAGE
(TOP VIEW)



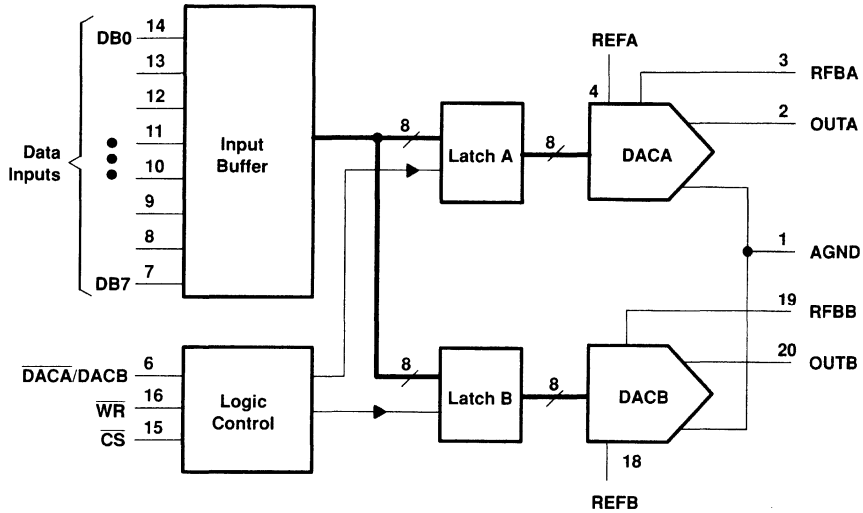
FN PACKAGE
(TOP VIEW)



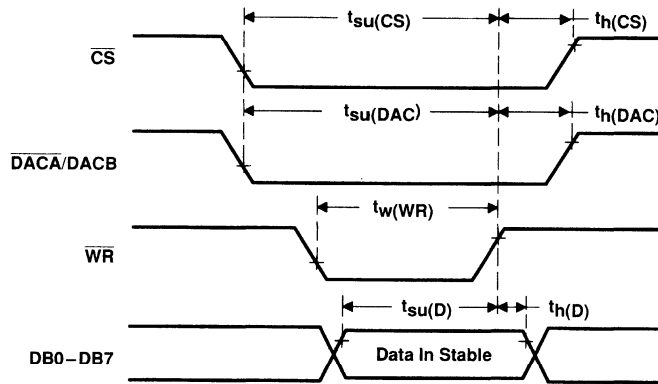
TLC7528C, TLC7528E, TLC7528I
DUAL 8-BIT MULTIPLYING
DIGITAL-TO-ANALOG CONVERTERS

SLAS062A - JANUARY 1987 - REVISED MARCH 1995

functional block diagram



operating sequence



TLC7528C, TLC7528E, TLC7528I
DUAL 8-BIT MULTIPLYING
DIGITAL-TO-ANALOG CONVERTERS
 SLAS062A – JANUARY 1987 – REVISED MARCH 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (to AGND or DGND)	–0.3 V to 16.5 V	
Voltage between AGND and DGND	$\pm V_{DD}$	
Input voltage range, V_I (to DGND)	–0.3 V to $V_{DD} + 0.3$	
Reference voltage, V_{refA} or V_{refB} (to AGND)	± 25 V	
Feedback voltage V_{RFBA} or V_{RFBB} (to AGND)	± 25 V	
Output voltage, V_{OA} or V_{OB} (to AGND)	± 25 V	
Peak input current	10 μ A	
Operating free-air temperature range, T_A :	TLC7528C	0°C to 70°C
	TLC7528I	–25°C to 85°C
	TLC7528E	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C	
Case temperature for 10 seconds, T_C : FN package	260°C	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package	260°C	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	$V_{DD} = 4.75$ V to 5.25 V			$V_{DD} = 14.5$ V to 15.5 V			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX		
Reference voltage, V_{refA} or V_{refB}	± 10			± 10			V	
High-level input voltage, V_{IH}	2.4			13.5			V	
Low-level input voltage, V_{IL}	0.8			1.5			V	
\overline{CS} setup time, $t_{su}(CS)$	50			50			ns	
\overline{CS} hold time, $t_h(CS)$	0			0			ns	
DAC select setup time, $t_{su}(DAC)$	50			50			ns	
DAC select hold time, $t_h(DAC)$	10			10			ns	
Data bus input setup time $t_{su}(D)$	25			25			ns	
Data bus input hold time $t_h(D)$	10			10			ns	
Pulse duration, \overline{WR} low, $t_w(WR)$	50			50			ns	
Operating free-air temperature, T_A	TLC7628C	0		70	0		70	°C
	TLC7628I	–25		85	–25		85	
	TLC7628E	–40		85	–40		85	



TLC7528C, TLC7528E, TLC7528I
DUAL 8-BIT MULTIPLYING
DIGITAL-TO-ANALOG CONVERTERS

SLAS062A – JANUARY 1987 – REVISED MARCH 1995

electrical characteristics over recommended operating free-air temperature range,
 $V_{refA} = V_{refB} = 10\text{ V}$, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$V_{DD} = 5\text{ V}$			$V_{DD} = 15\text{ V}$			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{IH}	High-level input current	$V_I = V_{DD}$			10			10	μA
I_{IL}	Low-level input current	$V_I = 0$	5	12	-10	5	12	-10	μA
	Reference input impedance REFA or REFB to AGND				20			20	$\text{k}\Omega$
I_{lkg}	Output leakage current	OUTA			± 400			± 200	nA
		OUTB			± 400			± 200	
	Input resistance match (REFA to REFB)				$\pm 1\%$			$\pm 1\%$	
	DC supply sensitivity, $\Delta\text{gain}/\Delta V_{DD}$	$\Delta V_{DD} = \pm 10\%$			0.04			0.02	%/%
I_{DD}	Supply current (quiescent)	All digital inputs at V_{IHmin} or V_{ILmax}			2			2	mA
I_{DD}	Supply current (standby)	All digital inputs at 0 V or V_{DD}			0.5			0.5	mA
C_i	Input capacitance	DB0–DB7			10			10	pF
		WR, CS, DACA/DACB			15			15	pF
C_o	Output capacitance (OUTA, OUTB)	DAC data latches loaded with 00000000			50			50	pF
		DAC data latches loaded with 11111111			120			120	

† All typical values are at $T_A = 25^\circ\text{C}$.



TLC7528C, TLC7528E, TLC7528I
DUAL 8-BIT MULTIPLYING
DIGITAL-TO-ANALOG CONVERTERS
 SLAS062A – JANUARY 1987 – REVISED MARCH 1995

**operating characteristics over recommended operating free-air temperature range,
 $V_{refA} = V_{refB} = 10\text{ V}$, V_{OA} and V_{OB} at 0 V (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	$V_{DD} = 5\text{ V}$			$V_{DD} = 15\text{ V}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Linearity error			±1/2			±1/2			LSB
Settling time (to 1/2 LSB)		See Note 1	100			100			ns
Gain error		See Note 2	2.5			2.5			LSB
AC feedthrough	REFA to OUTA	See Note 3	-65			-65			dB
	REFB to OUTB		-65			-65			
Temperature coefficient of gain		See Note 4	0.007			0.0035			%FSR/°C
Propagation delay (from digital input to 90% of final analog output current)		See Note 5	80			80			ns
Channel-to-channel isolation	REFA to OUTB	See Note 6	77			77			dB
	REFB to OUTA	See Note 7	77			77			
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, $T_A = 25^\circ\text{C}$	160			440			nV•s
Digital crosstalk		Measured for code transition from 00000000 to 11111111, $T_A = 25^\circ\text{C}$	30			60			nV•s
Harmonic distortion		$V_i = 6\text{ V}$, $f = 1\text{ kHz}$, $T_A = 25^\circ\text{C}$	-85			-85			dB

- NOTES: 1. OUTA, OUTB load = 100 Ω , $C_{ext} = 13\text{ pF}$; \overline{WR} and \overline{CS} at 0 V; DB0–DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
 2. Gain error is measured using an internal feedback resistor. Nominal full scale range (FSR) = $V_{ref} - 1\text{ LSB}$.
 3. $V_{ref} = 20\text{ V}$ peak-to-peak, 100-kHz sine wave; DAC data latches loaded with 00000000.
 4. Temperature coefficient of gain measured from 0°C to 25°C or from 25°C to 70°C.
 5. $V_{refA} = V_{refB} = 10\text{ V}$; OUTA/OUTB load = 100 Ω , $C_{ext} = 13\text{ pF}$; \overline{WR} and \overline{CS} at 0 V; DB0–DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
 6. Both DAC latches loaded with 11111111; $V_{refA} = 20\text{ V}$ peak to peak, 100-kHz sine wave; $V_{refB} = 0$; $T_A = 25^\circ\text{C}$.
 7. Both DAC latches loaded with 11111111; $V_{refB} = 20\text{ V}$ peak-to-peak, 100-kHz sine wave; $V_{refA} = 0$; $T_A = 25^\circ\text{C}$.

PRINCIPLES OF OPERATION

These devices contain two identical, 8-bit-multiplying D/A converters, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA with all digital inputs low is shown in Figure 1.

Figure 2 shows the DACA equivalent circuit. A similar equivalent circuit can be drawn for DACB. Both DACs share the analog ground terminal 1 (AGND). With all digital inputs high, the entire reference current flows to OUTA. A small leakage current (I_{lkG}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. C_O is due to the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_O is 50 pF to 120 pF maximum. The equivalent output resistance (r_O) varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

These devices interface to a microprocessor through the data bus, \overline{CS} , \overline{WR} , and $\overline{DACA}/\overline{DACB}$ control signals. When \overline{CS} and \overline{WR} are both low, the TLC7528 analog output, specified by the $\overline{DACA}/\overline{DACB}$ control line, responds to the activity on the DB0–DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the \overline{CS} signal or \overline{WR} signal goes high, the data on the DB0–DB7 inputs is latched until the \overline{CS} and \overline{WR} signals go low again. When \overline{CS} is high, the data inputs are disabled regardless of the state of the \overline{WR} signal.



TLC7528C, TLC7528E, TLC7528I DUAL 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS062A – JANUARY 1987 – REVISED MARCH 1995

PRINCIPLES OF OPERATION

The digital inputs of these devices provide TTL compatibility when operated from a supply voltage of 5 V. These devices can operate with any supply voltage in the range from 5 V to 15 V; however, input logic levels are not TTL compatible above 5 V.

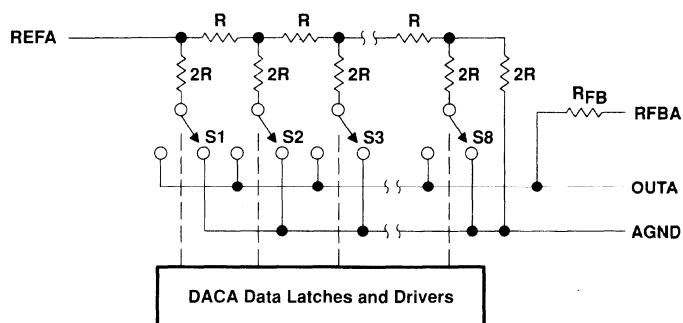


Figure 1. Simplified Functional Circuit for DACA

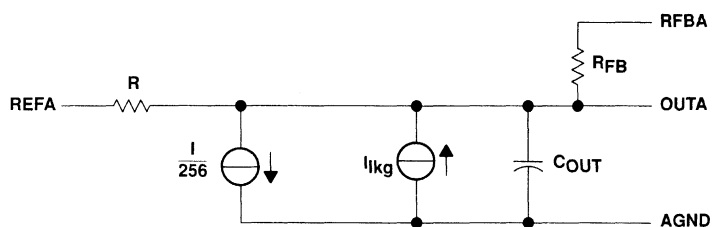


Figure 2. TLC7528 Equivalent Circuit, DACA Latch Loaded With 11111111

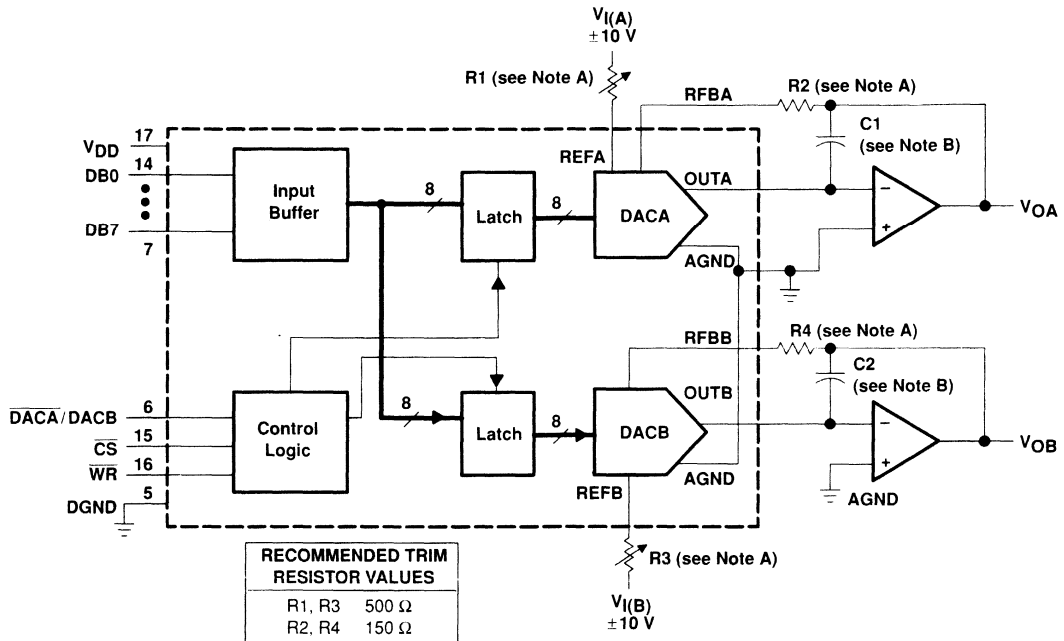
MODE SELECTION TABLE

DACA/DACB	CS	WR	DACA	DACB
L	L	L	Write	Hold
H	L	L	Hold	Write
X	H	X	Hold	Hold
X	X	H	Hold	Hold

L = low level, H = high level, X = don't care

APPLICATION INFORMATION

These devices are capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 3 and 4. Tables 1 and 2 summarize input coding for unipolar and bipolar operation.



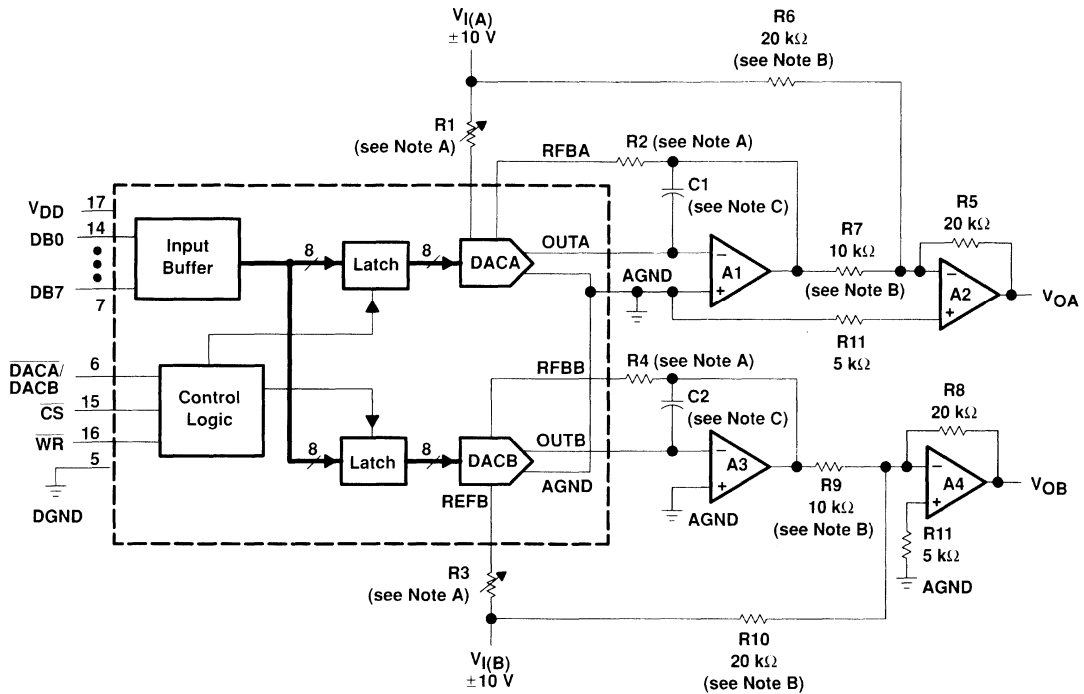
- NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
 B. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

Figure 3. Unipolar Operation (2-Quadrant Multiplication)

TLC7528C, TLC7528E, TLC7528I DUAL 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS062A – JANUARY 1987 – REVISED MARCH 1995

APPLICATION INFORMATION



- NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table in Figure 3 for recommended values. Adjust R1 for $V_{OA} = 0\text{ V}$ with code 10000000 in DACA latch. Adjust R3 for $V_{OB} = 0\text{ V}$ with 10000000 in DACB latch.
 B. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
 C. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

Figure 4. Bipolar Operation (4-Quadrant Operation)

Table 1. Unipolar Binary Code

DAC LATCH CONTENTS		ANALOG OUTPUT
MSB	LSB†	
1	1	$-V_I (255/256)$
1	0	$-V_I (129/256)$
1	0	$-V_I (128/256) = -V_I/2$
0	1	$-V_I (127/256)$
0	0	$-V_I (1/256)$
0	0	$-V_I (0/256) = 0$

† 1 LSB = $(2^{-8})V_I$

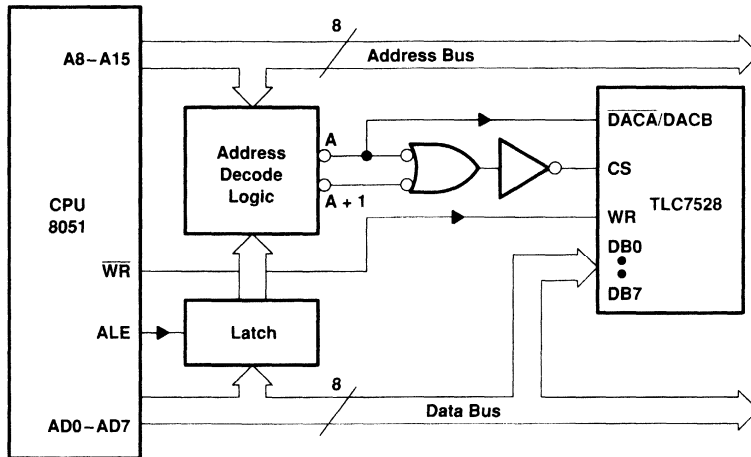
Table 2. Bipolar (Offset Binary) Code

DAC LATCH CONTENTS		ANALOG OUTPUT
MSB	LSB‡	
1	1	$V_I (127/128)$
1	0	$V_I (1/128)$
1	0	0 V
0	1	$-V_I (1/128)$
0	0	$-V_I (127/128)$
0	0	$-V_I (128/128)$

‡ 1 LSB = $(2^{-7})V_I$

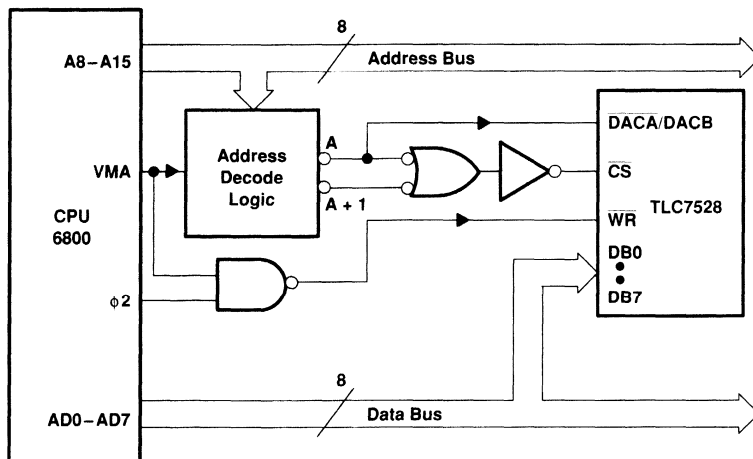
APPLICATION INFORMATION

microprocessor interface information



NOTE A: A = decoded address for TLC7528 DACA
 A + 1 = decoded address for TLC7528 DACB

Figure 5. TLC7528 - Intel 8051 Interface



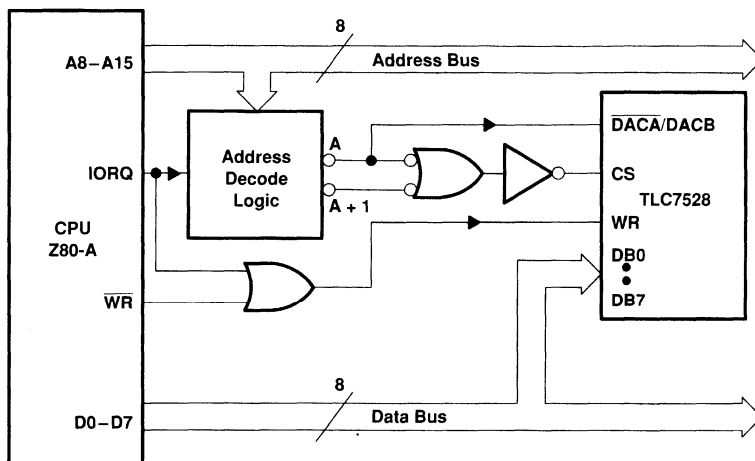
NOTE A: A = decoded address for TLC7528 DACA
 A + 1 = decoded address for TLC7528 DACB

Figure 6. TLC7528 - 6800 Interface

TLC7528C, TLC7528E, TLC7528I
DUAL 8-BIT MULTIPLYING
DIGITAL-TO-ANALOG CONVERTERS

SLAS062A - JANUARY 1987 - REVISED MARCH 1995

APPLICATION INFORMATION



NOTE A: A = decoded address for TLC7528 DACA
 A + 1 = decoded address for TLC7528 DACB

Figure 7. TLC7528 To Z-80A Interface

programmable window detector

The programmable window comparator shown in Figure 8 determines if voltage applied to the DAC feedback resistors are within the limits programmed into the data latches of these devices. Input signal range depends on the reference and polarity, that is, the test input range is 0 to $-V_{ref}$. The DACA and DACB data latches are programmed with the upper and lower test limits. A signal within the programmed limits drives the output high.

APPLICATION INFORMATION

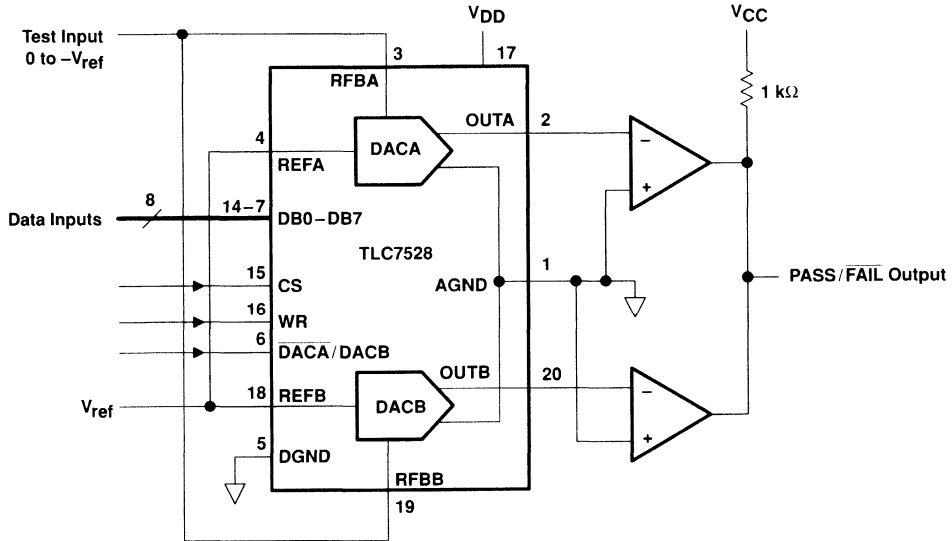


Figure 8. Digitally-Programmable Window Comparator (Upper- and Lower-Limit Tester)

digitally controlled signal attenuator

Figure 9 shows a TLC7528 configured as a two-channel programmable attenuator. Applications include stereo audio and telephone signal level control. Table 3 shows input codes vs attenuation for a 0 to 15.5 dB range.

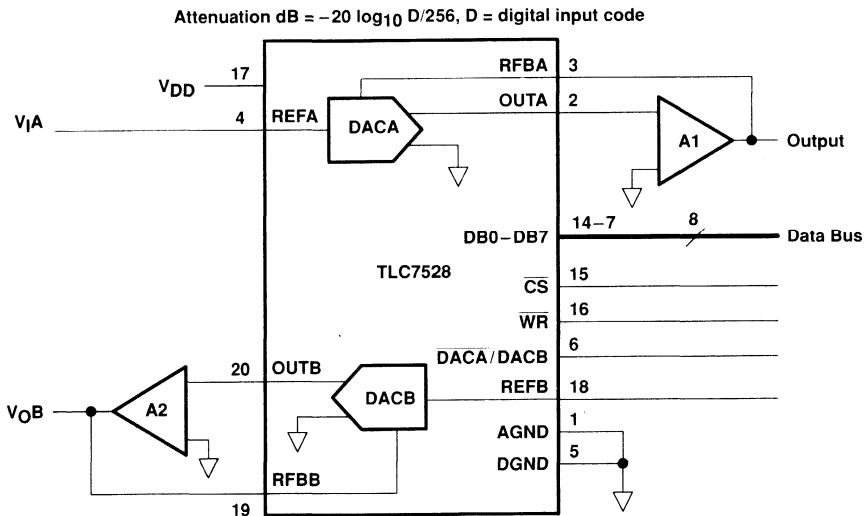


Figure 9. Digitally Controlled Dual Telephone Attenuator

TLC7528C, TLC7528E, TLC7528I
DUAL 8-BIT MULTIPLYING
DIGITAL-TO-ANALOG CONVERTERS

SLAS062A – JANUARY 1987 – REVISED MARCH 1995

APPLICATION INFORMATION

Table 3. Attenuation vs DACA, DACB Code

ATTN (dB)	DAC INPUT CODE	CODE IN DECIMAL	ATTN (dB)	DAC INPUT CODE	CODE IN DECIMAL
0	1 1 1 1 1 1 1 1	255	8.0	0 1 1 0 0 1 1 0	102
0.5	1 1 1 1 0 0 1 0	242	8.5	0 1 1 0 0 0 0 0	96
1.0	1 1 1 0 0 1 0 0	228	9.0	0 1 0 1 1 0 1 1	91
1.5	1 1 0 1 0 1 1 1	215	9.5	0 1 0 1 0 1 1 0	86
2.0	1 1 0 0 1 0 1 1	203	10.0	0 1 0 1 0 0 0 1	81
2.5	1 1 0 0 0 0 0 0	192	10.5	0 1 0 0 1 1 0 0	76
3.0	1 0 1 1 0 1 0 1	181	11.0	0 1 0 0 1 0 0 0	72
3.5	1 0 1 0 1 0 1 1	171	11.5	0 1 0 0 0 1 0 0	68
4.0	1 0 1 0 0 0 1 0	162	12.0	0 1 0 0 0 0 0 0	64
4.5	1 0 0 1 1 0 0 0	152	12.5	0 0 1 1 1 1 0 1	61
5.0	1 0 0 1 1 1 1 1	144	13.0	0 0 1 1 1 0 0 1	57
5.5	1 0 0 0 1 0 0 0	136	13.5	0 0 1 1 0 1 1 0	54
6.0	1 0 0 0 0 0 0 0	128	14.0	0 0 1 1 0 0 1 1	51
6.5	0 1 1 1 1 0 0 1	121	14.5	0 0 1 1 0 0 0 0	48
7.0	0 1 1 1 0 0 1 0	114	15.0	0 0 1 0 1 1 1 0	46
7.5	0 1 1 0 1 1 0 0	108	15.5	0 0 1 0 1 0 1 1	43

programmable state-variable filter

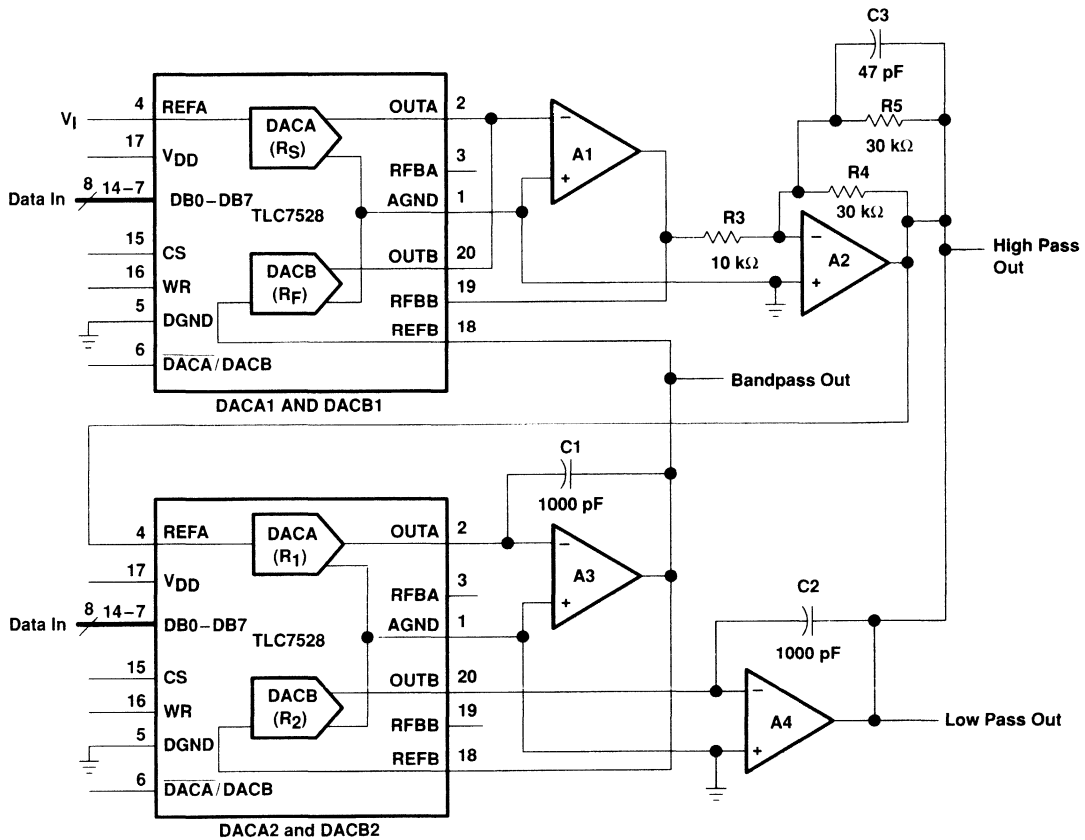
This programmable state-variable or universal filter configuration provides low-pass, high-pass, and bandpass outputs, and is suitable for applications requiring microprocessor control of filter parameters.

As shown in Figure 10, DACA1 and DACB1 control the gain and Q of the filter while DACA2 and DACB2 control the cutoff frequency. Both halves of the DACA2 and DACB2 must track accurately in order for the cutoff-frequency equation to be true. With the TLC7528, this is easy to achieve.

$$f_c = \frac{1}{2\pi R1C1}$$

The programmable range for the cutoff or center frequency is 0 to 15 kHz with a Q ranging from 0.3 to 4.5. This defines the limits of the component values.

APPLICATION INFORMATION



Circuit Equations:

$$C_1 = C_2, R_1 = R_2, R_4 = R_5$$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{fb}(DACB1)}$$

where:

R_{fb} is the internal resistor connected between OUTB and RFBB

$$G = -\frac{R_F}{R_S}$$

- NOTES: A. Op-amps A1, A2, A3, and A4 are TL287.
 B. CS compensates for the op-amp gain-bandwidth limitations.
 C. DAC equivalent resistance equals $\frac{256 \times (\text{DAC ladder resistance})}{\text{DAC digital code}}$

Figure 10. Digitally Controlled State-Variable Filter

TLC7528C, TLC7528E, TLC7528I
DUAL 8-BIT MULTIPLYING
DIGITAL-TO-ANALOG CONVERTERS

SLAS062A – JANUARY 1987 – REVISED MARCH 1995

APPLICATION INFORMATION

voltage-mode operation

It is possible to operate the current multiplying D/A converter of these devices in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output terminal. The analog output voltage is then available at the reference voltage terminal. Figure 11 is an example of a current multiplying D/A, that operates in the voltage mode.

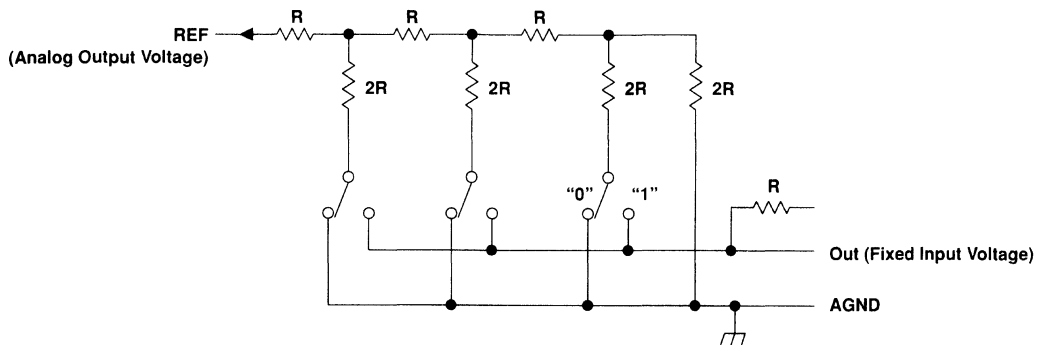


Figure 11. Voltage-Mode Operation

The following equation shows the relationship between the fixed input voltage and the analog output voltage:

$$V_O = V_I (D/256)$$

where

V_O = analog output voltage

V_I = fixed input voltage

D = digital input code converted to decimal

In voltage-mode operation, these devices meet the following specification:

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Linearity error at REFA or REFB	$V_{DD} = 5 \text{ V}$, O_{UTA} or O_{UTB} at 2.5 V, $T_A = 25^\circ\text{C}$		1	LSB

TLC7628C, TLC7628E, TLC7628I DUAL 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS063A – APRIL 1989 – REVISED MAY 1995

- Easy Microprocessor Interface
- On-Chip Data Latches
- Digital Inputs Are TTL-Compatible With 10.8-V to 15.75-V Power Supply
- Monotonic Over the Entire A/D Conversion Range
- Fast Control Signaling for Digital Signal Processor (DSP) Applications Including Interface With TMS320
- CMOS Technology

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation	20 mW
Settling Time	100 ns
Propagation Delay Time	80 ns

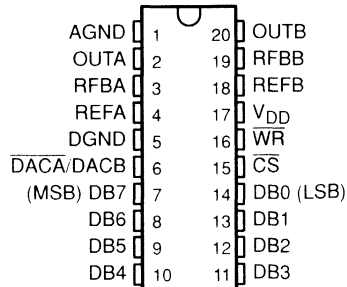
description

The TLC7628C, TLC7628E, and TLC7628I are dual, 8-bit, digital-to-analog converters (DACs) designed with separate on-chip data latches and feature exceptionally close DAC-to-DAC matching. Data is transferred to either of the two DAC data latches through a common, 8-bit input port. Control input $\overline{\text{DACA/DACB}}$ determines which DAC is loaded. The load cycle of these devices is similar to the write cycle of a random-access memory, allowing easy interface to most popular microprocessor buses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

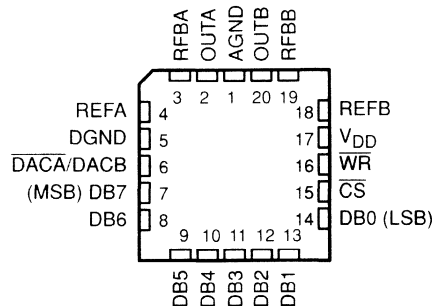
The TLC7628C operates from a 10.8-V to 15.75-V power supply and is TTL-compatible over this range. 2- or 4-quadrant multiplying makes these devices a sound choice for many microprocessor-controlled gain-setting and signal-control applications.

The TLC7628C is characterized for operation from 0°C to 70°C. The TLC7628I is characterized for operation from -25°C to 85°C. The TLC7628E is characterized for operation from -40°C to 85°C.

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T _A	PACKAGE		
	SMALL OUTLINE PLASTIC DIP (DW)	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC7628CDW	TLC7628CFN	TLC7628CN
-25°C to 85°C	TLC7628IDW	TLC7628IFN	TLC7628IN
-40°C to 85°C	TLC7628EDW	TLC7628EFN	TLC7628EN

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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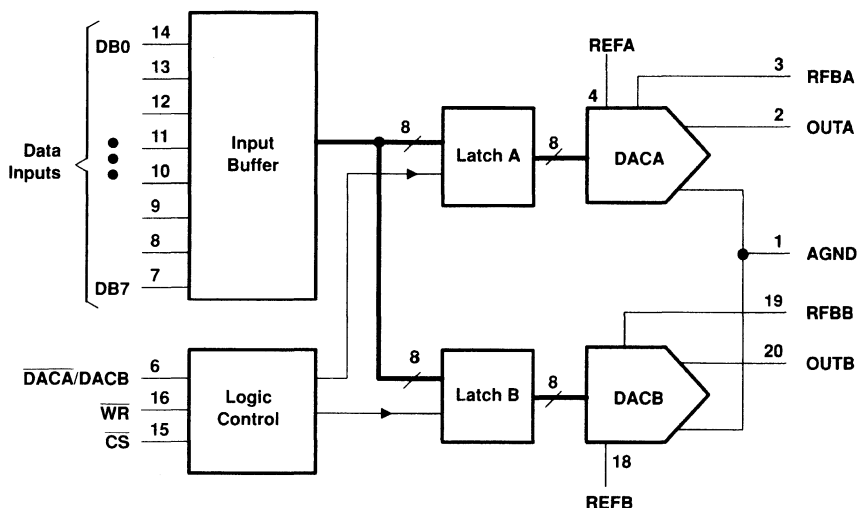
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TLC7628C, TLC7628E, TLC7628I

DUAL 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS063A - APRIL 1989 - REVISED MAY 1995

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (to AGND or DGND)	-0.3 V to 17 V
Voltage between AGND and DGND	V_{DD}
Input voltage range, V_I (to DGND)	-0.3 V to $V_{DD} + 0.3$ V
Reference voltage range, V_{refA} or V_{refB} (to AGND)	± 25 V
Feedback voltage range, V_{RFBA} or V_{RFBB} (to AGND)	± 25 V
Output voltage range, V_{OA} or V_{OB} (to AGND)	± 25 V
Peak input current	10 μ A
Operating free-air temperature range, T_A :	
TLC7628C	0°C to 70°C
TLC7628I	-25°C to 85°C
TLC7628E	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Case temperature for 10 seconds, T_C : FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



TLC7628C, TLC7628E, TLC7628I
DUAL 8-BIT MULTIPLYING
DIGITAL-TO-ANALOG CONVERTERS
 SLAS063A – APRIL 1989 – REVISED MAY 1995

recommended operating conditions

		MIN	NOM	MAX	UNIT	
Supply voltage, V_{DD}		10.8		15.75	V	
Reference voltage, V_{refA} or V_{refB}		± 10			V	
High-level input voltage, V_{IH}		2.4			V	
Low-level input voltage, V_{IL}					0.8	V
CS setup time, $t_{su}(CS)$		50			ns	
CS hold time, $t_h(CS)$ (see Figure 1)		0			ns	
DAC select setup time, $t_{su}(DAC)$ (see Figure 1)		60			ns	
DAC select hold time, $t_h(DAC)$ (see Figure 1)		10			ns	
Data bus input setup time $t_{su}(D)$ (see Figure 1)		25			ns	
Data bus input hold time $t_h(D)$ (see Figure 1)		10			ns	
Pulse duration, WR low, $t_w(WR)$ (see Figure 1)		50			ns	
Operating free-air temperature, T_A	TLC7628C	0			70	°C
	TLC7628I	-25			85	
	TLC7628E	-40			85	

electrical characteristics over recommended ranges of operating free-air temperature and V_{DD} , $V_{refA} = V_{refB} = 10$ V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT		
I_{IH}	High-level input current	$V_I = V_{DD}$	Full range	10		μA		
			25 °C	1				
I_{IL}	Low-level input current	$V_I = 0$	Full range	-10		μA		
			25 °C	-1				
Reference input impedance REFA or REFB to AGND				5	20	k Ω		
I_{kg}	Output leakage current	OUTA	DAC data latch loaded with 00000000, $V_{refA} = \pm 10$ V	Full range	± 200		nA	
			25 °C	± 50				
		OUTB	DAC data latch loaded with 00000000, $V_{refB} = \pm 10$ V	Full range	± 200			
			25 °C	± 50				
Input resistance match (REFA to REFB)				$\pm 1\%$				
DC supply sensitivity $\Delta gain/\Delta V_{DD}$		$\Delta V_{DD} = \pm 5\%$		Full range	0.02		%/%	
				25 °C	0.01			
I_{DD}	Supply current	Quiescent	All digital inputs at V_{IHmin} or V_{ILmax}		2		mA	
			Standby	All digital inputs at 0 V or V_{DD}		Full range		0.5
						25 °C		0.1
C_i	Input capacitance	DB0 - DB7			10		μF	
			WR, CS, DACA/DACB			15		
						25		
C_o	Output capacitance (OUTA, OUTB)	DAC data latches loaded with 00000000		25		μF		
		DAC data latches loaded with 11111111		60				



TLC7628C, TLC7628E, TLC7628I

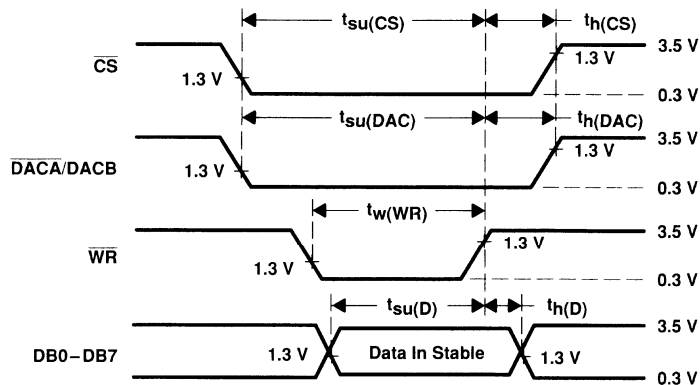
DUAL 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS063A – APRIL 1989 – REVISED MAY 1995

operating characteristics over recommended ranges of operating free-air temperature and V_{DD} , $V_{refA} = V_{refB} = 10\text{ V}$, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Linearity error						±1/2	LSB
Settling time (to 1/2 LSB)		See Note 1				100	ns
Gain error		See Note 2	Full range			±3	LSB
			25°C			±2	
AC feedthrough	REFA to OUTA	See Note 3	Full range			-65	dB
	REFB to OUTB		25°C			-75	
Temperature coefficient of gain						±0.0035	%FSR/°C
Propagation delay (from digital input to 90% of final analog output current)		See Note 4				80	ns
Channel-to-channel isolation	REFA to OUTB	See Note 5	25°C			80	dB
	REFB to OUTA	See Note 6	25°C			80	
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, $T_A = 25^\circ\text{C}$				330	nV•s
Digital crosstalk		Measured for code transition from 00000000 to 11111111, $T_A = 25^\circ\text{C}$				60	nV•s
Harmonic distortion		$V_i = 6\text{ V}$, $f = 1\text{ kHz}$, $T_A = 25^\circ\text{C}$				-85	dB

- NOTES: 1. OUTA, OUTB load = 100 Ω , $C_{ext} = 13\text{ pF}$; \overline{WR} and \overline{CS} at 0 V; DB0–DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
 2. Gain error is measured using an internal feedback resistor. Nominal full scale range (FSR) = $V_{ref} - 1\text{ LSB}$. Both DAC latches are loaded with 11111111.
 3. $V_{ref} = 20\text{ V}$ peak-to-peak, 10-kHz sine wave
 4. $V_{refA} = V_{refB} = 10\text{ V}$; OUTA/OUTB load = 100 Ω , $C_{ext} = 13\text{ pF}$; \overline{WR} and \overline{CS} at 0 V; DB0–DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
 5. $V_{refA} = 20\text{ V}$ peak-to-peak, 10-kHz sine wave; $V_{refB} = 0$
 6. $V_{refB} = 20\text{ V}$ peak-to-peak, 10-kHz sine wave; $V_{refA} = 0$



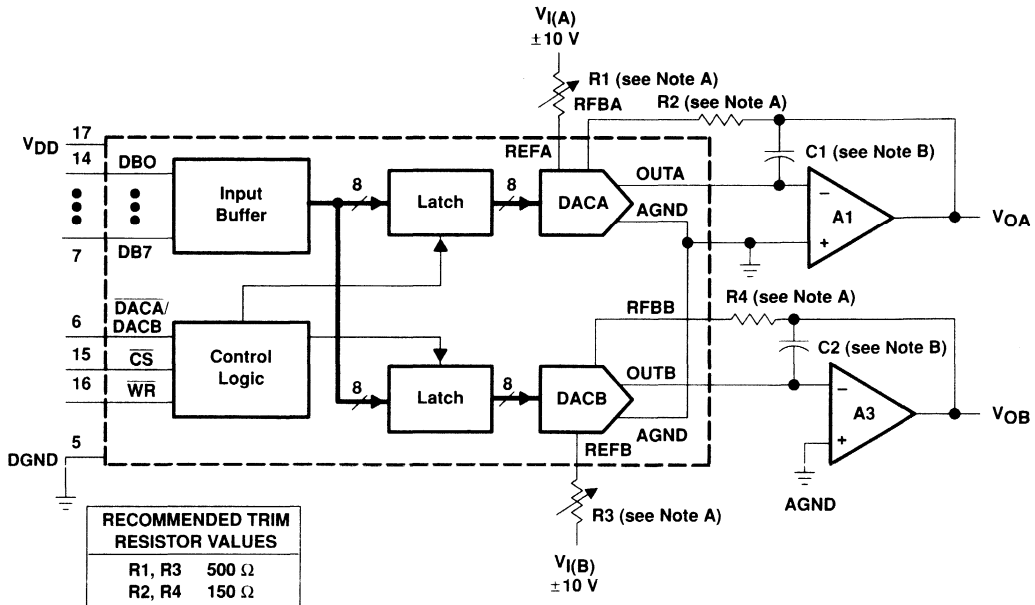
For all input signals, $t_r = t_f = 5\text{ ns}$ (10% to 90% points).

Figure 1. Setup and Hold Times



APPLICATION INFORMATION

These devices are capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 2 and 3, respectively.

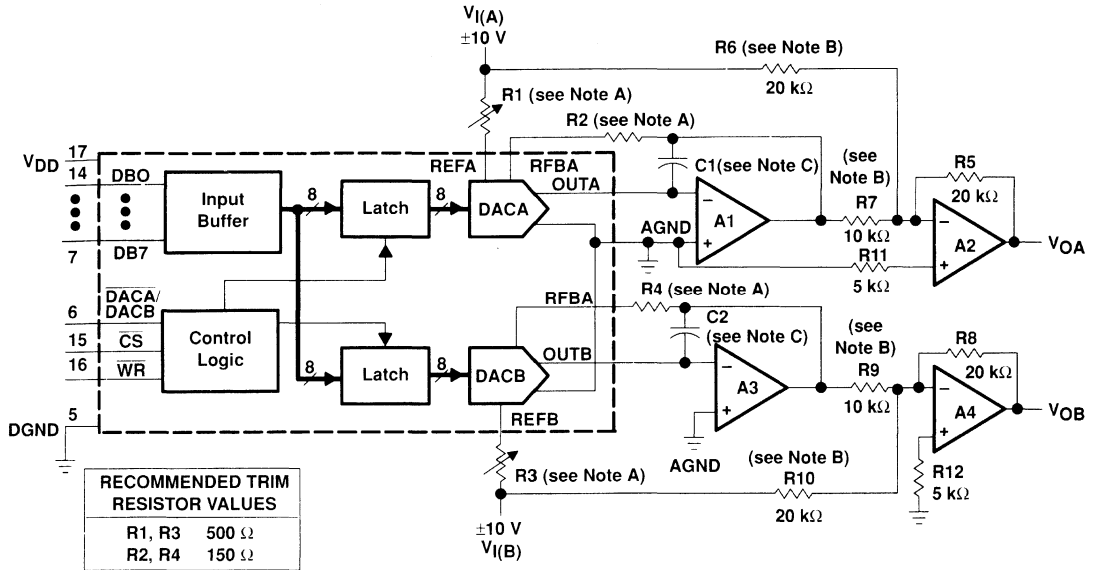


- NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
 B. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

Figure 2. Unipolar Operation (2-Quadrant Multiplication)

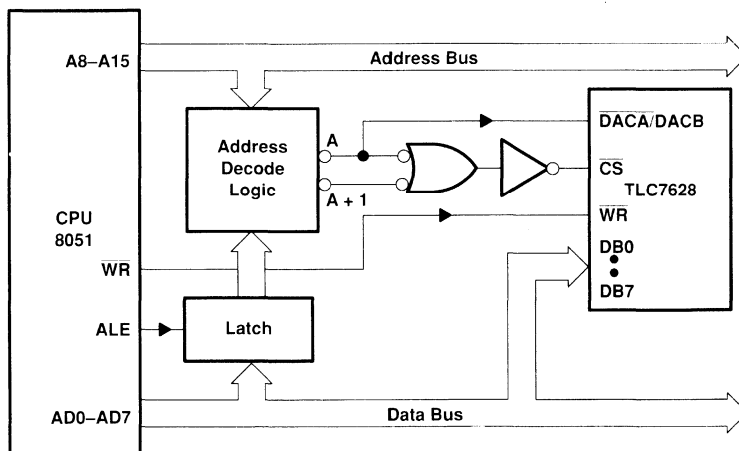
TLC7628C, TLC7628E, TLC7628I
DUAL 8-BIT MULTIPLYING
DIGITAL-TO-ANALOG CONVERTERS
 SLAS063A – APRIL 1989 – REVISED MAY 1995

APPLICATION INFORMATION



- NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Adjust R1 for $V_{OA} = 0$ V with code 10000000 in DACA latch. Adjust R3 for $V_{OB} = 0$ V with 10000000 in DACB latch.
 B. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
 C. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

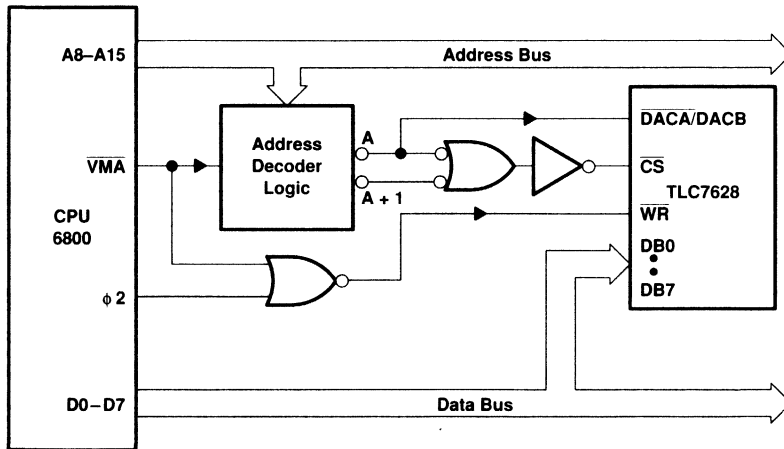
Figure 3. Bipolar Operation (4-Quadrant Operation)



NOTE D: A = decoded address for TLC7628 DACA
 A + 1 = decoded address for TLC7628 DACB

Figure 4. TLC7628 — Intel 8051 Interface

APPLICATION INFORMATION



NOTE D: A = decoded address for TLC7628 DAC
 A + 1 = decoded address for TLC7628 DACB

Figure 5. TLC7628 – 6800 Interface

voltage-mode operation

The current-multiplying DAC in these devices can be operated in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output terminal. The analog output voltage is then available at the reference voltage terminal. An example of a current-multiplying DAC operating in voltage mode is shown in Figure 6. The relationship between the fixed input voltage and the analog output voltage is given by the following equation:

$$\text{Analog output voltage} = \text{fixed input voltage} (D/256)$$

where D = the digital input. In voltage-mode operation, these devices meet the following specification:

LINEARITY ERROR	TEST CONDITIONS	MIN	MAX	UNIT
Analog output voltage for REFA, REFB	V _{DD} = 12 V, OUTA or OUTB at 5 V, T _A = 25°C		1	LSB

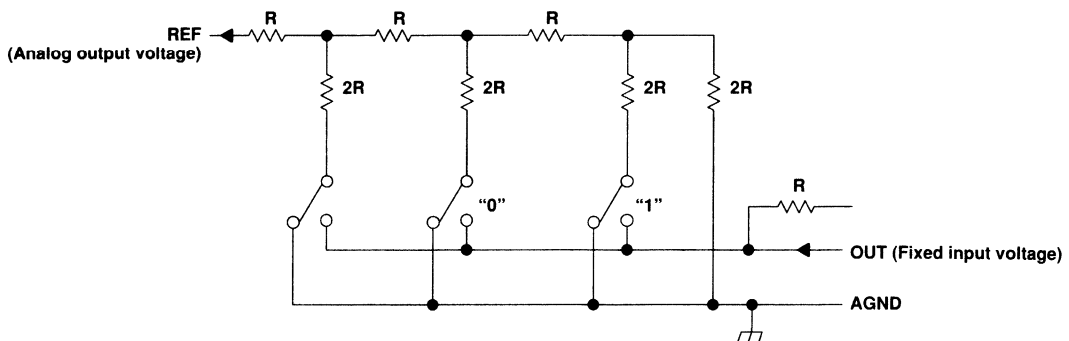


Figure 6. Current-Multiplying DAC Operating in Voltage Mode

TLC7628C, TLC7628E, TLC7628I
DUAL 8-BIT MULTIPLYING
DIGITAL-TO-ANALOG CONVERTERS

SLAS063A – APRIL 1989 – REVISED MAY 1995

PRINCIPLES OF OPERATION

These devices contain two, identical, 8-bit, multiplying DACs: DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between the DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA or DACB with all digital inputs low is shown in Figure 7.

Figure 8 shows the DACA or DACB equivalent circuit. Both DACs share the analog ground terminal 1 (AGND). With all digital inputs high, the reference current flows to OUTA. A small leakage current (I_{lkg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C . The C_o is caused by the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_o is 25 pF to 60 pF maximum. The equivalent output resistance (r_o) varies with the input code from $0.8R$ to $3R$ where R is the nominal value of the ladder resistor in the R-2R network.

These devices interface to a microprocessor through the data bus, \overline{CS} , \overline{WR} , and $\overline{DACA/DACB}$ control signals. When \overline{CS} and \overline{WR} are both low, the analog output on these devices, specified by the $\overline{DACA/DACB}$ control line, responds to the activity on the DB0–DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the \overline{CS} signal or \overline{WR} signal goes high, the data on the DB0–DB7 inputs is latched until the \overline{CS} and \overline{WR} signals go low again. When \overline{CS} is high, the data inputs are disabled, regardless of the state of the \overline{WR} signal.

The digital inputs of these devices provide TTL compatibility when operated from a supply voltage of 10.8 V to 15.75 V.

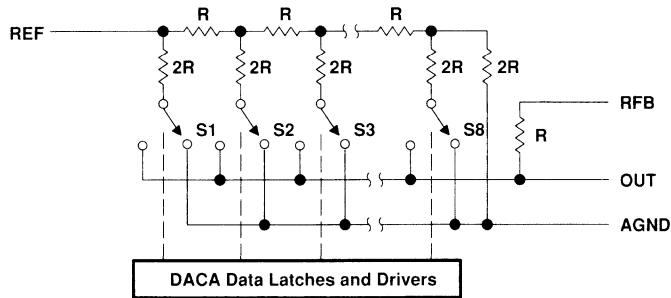


Figure 7. Simplified Functional Circuit for DACA or DACB

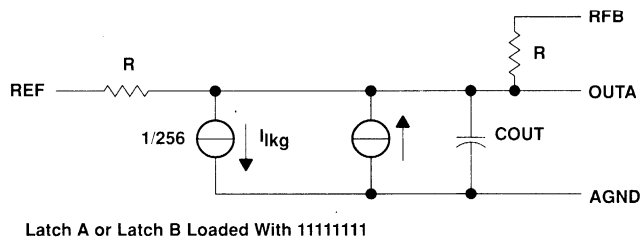


Figure 8. TLC7628 Equivalent Circuit for DACA or DACB

TLC7628C, TLC7628E, TLC7628I
DUAL 8-BIT MULTIPLYING
DIGITAL-TO-ANALOG CONVERTERS
SLAS063A – APRIL 1989 – REVISED MAY 1995

PRINCIPLES OF OPERATION

Table 1. Mode Selection Table

DACA/DACB	CS	WR	DACA	DACB
L	L	L	Write	Hold
H	L	L	Hold	Write
X	H	X	Hold	Hold
X	X	H	Hold	Hold

L = low level, H = high level, X = don't care

Table 2. Unipolar Binary Code

DAC LATCH CONTENTS (see Note 7)		ANALOG OUTPUT
MSB	LSB	
1	1111111	$-V_I (255/256)$
1	0000001	$-V_I (129/256)$
1	0000000	$-V_I (128/256) = -V_I/2$
0	1111111	$-V_I (127/256)$
0	0000001	$-V_I (1/256)$
0	0000000	$-V_I (0/256) = 0$

Table 3. Bipolar (Offset Binary) Code

DAC LATCH CONTENTS (see Note 8)		ANALOG OUTPUT
MSB	LSB	
1	1111111	$V_I (127/128)$
1	0000001	$V_I (1/128)$
1	0000000	0 V
0	1111111	$-V_I (1/128)$
0	0000001	$-V_I (127/128)$
0	0000000	$-V_I (128/128)$

NOTES: 7. 1 LSB = $(2^{-8})V_I$
 8. 1 LSB = $(2^{-7})V_I$

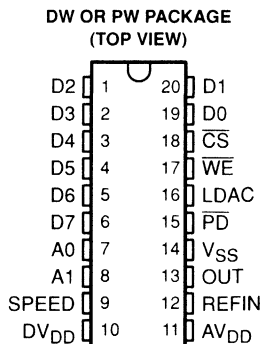


TLV5613C, TLV5613I
3 V TO 5 V 8-BIT PARALLEL DIGITAL-TO-ANALOG CONVERTERS
WITH POWER DOWN
SLAS174 – DECEMBER 1997

- **8 + 4 Bit Parallel Interface**
- **Compatible with 8-Bit Microprocessor**
- **Low Power Mode**
- **Low Power Consumption:**
 7.25 mW or 1.8 mW for 5 V
 3.93 mW or 0.87 mW for 3 V
- **Reference Input Buffers**
- **Voltage Output Range 2 Times the Reference Input Voltage**
- **Monotonic Over Temperature**

Applications

- **Battery Powered Test Instruments**
- **Digital Offset and Gain Adjustment**
- **Battery Operated/Remote Industrial Controls**
- **Machine and Motion Control Devices**
- **Cellular Telephones**



description

The TLV5613 device is a 8-bit voltage output digital-to-analog converter (DAC) with a parallel interface compatible with most 8-bit microprocessors. The TLV5613 has a low power mode, and address lines A1 and A0 which determine whether the parallel data (up to eight bits) consists of LSB DAC data, MSB DAC data, or control data. This control data gives the TLV5613 another method of setting power down and makes the low power mode available.

There is an asynchronous LDAC pin for updating the output voltage, and a power down pin to ensure repeatable startup conditions.

The resistor string output voltage is buffered by a $\times 2$ gain rail-to-rail output buffer. The buffer operates with a Class A output stage to improve stability and reduce settling time.

AVAILABLE OPTIONS

PACKAGE		
T_A	SMALL OUTLINE (DW)	SMALL OUTLINE (PW)
0°C to 70°C	TLV5613CDW	TLV5613CPW
-40°C to 85°C	TLV5613IDW	TLV5613IPW

PRODUCT PREVIEW

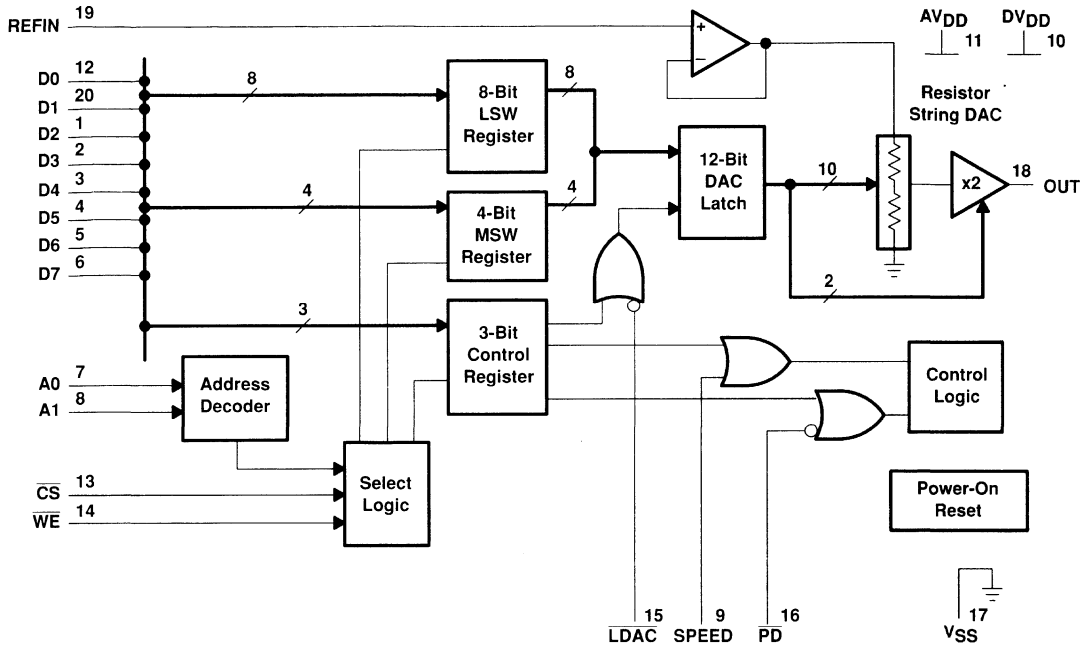
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



TLV5613C, TLV5613I
3 V TO 5 V 8-BIT PARALLEL DIGITAL-TO-ANALOG CONVERTERS
WITH POWER DOWN

SLAS174 – DECEMBER 1997

functional block diagram



PRODUCT PREVIEW



TLV5613C, TLV5613I
**3 V TO 5 V 8-BIT PARALLEL DIGITAL-TO-ANALOG CONVERTERS
 WITH POWER DOWN**
 SLAS174 – DECEMBER 1997

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AV _{DD}	11		Power supply
A0	7	I	Address line
A1	8	I	Address line
CS	13	I	Chip select
DV _{DD}	10		Power supply
D0 (LSB) – D7 (MSB)	1–6, 12, 20	I	Parallel data input
LDAC	15	I	Load DAC
OUT	18	O	Analog output
PD	16	I	Power down
REFIN	19	I	Voltage reference input
SPEED	9		Speed control
V _{SS}	17		Ground
WE	14	I	Write enable

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V _{DD} to GND)	7 V
Analog input voltage range	–0.3 V to V _{DD} + 0.3 V
Reference input voltage range	V _{DD} + 0.3 V
Digital input voltage range to GND	–0.3 V to V _{DD} + 0.3 V
Operating free-air temperature range, T _A : TLV5613C	0°C to 70°C
TLV5613I	–40°C to 85°C
Storage temperature range, T _{stg}	–65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT	
Supply voltage, V _{DD} (5-V Supply)	4.5	5	5.5	V	
Supply voltage, V _{DD} (3-V Supply)	2.7	3	3.3	V	
High-level digital input voltage, V _{IH}	V _{DD}		2	V	
Low-level digital input voltage, V _{IL}	V _{DD}		0.8 V _{DD}	V	
Reference voltage, V _{ref} to REFIN terminal (5V Supply)	2	2.048	V _{DD} –1.1	V	
Reference voltage, V _{ref} to REFIN terminal (3V Supply)	2	1.024	V _{DD} –1.1	V	
Load resistance, R _L	2			kΩ	
Load capacitance, C _L			100	pF	
Operating free-air temperature, T _A	TLV5613C		0	70	°C
	TLV5613I		–40	85	°C

PRODUCT PREVIEW



TLV5613C, TLV5613I
3 V TO 5 V 8-BIT PARALLEL DIGITAL-TO-ANALOG CONVERTERS
WITH POWER DOWN

SLAS174 – DECEMBER 1997

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5 V \pm 10\%$, $V_{DD} = 3 V \pm 10\%$, $V_{ref}(REFIN) = 2.048 V$, $V_{ref}(REFIN) = 1.024 V$ (unless otherwise noted)

static DAC specifications

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Resolution		$V_{ref}(REFIN) = 2.048V, 1.024V$		8			bits
Integral nonlinearity (INL), end point adjusted		$V_{ref}(REFIN) = 2.048V, 1.024V$, See Note 1				± 3	LSB
Differential nonlinearity (DNL)		$V_{ref}(REFIN) = 2.048V, 1.024V$, See Note 2				± 0.5	LSB
E _{ZS}	Zero-scale error (offset error at zero scale)	$V_{ref}(REFIN) = 2.048V, 1.024V$, See Note 3				± 12	MV
Zero-scale-error temperature coefficient		$V_{ref}(REFIN) = 2.048V, 1.024V$, See Note 4			3		Ppm/°C
E _G	Gain error	$V_{ref}(REFIN) = 2.048V, 1.024V$, See Note 5				± 0.29	% of FS voltage
Gain error temperature coefficient		$V_{ref}(REFIN) = 2.048V, 1.024V$, See Note 6			1		Ppm/°C
PSRR	Power-supply rejection ratio	Zero scale Gain Zero scale Gain	See Notes 7 and 8	5-V supply	65	dB	
					65		
				3-V Supply	65		
					65		

- NOTES: 1. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.
2. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
4. Zero-scale-error temperature coefficient is given by: $E_{ZS} TC = [E_{ZS}(T_{max}) - E_{ZS}(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
5. Gain error is the deviation from the ideal output ($V_{ref} - 1$ LSB) with an output load of 10 k Ω excluding the effects of the zero-error.
6. Gain temperature coefficient is given by: $E_G TC = [E_G(T_{max}) - E_G(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
7. Zero-scale-error rejection ratio (E_{ZS}-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
8. Gain-error rejection ratio (E_G-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero scale change.

output specifications

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _O	Voltage output range				TBD		V
Output load regulation accuracy		$V_{O(OUT)} = 4.096 V$, $V_{ref}(REFIN) = 2.048 V$ $R_L = 2 k\Omega$			TBD		% of FS voltage
I _{OSC(sink)}	Output short circuit sink current	5-V Supply			TBD		mA
		3-V Supply			TBD		
I _{OSC(source)}	Output short circuit source current	5-V Supply			TBD		mA
		3-V Supply			TBD		
I _{O(sink)}	Output sink current				TBD		mA
I _{O(source)}	Output source current				TBD		mA

PRODUCT PREVIEW



TLV5613C, TLV5613I
3 V TO 5 V 8-BIT PARALLEL DIGITAL-TO-ANALOG CONVERTERS
WITH POWER DOWN

SLAS174 – DECEMBER 1997

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 10\%$, $V_{DD} = 3\text{ V} \pm 10\%$, $V_{ref}(REFIN) = 2.048\text{ V}$, $V_{ref}(REFIN) = 1.024\text{ V}$ (unless otherwise noted)

reference input (REFIN)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I Input voltage range		0		$V_{DD}-1.1$	V
R_i Input resistance			10		$M\Omega$
C_i Input capacitance			5		pF
Reference feed through	REFIN = 1 V_{pp} at 1 kHz + 1.024 V dc (see Note 9)		TBD		
Reference input bandwidth	REFIN = 0.2 V_{pp} + 1.024 V dc	Fast mode	Small signal	1.6	MHz
			Large signal	$3.3/2\pi V_m$	MHz
		Slow mode	Small signal	1	MHz
			Large signal	$3.3/9\pi V_m$	MHz

NOTE 9: Reference feedthrough is measured at the DAC output with an input code = 000 hex and a $V_{ref}(REFIN)$ input = 1.024 V dc + 1 V_{pp} at 1 kHz.

digital inputs (D0 – D11, CS, WE, LDAC, Power Down)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH} High-level digital input current	$V_I = V_{DD}$			± 1	μA
I_{IL} Low-level digital input current	$V_I = 0\text{ V}$			± 1	μA
C_i Input capacitance			8		pF

power supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD} Power supply current	No load All inputs 0 V or V_{DD}	5-V Supply	1.45	1.9	mA
		3-V Supply	1.31	1.69	
Power down supply current			0.17		μA

PRODUCT PREVIEW



TLV5613C, TLV5613I
3 V TO 5 V 8-BIT PARALLEL DIGITAL-TO-ANALOG CONVERTERS
WITH POWER DOWN

SLAS174 – DECEMBER 1997

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 10\%$, $V_{DD} = 3\text{ V} \pm 10\%$, $V_{\text{ref}}(\text{REFIN}) = 2.048\text{ V}$, $V_{\text{ref}}(\text{REFIN}) = 1.024\text{ V}$

analog output dynamic performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
SR+	Output slew rate, positive	$C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, Code 32 to Code 4096.	$V_{\text{ref}}(\text{REFIN}) = 2.048\text{ V}, 1.024\text{ V}$, $T_A = 25^\circ\text{C}$, V_O from 10% to 90%		8		$\text{V}/\mu\text{s}$	
SR-	Slew rate, negative	$C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, Code 32 to Code 4096.	$V_{\text{ref}}(\text{REFIN}) = 2.048\text{ V}, 1.024\text{ V}$, $T_A = 25^\circ\text{C}$, V_O from 10% to 90%		8		$\text{V}/\mu\text{s}$	
t_s	Output settling time (Full scale)	$T_o \pm 0.5\text{ LSB}$, $R_L = 10\text{ k}\Omega$,	$C_L = 100\text{ pF}$, See Note 10	5V	Fast	0.9	1.3	μs
					Slow	3.4	5.2	
				3V	Fast	0.8	1.1	
					Slow	3.1	3.9	
$t_{s(c)}$	Output settling time, (Code-to-Code)	$T_o \pm 0.5\text{ LSB}$, $R_L = 10\text{ k}\Omega$,	$C_L = 100\text{ pF}$, See Note 11	5V	Fast	TBD	μs	
					Slow	TBD		
				3V	Fast	TBD		
					Slow	TBD		
Glitch energy							TBD	
S/(N+D)	Signal to noise + distortion						TBD	

NOTES: 10. Settling time is the time for the output signal to remain within $\pm 0.5\text{ LSB}$ of the final measured value for a digital input code change of 020 hex to 3FF hex or 3FF hex to 020 hex.

11. Settling time is the time for the output signal to remain within $\pm 0.5\text{ LSB}$ of the final measured value for a digital input code change of one count.

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{DD} = 3\text{ V} \pm 5\%$, $V_{\text{ref}}(\text{REFIN}) = 2.048\text{ V}$, $V_{\text{ref}}(\text{REFIN}) = 1.024\text{ V}$

digital input timing requirements

		MIN	NOM	MAX	UNIT
$t_{su}(\text{D-WE})$	Setup time, data ready before positive WE edge	9			ns
$t_{su}(\text{CS-WE})$	Setup time, CS low before positive WE edge	13			ns
$t_{su}(\text{A-WE})$	Setup time, address bits A0, A1		TBD		ns
$t_H(\text{D})$	Hold time, data held after positive WE edge	0			ns
t_s	Settling time, full scale		0.9		μs

PRODUCT PREVIEW



TLV5613C, TLV5613I
**3 V TO 5 V 8-BIT PARALLEL DIGITAL-TO-ANALOG CONVERTERS
 WITH POWER DOWN**
 SLAS174 – DECEMBER 1997

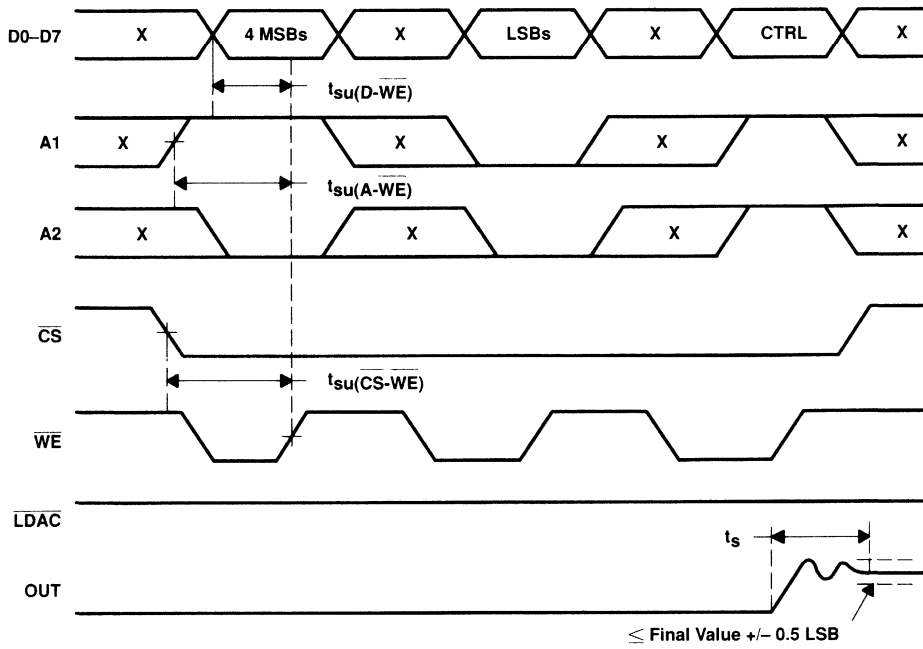


Figure 1. Timing Diagram

PRODUCT PREVIEW

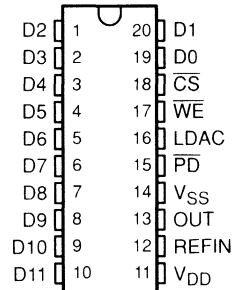
TLV5619C, TLV5619I

3 V TO 5 V 12-BIT PARALLEL DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN

SLAS172 – DECEMBER 1997

- **New 12-Bit Parallel Interface**
- **Compatible with TMS320 DSP Line**
- **Internal Power on Reset**
- **Low Power Consumption:**
7.25 mW for 5-V Supply
3.93 mW for 3-V Supply
- **Reference Input Buffers**
- **Voltage Output Range 2 Times the Reference Input Voltage**
- **Monotonic Over Temperature**
- **Asynchronous or Synchronous Update**

DW OR PW PACKAGE
(TOP VIEW)



applications

- **Battery Powered Test Instruments**
- **Digital Offset and Gain Adjustment**
- **Battery Operated/Remote Industrial Controls**
- **Machine and Motion Control Devices**
- **Cellular Telephones**

description

The TLV5619 device is a 12-bit voltage output digital-to-analog converter (DAC) with a TMS320 compatible parallel interface. While accepting 12-bit data words, the TLV5619 only dissipates 7.25 mW of power with a 5-V supply and 3.93 mW of power with a 3-V supply.

There is an asynchronous LDAC pin for updating the output voltage, and a power down pin to ensure repeatable startup conditions.

The resistor string output voltage is buffered by a $\times 2$ gain rail-to-rail output buffer. The buffer operates with a Class A output stage to improve stability and reduce settling time.

AVAILABLE OPTIONS

PACKAGE		
T _A	SMALL OUTLINE (DW)	SMALL OUTLINE (PW)
0°C to 70°C	TLV5619CDW	TLV5619CPW
-40°C to 85°C	TLV5619IDW	TLV5619IPW

PRODUCT PREVIEW

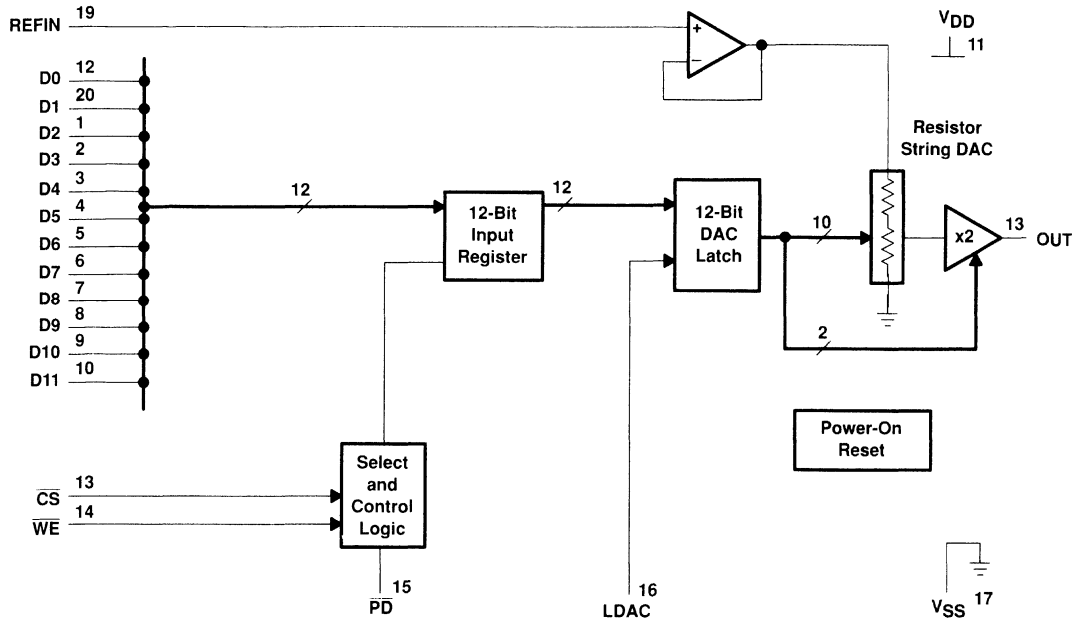
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



TLV5619C, TLV5619I
3 V TO 5 V 12-BIT PARALLEL DIGITAL-TO-ANALOG CONVERTERS
WITH POWER DOWN

SLAS172 – DECEMBER 1997

functional block diagram



PRODUCT PREVIEW



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TLV5619C, TLV5619I
3 V TO 5 V 12-BIT PARALLEL DIGITAL-TO-ANALOG CONVERTERS
WITH POWER DOWN

SLAS172 – DECEMBER 1997

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CS	13	I	Chip select
D0 (LSB)	12	I	Parallel data input
D1	20	I	Parallel data input
D2	1	I	Parallel data input
D3	2	I	Parallel data input
D4	3	I	Parallel data input
D5	4	I	Parallel data input
D6	5	I	Parallel data input
D7	6	I	Parallel data input
D8	7	I	Parallel data input
D9	8	I	Parallel data input
D10	9	I	Parallel data input
D11 (MSB)	10	I	Parallel data input
V _{SS}	17		Ground
LDAC	15	I	Load DAC
OUT	18	O	Analog output
$\overline{\text{PD}}$	16	I	
REFIN	19	I	Voltage reference input
V _{DD}	11		Positive power supply
WE	14	I	Write enable

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V _{DD} to GND)	7 V
Analog input voltage range	– 0.3 V to V _{DD} + 0.3 V
Reference input voltage	V _{DD} + 0.3 V
Digital input voltage range to GND	– 0.3 V to V _{DD} + 0.3 V
Operating free-air temperature range, T _A : TLV5619C	0°C to 70°C
TLV5619I	–40°C to 85°C
Storage temperature range, T _{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



TLV5619C, TLV5619I
3 V TO 5 V 12-BIT PARALLEL DIGITAL-TO-ANALOG CONVERTERS
WITH POWER DOWN

SLAS172 – DECEMBER 1997

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (5-V Supply)		4.5	5	5.5	V
Supply voltage, V_{DD} (3-V Supply)		2.7	3	3.3	V
High-level digital input voltage, V_{IH}	V_{DD}	2			V
Low-level digital input voltage, V_{IL}	V_{DD}	0.8 V_{DD}			V
Reference voltage, V_{ref} to REFIN terminal (5-V Supply)		2	2.048	$V_{DD}-1.1$	V
Reference voltage, V_{ref} to REFIN terminal (3-V Supply)		2	1.024	$V_{DD}-1.1$	V
Load resistance, R_L		2			k Ω
Load capacitance, C_L		100			pF
Operating free-air temperature, T_A	TLV5619C	0			$^{\circ}$ C
	TLV5619I	-40			$^{\circ}$ C

PRODUCT PREVIEW



TLV5619C, TLV5619I
3 V TO 5 V 12-BIT PARALLEL DIGITAL-TO-ANALOG CONVERTERS
WITH POWER DOWN

SLAS172 – DECEMBER 1997

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 10\%$, $V_{DD} = 3\text{ V} \pm 10\%$, $V_{ref}(REFIN) = 2.048\text{ V}$, $V_{ref}(REFIN) = 1.024\text{ V}$ (unless otherwise noted)

static DAC specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		$V_{ref}(REFIN) = 2.048\text{ V}, 1.024\text{ V}$	12			bits
Integral nonlinearity (INL), end point adjusted		$V_{ref}(REFIN) = 2.048\text{ V}, 1.024\text{ V}$, See Note 1	±3			LSB
Differential nonlinearity (DNL)		$V_{ref}(REFIN) = 2.048\text{ V}, 1.024\text{ V}$, See Note 2	±0.5			LSB
E _{ZS}	Zero-scale error (offset error at zero scale)	$V_{ref}(REFIN) = 2.048\text{ V}, 1.024\text{ V}$, See Note 3	±12			mV
	Zero-scale-error temperature coefficient	$V_{ref}(REFIN) = 2.048\text{ V}, 1.024\text{ V}$, See Note 4	3			ppm/°C
E _G	Gain error	$V_{ref}(REFIN) = 2.048\text{ V}, 1.024\text{ V}$, See Note 5	±0.29			% of FS voltage
	Gain error temperature coefficient	$V_{ref}(REFIN) = 2.048\text{ V}, 1.024\text{ V}$, See Note 6	1			ppm/°C
PSRR	Power-supply rejection ratio	See Notes 7 and 8	5-V Supply	Zero scale	65	dB
				Gain	65	
			3-V Supply	Zero scale	65	
				Gain	65	

- NOTES:
1. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.
 2. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
 3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
 4. Zero-scale-error temperature coefficient is given by: $E_{ZS} TC = [E_{ZS}(T_{max}) - E_{ZS}(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
 5. Gain error is the deviation from the ideal output ($V_{ref} - 1\text{ LSB}$) with an output load of 10 k Ω excluding the effects of the zero-error.
 6. Gain temperature coefficient is given by: $E_G TC = [E_G(T_{max}) - E_G(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
 7. Zero-scale-error rejection ratio (E_{ZS}-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
 8. Gain-error rejection ratio (E_G-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero scale change.

output specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _O	Voltage output range		TBD			V
Output load regulation accuracy		$V_{O(OUT)} = 4.096\text{ V}, 2.048\text{ V}$ $R_L = 2\text{ k}\Omega$	TBD			% of FS voltage
I _{OSC(sink)}	Output short circuit sink current	5-V Supply	TBD			mA
		3-V Supply	TBD			
I _{OSC(source)}	Output short circuit source current	5-V Supply	TBD			mA
		3-V Supply	TBD			
I _{O(sink)}	Output sink current		TBD			mA
I _{O(source)}	Output source current		TBD			mA

PRODUCT PREVIEW



TLV5619C, TLV5619I
3 V TO 5 V 12-BIT PARALLEL DIGITAL-TO-ANALOG CONVERTERS
WITH POWER DOWN

SLAS172 – DECEMBER 1997

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 10\%$, $V_{DD} = 3\text{ V} \pm 10\%$, $V_{\text{ref}}(\text{REFIN}) = 2.048\text{ V}$, $V_{\text{ref}}(\text{REFIN}) = 1.024\text{ V}$ (unless otherwise noted)

reference input (REFIN)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I Input voltage range		0		$V_{DD}-1.1$	V
R_i Input resistance			10		M Ω
C_i Input capacitance			5		pF
Reference feed through	REFIN = $1 V_{pp}$ at 1 kHz + 1.024 V dc (see Note 9)				
Reference input bandwidth	REFIN = $0.2 V_{pp}$ + 1.024 V dc		1.6		MHz

NOTE 9: Reference feedthrough is measured at the DAC output with an input code = 000 hex and a $V_{\text{ref}}(\text{REFIN})$ input = 1.024 V dc + 1 V_{pp} at 1 kHz.

digital inputs (D0 – D11, $\overline{\text{CS}}$, $\overline{\text{WE}}$, LDAC, Power Down)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH} High-level digital input current	$V_I = V_{DD}$			± 1	μA
I_{IL} Low-level digital input current	$V_I = 0\text{ V}$			± 1	μA
C_i Input capacitance			8		pF

power supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD} Power supply current	No load All inputs 0V or V_{DD}	5-V Supply	1.45	1.9	mA
		3-V Supply	1.31	1.69	
Power down supply current			0.17		μA

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 10\%$, $V_{DD} = 3\text{ V} \pm 10\%$, $V_{\text{ref}}(\text{REFIN}) = 2.048\text{ V}$, $V_{\text{ref}}(\text{REFIN}) = 1.024\text{ V}$

analog output dynamic performance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR+ Output slew rate, positive	$C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, Code 32 to Code 4096, $V_{\text{ref}}(\text{REFIN}) = 2.048\text{ V}, 1.024\text{ V}$, $T_A = 25^\circ\text{C}$, V_O from 10% to 90%		8		V/ μs
SR- Slew rate, negative	$C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, Code 32 to Code 4096, $V_{\text{ref}}(\text{REFIN}) = 2.048\text{ V}, 1.024\text{ V}$, $T_A = 25^\circ\text{C}$, V_O from 10% to 90%		8		V/ μs
t_s Output settling time (Full scale)	$T_o \pm 0.5\text{ LSB}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, See Note 10	5 V	0.9	1.3	μs
		3 V	0.8	1.1	
$t_{s(c)}$ Output settling time, (Code-to-Code)	$T_o \pm 0.5\text{ LSB}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, See Note 11	5 V	TBD		μs
		3 V	TBD		
Glitch energy			TBD		
S/(N+D) Signal to noise + distortion			TBD		

NOTES: 10. Settling time is the time for the output signal to remain within $\pm 0.5\text{ LSB}$ of the final measured value for a digital input code change of 020 hex to 3FF hex or 3FF hex to 020 hex.

11. Settling time is the time for the output signal to remain within $\pm 0.5\text{ LSB}$ of the final measured value for a digital input code change of one count.

PRODUCT PREVIEW



TLV5619C, TLV5619I
**3 V TO 5 V 12-BIT PARALLEL DIGITAL-TO-ANALOG CONVERTERS
 WITH POWER DOWN**

SLAS172 - DECEMBER 1997

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$,
 $V_{DD} = 3\text{ V} \pm 5\%$, $V_{ref}(REFIN) = 2.048\text{ V}$, $V_{ref}(REFIN) = 1.024\text{ V}$

digital input timing requirements

		MIN	NOM	MAX	UNIT
$t_{su}(D-\overline{WE})$	Setup time, data ready before positive \overline{WE} edge	9			ns
$t_{su}(CS-\overline{WE})$	Setup time, \overline{CS} low before positive \overline{WE} edge	13			ns
$t_H(D)$	Hold time, data held after positive \overline{WE} edge	0			ns
t_s	Settling time, full scale		0.9		μs

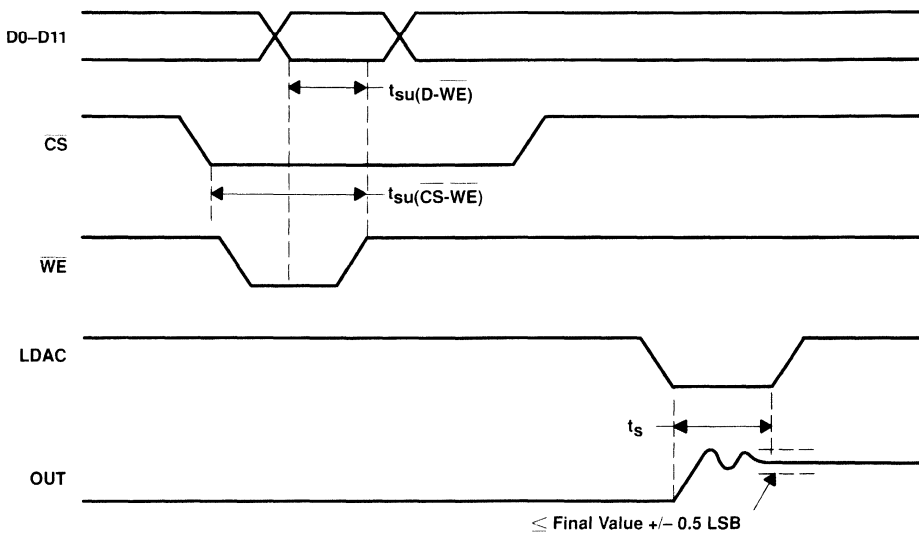


Figure 1. Timing Diagram

PRODUCT PREVIEW



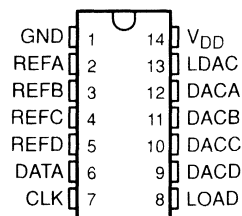
TLV5620C, TLV5620I

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS110B – JANUARY 1995 – REVISED APRIL 1997

- Four 8-Bit Voltage Output DACs
- 3-V Single-Supply Operation
- Serial Interface
- High-Impedance Reference Inputs
- Programmable for 1 or 2 Times Output Range
- Simultaneous Update Facility
- Internal Power-On Reset
- Low-Power Consumption
- Half-Buffered Output

D OR N PACKAGE
(TOP VIEW)



applications

- Programmable Voltage Sources
- Digitally Controlled Amplifiers/Attenuators
- Mobile Communications
- Automatic Test Equipment
- Process Monitoring and Control
- Signal Synthesis

description

The TLV5620C and TLV5620I are quadruple 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that ranges between either one or two times the reference voltages and GND; and, the DACs are monotonic. The device is simple to use, because it runs from a single supply of 3 V to 3.6 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLV5620C and TLV5620I is over a simple three-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 11-bit command word comprises eight bits of data, two DAC select bits, and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs update simultaneously through control of LDAC. The digital inputs feature Schmitt triggers for high noise immunity.

The 14-terminal small-outline (SO) package allows digital control of analog functions in space-critical applications. The TLV5620C is characterized for operation from 0°C to 70°C. The TLV5620I is characterized for operation from -40°C to 85°C. The TLV5620C and TLV5620I do not require external trimming.

AVAILABLE OPTIONS

PACKAGE		
T _A	SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	TLV5620CD	TLV5620CN
-40°C to 85°C	TLV5620ID	TLV5620IN

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



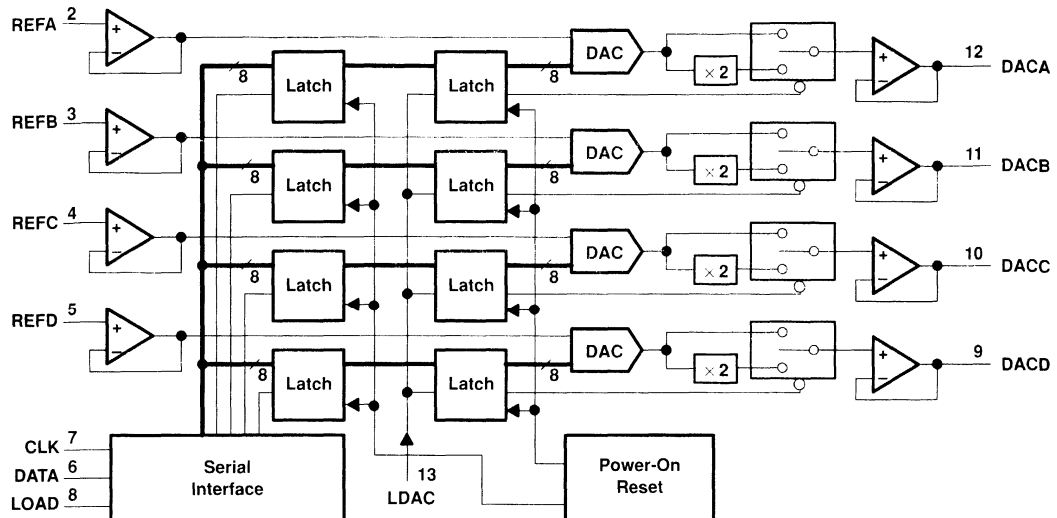
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TLV5620C, TLV5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CLK	7	I	Serial interface clock. The input digital data is shifted into the serial interface register on the falling edge of the clock applied to the CLK terminal.
DACA	12	O	DAC A analog output
DACB	11	O	DAC B analog output
DACC	10	O	DAC C analog output
DACD	9	O	DAC D analog output
DATA	6	I	Serial interface digital data input. The digital code for the DAC is clocked into the serial interface register serially. Each data bit is clocked into the register on the falling edge of the clock signal.
GND	1	I	Ground return and reference terminal
LDAC	13	I	Load DAC. When this signal is high, no DAC output updates occur when the input digital data is read into the serial interface. The DAC outputs are only updated when LDAC is taken from high to low.
LOAD	8	I	Serial interface load control. When the LDAC terminal is low, the falling edge of the LOAD signal latches the digital data into the output latch and immediately produces the analog voltage at the DAC output terminal.
REFA	2	I	Reference voltage input to DAC A. This voltage defines the output analog range.
REFB	3	I	Reference voltage input to DAC B. This voltage defines the analog output range.
REFC	4	I	Reference voltage input to DAC C. This voltage defines the analog output range.
REFD	5	I	Reference voltage input to DAC D. This voltage defines the analog output range.
VDD	14	I	Positive supply voltage

TLV5620C, TLV5620I

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS110B – JANUARY 1995 – REVISED APRIL 1997

detailed description

The TLV5620 is implemented using four resistor-string DACs. The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 1. One end of each resistor string is connected to GND and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor segments and upon the performance of the output buffer. Since the inputs are buffered, the DACs always presents a high-impedance load to the reference source.

Each DAC output is buffered by a configurable-gain output amplifier, which can be programmed to times 1 or times 2 gain.

On power up, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_{O(DACA|B|C|D)} = \text{REF} \times \frac{\text{CODE}}{256} \times (1 + \text{RNG bit value})$$

where CODE is in the range 0 to 255 and the range (RNG) bit is a 0 or 1 within the serial control word.

Table 1. Ideal Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	$(1/256) \times \text{REF} (1+\text{RNG})$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	$(127/256) \times \text{REF} (1+\text{RNG})$
1	0	0	0	0	0	0	0	$(128/256) \times \text{REF} (1+\text{RNG})$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	$(255/256) \times \text{REF} (1+\text{RNG})$

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial input register to the selected DAC as shown in Figure 1. When LDAC is low, the selected DAC output voltage is updated when LOAD goes low. When LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered MSB first. Data transfers using two 8-clock-cycle periods are shown in Figures 3 and 4.

Table 2 lists the A1 and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = low, the output range is between the applied reference voltage and GND, and when RNG = high, the range is between twice the applied reference voltage and GND.

Table 2. Serial Input Decode

A1	A0	DAC UPDATED
0	0	DACA
0	1	DACB
1	0	DACC
1	1	DACD



TLV5620C, TLV5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS110B – JANUARY 1995 – REVISED APRIL 1997

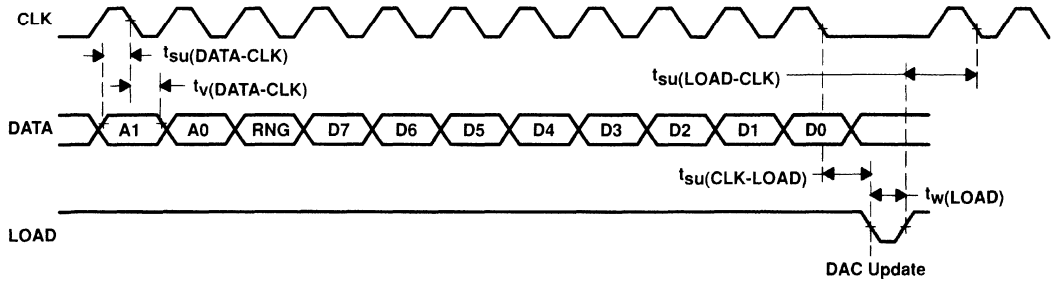


Figure 1. LOAD-Controlled Update (LDAC = Low)

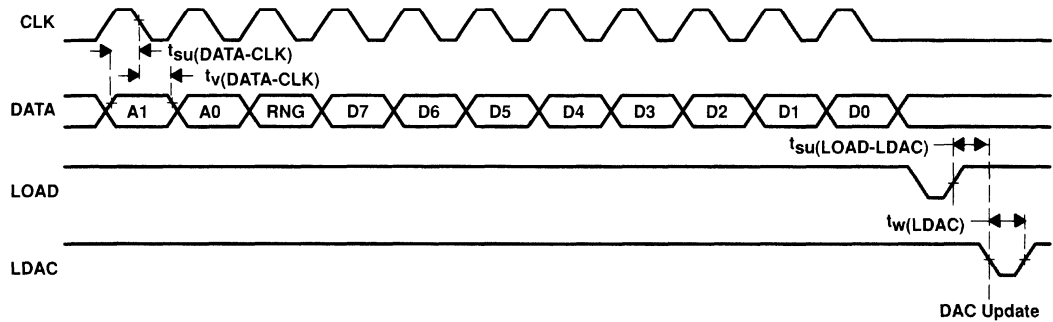


Figure 2. LDAC-Controlled Update

TLV5620C, TLV5620I
 QUADRUPLE 8-DIGITAL-TO-ANALOG CONVERTERS

SLAS110B – JANUARY 1995 – REVISED APRIL 1997

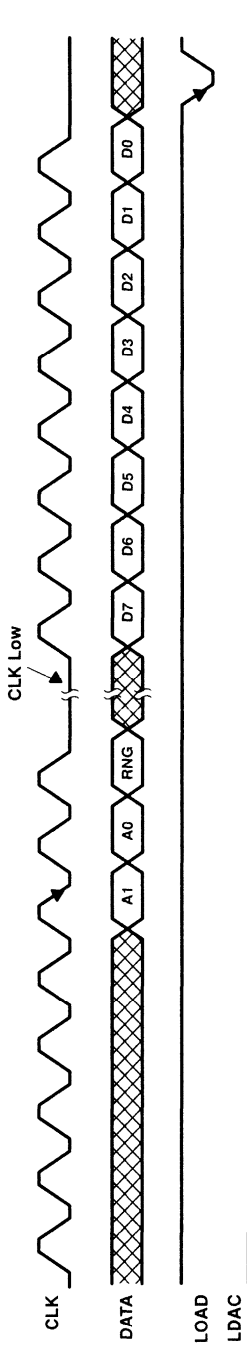


Figure 3. Load Controlled Update Using 8-Bit Serial Word (LDAC = Low)

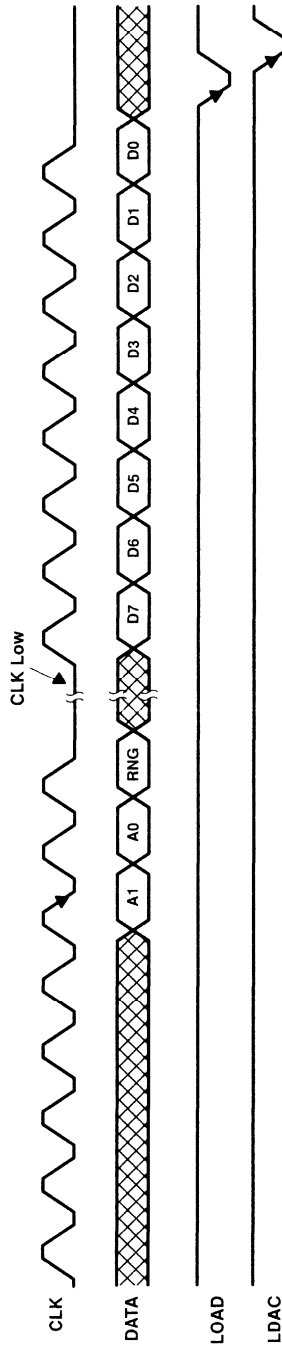


Figure 4. LDAC Controlled Update Using 8-Bit Serial Word

TLV5620C, TLV5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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linearity, offset, and gain error using single-end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset voltage, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier, therefore, attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 5.

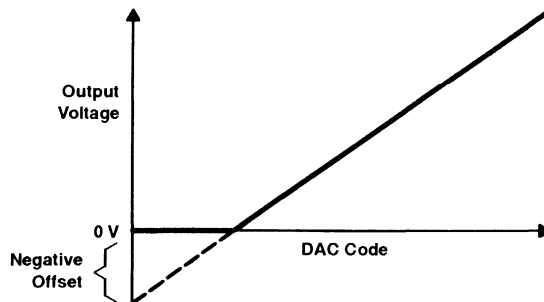


Figure 1. Effect of Negative Offset (Single Supply)

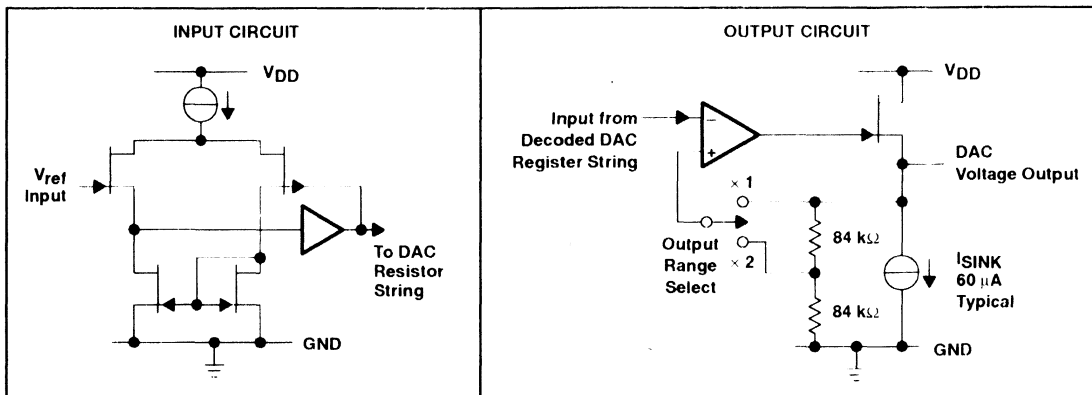
This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below ground.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single-supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. The code is calculated from the maximum specification for the negative offset.

TLV5620C, TLV5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS110B JANUARY 1995 REVISED APRIL 1997

equivalent inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage ($V_{DD} - GND$)	7 V
Digital input voltage range	$GND - 0.3 V$ to $V_{DD} + 0.3 V$
Reference input voltage range, V_{ID}	$GND - 0.3 V$ to $V_{DD} + 0.3 V$
Operating free-air temperature range, T_A : TLV5620C	0°C to 70°C
TLV5620I	-40°C to 85°C
Storage temperature range, T_{stg}	-50°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	2.7	3.3	5.25	V
High-level input voltage, V_{IH}	0.8 V_{DD}			V
Low-level input voltage, V_{IL}		0.8		V
Reference voltage, V_{ref} [A/B/C/D], x1 gain			$V_{DD} - 1.5$	V
Load resistance, R_L	10			kΩ
Setup time, data input, $t_{su}(DATA-CLK)$ (see Figures 1 and 2)	50			ns
Valid time, data input valid after $CLK\downarrow$, $t_v(DATA-CLK)$ (see Figures 1 and 2)	50			ns
Setup time, CLK eleventh falling edge to $LOAD$, $t_{su}(CLK-LOAD)$ (see Figure 1)	50			ns
Setup time, $LOAD\uparrow$ to $CLK\downarrow$, $t_{su}(LOAD-CLK)$ (see Figure 1)	50			ns
Pulse duration, $LOAD$, $t_w(LOAD)$ (see Figure 1)	250			ns
Pulse duration, $LDAC$, $t_w(LDAC)$ (see Figure 2)	250			ns
Setup time, $LOAD\uparrow$ to $LDAC\downarrow$, $t_{su}(LOAD-LDAC)$ (see Figure 2)	0			ns
CLK frequency			1	MHz
Operating free-air temperature, T_A	TLV5620C	0	70	°C
	TLV5620I	-40	85	



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TLV5620C, TLV5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS110B – JANUARY 1995 – REVISED APRIL 1997

**electrical characteristics over recommended operating free-air temperature range,
V_{DD} = 3 V to 3.6 V, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{IH}	High-level input current	V _I = V _{DD}			± 10	μA
I _{IL}	Low-level input current	V _I = 0 V			± 10	μA
I _{O(sink)}	Output sink current	Each DAC output	20			μA
I _{O(source)}	Output source current		1			mA
C _i	Input capacitance			15		pF
	Reference input capacitance			15		
I _{DD}	Supply current	V _{DD} = 3.3 V			2	mA
I _{ref}	Reference input current	V _{DD} = 3.3 V, V _{ref} = 1.5 V			± 10	μA
E _L	Linearity error (end point corrected)	V _{ref} = 1.25 V, × 2 gain, See Note 1			± 1	LSB
E _D	Differential linearity error	V _{ref} = 1.25 V, × 2 gain, See Note 2			± 0.9	LSB
E _{ZS}	Zero-scale error	V _{ref} = 1.25 V, × 2 gain, See Note 3	0		30	mV
	Zero-scale error temperature coefficient	V _{ref} = 1.25 V, × 2 gain, See Note 4		10		μV/°C
E _{FS}	Full-scale error	V _{ref} = 1.25 V, × 2 gain, See Note 5			± 60	mV
	Full-scale error temperature coefficient	V _{ref} = 1.25 V, × 2 gain, See Note 6		± 25		μV/°C
PSRR	Power-supply sensitivity	See Notes 7 and 8		0.5		mV/V

- NOTES:
1. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
 2. Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
 3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
 4. Zero-scale error temperature coefficient is given by: ZSETC = [ZSE(T_{max}) - ZSE(T_{min})]/V_{ref} × 10⁶/(T_{max} - T_{min}).
 5. Full-scale error is the deviation from the ideal full-scale output (V_{ref} - 1 LSB) with an output load of 10 kΩ.
 6. Full-scale error temperature coefficient is given by: FSETC = [FSE(T_{max}) - FSE(T_{min})]/V_{ref} × 10⁶/(T_{max} - T_{min}).
 7. Zero-scale error rejection ratio (ZSE-RR) is measured by varying the V_{DD} voltage from 4.5 V to 5.5 V dc and measuring the effect of this signal on the zero-code output voltage.
 8. Full-scale error rejection ratio (FSE-RR) is measured by varying the V_{DD} voltage from 3 V to 3.6 V dc and measuring the effect of this signal on the full-scale output voltage.

**operating characteristics over recommended operating free-air temperature range,
V_{DD} = 3 V to 3.6 V, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)**

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	C _L = 100 pF, R _L = 10 kΩ		1		V/μs
Output settling time	To ± 0.5 LSB, C _L = 100 pF, R _L = 10 kΩ, See Note 9		10		μs
Large-signal bandwidth	Measured at -3 dB point		100		kHz
Digital crosstalk	CLK = 1-MHz square wave measured at DACA-DACD		-50		dB
Reference feedthrough	See Note 10		-60		dB
Channel-to-channel isolation	See Note 11		-60		dB
Reference input bandwidth	See Note 12		100		kHz

- NOTES:
9. Settling time is the time between a LOAD falling edge and the DAC output reaching full-scale voltage within ± 0.5 LSB starting from an initial output voltage equal to zero.
 10. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
 11. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
 12. Reference bandwidth is the -3 dB bandwidth with an input at V_{ref} = 1.25 V dc + 2 V_{pp} and with a digital input code of full-scale.



TLV5620C, TLV5620I

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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PARAMETER MEASUREMENT INFORMATION

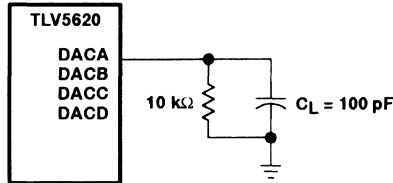
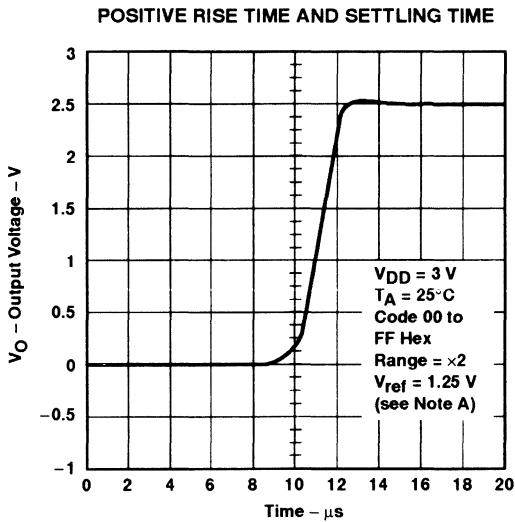


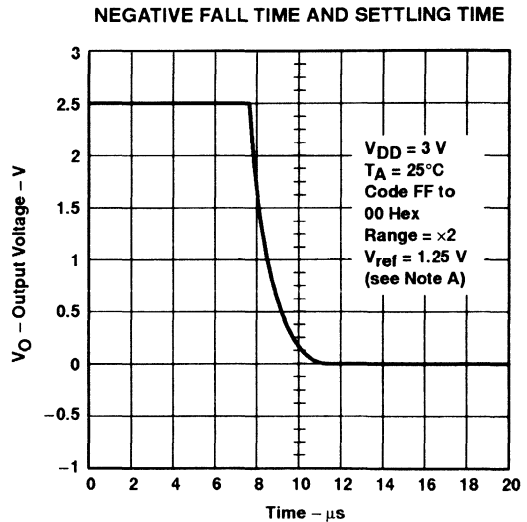
Figure 2. Slew, Settling Time, and Linearity Measurements

TYPICAL CHARACTERISTICS



NOTE A: Rise time = 2.05 μs , positive slew rate = 0.96 V/ μs , settling time = 4.5 μs .

Figure 3



NOTE A: Fall time = 4.25 μs , negative slew rate = 0.46 V/ μs , settling time = 8.5 μs .

Figure 4

TLV5620C, TLV5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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TYPICAL CHARACTERISTICS

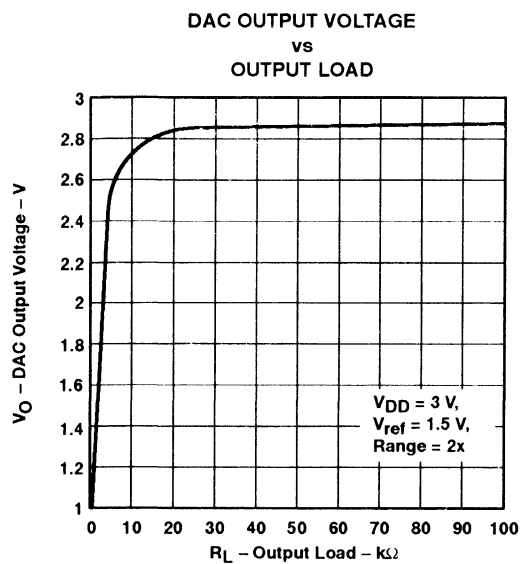


Figure 5

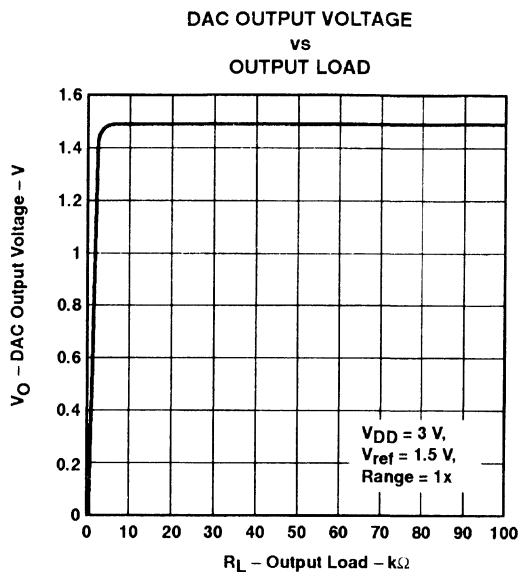


Figure 6

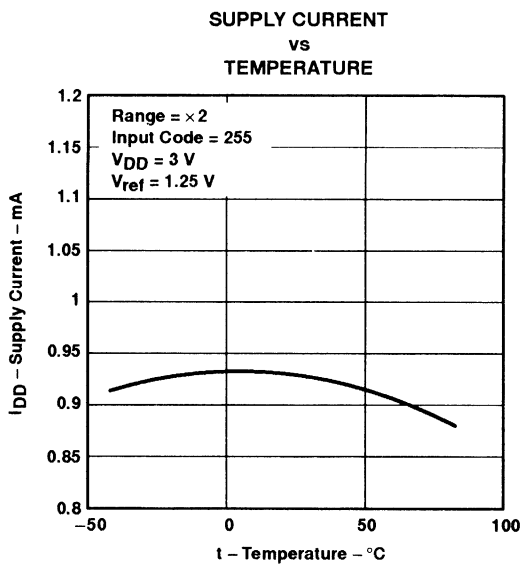
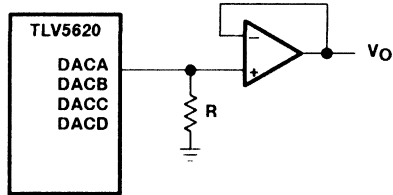


Figure 7

TLV5620C, TLV5620I
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APPLICATION INFORMATION



NOTE A: Resistor $R \geq 10 \text{ k}\Omega$

Figure 8. Output Buffering Scheme

TLV56211

LOW-POWER QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTER

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- 2.7-V to 5.5-V Single-Supply Operation
- Three 8-Bit Voltage Output DACs
- One-Half Power 8-Bit Voltage Output DAC
- Fast Serial Interface . . . 1 MHz Max
- Simple Two-Wire Interface In Single Buffered Mode
- High-Impedance Reference Inputs For Each DAC
- Programmable for 1 or 2 Times Output Range
- Simultaneous-Update Facility In Double-Buffered Mode
- Internal Power-On Reset
- Industry Temperature Range
- Low Power Consumption
- Half-Buffered Output
- Power-Down Mode

applications

- Programmable Voltage Sources
- Digitally-Controlled Amplifiers/Attenuators
- Cordless/Wireless Communications
- Automatic Test Equipment
- Portable Test Equipment
- Process Monitoring and Control
- Signal Synthesis

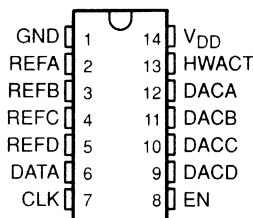
description

The TLV56211 is a quadruple 8-bit voltage output digital-to-analog converter (DAC) with buffered reference inputs (high impedance). The DAC produces an output voltage that ranges between either one or two times the reference voltages and GND, and the DAC is monotonic. The device is simple to use since it operates from a single supply of 2.7 V to 5.5 V. A power-on reset function is incorporated to provide repeatable start-up conditions. A global hardware shut-down terminal and the capability to shut down each individual DAC with software are provided to minimize power consumption.

Digital control of the TLV56211 is over a simple 3-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. A TLV56211 11-bit command word consists of eight bits of data, two DAC select bits, and a range bit for selection between the times one or times two output range. The TLV56211 digital inputs feature Schmitt triggers for high noise immunity. The DAC registers are double buffered which allows a complete set of new values to be written to the device, and then under control of the HWACT signal, all of the DAC outputs are updated simultaneously.

The 14-terminal small-outline (D) package allows digital control of analog functions in space-critical applications. The TLV56211 does not require external trimming. The TLV56211 is characterized for operation from -40°C to 85°C.

**D PACKAGE
(TOP VIEW)**



AVAILABLE OPTIONS

PACKAGE	
T _A	SMALL OUTLINE (D)
-40°C to 85°C	TLV56211D

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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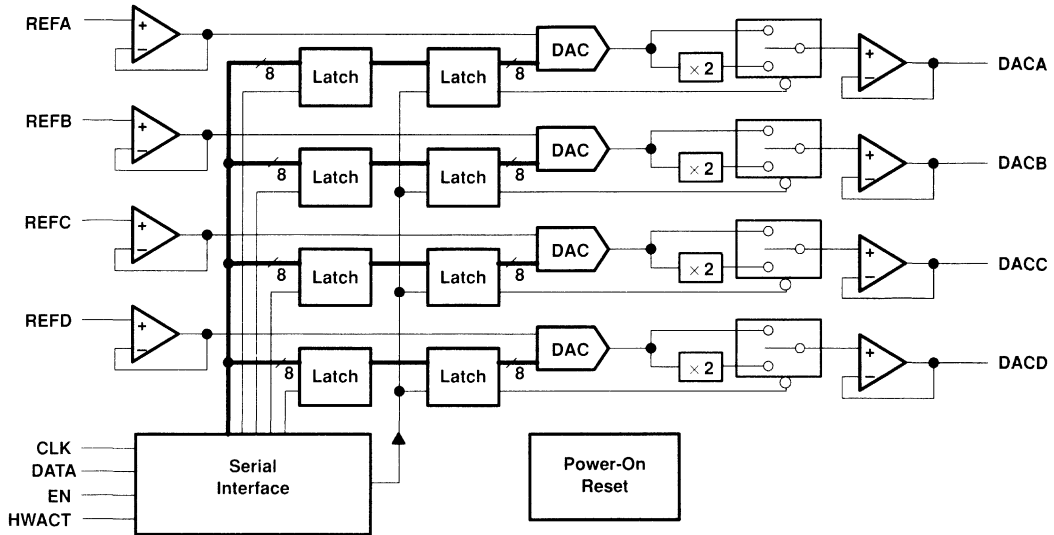
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TLV5621I

LOW-POWER QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTER

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functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CLK	7	I	Serial interface clock, data enters on the negative edge
DACA	12	O	DAC A analog output
DACB	11	O	DAC B analog output
DACC	10	O	DAC C analog output
DACD	9	O	DAC D analog output
DATA	6	I	Serial-interface digital-data input
EN	8	I	Input enable
GND	1		Ground return and reference
HWACT	13	I	Global hardware activate
REFA	2	I	Reference voltage input to DACA
REFB	3	I	Reference voltage input to DACB
REFC	4	I	Reference voltage input to DACC
REFD	5	I	Reference voltage input to DACD
VDD	14		Positive supply voltage

detailed description

The TLV5621 is implemented using four resistor-string DACs. The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 1. One end of each resistor string is connected to GND and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor elements and upon the performance of the output buffer. Because the inputs are buffered, the DACs always present a high-impedance load to the reference source.



TLV5621I

LOW-POWER QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTER

SLAS138B – APRIL 1996 – REVISED FEBRUARY 1997

Each DAC output is buffered by a configurable-gain output amplifier, which can be programmed to times one or times two gain.

On power-up, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(\text{DACA|B|C|D}) = \text{REF} \times \frac{\text{CODE}}{256} \times (1 + \text{RNG bit value})$$

where CODE is in the range 0 to 255 and the range (RNG) bit is a 0 or 1 within the serial control word.

Table 1. Ideal-Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	$(1/256) \times \text{REF} (1+\text{RNG})$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	$(127/256) \times \text{REF} (1+\text{RNG})$
1	0	0	0	0	0	0	0	$(128/256) \times \text{REF} (1+\text{RNG})$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	$(255/256) \times \text{REF} (1+\text{RNG})$

data interface

The data interface has two modes of operation; single and double buffered. Both modes serially clock in bits of data using DATA and CLK whenever EN is high. When EN is low, CLK is disabled and data cannot be loaded into the buffers.

In the single buffered mode, the DAC outputs are updated on the last/twelfth falling edge of CLK, so this mode only requires a two-wire interface with EN tied high (see Figure 1 and Figure 2).

In the double buffered mode (startup default), the outputs of the DACs are updated on the falling edge of the EN strobe (see Figure 3 and Figure 4). This allows multiple devices to share data and clock lines by having only separate EN lines.

single-buffer mode (MODE = 1)

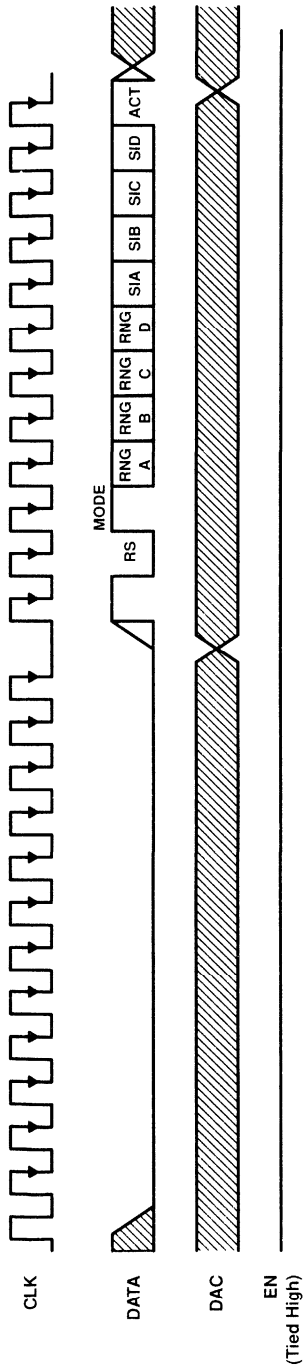
When a two wire interface is used, EN is tied high and the input to the device is always active; therefore, random data can be clocked into the input latch. In order to regain word synchronization, twelve zeros are clocked in as shown in Figure 1, and then a data or control word is clocked in. In Figure 1, the MODE bit is set to one, and a control word is clocked in with the DAC outputs becoming active after the last falling edge of the control word.

Figure 2 shows valid data being written to a DAC, note that CLK is held low while the data is invalid. Data can be written to all four DACs and then the control word is clocked in which sets the MODE bit to 1. At the end of the control word, the data is latched to the inputs of the DACs.

Note that once the MODE bit has been set, it is not possible to clear it, i.e., it is not possible to move from single to double-buffered mode.

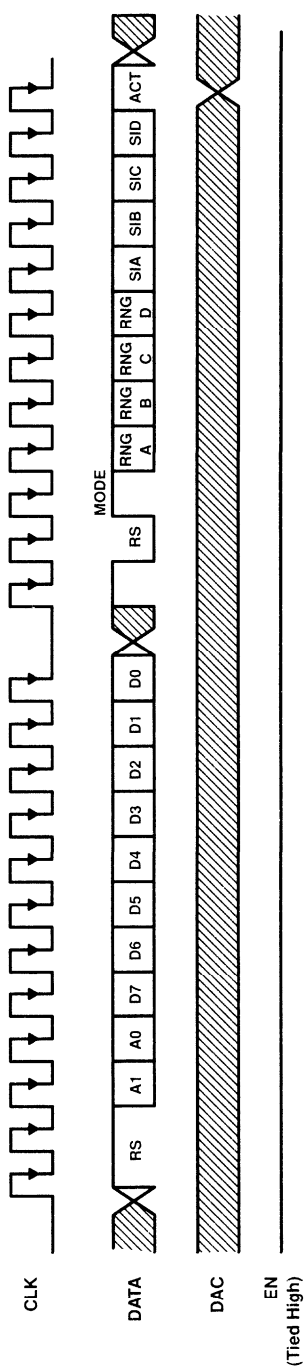
TLV5621I LOW-POWER QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTER

SLAS138B – APRIL 1996 – REVISED FEBRUARY 1997



NOTE A: Twelve zeros enable word synchronization and the output can change after the leading edge of CLK depending on the data in the latches.

Figure 1. Register Write Operation Following Noise or Undefined Levels on DATA or CLK (Single-Buffer Mode)



NOTE A: EN is held high and data is written to a DAC register. The data is latched to the output of the DAC on the falling edge of the last CLK of the control word, where the mode is set.

Figure 2. First Nonzero Write Operation After Startup (EN = High)

TLV56211 LOW-POWER QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTER

SLAS138B – APRIL 1996 – REVISED FEBRUARY 1997

double-buffered mode (MODE = 0)

In this mode, data is only latched to the output of the DACs on the falling edge of the EN strobe. Therefore, all four DACs can be written to before updating their outputs.

Any number of input data blocks can be written with all having the same length. Subsequent data blocks simply overwrite previous ones with the same address until EN goes low.

Multiple data blocks can be written in any sequence provided signal timing limits are met. The negative going edge of EN terminates and latches all data.

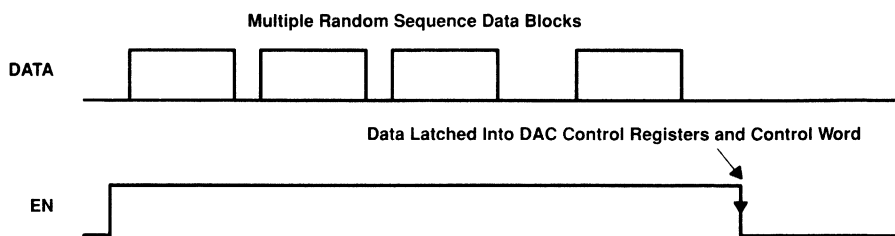
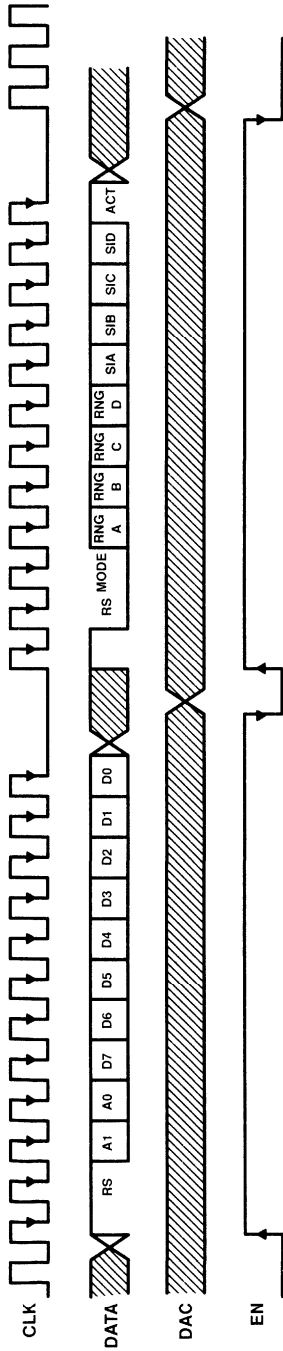


Figure 3. Data and Control Serial Control

TLV56211 LOW-POWER QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTER

SLAS138B – APRIL 1996 – REVISED FEBRUARY 1997



NOTE A: Data is written to the output of a DAC, and the data is latched to the output on the falling edge of EN. A control word then selects double-buffered mode. When the range is changed, the output changes on the falling edge of EN.

Figure 4. First Nonzero Write Operation After Startup

TLV5621I

LOW-POWER QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTER

SLAS138B – APRIL 1996 – REVISED FEBRUARY 1997

control register

The control register contains ten active bits. Four bits are range select bits as on the TLC5620. The register also contains a software shutdown bit (ACT) and four shutdown inhibit bits (SIA, SIB, SIC, SID). The shutdown inhibit bits act on each DAC (DACA through DACD). The mode select bit is used to change between single and double buffered modes. The bits in the control register are listed in Table 2.

Table 2. Control Register Bits

BIT	FUNCTION
MODE	Selection bit for type of interface (see data interface section)
RNG A	Range select bit for DACA, 0 = $\times 1$, 1 = $\times 2$
RNG B	Range select bit for DACB, 0 = $\times 1$, 1 = $\times 2$
RNG C	Range select bit for DACC, 0 = $\times 1$, 1 = $\times 2$
RNG D	Range select bit for DACD, 0 = $\times 1$, 1 = $\times 2$
SIA	Shutdown inhibit bit for DACA
SIB	Shutdown inhibit bit for DACB
SIC	Shutdown inhibit bit for DACC
SID	Shutdown inhibit bit for DACD
ACT	Software shutdown bit

The S_{ix} bits inhibit the actions of the shutdown bits as shown in Table 3. When the ACT bit is 1 or the HWACT signal is high (active), the inhibit bits act as enable bits in inverse logic terms. The ACT software shutdown bit and HWACT (asynchronously acting hardware terminal) are logically ORed together.

This configuration allows any combination of DACs to be shut down to save power.

Table 3. Shutdown Inhibit Bits and HWACT Signal

S _{ix}	ACT	HWACT	DAC _x STATUS
0	0	L	Shutdown (see Note 1)
0	0	H	Shutdown
0	1	L	Shutdown
0	1	H	Active (see Note 1)
1	0	L	Active
1	0	H	Active
1	1	L	Active
1	1	H	Active

NOTE 1: Sense of HWACT terminal and ACT bit were changed from early versions of this specification.

The values of the input address select bits, A0 and A1, and the updated DAC are listed in Table 4.

Table 4. Serial Input Decode

INPUT ADDRESS SELECT BITS		DAC UPDATED
A1	A0	
0	0	DACA
0	1	DACB
1	0	DACC
1	1	DACD



TLV56211

LOW-POWER QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTER

SLAS138B – APRIL 1996 – REVISED FEBRUARY 1997

power-on reset

Power-on reset circuitry is available on the TLV56211. The threshold to trigger a power-on reset is 1.95 V typical (1.4 V min and 2.5 V max). For a power-on reset, all DACs are shut down. The control register bit values and states after a power-on reset are listed in Table 5.

Table 5. Control Register Bit Values and States After Power-On Reset

BIT	VALUE	STATE AFTER POWER-ON RESET
MODE	0	Double buffer mode selected
RNG A	1	Range $\times 2$
RNG B	1	Range $\times 2$
RNG C	1	Range $\times 2$
RNG D	1	Range $\times 2$
SIA	0	Shutdown affects DACA according to ACT state
SIB	0	Shutdown affects DACB according to ACT state
SIC	0	Shutdown affects DACC according to ACT state
SID	0	Shutdown affects DACD according to ACT state
ACT	0	DACs in shutdown state

TLV5621I

LOW-POWER QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTER

SLAS138B – APRIL 1996 – REVISED FEBRUARY 1997

linearity, offset, and gain error using single-end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 5.

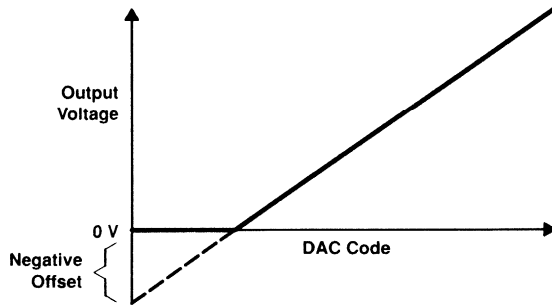
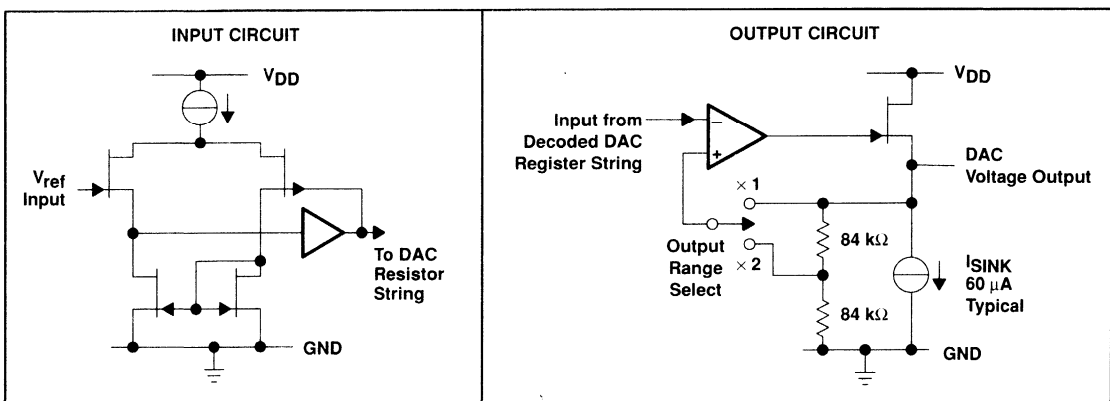


Figure 5. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. The code is calculated from the maximum specification for the negative offset.

equivalent inputs and outputs



TLV5621I

LOW-POWER QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTER

SLAS138B – APRIL 1996 – REVISED FEBRUARY 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage ($V_{DD} - GND$)	7 V
Digital input voltage range	$GND - 0.3 V$ to $V_{DD} + 0.3 V$
Reference input voltage range, V_{ID}	$GND - 0.3 V$ to $V_{DD} + 0.3 V$
Operating free-air temperature range, T_A	$-40^{\circ}C$ to $85^{\circ}C$
Storage temperature range, T_{stg}	$-50^{\circ}C$ to $150^{\circ}C$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	$260^{\circ}C$

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (see Note 2)	2.7	3.3	5.5	V
High-level digital input voltage, V_{IH}	0.8 V_{DD}			V
Low-level digital input voltage, V_{IL}	0.2 V_{DD}			V
Reference voltage, V_{ref} [A B C D], x1 gain	GND		$V_{DD} - 1.5$	V
Load resistance, R_L	10			k Ω
Setup time, data input, $t_{su}(DATA-CLK)$ (see Figure 6)	50			ns
Hold time, data input valid after $CLK\downarrow$, $t_h(DATA-CLK)$ (see Figure 6)	50			ns
Setup time, $CLK\downarrow$ to $EN\downarrow$, $t_{su}(CLK-EN)$ (see Figure 7)	100			ns
Setup time, $EN\uparrow$ to $CLK\downarrow$, $t_{su}(EN-CLK)$ (see Figure 7) (see Note 3)	100			ns
Pulse duration, EN low, $t_w(EN)$ (see Figure 7) (see Note 3)	200			ns
Pulse duration, CLK high, $t_w(CLK)$ (see Figure 6) (see Note 3)	400			ns
CLK frequency	1			MHz
Operating free-air temperature, T_A	-40	85		$^{\circ}C$

- NOTES: 2. The device operates over the supply voltage range of 2.7 V to 5.5 V. Over this voltage range the device responds correctly to data input by changing the output voltage but conversion accuracy is not specified over this extended range.
3. This is specified by design but is not production tested.

TLV56211

LOW-POWER QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTER

SLAS138B – APRIL 1996 – REVISED FEBRUARY 1997

**electrical characteristics over recommended operating free-air temperature range,
 $V_{DD} = 3\text{ V to }3.6\text{ V}$, $V_{ref} = 1.25\text{ V}$, $GND = 0\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $\times 1$ gain output range
(unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{Omax}	Maximum full-scale output voltage	$V_{ref} = 1.5\text{ V}$, open circuit output, $\times 2$ gain	$V_{DD} - 100$	2		mV
$I_{IH}(\text{digital})$	High-level digital input current	$V_I = V_{DD}$			± 10	μA
$I_{IL}(\text{digital})$	Low-level digital input current	$V_I = 0\text{ V}$			± 10	μA
$I_{O}(\text{sink})$	Output sink current, DACA	DAC code 0	5			μA
	Output sink current, DACB, DACC, DACD	DAC code 0	20			μA
$I_{O}(\text{source})$	Output source current	Each DAC output, DAC code 255	1			mA
C_i	Input capacitance			15		pF
	Reference input capacitance	A, B, C, D inputs		15		
I_{DD}	Supply current	$V_{DD} = 3.6\text{ V}$		1	1.5	mA
		$V_{DD} = 5\text{ V}$		1	1.5	mA
$I_{DD}(\text{active})$	Supply current, one low power DAC active	$V_{DD} = 3.6\text{ V}$, See Note 4		150	250	μA
$I_{DD}(\text{shutdown})$	Supply current, all DACs shut down	$V_{DD} = 3.6\text{ V}$, See Note 4		50	100	μA
I_{ref}	Reference input current	A, B, C, D inputs			± 10	μA
E_L	Integral linearity error	$V_{ref} = 1.25\text{ V}$, $\times 2$ gain, See Notes 5 and 13			± 1	LSB
E_D	Differential linearity error	$V_{ref} = 1.25\text{ V}$, $\times 2$ gain, See Notes 6 and 13		± 0.1	± 0.9	LSB
E_{ZS}	Zero-scale error	$V_{ref} = 1.25\text{ V}$, $\times 2$ gain, See Note 7	0		30	mV
	Zero-scale error temperature coefficient	$V_{ref} = 1.25\text{ V}$, $\times 2$ gain, See Note 8		10		$\mu\text{V}/^\circ\text{C}$
	Zero-scale error supply rejection			2		mV/V
E_{FS}	Full-scale error	$V_{ref} = 1.25\text{ V}$, $\times 2$ gain, See Note 9			± 60	mV
	Full-scale error temperature coefficient	$V_{ref} = 1.25\text{ V}$, $\times 2$ gain, See Note 10		± 25		$\mu\text{V}/^\circ\text{C}$
	Full-scale error supply rejection			2		mV/V
PSRR	Power-supply sensitivity	See Notes 11 and 12		0.5		mV/V
	Feedback resistor network resistance			168		k Ω

- NOTES: 4. This is measured with no load (open circuit output), $V_{ref} = 1.25\text{ V}$, range = $\times 2$.
5. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
6. Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
7. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
8. Zero-scale error temperature coefficient is given by: $ZSETC = [ZSE(T_{max}) - ZSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
9. Full-scale error is the deviation from the ideal full-scale output ($V_{ref} - 1\text{ LSB}$) with an output load of 10 k Ω .
10. Full-scale temperature coefficient is given by: $FSETC = [FSE(T_{max}) - FSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
11. Zero-scale error rejection ratio (ZSE-RR) is measured by varying the V_{DD} voltage from 4.5 V to 5.5 V dc and measuring the effect of this signal on the zero-code output voltage.
12. Full-scale error rejection ratio (FSE-RR) is measured by varying the V_{DD} voltage from 3 V to 3.6 V dc and measuring the effect of this signal on the full-scale output voltage.
13. Linearity is only specified for DAC codes 1 through 255.



TLV56211

LOW-POWER QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTER

SLAS138B – APRIL 1996 – REVISED FEBRUARY 1997

operating characteristics over recommended operating free-air temperature range,
 $V_{DD} = 3\text{ V to }3.6\text{ V}$, $V_{ref} = 1.25\text{ V}$, $GND = 0\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $\times 1$ gain output range
 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate, rising (DACA)			0.8		V/ μ s
Output slew rate, falling (DACA)			0.5		V/ μ s
Output slew rate (DACB, DACC, DACD)			1		V/ μ s
Output settling time, rising (DACA)	To 1/2 LSB, $V_{DD} = 3\text{ V}$		20		μ s
Output settling time, falling (DACA)	To 1/2 LSB, $V_{DD} = 3\text{ V}$		75		μ s
Output settling time, rising (DACB, DACC, DACD)	To 1/2 LSB, $V_{DD} = 3\text{ V}$		10		μ s
Output settling time, falling (DACB, DACC, DACD)	To 1/2 LSB, $V_{DD} = 3\text{ V}$		75		μ s
Output settling time, HWACT or ACT \uparrow to output volts (DACA) (see Note 14)	To 1/2 LSB, $V_{DD} = 3\text{ V}$		40	120 \uparrow	μ s
Output settling time, HWACT or ACT \uparrow to output volts (DACB, DACC, DACD) (see Note 14)	To 1/2 LSB, $V_{DD} = 3\text{ V}$		25	75 \uparrow	μ s
Large-signal bandwidth	Measured at -3 dB point		100		kHz
Digital crosstalk	CLK = 1-MHz square wave measured at DACA–DACD		-50		dB
Reference feedthrough	A, B, C, D inputs. See Note 15		-60		dB
Channel-to-channel isolation	A, B, C, D inputs, See Note 16		-60		dB
Channel-to-channel isolation when in shutdown	A, B, C, D inputs		-40		dB
Reference bandwidth (DACA)	See Note 17		20		kHz
Reference bandwidth (DACB, DACC, DACD)	See Note 17		100		kHz

\uparrow This is specified by characterization but is not production tested.

NOTES: 14. The ACT bit is latched on EN \downarrow .

15. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
16. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
17. Reference bandwidth is the -3 dB bandwidth with an ideal input at $V_{ref} = 1.25\text{ V}$ dc + 2 V_{pp} and with a digital input code of full-scale (range set to $\times 1$ and $V_{DD} = 5\text{ V}$).

TLV5621I LOW-POWER QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTER

SLAS138B – APRIL 1996 – REVISED FEBRUARY 1997

PARAMETER MEASUREMENT INFORMATION

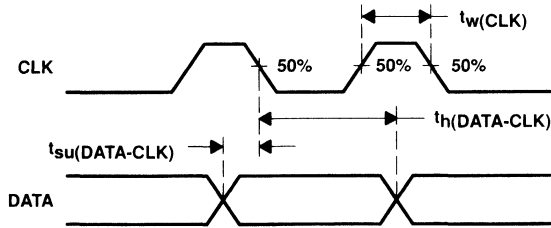


Figure 6. Timing of DATA Relative to CLK

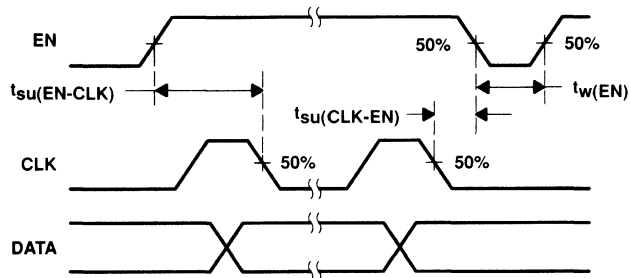


Figure 7. Timing of CLK Relative to EN

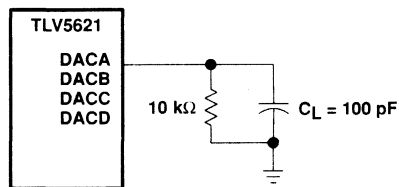


Figure 8. Slewing Settling Time and Linearity Measurements

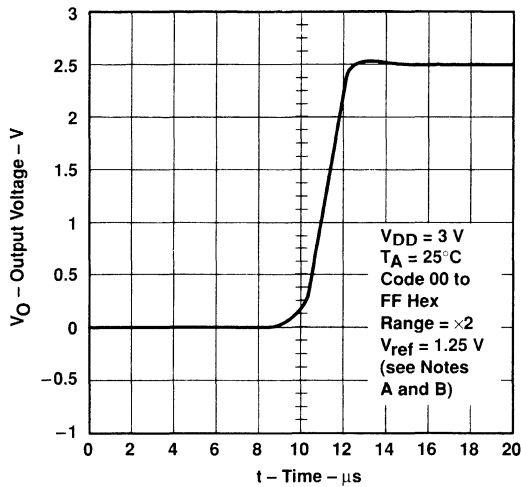
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LOW-POWER QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTER

SLAS138B – APRIL 1996 – REVISED FEBRUARY 1997

TYPICAL CHARACTERISTICS

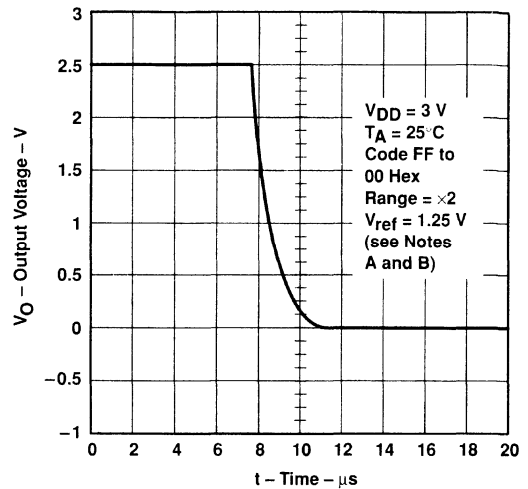
POSITIVE RISE TIME AND SETTLING TIME



NOTES: A. Rise time = 2.05 μ s, positive slew rate = 0.96 V/ μ s, settling time = 4.5 μ s.
B. For DACB, DACC, and DACD

Figure 9

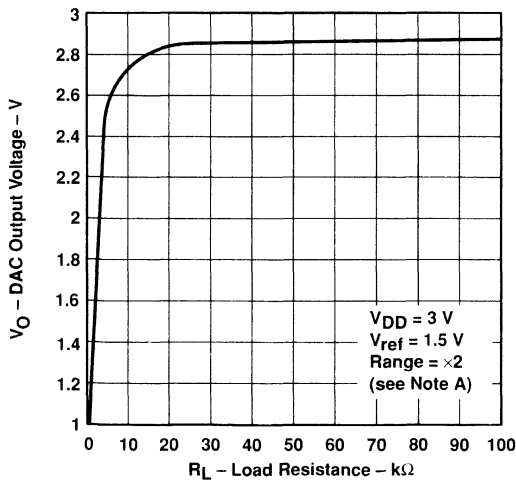
NEGATIVE FALL TIME AND SETTLING TIME



NOTES: A. Fall time = 4.25 μ s, negative slew rate = 0.46 V/ μ s, settling time = 8.5 μ s.
B. For DACB, DACC, and DACD

Figure 10

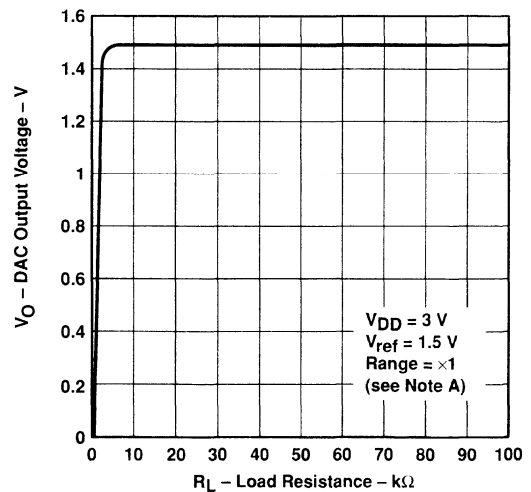
**DAC OUTPUT VOLTAGE
vs
LOAD RESISTANCE**



NOTE A: For DACB, DACC, and DACD

Figure 11

**DAC OUTPUT VOLTAGE
vs
LOAD RESISTANCE**



NOTE A: For DACB, DACC, and DACD

Figure 12

TLV5621I LOW-POWER QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTER

SLAS138B – APRIL 1996 – REVISED FEBRUARY 1997

TYPICAL CHARACTERISTICS

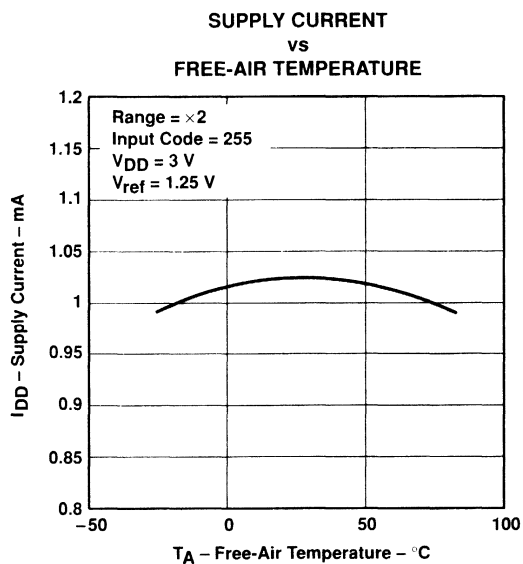
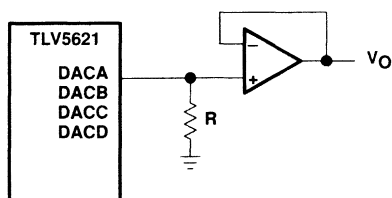


Figure 13

APPLICATION INFORMATION



NOTE A: Resistor $R \geq 10\text{ k}\Omega$

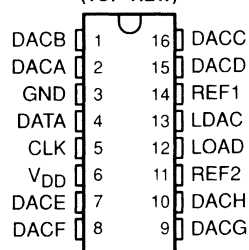
Figure 14. Output Buffering Scheme

TLV5628C, TLV5628I OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS108B – JANUARY 1995 – REVISED APRIL 1997

- Eight 8-Bit Voltage Output DACs
- 3-V Single Supply Operation
- Serial Interface
- High-Impedance Reference Inputs
- Programmable for 1 or 2 Times Output Range
- Simultaneous Update Facility
- Internal Power-On Reset
- Low Power Consumption
- Half-Buffered Output

DW OR N PACKAGE
(TOP VIEW)



applications

- Programmable Voltage Sources
- Digitally Controlled Amplifiers/Attenuators
- Mobile Communications
- Automatic Test Equipment
- Process Monitoring and Control
- Signal Synthesis

description

The TLV5628C and TLV5628I are octal 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that varies between one or two times the reference voltages and GND, and the DACs are monotonic. The device is simple to use, running from a single supply of 3 to 3.6 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLV5628C and TLV5628I is over a simple three-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 12-bit command word comprises eight bits of data, three DAC select bits, and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs are updated simultaneously through control of LDAC. The digital inputs feature Schmitt triggers for high noise immunity.

The 16-terminal small-outline DW package allows digital control of analog functions in space-critical applications. The TLV5628C is characterized for operation from 0°C to 70°C. The TLV5628I is characterized for operation from -40°C to 85°C. The TLV5628C and TLV5628I do not require external trimming.

AVAILABLE OPTIONS

T _A	PACKAGE	
	SMALL OUTLINE (DW)	PLASTIC DIP (N)
0°C to 70°C	TLV5628CDW	TLV5628CN
-40°C to 85°C	TLV5628IDW	TLV5628IN

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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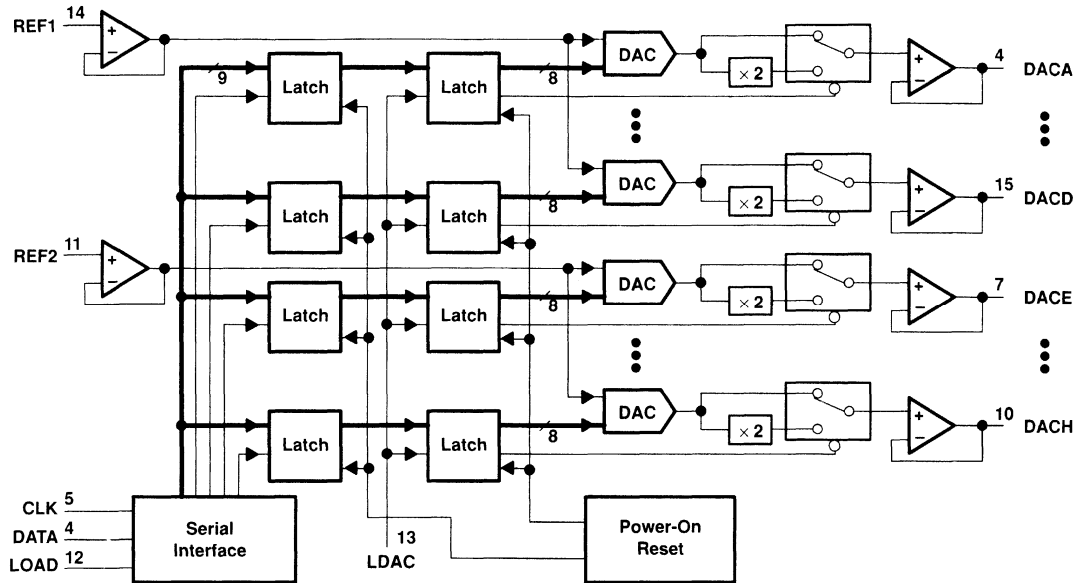
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3-231

TLV5628C, TLV5628I OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS108B – JANUARY 1995 – REVISED APRIL 1997

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CLK	5	I	Serial interface clock. The input digital data is shifted into the serial interface register on the falling edge of the clock applied to the CLK terminal.
DACA	2	O	DAC A analog output
DACB	1	O	DAC B analog output
DACC	16	O	DAC C analog output
DACD	15	O	DAC D analog output
DACE	7	O	DAC E analog output
DACF	8	O	DAC F analog output
DACG	9	O	DAC G analog output
DACH	10	O	DAC H analog output
DATA	4	I	Serial interface digital data input. The digital code for the DAC is clocked into the serial interface register serially. Each data bit is clocked into the register on the falling edge of the clock signal.
GND	3	I	Ground return and reference terminal
LDAC	13	I	Load DAC. When this signal is high, no DAC output updates occur when the input digital data is read into the serial interface. The DAC outputs are only updated when LDAC is taken from high to low.
LOAD	12	I	Serial Interface load control. When the LDAC terminal is low, the falling edge of the LOAD signal latches the digital data into the output latch and immediately produces the analog voltage at the DAC output terminal.
REF1	14	I	Reference voltage input to DAC A B C D. This voltage defines the output analog range.
REF2	11	I	Reference voltage input to DAC E F G H. This voltage defines the analog output range.
VDD	6	I	Positive supply voltage



TLV5628C, TLV5628I

OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS108B – JANUARY 1995 – REVISED APRIL 1997

detailed description

The TLV5620 is implemented using four resistor-string DACs. The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 1. One end of each resistor string is connected to GND and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor segments and upon the performance of the output buffer. Since the inputs are buffered, the DACs always presents a high-impedance load to the reference source.

Each DAC output is buffered by a configurable-gain output amplifier, that can be programmed to times 1 or times 2 gain.

On power up, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_{O(DACA|B|C|D)} = REF \times \frac{CODE}{256} \times (1 + RNG \text{ bit value})$$

where CODE is in the range 0 to 255 and the range (RNG) bit is a 0 or 1 within the serial control word.

Table 1. Ideal-Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	$(1/256) \times REF (1+RNG)$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	$(127/256) \times REF (1+RNG)$
1	0	0	0	0	0	0	0	$(128/256) \times REF (1+RNG)$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	$(255/256) \times REF (1+RNG)$

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial input register to the selected DAC as shown in Figure 1. When LDAC is low, the selected DAC output voltage is updated when LOAD goes low. When LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered MSB first. Data transfers using two 8-clock-cycle periods are shown in Figures 3 and 4.



TLV5628C, TLV5628I OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS108B – JANUARY 1995 – REVISED APRIL 1997

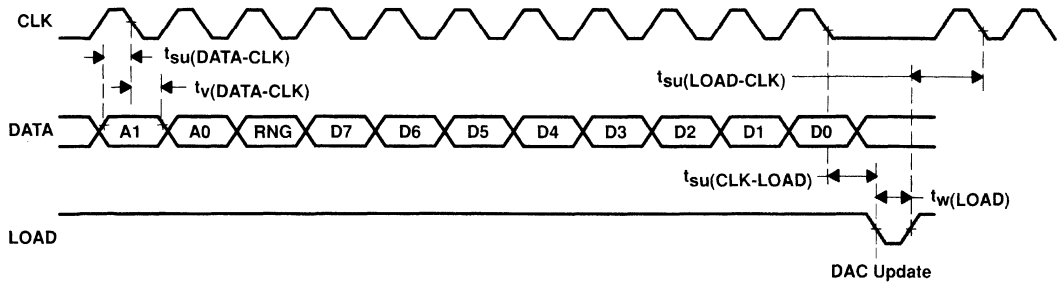


Figure 1. LOAD-Controlled Update (LDAC = Low)

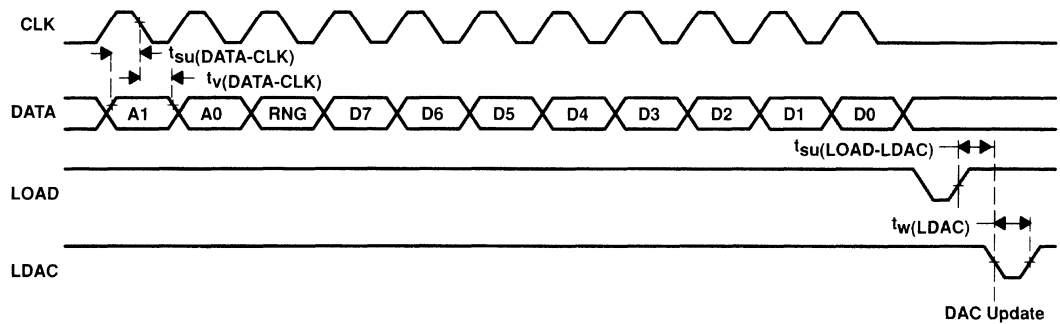


Figure 2. LDAC-Controlled Update

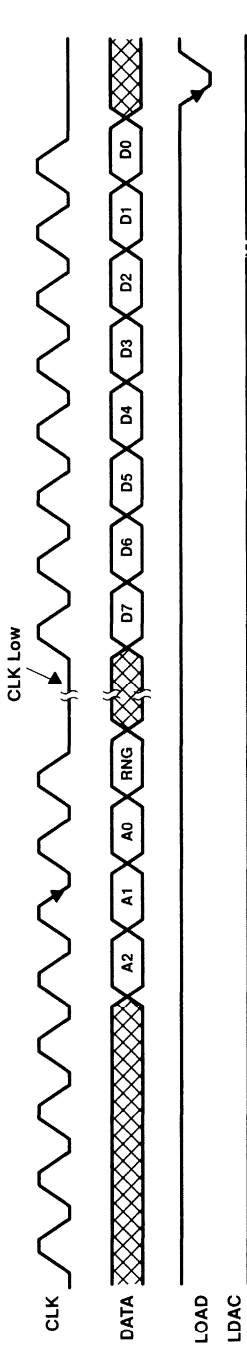


Figure 3. Load-Controlled Update Using 8-Bit Serial Word (LDAC = Low)

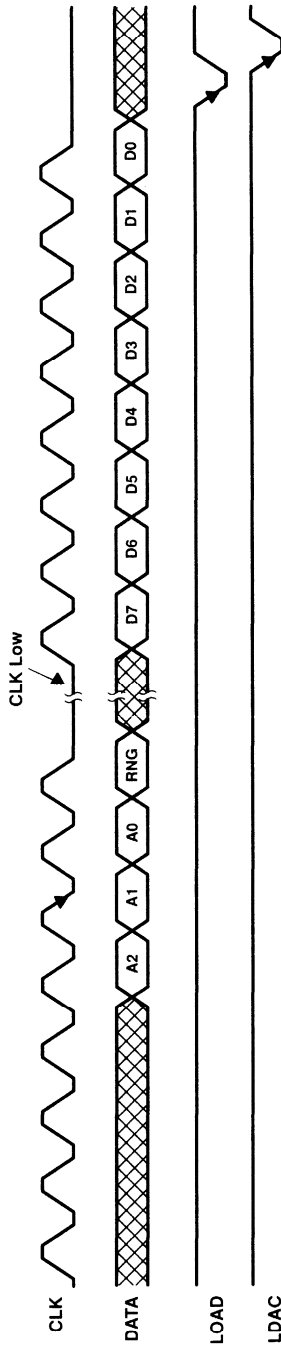


Figure 4. LDAC-Controlled Update Using 8-Bit Serial Word

TLV5628C, TLV5628I OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS108B – JANUARY 1995 – REVISED APRIL 1997

data interface (continued)

Table 2 lists the A2, A1, and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = low, the output range is between the applied reference voltage and GND, and when RNG = high, the range is between twice the applied reference voltage and GND.

Table 2. Serial Input Decode

A2	A1	A0	DAC UPDATED
0	0	0	DACA
0	0	1	DACB
0	1	0	DACC
0	1	1	DACD
1	0	0	DACE
1	0	1	DACF
1	1	0	DACG
1	1	1	DACH

linearity, offset, and gain error

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset voltage, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier, therefore, attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 5.

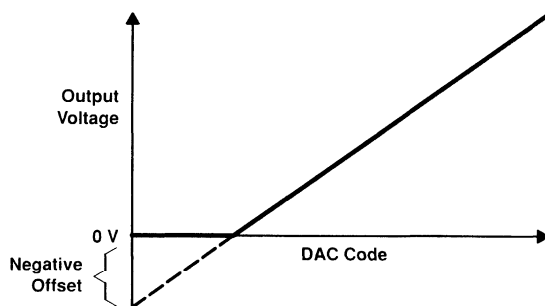


Figure 5. Effect of Negative Offset (Single Supply)

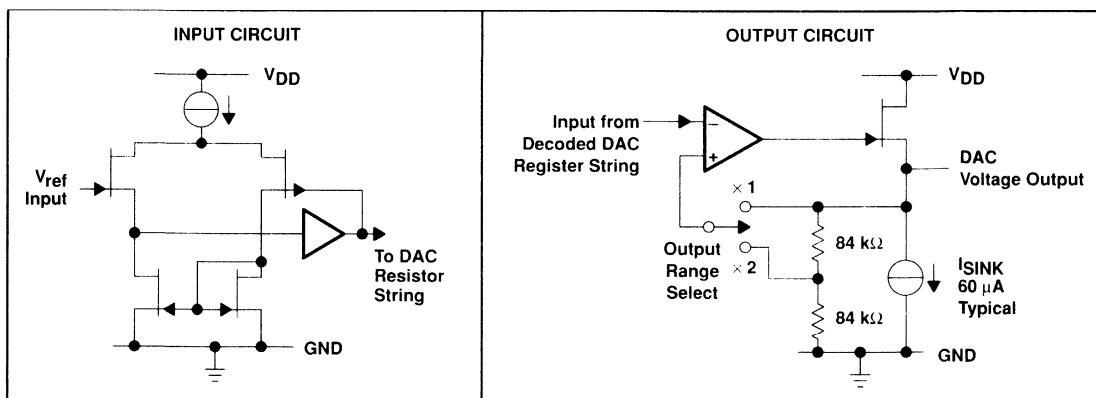
The offset error, not the linearity error, produces the breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below ground.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. The code is calculated from the maximum specification for the negative offset.

TLV5628C, TLV5628I OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS108B – JANUARY 1995 – REVISED APRIL 1997

equivalent inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage ($V_{DD} - GND$)	7 V
Digital input voltage range, V_{ID}	$GND - 0.3 V$ to $V_{DD} + 0.3 V$
Reference input voltage range	$GND - 0.3 V$ to $V_{DD} + 0.3 V$
Operating free-air temperature range, T_A : TLV5628C	$0^{\circ}C$ to $70^{\circ}C$
TLV5628I	$-40^{\circ}C$ to $85^{\circ}C$
Storage temperature range, T_{stg}	$-50^{\circ}C$ to $150^{\circ}C$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	$230^{\circ}C$

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	2.7	3.3	5.25	V
High-level input voltage, V_{IH}	$0.8 V_{DD}$			V
Low-level input voltage, V_{IL}			0.8	V
Reference voltage, V_{ref} [A B C D E F G H], X1 gain			$V_{DD} - 1.5$	V
Load resistance, R_L	10			k Ω
Setup time, data input, $t_{su}(DATA-CLK)$ (see Figures 1 and 2)	50			ns
Valid time, data input valid after $CLK\downarrow$, $t_v(DATA-CLK)$ (see Figures 1 and 2)	50			ns
Setup time, CLK eleventh falling edge to $LOAD$, $t_{su}(CLK-LOAD)$ (see Figure 1)	50			ns
Setup time, $LOAD\uparrow$ to $CLK\downarrow$, $t_{su}(LOAD-CLK)$ (see Figure 1)	50			ns
Pulse duration, $LOAD$, $t_w(LOAD)$ (see Figure 1)	250			ns
Pulse duration, LDAC, $t_w(LDAC)$ (see Figure 2)	250			ns
Setup time, $LOAD\uparrow$ to $LDAC\downarrow$, $t_{su}(LOAD-LDAC)$ (see Figure 2)	0			ns
CLK frequency			1	MHz
Operating free-air temperature, T_A	TLV5628C	0	70	$^{\circ}C$
	TLV5628I	-40	85	$^{\circ}C$



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TLV5628C, TLV5628I

OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS108B – JANUARY 1995 – REVISED APRIL 1997

**electrical characteristics over recommended operating free-air temperature range,
V_{DD} = 3 V to 3.6 V, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{IH}	High-level input current	V _I = V _{DD}			±10	μA
I _{IL}	Low-level input current	V _I = 0 V			±10	μA
I _{O(sink)}	Output sink current	Each DAC output	20			μA
I _{O(source)}	Output source current		1			mA
C _i	Input capacitance			15		pF
	Reference input capacitance			15		
I _{DD}	Supply current	V _{DD} = 3.3 V			4	mA
I _{ref}	Reference input current	V _{DD} = 3.3 V, V _{ref} = 1.5 V			±10	μA
E _L	Linearity error (end point corrected)	V _{ref} = 1.25 V, × 2 gain, See Note 1			±1	LSB
E _D	Differential linearity error	V _{ref} = 1.25 V, × 2 gain, See Note 2			±0.9	LSB
E _{ZS}	Zero-scale error	V _{ref} = 1.25 V, × 2 gain, See Note 3	0		30	mV
	Zero-scale error temperature coefficient	V _{ref} = 1.25 V, × 2 gain, See Note 4		10		
E _{FS}	Full-scale error	V _{ref} = 1.25 V, × 2 gain, See Note 5			±60	mV
	Full-scale error temperature coefficient	V _{ref} = 1.25 V, × 2 gain, See Note 6		±25		
PSRR	Power supply sensitivity	See Notes 7 and 8		0.5		mV/V

- NOTES: 1. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero-scale and full scale (excluding the effects of zero code and full-scale errors).
2. Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
4. Zero-scale error temperature coefficient is given by: $ZSETC = [ZSE(T_{max}) - ZSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
5. Full-scale error is the deviation from the ideal full-scale output (V_{ref} - 1 LSB) with an output load of 10 kΩ.
6. Full-scale error temperature coefficient is given by: $FSETC = [FSE(T_{max}) - FSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
7. Zero-scale error rejection ratio (ZSE-RR) is measured by varying the V_{DD} voltage from 4.5 V to 5.5 V dc and measuring the effect of this signal on the zero-code output voltage.
8. Full-scale error rejection ratio (FSE-RR) is measured by varying the V_{DD} voltage from 3 V to 3.6 V dc and measuring the effect of this signal on the full-scale output voltage.

**operating characteristics over recommended operating free-air temperature range,
V_{DD} = 3 V to 3.6 V, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)**

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	C _L = 100 pF, R _L = 10 kΩ		1		V/μs
Output settling time	To ±0.5 LSB, C _L = 100 pF, R _L = 10 kΩ, See Note 9		10		μs
Large-signal bandwidth	Measured at -3 dB point		100		kHz
Digital crosstalk	CLK = 1-MHz square wave measured at DACA-DACH		-50		dB
Reference feedthrough	See Note 10		-60		dB
Channel-to-channel isolation	See Note 11		-60		dB
Reference input bandwidth	See Note 12		100		kHz

- NOTES: 9. Settling time is the time between a LOAD falling edge and the DAC output reaching full-scale voltage within ±0.5 LSB starting from an initial output voltage equal to zero.
10. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
11. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
12. Reference bandwidth is a -3 dB bandwidth with an input at V_{ref} = 1.25 V dc + 2 V_{pp} and with a full-scale digital input code.



TLV5628C, TLV5628I OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS108B – JANUARY 1995 – REVISED APRIL 1997

PARAMETER MEASUREMENT INFORMATION

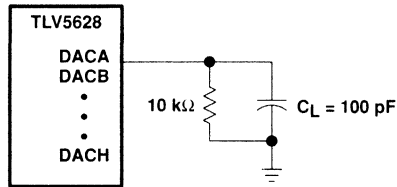
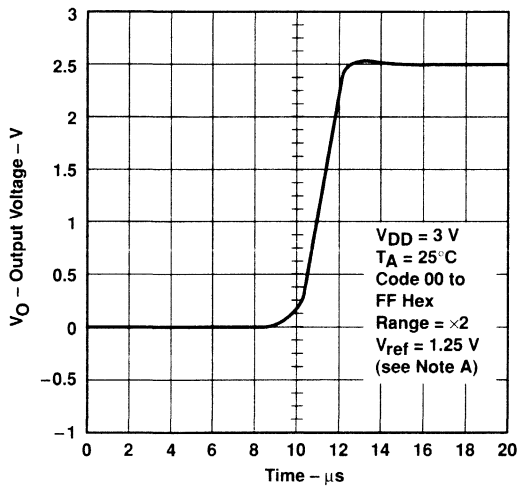


Figure 6. Slew, Settling Time, and Linearity Measurements

TYPICAL CHARACTERISTICS

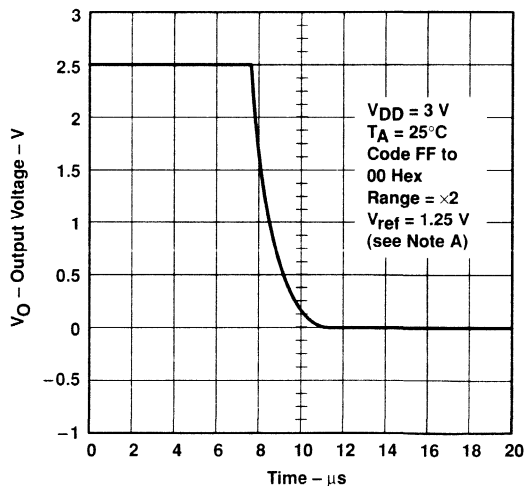
POSITIVE RISE TIME AND SETTLING TIME



NOTE A: Rise time = 2.05 μs, positive slew rate = 0.96 V/μs, settling time = 4.5 μs.

Figure 7

NEGATIVE FALL TIME AND SETTLING TIME



NOTE A: Fall time = 4.25 μs, negative slew rate = 0.46 V/μs, settling time = 8.5 μs.

Figure 8



TLV5628C, TLV5628I OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS108B – JANUARY 1995 – REVISED APRIL 1997

TYPICAL CHARACTERISTICS

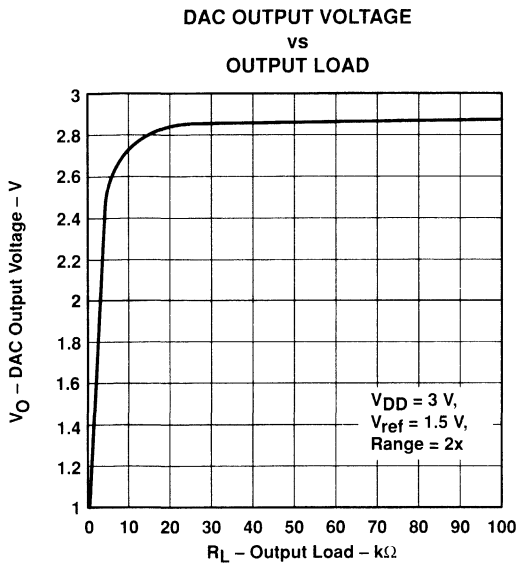


Figure 9

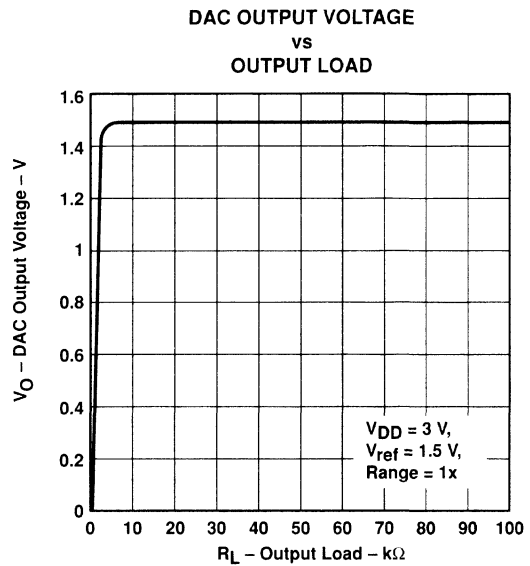


Figure 10

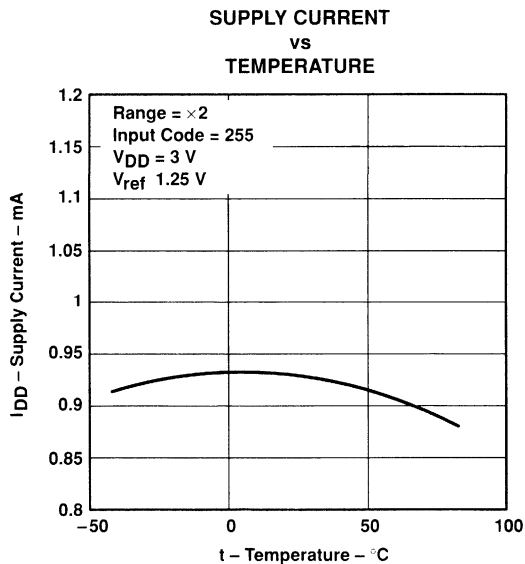
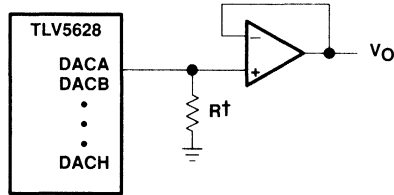


Figure 11

TLV5628C, TLV5628I
OCTAL 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS108B – JANUARY 1995 – REVISED APRIL 1997

APPLICATION INFORMATION



† Resistor $R \geq 10 \text{ k}\Omega$

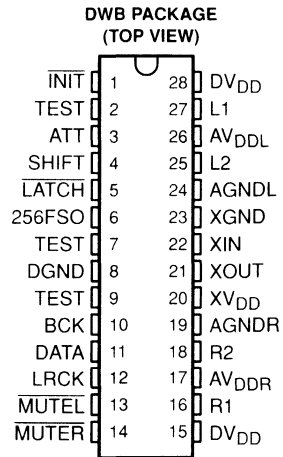
Figure 12. Output Buffering Scheme

TMS57014A

DUAL AUDIO DIGITAL-TO-ANALOG CONVERTER

SLAS077D – SEPTEMBER 1993 – REVISED NOVEMBER 1995

- Single 5-V Power Supply
- Sample Rates (F_s) up to 48 kHz
- 18-Bit Resolution
- Pulse-Width-Modulation (PWM) Output
- De-emphasis Filter for Sample Rates of 32, 37.8, 44.1, and 48 kHz
- Mute With Zero-Data-Detect Flags
- Digital Attenuation to –60 dB
- Total Harmonic Distortion of 0.004% Maximum
- Total-Channel Dynamic Range of 96 dB Minimum
- Serial-Port Interface
- Differential Architecture
- CMOS Technology
- 2s-Complement Data Format



description

The TMS57014A is a stereo oversampled-sigma-delta digital-to-analog converter (DAC) designed for use in systems such as compact disks, digital audio tapes, multimedia, and video cassette recorders. The device provides high-resolution signal conversion. This device consists of two identical synchronous conversion paths for left and right audio channels. Other overhead functions provide on-chip timing and control.

Additional features include muting, attenuation, de-emphasis, and zero-data detection. Control words (16-bit) from a host controller or processor implement these functions.

The TMS57014A is characterized for operation from 0°C to 70°C.

AVAILABLE OPTION†

T _A	PACKAGE
	SMALL OUTLINE (DWB)
0 C to 70 C	TMS57014ADWBLE

† Available on tape and reel (LE) only.



This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

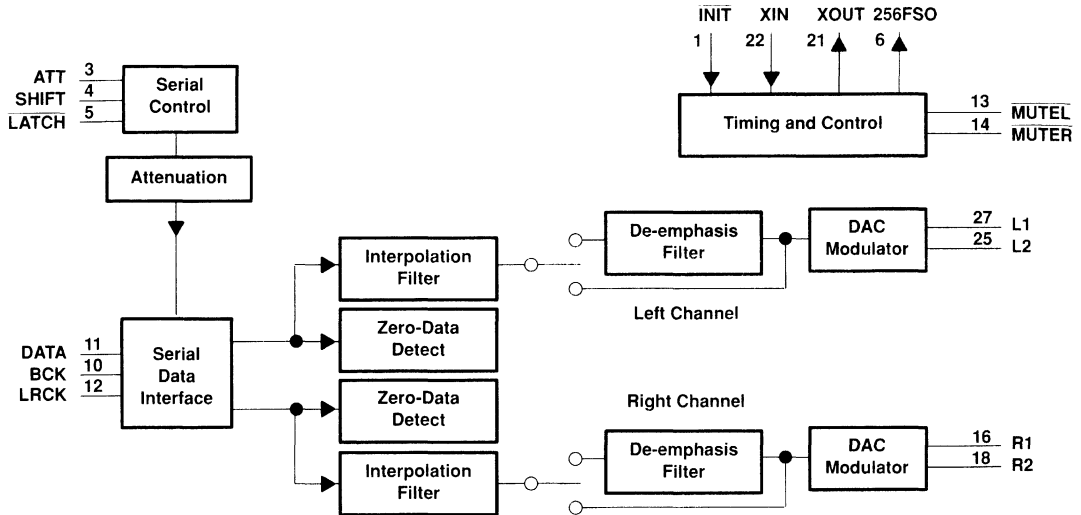
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functional block diagram



TMS57014A

DUAL AUDIO DIGITAL-TO-ANALOG CONVERTER

SLAS077D – SEPTEMBER 1993 – REVISED NOVEMBER 1995

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ATT	3	I	Serial control data. ATT is a 16-bit word configured as LSB first (see Tables 2, 3, and 4).
AVDDL	26	I	Analog power supply (left channel)
AVDDR	17	I	Analog power supply (right channel)
AGNDL	24	I	Analog ground (left channel)
AGNDR	19	I	Analog ground (right channel)
BCK	10	I	Bit clock input. BCK clocks serial audio data into the device.
DATA	11	I	Audio data input. DATA can be configured as 16 or 18 bits with MSB or LSB first. DATA is 2s complement.
DVDD	15, 28	I	Digital supply
DGND	8	I	Digital ground
INIT	1	I	Reset. When $\overline{\text{INIT}}$ is brought low, the device is reset. The device is activated on the rising edge of $\overline{\text{INIT}}$. The LRCK signal must be applied to the device for a reset to occur.
LATCH	5	I	Serial-control data latch. Control data loads into the internal registers when LATCH is brought low.
LRCK	12	I	Left/right clock. LRCK signifies whether the serial data is associated with the left-channel DAC (when high) or the right-channel DAC (when low).
MUTEL	13	O	Left-channel mute flag active. When the left channel is mute or the data through the channel remains at zero for the system-register selected time, MUTEL is brought low.
MUTER	14	O	Right-channel mute flag active. When the right channel is mute or the data through the channel remains at zero for the system-register selected time, MUTER is brought low.
L1	27	O	Left PWM output 1
L2	25	O	Left PWM output 2
R1	16	O	Right PWM output 1
R2	18	O	Right PWM output 2
SHIFT	4	I	Shift clock. SHIFT clocks the control data into the internal registers.
TEST	2, 7, 9	I	All TEST inputs should be tied low.
XIN	22	I	Master clock in. XIN derives all the key logic signals of the device. XIN runs at $512 F_s$, where F_s is the sample rate.
XOUT	21	O	Master clock out
XVDD	20	I	Power supply for clock section
XGND	23	I	Ground for clock section
256FSO	6	O	System clock out. 256FSO reflects the master clock input divided by 2. The rate is $256F_s$, where F_s is the sample rate.

detailed description

The TMS57014A incorporates an interpolation impulse-response filter (FIR) and oversampled modulator. The pulse-width modulation (PWM) digital output feeds into an external low-pass filter to recover the analog audio signal.

Two control registers configure the device, the attenuation register controls the attenuation range and the system register controls additional functions (see register set section).

reset/initialization

When $\overline{\text{INIT}}$ is brought low, an internal reset signal becomes active approximately 120 cycles of the sampling frequency (F_s) after the falling edge of $\overline{\text{INIT}}$. Under this condition, all internal circuits are initialized and the PWM output is held at zero data (50% duty cycle). When $\overline{\text{INIT}}$ is brought high, the internal reset signal goes inactive for a maximum of five LRCK periods after the rising edge of $\overline{\text{INIT}}$. At this point, internal clocks are synchronous with LRCK and the PWM output is valid (see Figure 1). The LRCK signal must be applied for proper initialization.



TMS57014A DUAL AUDIO DIGITAL-TO-ANALOG CONVERTER

SLAS077D – SEPTEMBER 1993 – REVISED NOVEMBER 1995

reset/initialization (continued)

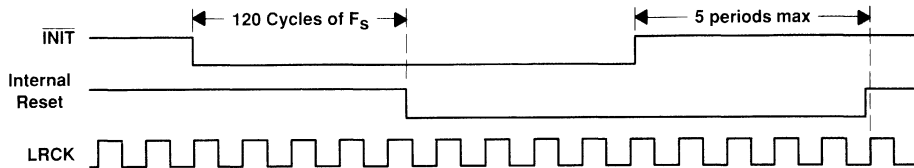


Figure 1. Reset Timing Relationships

timing and control

The timing and control circuit generates and distributes necessary clocks throughout this design. XIN is the external master clock input. The sample rate of the data paths is set as $LRCK = XIN/512$. With a fixed oversampling ratio of 32x and each PWM output value requiring 16 XIN cycles, the effect of changing XIN is shown in Table 1.

The DAC can be operated at any conversion rate between 48 kHz and 32 kHz by choosing the appropriate master-clock frequency. Some of the functions of the converter, such as the de-emphasis filter, operate only at the frequencies in Table 1.

Table 1. Master Clock to Sample Rate Comparison

XIN (MHz)	256FSO (MHz)	LRCK (kHz)
24.5760	12.2880	48.0
22.5792	11.2896	44.1
19.3536	9.6768	37.8
16.3840	8.1920	32.0

digital-audio data interface

The conversion cycle is synchronized to the rising edge of LRCK, and the data must meet the setup requirements specified in the timing requirements table. The input data is 16 or 18 bits with the MSB or LSB first as selected in the system register. The BCK frequency must be equal to or greater than $32 F_s$ for 16-bit data or $36 F_s$ for 18-bit data where F_s is the sample rate. Figure 2 illustrates the input timing.

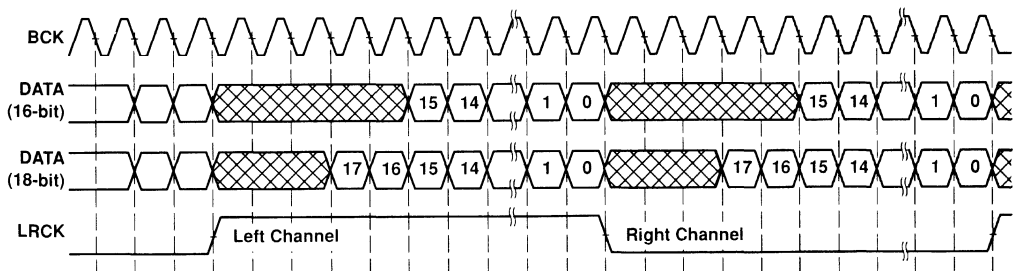


Figure 2. Audio-Data Input Timing

TMS57014A DUAL AUDIO DIGITAL-TO-ANALOG CONVERTER

SLAS077D – SEPTEMBER 1993 – REVISED NOVEMBER 1995

serial-control interface

This device uses the least-significant-bit-first format. Therefore, for a 16-bit word, D15 is the most significant bit and D0 is the least significant bit. Unless otherwise specified, all values are in 2s-complement format.

serial-control-data input

The 16-bit control-data input implements the device-control functions. The TMS57014A has two registers for this data: the system register and the attenuation register. The system register contains most of the system configuration information, and the attenuation register controls audio output level, de-emphasis, and mute. Figure 3 illustrates the input timing for ATT, SHIFT, and LATCH. The data loads internally on the falling edge of LATCH. The shift clock should be high for the LATCH setup time before LATCH goes low.

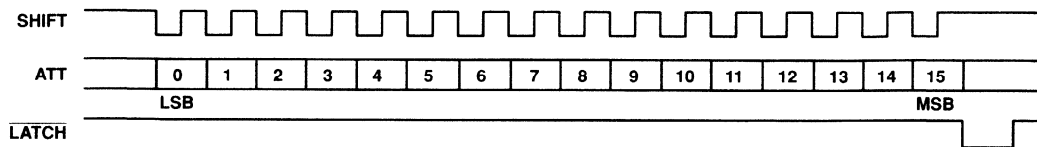


Figure 3. Control-Data-Input Timing

mute

When mute is activated, the output PWM becomes zero data (50% duty cycle). The two mute flags, $\overline{\text{MUTEL}}$ and $\overline{\text{MUTER}}$, are independently set low based on the data in the respective channel being zero. This function becomes active under the following conditions:

1. When the zero-data detector detects that the input data has been zero for 2500 cycles of F_s or 12500 cycles of F_s (as selected in the control registers), output is 50% duty cycle.
2. When the MUTE register value is set high by means of the serial-control data.
3. When $\overline{\text{INIT}}$ is active (low), output is 50% duty cycle.

zero-data detect

After the input data remains zero for 2500 or 12500 cycles of F_s as set by the system register (D4, D5), the channel-mute flag becomes active. Zero-data detection is available for both channels independently, so the two outputs ($\overline{\text{MUTER}}$ and $\overline{\text{MUTEL}}$) indicate that zero data has been detected on the respective channel. The zero-detect register value in the serial-control data selects the detection period. The mute flag returns high immediately when nonzero input data is received.

de-emphasis filter

Four sets of de-emphasis-filter coefficients support four sampling rates (F_s): 32, 37.8, 44.1, and 48 kHz. Internal register values select the filter coefficients. The internal register values enable or disable the filter. Figure 4 illustrates the de-emphasis characteristics.

Many audio sources have been recorded with pre-emphasis characteristics that are the inverse of the de-emphasis characteristics shown in Figure 4. This device provides reconstruction of the original frequency response.

TMS57014A DUAL AUDIO DIGITAL-TO-ANALOG CONVERTER

SLAS077D – SEPTEMBER 1993 – REVISED NOVEMBER 1995

de-emphasis filter (continued)

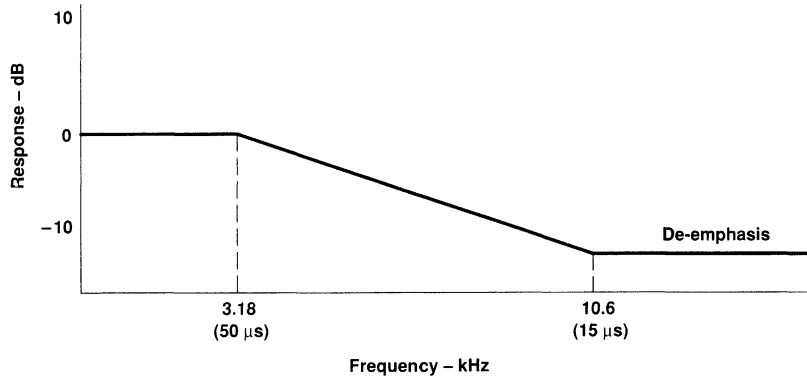


Figure 4. De-emphasis Characteristics

digital attenuation

A value selected in the internal attenuation register determines the attenuation of the digital-audio-data input. The attenuation value is 11 bits long with a valid range of hex values from 400h to 000h. A data value of 001h corresponds to an attenuation value of -60 dB and a data value of 400h corresponds to 0 dB. The attenuation function is nonlinear (see equation 1). Figure 5 illustrates the attenuation function in dB. The default attenuation value is 400h.

$$\text{Attenuation} = 20 \log \left(\frac{\text{attenuation data}}{1024} \right) \quad (1)$$

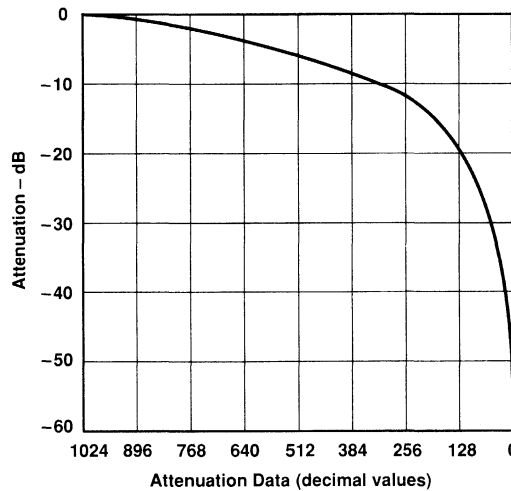


Figure 5. Digital Attenuation Characteristics

TMS57014A DUAL AUDIO DIGITAL-TO-ANALOG CONVERTER

SLAS077D – SEPTEMBER 1993 – REVISED NOVEMBER 1995

register set

Table 2 contains the register-set selection. Tables 3 and 4 list the bit functions.

Table 2. Register-Set Selection

BITS		DESCRIPTION
15	14	
0	0	Attenuation register
0	1	System register
1	x	Invalid condition†

† Bit 15 should always be set to 0 when writing data for proper operation.

Table 3. Attenuation-Register Bit Functions

BITS‡				FUNCTION
13	12	11	10–0	
0	—	—	—	De-emphasis off
1	—	—	—	De-emphasis on
—	0	—	—	Channel mute off
—	1	—	—	Channel mute on
—	—	0	—	Bit 11 must be low
—	—	—	0	Digital attenuation, mute
—	—	—	1	Digital attenuation, –60.2 dB§
—	—	—	2	Digital attenuation, –54.2 dB§
—	—	—	3	Digital attenuation, –50.7 dB§
—	—	—	...	
—	—	—	1FF	Digital attenuation, –6.04 dB§
—	—	—	200	Digital attenuation, –6.02 dB§
—	—	—	201	Digital attenuation, –6.00 dB§
—	—	—	...	
—	—	—	3FF	Digital attenuation, –0.01 dB§
—	—	—	400	Digital attenuation, 0.00 dB§

‡ Default value = 0400h

§ The attenuation values shown are typical values. Refer to the digital attenuation section for a description of the attenuation function.

TMS57014A DUAL AUDIO DIGITAL-TO-ANALOG CONVERTER

SLAS077D – SEPTEMBER 1993 – REVISED NOVEMBER 1995

Table 4. System-Register Bit Functions

BITS†								FUNCTION
13	12	11–6	5	4	3–2	1	0	
0	—	—	—	—	—	—	—	MSB first, audio data
1	—	—	—	—	—	—	—	LSB first, audio data
—	0	—	—	—	—	—	—	16-bit, audio data
—	1	—	—	—	—	—	—	18-bit, audio data
—	—	0	—	—	—	—	—	Bits 11–6 must be low
—	—	—	0	—	—	—	—	Zero data detect period (2500 cycles of F_S)
—	—	—	1	—	—	—	—	Zero data detect period (12500 cycles of F_S)
—	—	—	—	0	—	—	—	Bit 4 must be low
—	—	—	—	—	0	—	—	De-emphasis – 44.1 kHz
—	—	—	—	—	1	—	—	De-emphasis – 48.0 kHz
—	—	—	—	—	2	—	—	De-emphasis – 37.8 kHz
—	—	—	—	—	3	—	—	De-emphasis – 32.0 kHz
—	—	—	—	—	—	0	—	LRCK and PWM are not synchronized
—	—	—	—	—	—	1	—	LRCK and PWM synchronized
—	—	—	—	—	—	—	0	Bit 0 must be low

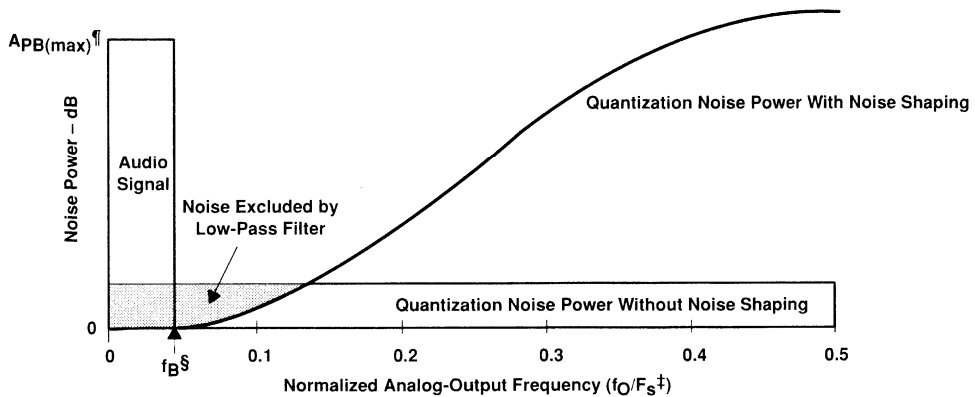
† Default value = 0000h

interpolation filter

The interpolation filter used prior to the DAC increases the digital-data rate from the LRCK speed to the oversampled rate by interpolating with a ratio of 1:32. The oversampling modulator receives the output of this filter with de-emphasis as an option.

DAC modulator

The DAC is a third-order modulator with 32 times oversampling. The DAC provides high-resolution, low-noise performance using a 15-value PWM output as shown in Figure 6.



† f_O is the output frequency at the low-pass filter output (V_O) shown in Figure 7.

§ f_B is the highest frequency of interest within the baseband.

¶ $APB(max)$ is the passband maximum amplitude.

Figure 6. Oversampling Noise Power With and Without Noise Shaping

TMS57014A DUAL AUDIO DIGITAL-TO-ANALOG CONVERTER

SLAS077D – SEPTEMBER 1993 – REVISED NOVEMBER 1995

PWM output (L2–L1 and R2–R1)

The L2–L1 and the R2–R1 output pairs are PWM signals with the L2–L1 differential pulse duration determining the left-channel analog voltage and the R2–R1 differential pulse duration determining the right-channel analog voltage.

Each DAC left and right output consists of 15 levels of PWM and provides a differential signal as the input to two external differential amplifiers configured as a low-pass filter to produce the left and right audio outputs (see Figure 7).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Analog supply voltage range, left and right, AV _{DDL} , AV _{DDR} (see Note 1)	–0.3 V to 7 V
Digital supply voltage range, DV _{DD} (see Note 2)	–0.3 V to 7 V
Clock supply voltage range, XV _{DD} (see Note 3)	–0.3 V to 7 V
Output voltage range, V _O : L1, L2	–0.3 V to AV _{DDL} + 0.3 V
R1, R2	–0.3 V to AV _{DDR} + 0.3 V
Input voltage range, V _I	–0.3 V to DV _{DD} + 0.3 V
Operating free-air temperature range, T _A	0°C to 70°C
Case temperature for 10 seconds, T _C	260°C
Storage temperature range, T _{stg}	–55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. Voltage values for maximum ratings are with respect to AGNDL and AGNDR respectively.
 2. Voltage values for maximum ratings are with respect to DGND.
 3. Voltage values for maximum ratings are with respect to XGND.

recommended operating conditions (see Note 4)

		MIN	NOM	MAX	UNIT
Analog supply voltage, left and right, AV _{DDL} , AV _{DDR}		4.75	5	5.25	V
Digital supply voltage, DV _{DD}		4.75	5	5.25	V
Clock supply voltage, XV _{DD}		4.75	5	5.25	V
High-level input voltage, V _{IH}	XIN	0.9 V _{DD}			V
	All other digital inputs	0.76 V _{DD}			
Low-level input voltage, V _{IL}	XIN	0.1 V _{DD}			V
	All other digital inputs	0.24 V _{DD}			
Load resistance at PWM, R _L		10			kΩ
Master clock frequency at XIN		16.3		24.6	MHz
Operating free-air temperature, T _A		0		70	°C

NOTE 4: DV_{DD}, AV_{DDL}, XV_{DD} and AV_{DDR} tied together represents V_{DD}.



TMS57014A

DUAL AUDIO DIGITAL-TO-ANALOG CONVERTER

SLAS077D – SEPTEMBER 1993 – REVISED NOVEMBER 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

digital interface, $AV_{DD} = DV_{DD} = 5\text{ V} \pm 5\%$ (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	256FSO	$I_O = -0.4\text{ mA}$		$V_{DD}-0.5$	V
		L1, L2, R1, R2	$I_O = -12\text{ mA}$		$V_{DD}-0.5$	
		XOUT	$I_O = -1.2\text{ mA}$		$V_{DD}-0.5$	
		MUTEL, MUTER	$I_O = -1\text{ mA}$		$V_{DD}-0.5$	
V_{OL}	Low-level output voltage	256FSO	$I_O = 0.4\text{ mA}$		0.4	V
		L1, L2, R1, R2	$I_O = 12\text{ mA}$		0.5	
		XOUT	$I_O = 1.2\text{ mA}$		0.5	
		MUTEL, MUTER	$I_O = 1\text{ mA}$		0.4	
I_{IH}	High-level input current, any digital input			±1	±5	μA
I_{IL}	Low-level input current, any digital input			±1	±5	μA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 4: DV_{DD} , AV_{DDL} , XV_{DD} and AV_{DDR} tied together represents V_{DD} .

supplies, $AV_{DD} = DV_{DD} = 5\text{ V} \pm 5\%$, no load

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Analog power supply current	AV_{DDL} and AV_{DDR} are shorted together		15		mA
Digital power supply current			15		mA
Total device supply current over operating temperature range				60	mA
Power dissipation				350	mW

† All typical values are at $T_A = 25^\circ\text{C}$.

DAC modulator, $AV_{DD} = DV_{DD} = 5\text{ V} \pm 5\%$, sample rate (F_S) = 44.1 kHz, full-scale input sine wave at 1 kHz, $T_A = 25^\circ\text{C}$, bandwidth is 20 Hz to 20 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Resolution	See Note 5	18			bits
Signal-to-noise ratio	A-weighted, 20 Hz to 20 kHz, See Figure 10, Table 5, and Note 5 De-emphasis not selected	96	100		dB
Total harmonic distortion	20 Hz to 20 kHz, See Note 5	0.003%	0.004%		

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 5: These specifications are measured at the output (V_O) of the low-pass filter shown in Figure 7.

filter characteristics, $AV_{DD} = DV_{DD} = 5\text{ V} \pm 5\%$, de-emphasis disabled

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Pass-band ripple	Sample rate (F_S) = 48 kHz, See Note 5	-0.002		0.002	dB
Stop-band attenuation		75			dB
Pass band (-3 dB) (DAC)	See Note 5	0		$0.46 F_S$	kHz
Stop band		$0.54 F_S$			kHz
Group delay		$29 / F_S$			s

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 5: These specifications are measured at the output (V_O) of the low-pass filter shown in Figure 7.



TMS57014A DUAL AUDIO DIGITAL-TO-ANALOG CONVERTER

SLAS077D – SEPTEMBER 1993 – REVISED NOVEMBER 1995

timing requirements (see Figures 8 and 9 and Note 6)

		MIN	MAX	UNIT
t_{w1}	Pulse duration, BCK	160		ns
t_{su1}	Setup time, DATA before BCK↑	20		ns
t_{h1}	Hold time, DATA after BCK↑	20		ns
t_{su2}	Setup time, LRCK before BCK↑	50		ns
t_{h2}	Hold time, LRCK after BCK↑	50		ns
t_{w2}	Pulse duration, SHIFT	100		ns
t_{su3}	Setup time, ATT before SHIFT↑	20		ns
t_{h3}	Hold time, ATT after SHIFT↑	20		ns
t_{w3}	Pulse duration, LATCH	100		ns
t_{su4}	Setup time, LATCH before SHIFT↑	100		ns
t_{h4}	Hold time, LATCH after SHIFT↑	$t_{w2} + 20$		ns

NOTE 6: All timing measurements were taken at the $V_{DD}/2$ voltage level.



TMS57014A DUAL AUDIO DIGITAL-TO-ANALOG CONVERTER

SLAS077D – SEPTEMBER 1993 – REVISED NOVEMBER 1995

PARAMETER MEASUREMENT INFORMATION

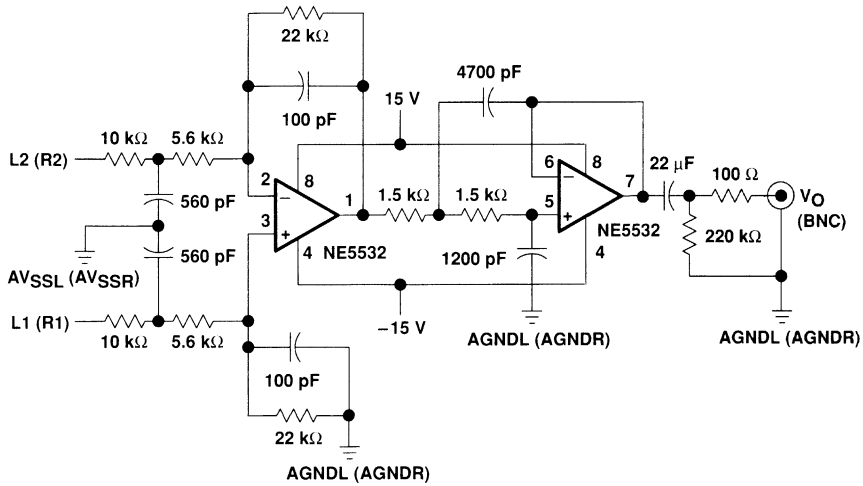


Figure 7. Analog Low-Pass Filter Recommended for Measuring the Dynamic Specifications of the TMS57014A

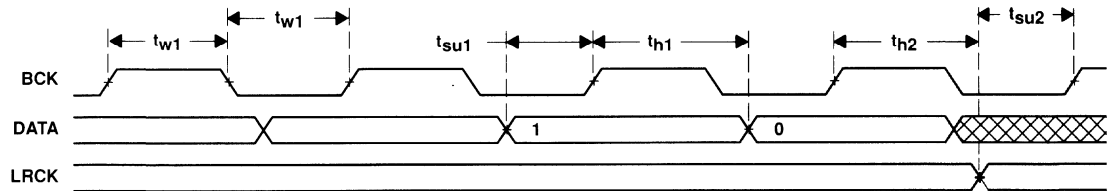


Figure 8. Audio-Data Serial Timing

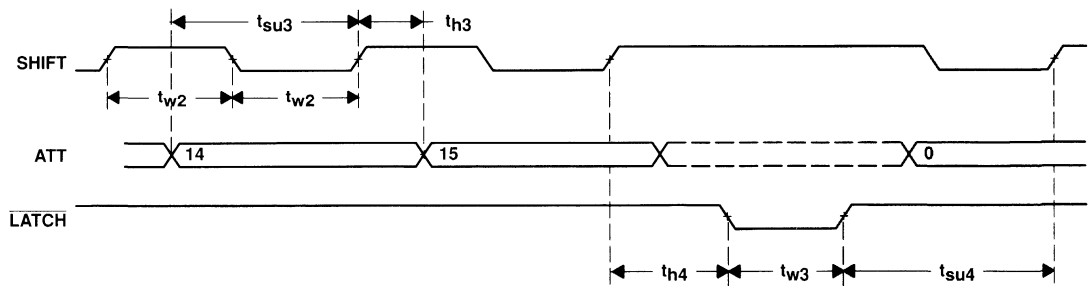


Figure 9. Control-Data Serial Timing

TMS57014A DUAL AUDIO DIGITAL-TO-ANALOG CONVERTER

SLAS077D – SEPTEMBER 1993 – REVISED NOVEMBER 1995

PARAMETER MEASUREMENT INFORMATION

Table 5. A-Weighted Data

FREQUENCY	A WEIGHTING (dB)	FREQUENCY	A WEIGHTING (dB)
25	-44.6 ± 2	800	-0.1 ± 1
31.5	-39.2 ± 2	1000	0 ± 0
40	-34.5 ± 2	1250	0.6 ± 1
50	-30.2 ± 2	1600	1.0 ± 1
63	-26.1 ± 2	2000	1.2 ± 1
80	-22.3 ± 2	2500	1.2 ± 1
100	-19.1 ± 1	3150	1.2 ± 1
125	-16.1 ± 1	4000	1.0 ± 1
160	-13.2 ± 1	5000	0.5 ± 1
200	-10.8 ± 1	6300	-0.1 ± 1
250	-8.6 ± 1	8000	-1.1 ± 1
315	-6.5 ± 1	10000	-2.4 ± 1
400	-4.8 ± 1	12500	-4.2 ± 2
500	-3.2 ± 1	16000	-6.5 ± 2
630	-1.9 ± 1		

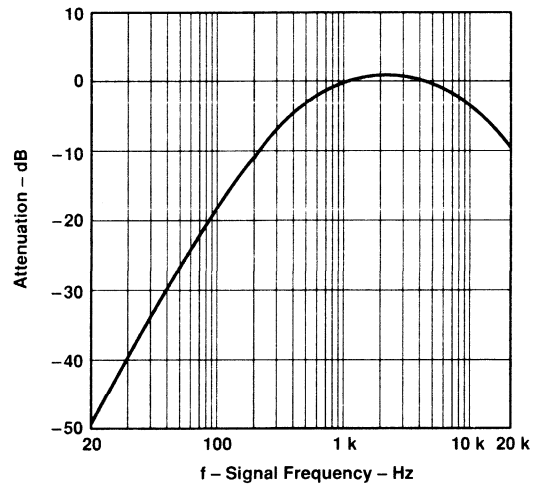


Figure 10. A-Weighted Function

TMS57014A DUAL AUDIO DIGITAL-TO-ANALOG CONVERTER

SLAS077D – SEPTEMBER 1993 – REVISED NOVEMBER 1995

APPLICATION INFORMATION

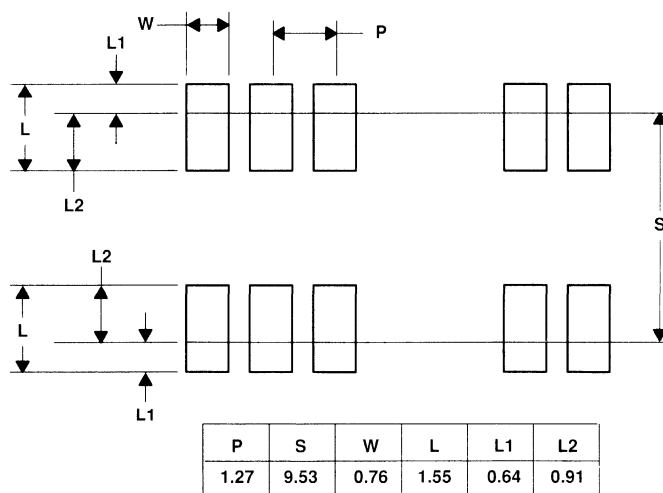
circuit and layout considerations

The designer should follow these guidelines for the best device performance.

- Separate digital and analog ground planes should be used. All digital device functions should be over the digital ground plane, and all analog device functions should be over the analog ground plane. The ground planes should be connected at only one point to the direct power supply, and this is usually at the connector edge of the board.
- A single crystal-controlled clock should synchronously generate all digital signals
- All power supply lines should include a 0.1- μ F and a 1- μ F capacitor. When clock noise is excessive, a toroidal inductance of 10 μ H should be placed in series with XV_{DD} before connecting to DV_{DD} .
- The digital input control signals should be buffered when they are generated off the card.
- Clock jitter should be minimized, and precautions taken to prevent clock overshoot. This minimizes any high-frequency coupling to the analog output.

PCB footprint

Figure 11 shows the printed-circuit-board (PCB) land pattern for the TMS57014A small-outline package.



NOTE A: All linear dimensions are in millimeters.

Figure 11. Land Pattern for PCB Layout

General Information	1
General Purpose ADCs	2
General IPurpose DACs	3
DSP AICs and CODECs	4
Special Functions	5
Video Interface Palettes	6
Digital Imaging Sensor Products	7
Mechanical Information	8

Contents

	Page
TLC32040, TLC32041 :	4-3
TLC32044, TLC32045 :	4-35
TLC32046 :	4-73
TLC32047 :	4-129
TLC320AC01 :	4-187
TLC320AC02 :	4-273
TLC320AD50, TLC320AD52 :	4-361
TLC320AD55 :	4-417
TLC320AD56 :	4-455
TLC320AD75 :	4-495
TLC320AD80 :	4-535

TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

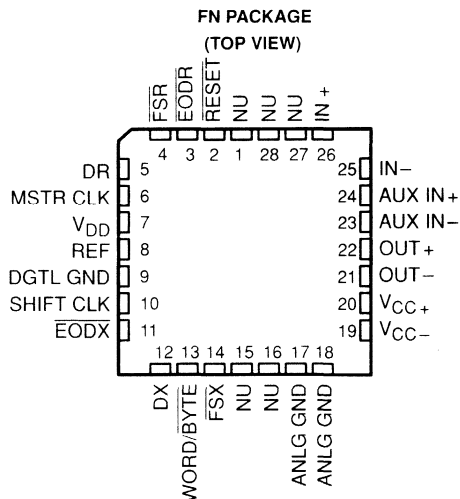
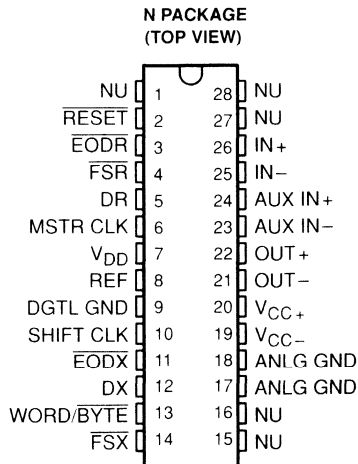
SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

- 14-Bit Dynamic Range ADC and DAC
- Variable ADC and DAC Sampling Rate Up to 19,200 Samples per Second
- Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter
- Serial Port for Direct Interface to TMS32011, TMS320C17, TMS32020, and TMS320C25 Digital Signal Process
- Synchronous or Asynchronous ADC and DAC Conversion Rate With Programmable Incremental ADC and DAC Conversion Timing Adjustments
- Serial Port Interface to SN74299 Serial-to-Parallel Shift Register for Parallel Interface to TMS32010, TMS320C15, or Other Digital Processors
- 600-Mil Wide N Package (C_L to C_L)
- 2s Complement Format
- CMOS Technology

PART NUMBER	DESCRIPTION
TLC32040	Analog interface circuit with internal reference. Also a plug-in replacement for TLC32041.
TLC32041	Analog interface circuit without internal reference

description

The TLC32040 and TLC32041 are complete analog-to-digital and digital-to-analog input/output systems, each on a single monolithic CMOS chip. This device integrates a bandpass switched-capacitor antialiasing input filter, a 14-bit-resolution A/D converter, four microprocessor-compatible serial port modes, a 14-bit-resolution D/A converter, and a low-pass switched-capacitor output-reconstruction filter.



NU - Nonusable; no external connection should be made to these terminals.

AVAILABLE OPTIONS

T _A	PACKAGE	
	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC32040CFN TLC32041CFN	TLC32040CN TLC32041CN
-40°C to 85°C		TLC32040IN TLC32041IN

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

description (continued)

The device offers numerous combinations of master clock input frequencies and conversion/sampling rates, which can be changed via digital processor control.

Typical applications for this integrated circuit include modems (7.2-, 8-, 9.6-, 14.4-, and 19.2-kHz sampling rate), analog interface for digital signal processors (DSPs), speech recognition/storage systems, industrial process control, biomedical instrumentation, acoustical signal processing, spectral analysis, data acquisition, and instrumentation recorders. Four serial modes, which allow direct interface to the TMS32011, TMS320C17, TMS32020, and TMS320C25 digital signal processors, are provided. Also, when the transmit and receive sections of the analog interface circuit (AIC) are operating synchronously, it can interface to two SN74299 serial-to-parallel shift registers. These serial-to-parallel shift registers can then interface in parallel to the TMS32010, TMS320C15, other digital signal processors, or external FIFO circuitry. Output data pulses are emitted to inform the processor that data transmission is complete or to allow the DSP to differentiate between two transmitted bytes. A flexible control scheme is provided so that the functions of this integrated circuit can be selected and adjusted coincidentally with signal processing via software control.

The antialiasing input filter comprises seventh-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively and a fourth-order equalizer. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When no filtering is desired, the entire composite filter can be switched out of the signal path. A selectable, auxiliary, differential analog input is provided for applications where more than one analog input is required.

The A/D and D/A converters each have 14 bits of resolution. The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided on the TLC32040 to ease the design task and to provide complete control over the performance of this integrated circuit. The internal voltage reference is brought out to a terminal and is available to the designer. Separate analog and digital voltage supplies and grounds are provided to minimize noise and ensure a wide dynamic range. Also, the analog circuit path contains only differential circuitry to keep noise to an absolute minimum. The only exception is the DAC sample and hold, which utilizes pseudo-differential circuitry.

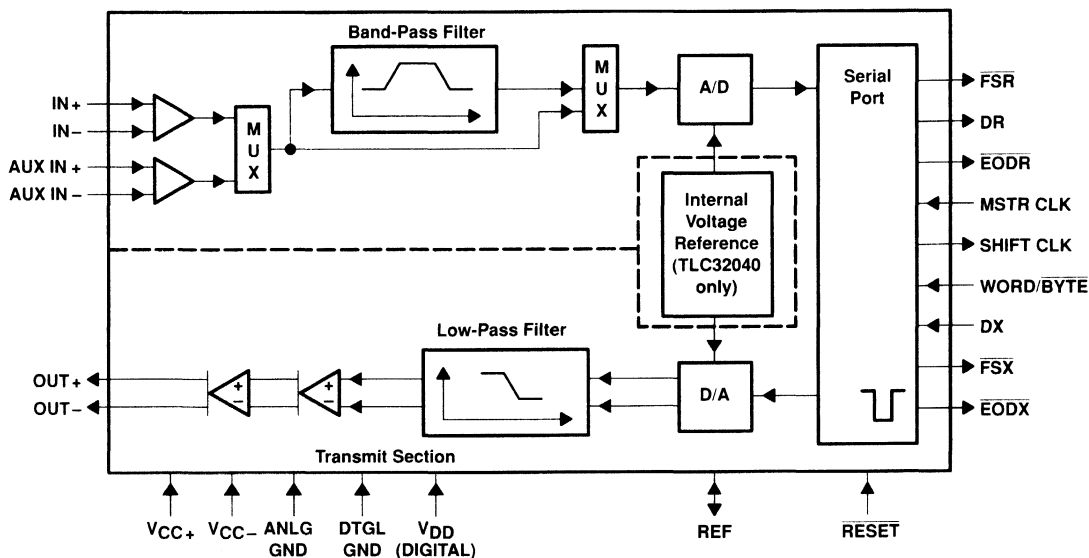
The output-reconstruction filter is a seventh-order CC-type (Chebyshev/elliptic transitional low-pass filter followed by a fourth-order equalizer) and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the digitally encoded signal.

The TLC32040C and TLC32041C are characterized for operation from 0°C to 70°C, and the TLC32040I and TLC32041I are characterized for operation from -40°C to 85°C.

TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN+	24	I	Noninverting auxiliary analog input state. This input can be switched into the bandpass filter and A/D converter path via software control. If the appropriate bit in the control register is a 1, the auxiliary inputs replace the IN+ and IN- inputs. If the bit is a 0, the IN+ and IN- inputs are used (see the AIC DX data word format section).
AUX IN-	23	I	Inverting auxiliary analog input (see the above AUX IN+ description)
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
DR	5	O	DR is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with the SHIFT CLK signal.
DX	12	I	DX is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port to the AIC is synchronized with the SHIFT CLK signal.
EODR	3	O	End of data receive. See the WORD/BYTE description and the Serial Port Timing diagrams. During the word-mode timing, EODR is a low-going pulse that occurs immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. EODR can be used to interrupt a microprocessor upon completion of serial communications. Also, EODR can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, EODR goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS32011 or TMS320C17 can use this low-going signal to differentiate between the two bytes as to which is first and which is second. EODR does not occur after secondary communication.



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TLC32040C, TLC32040I, TLC32041C, TLC32041I

ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

Terminal Functions (continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
EODX	11	O	End of data transmit. See the WORD/BYTE description and the Serial Port Timing diagram. During the word-mode timing, EODX is a low-going pulse that occurs immediately after the 16 bits of D/A converter and control or register information have been transmitted from the TMS320 serial port to the AIC. EODX can be used to interrupt a microprocessor upon the completion of serial communications. Also, EODX can be used to strobe and enable external serial-to-parallel shift registers, latches, or an external FIFO RAM, and to facilitate parallel data-bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, EODX goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS32011 or TMS320C17 can use this low-going signal to differentiate between the two bytes as to which is first and which is second.
FSR	4	O	Frame sync receive. In the serial transmission modes, which are described in the WORD/BYTE description, FSR is held low during bit transmission. When FSR goes low, the TMS320 serial port begins receiving bits from the AIC via DR of the AIC. The most significant DR bit is present on DR before FSR goes low. (See Serial Port Timing and Internal Timing Configuration diagrams.) FSR does not occur after secondary communication.
FSX	14	O	Frame sync transmit. When FSX goes low, the TMS320 serial port begins transmitting bits to the AIC via DX of the AIC. In all serial transmission modes, which are described in the WORD/BYTE description, FSX is held low during bit transmission (see the Serial Port Timing and Internal Timing Configuration diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN-	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	Master clock. MSTR CLK is used to derive all the key logic signals of the AIC, such as the shift clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these key signals are synchronous submultiples of the master clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the A/D and D/A converters (see the Internal Timing Configuration).
OUT+	22	O	Noninverting output of analog output power amplifier. OUT+ can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
OUT-	21	O	Inverting output of analog output power amplifier. OUT- is functionally identical with and complementary to OUT+.
REF	8	I/O	Internal voltage reference for the TLC32040. For the TLC32040 and TLC32041 an external voltage reference can be applied to this terminal.
RESET	2	I	Reset. A reset function is provided to initialize the TA, TA', TB, RA, RA', RB, and control registers. This reset function initiates serial communications between the AIC and DSP. The reset function initializes all AIC registers including the control register. After a negative-going pulse on RESET, the AIC registers are initialized to provide an 8-kHz data conversion rate for a 5.184-MHz master clock input signal. The conversion rate adjust registers, TA' and RA', are reset to 1. The control register bits are reset as follows (see AIC DX data word format section): d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1 This initialization allows normal serial-port communication to occur between AIC and DSP.
SHIFT CLK	10	O	Shift clock. SHIFT CLK is obtained by dividing the master clock signal frequency by four. SHIFT CLK is used to clock the serial data transfers of the AIC, described in the WORD/BYTE description below (see the Serial Port Timing and Internal Timing Configuration diagrams).
VDD	7		Digital supply voltage, 5 V ± 5%
VCC+	20		Positive analog supply voltage, 5 V ± 5%
VCC-	19		Negative analog supply voltage, -5 V ± 5%



TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

Terminal Functions (continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
WORD/BYTE	13	I	<p>WORD/BYTE, in conjunction with a bit in the control register, is used to establish one of four serial modes. These four serial modes are described below.</p> <p><i>AIC transmit and receive sections are operated asynchronously.</i></p> <p>The following description applies when the AIC is configured to have asynchronous transmit and receive sections. If the appropriate data bit in the control register is a 0 (see the AIC DX data word format section), the transmit and receive sections are asynchronous.</p> <ul style="list-style-type: none"> L Serial port directly interfaces with the serial port of the TMS32011 or TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams): <ol style="list-style-type: none"> 1. FSX or FSR is brought low. 2. One 8-bit byte is transmitted or one 8-bit byte is received. 3. EODX or EODR is brought low. 4. FSX or FSR emits a positive frame-sync pulse that is four shift clock cycles wide. 5. One 8-bit byte is transmitted or one 8-bit byte is received. 6. EODX or EODR is brought high. 7. FSX or FSR is brought high. H Serial port directly interfaces with the serial port of the TMS32020, TMS320C25, or TMS320C30 and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): <ol style="list-style-type: none"> 1. FSX or FSR is brought low. 2. One 16-bit word is transmitted or one 16-bit word is received. 3. FSX or FSR is brought high. 4. EODX or EODR emits a low-going pulse. <p><i>AIC transmit and receive sections are operated synchronously.</i></p> <p>If the appropriate data bit in the control register is a 1, the transmit and receive sections are configured to be synchronous. In this case, the bandpass switched-capacitor filter and the A/D conversion timing are derived from the TX counter A, TX counter B, and TA, TA', and TB registers, rather than the RX counter A, RX counter B, and RA, HA, and RB registers. In this case, the AIC FSX and FSR timing are identical during primary data communication; however, FSR is not asserted during secondary data communication since there is no new A/D conversion result. The synchronous operation sequences are as follows (see Serial Port Timing diagrams):</p> <ul style="list-style-type: none"> L Serial port directly interfaces with the serial port of the TMS32011 or TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams): <ol style="list-style-type: none"> 1. FSX and FSR are brought low. 2. One 8-bit byte is transmitted and one 8-bit byte is received. 3. EODX and EODR are brought low. 4. FSX and FSR emit positive frame-sync pulses that are four shift clock cycles wide 5. One 8-bit byte is transmitted and one 8-bit byte is received. 6. EODX and EODR are brought high. 7. FSX and FSR are brought high. H Serial port directly interfaces with the serial port of the TMS32020, TMS320C25, or TMS320C30 and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): <ol style="list-style-type: none"> 1. FSX and FSR are brought low. 2. One 16-bit word is transmitted and one 16-bit word is received. 3. FSX and FSR are brought high. 4. EODX or EODR emit low-going pulses. <p>Since the transmit and receive sections of the AIC are now synchronous, the AIC serial port with additional NOR and AND gates will interface to two SN74299 serial-to-parallel shift registers. Interfacing the AIC to the SN74299 shift register allows the AIC to interface to an external FIFO RAM and facilitates parallel data bus communications between the AIC and the digital signal processor. The operation sequence is the same as the above sequence (see Serial Port Timing diagrams).</p>



TLC32040C, TLC32040I, TLC32041C, TLC32041I

ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

detailed description

analog input

Two sets of analog inputs are provided. Normally, the IN+ and IN– input set is used; however, the auxiliary input set, AUX IN+ and AUX IN–, can be used if a second input is required. Each input set can be operated in either differential or single-ended modes, since sufficient common-mode range and rejection are provided. The gain for the IN+, IN–, AUX IN+, and AUX IN– inputs can be programmed to be either 1, 2, or 4 (see Table 2). Either input circuit can be selected via software control. It is important to note that a wide dynamic range is assured by the differential internal analog architecture and by the separate analog and digital voltage supplies and grounds.

A/D bandpass filter, A/D bandpass filter clocking, and A/D conversion timing

The A/D bandpass filter can be selected or bypassed via software control. The frequency response of this filter is presented in the following pages. This response results when the switched-capacitor filter clock frequency is 288 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the filter transfer function is frequency scaled by the ratio of the actual clock frequency to 288 kHz. The low-frequency roll-off of the high-pass section is 300 Hz.

The internal timing configuration and AIC DX data word format sections of this data sheet indicate the many options for attaining a 288-kHz bandpass switched-capacitor filter clock. These sections indicate that the RX counter A can be programmed to give a 288-kHz bandpass switched-capacitor filter clock for several master clock input frequencies.

The A/D conversion rate is then attained by frequency dividing the 288-kHz bandpass switched-capacitor filter clock with the RX counter B. Thus, unwanted aliasing is prevented because the A/D conversion rate is an integral submultiple of the bandpass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

A/D converter performance specifications

Fundamental performance specifications for the A/D converter circuitry are presented in the A/D converter operating characteristics section of this data sheet. The realization of the A/D converter circuitry with switched-capacitor techniques provides an inherent sample-and-hold.

analog output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of this integrated circuit. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

D/A low-pass filter, D/A low-pass filter clocking, and D/A conversion timing

The frequency response of this filter is presented in the following pages. This response results when the low-pass switched-capacitor filter clock frequency is 288 kHz. Like the A/D filter, the transfer function of this filter is frequency scaled when the clock frequency is not 288 kHz. A continuous-time filter is provided on the output on the output of the D/A low-pass filter to greatly attenuate any switched-capacitor clock feedthrough.

The D/A conversion rate is then attained by frequency dividing the 288-kHz switched-capacitor filter clock with TX counter B. Thus, unwanted aliasing is prevented because the D/A conversion rate is an integral submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.



TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

asynchronous versus synchronous operation

If the transmit section of the AIC (low-pass filter and DAC) and receive section (bandpass filter and ADC) are operated asynchronously, the low-pass and band-pass filter clocks are independently generated from the master clock signal. Also, the D/A and A/D conversion rates are independently determined. If the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and bandpass filters. In synchronous operation, the A/D conversion timing is derived from, and is equal to, the D/A conversion timing. (See description of WORD/BYTE in the Terminal Functions table.)

D/A converter performance specifications

Fundamental performance specifications for the D/A converter circuitry are presented in the D/A converter operating characteristics section of the data sheet. The D/A converter has a sample-and-hold that is realized with a switched-capacitor ladder.

system frequency response correction

The $(\sin x)/x$ correction circuitry is performed in the digital processor software. The system frequency response can be corrected via DSP software to ± 0.1 -dB accuracy to band edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, which requires only seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of only 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the $(\sin x)/x$ correction section for more details).

serial port

The serial port has four possible modes that are described in detail in the Terminal Functions table. These modes are briefly described below and in the description for WORD/BYTE in the Terminal Functions Table.

- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32011 and TMS320C17.
- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020 and the TMS320C25.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32011 and TMS320C17.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, or two SN74299 serial-to-parallel shift registers, which can then interface in parallel to the TMS320C10, TMS32015, to any other digital signal processor, or to external FIFO circuitry.

operation of TLC32040 with internal voltage reference

The internal reference of the TLC32040 eliminates the need for an external voltage reference and provides overall circuit cost reduction. Thus, the internal reference eases the design task and provides complete control over the performance of this integrated circuit. The internal reference is brought out to a terminal and is available to the designer. To keep the amount of noise on the reference signal to a minimum, an external capacitor may be connected between REF and ANLG GND.

operation of TLC32040 or TLC32041 with external voltage reference

REF can be driven from an external reference circuit if so desired. This external circuit must be capable of supplying 250 μ A and must be adequately protected from noise such as crosstalk from the analog input.



TLC32040C, TLC32040I, TLC32041C, TLC32041I

ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

reset

A reset function is provided to initiate serial communications between the AIC and DSP and allow fast, cost-effective testing during manufacturing. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on RESET, the AIC is initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX data word format section).

loopback

This feature allows the user to test the circuit remotely. In loopback, OUT+ and OUT– are internally connected to IN+ and IN–. Thus, the DAC bits (d15 to d2), which are transmitted to DX, can be compared with the ADC bits (d15 to d2), which are received from DR. An ideal comparison would be that the bits on DR equal the bits on DX. However, in practice there is some difference in these bits due to the ADC and DAC output offsets.

In loopback, if IN+ and IN– are enabled, the external signals on IN+ and IN– are ignored. If AUX IN+ and AUX IN– are enabled, the external signals on these terminals are added to the OUT+ and OUT– signals in loopback operation.

The loopback feature is implemented with digital signal processor control by transmitting the appropriate serial port bit to the control register (see AIC DX data word format section).

explanation of internal timing configuration

All of the internal timing of the AIC is derived from the high-frequency clock signal that drives the master clock input. The shift clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the master clock input signal frequency by four.

$$\text{SCF Clock Frequency} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

$$\text{Conversion Frequency} = \frac{\text{SCF Clock Frequency}}{\text{Contents of Counter B}}$$

$$\text{Shift Clock Frequency} = \frac{\text{Master Clock Frequency}}{4}$$

TX counter A and TX counter B, which are driven by the master clock signal, determine the D/A conversion timing. Similarly, RX counter A and RX counter B determine the A/D conversion timing. In order for the switched-capacitor low-pass and band pass filters to meet their transfer function specifications, the frequency of the clock inputs of the switched-capacitor filters must be 288 kHz. If the frequencies of the clock inputs are not 288 kHz, the filter transfer function frequencies are scaled by the ratios of the clock frequencies to 288 kHz. Thus, to obtain the specified filter responses, the combination of master clock frequency and TX counter A and RX counter A values must yield 288-kHz switched-capacitor clock signals. These 288-kHz clock signals can then be divided by the TX counter B and RX counter B to establish the D/A and A/D conversion timings.

TX counter A and TX counter B are reloaded every D/A conversion period, while RX counter A and RX counter B are reloaded every A/D conversion period. The TX counter B and RX counter B are loaded with the values in the TB and RB registers, respectively. Via software control, the TX counter A can be loaded with either the TA register, the TA register less the TA' register, or the TA register plus the TA' register. By selecting the TA register less the TA' register option, the upcoming conversion timing will occur earlier by an amount of time that equals TA' times the signal period of the master clock. By selecting the TA register plus the TA' register option, the upcoming conversion timing will occur later by an amount of time that equals TA' times the signal period of the master clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. In this case, however, the RX counter A can be programmed via software control with the RA register, the RA register less the RA' register, or the RA register plus the RA' register.



TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

explanation of internal timing configuration (continued)

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing. This feature can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

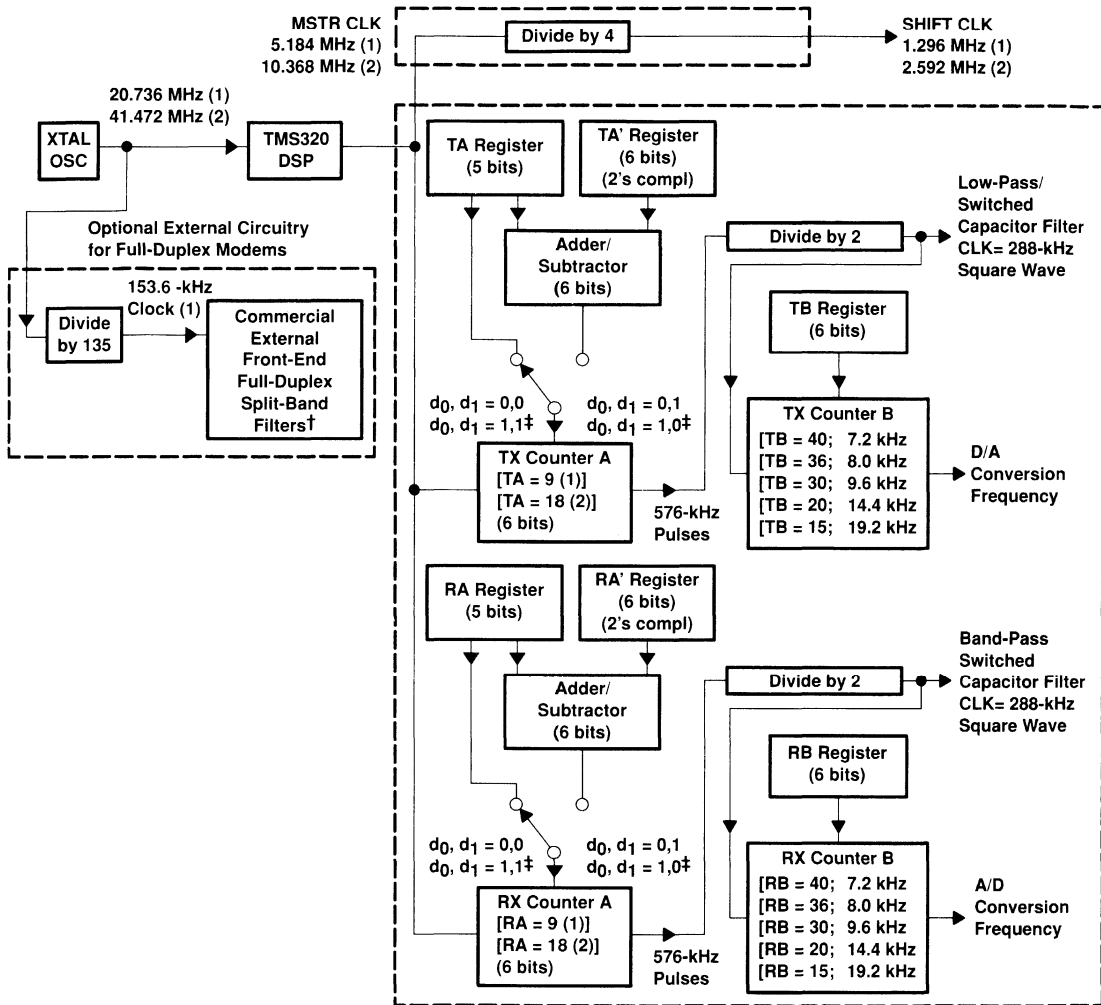
If the transmit and receive sections are configured to be synchronous (see WORD/BYTE description), then both the low-pass and bandpass switched-capacitor filter clocks are derived from TX counter A. Also, both the D/A and A/D conversion timing are derived from the TX counter A and TX counter B. When the transmit and receive sections are configured to be asynchronous, the RX counter A, RX counter B, RA register, RA' register, and RB registers are not used.



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TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995



$$\text{SCF Clock Frequency} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

† Split-band filtering can alternatively be performed after the analog input function via software in the TMS320.

‡ These control bits are described in the AIC DX data word format section.

NOTE A: Frequency 1 (20.736 MHz) is used to show how 153.6 kHz (for commercially available modem split-band filter clock), popular speech and modem sampling signal frequencies, and an internal 288-kHz switched-capacitor filter clock can be derived synchronously and as submultiples of the crystal oscillator frequency. Since these derived frequencies are synchronous submultiples of the crystal frequency, aliasing does not occur as the sampled analog signal passes between the analog converter and switched-capacitor filter stages. Frequency 2 (41.472 MHz) is used to show that the AIC can work with high-frequency signals, which are used by high-speed digital signal processors.

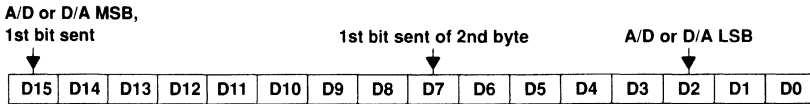
Figure 1. Internal Timing Configuration



TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

AIC DR or DX word bit pattern



AIC DX data word format section

d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	COMMENTS	
primary DX serial communication protocol																	
←d15 (MSB) through d2 go to the D/A converter register														→	0	0	The TX and RX counter As are loaded with the TA and RA register values. The TX and RX counter Bs are loaded with TB and RB register values.
←d15 (MSB) through d2 go to the D/A converter register														→	0	1	The TX and RX counter As are loaded with the TA + TA' and RA + RA' register values. The TX and RX counter Bs are loaded with TB and RB register values. Bits d1 = 0 and d0 = 1 cause the next D/A and A/D conversion periods to be changed by the addition of TA' and RA' master clock cycles, in which TA' and RA' can be positive or negative or zero (refer to Table 1).
←d15 (MSB) through d2 go to the D/A converter register														→	1	0	The TX and RX counter As are loaded with the TA – TA' and RA – RA' register values. The TX and RX counter Bs are loaded with TB and RB register values. Bits d1 = 1 and d0 = 0 cause the next D/A and A/D conversion periods to be changed by the subtraction of TA' and RA' master clock cycles, in which TA' and RA' can be positive or negative or zero (refer to Table 1).
←d15 (MSB) through d2 go to the D/A converter register														→	1	1	The TX and RX counter As are loaded with the TA and RA register values. The TX and RX counter Bs are loaded with the TB and RB register values. After a delay of four shift clock cycles, a secondary transmission immediately follows to program the AIC to operate in the desired configuration.

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (primary communications) to the AIC initiates secondary communications upon completion of the primary communications.

Upon completion of the primary communication, FSX remains high for four SHIFT CLK cycles and then goes low and initiates the secondary communication. The timing specifications for the primary and secondary communications are identical. In this manner, the secondary communication, if initiated, is interleaved between successive primary communications. This interleaving prevents the secondary communication from interfering with the primary communications and DAC timing, thus preventing the AIC from skipping a DAC output. In the synchronous mode, FSR is not asserted during secondary communications.



TLC32040C, TLC32040I, TLC32041C, TLC32041I

ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

secondary DX serial communication protocol

x x ← to TA register → x x ← to RA register →	0 0	d13 and d6 are MSBs (unsigned binary)
x ← to TA' register → x ← to RA' register →	0 1	d14 and d7 are 2's complement sign bits
x ← to TB register → x ← to RB register →	1 0	d14 and d7 are MSBs (unsigned binary)
x x x x x x x x d7 d6 d5 d4 d3 d2 1 1 <div style="text-align: center;"> <p>Control register</p> </div>		d2 = 0/1 deletes/inserts the bandpass filter d3 = 0/1 disables/enables the loopback function d4 = 0/1 disables/enables the AUX IN+ and AUX IN- terminals d5 = 0/1 asynchronous/synchronous transmit receive sections d6 = 0/1 gain control bits (see gain control section) d7 = 0/1 gain control bits (see gain control section)

reset function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on $\overline{\text{RESET}}$ initializes the AIC registers to provide an 8-kHz A/D and D/A conversion rate for a 5.184-MHz master clock input signal. The AIC, except the control register, is initialized as follows (see AIC DX data word format section):

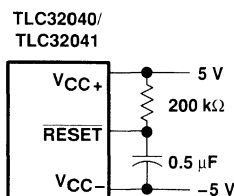
REGISTER	INITIALIZED REGISTER VALUE (HEX)
TA	9
TA'	1
TB	24
RA	9
RA'	1
RB	24

The control register bits are reset as follows (see AIC DX data word format section):

$$d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1$$

This initialization allows normal serial port communications to occur between AIC and DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA', and TB register need to be programmed, since both transmit and receive timing are synchronously derived from these registers (see the terminal descriptions and AIC DX word format sections).

The circuit shown below provides a reset on power up when power is applied in the sequence given under power-up sequence. The circuit depends on the power supplies reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.



TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

power-up sequence

To ensure proper operation of the AIC, and as a safeguard against latch-up, it is recommended that a Schottky diode with a forward voltage less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND (see Figure 17). In the absence of such a diode, power should be applied in the following sequence: ANLG GND and DGTL GND, V_{CC-} , then V_{CC+} and V_{DD} . Also, no input signal should be applied until after power up.

AIC responses to improper conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 1 below.

AIC register constraints

The following constraints are placed on the contents of the AIC registers:

1. TA register must be ≥ 4 in word mode ($\overline{\text{WORD/BYTE}} = \text{high}$).
2. TA register must be ≥ 5 in byte mode ($\overline{\text{WORD/BYTE}} = \text{low}$).
3. TA' register can be either positive, negative, or zero.
4. RA register must be ≥ 4 in word mode ($\overline{\text{WORD/BYTE}} = \text{high}$).
5. RA register must be ≥ 5 in byte mode ($\overline{\text{WORD/BYTE}} = \text{low}$).
6. RA' register can be either positive, negative, or zero.
7. (TA register \pm TA' register) must be > 1 .
8. (RA register \pm RA' register) must be > 1 .
9. TB register must be > 1 .

Table 1. AIC Responses To Improper Conditions

IMPROPER CONDITIONS	AIC RESPONSE
TA register + TA' register = 0 or 1 TA register - TA' register = 0 or 1	Reprogram TX counter A with TA register value
TA register + TA' register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into the TX counter A, i.e., TA register + TA' register + 40 hex is loaded into TX counter A.
RA register + RA' register = 0 or 1 RA register - RA' register = 0 or 1	Reprogram RX counter A with RA register value
RA register + RA' register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX counter A, i.e., RA register + RA' register + 40 hex is loaded into RX counter A.
TA register = 0 or 1 RA register = 0 or 1	The AIC is shut down.
TA register < 4 in word mode TA register < 5 in byte mode RA register < 4 in word mode RA register < 5 in byte mode	The AIC serial port no longer operates.
TB register = 0 or 1	Reprogram TB register with 24 hex
RB register = 0 or 1	Reprogram RB register with 24 hex
AIC and DSP cannot communicate	Hold last DAC output



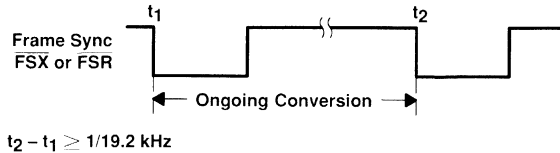
TLC32040C, TLC32040I, TLC32041C, TLC32041I

ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

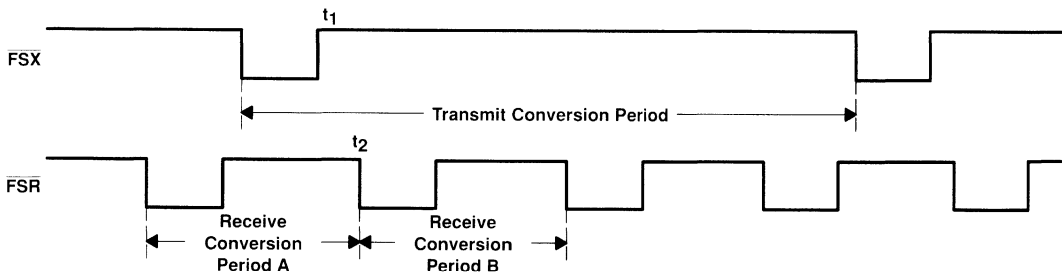
improper operation due to conversion times being too close together

If the difference between two successive D/A conversion frame syncs is less than 1/19.2 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A' register or A - A' register result is too small. When incrementally adjusting the conversion period via the A + A' register options, the designer should be very careful not to violate this requirement (see following diagram).



asynchronous operation — more than one receive frame sync occurring between two transmit frame syncs

When incrementally adjusting the conversion period via the A + A' or A - A' register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during a FSX frame sync. The ongoing conversion period is then adjusted. However, either receive conversion period A or B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. Therefore, if there is sufficient time between t_1 and t_2 , the receive conversion period adjustment is performed during receive conversion period A. Otherwise, the adjustment is performed during receive conversion period B. The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent FSX frame (see figure below).

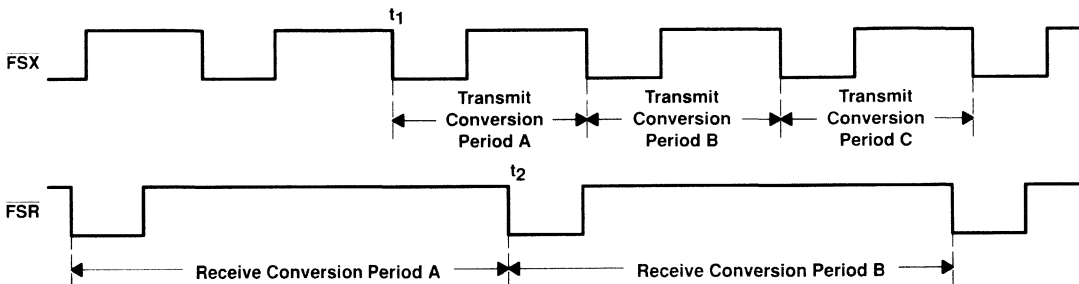


TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

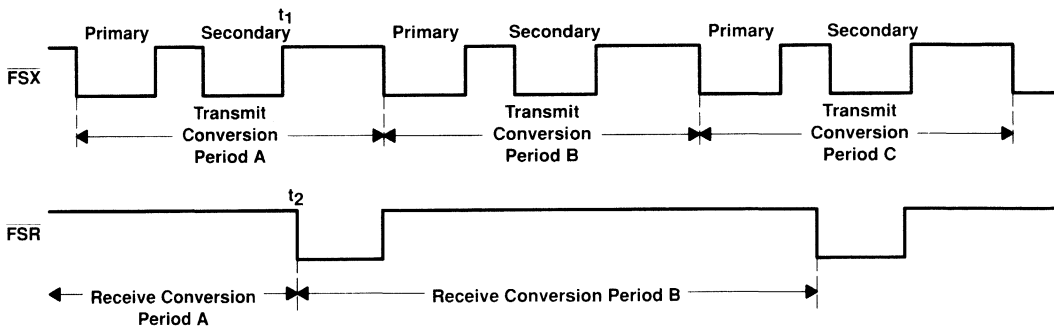
asynchronous operation — more than one receive frame sync occurring between two receive frame syncs

When incrementally adjusting the conversion period via the $A + A'$ or $A - A'$ register options, a specific protocol is followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during a $\overline{\text{FSX}}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment in the diagram as shown in the following figure. If the adjustment command is issued during transmit conversion period A, receive conversion period A is adjusted if there is sufficient time between t_1 and t_2 . Or, if there is not sufficient time between t_1 and t_2 , receive conversion period B is adjusted. Or, the receive portion of an adjustment command can be ignored if the adjustment command is sent during a receive conversion period, which is already being or is adjusted due to a prior adjustment command. For example, if adjustment commands are issued during transmit conversion periods A, B, and C, the first two commands can cause receive conversion periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during receive conversion period B, which already is adjusted via the transmit conversion period B adjustment command.



asynchronous operation — more than one set of primary and secondary DX serial communication occurring between two receive frame sync (see AIC DX data word format section)

The TA , TA' , TB , and control register information that is transmitted in the secondary communications is always accepted and is applied during the ongoing transmit conversion period. If there is sufficient time between t_1 and t_2 , the TA , RA' , and RB register information, which is sent during transmit conversion period A, is applied to receive conversion period A. Otherwise, this information is applied during receive conversion period B. If RA , RA' , and RB register information has already been received and is being applied during an ongoing conversion period, any subsequent RA , RA' , or RB information that is received during this receive conversion period is disregarded (see diagram below).



TLC32040C, TLC32040I, TLC32041C, TLC32041I

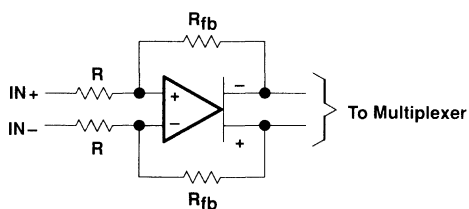
ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

Table 2. Gain Control Table Analog Input Signal Required for Full-Scale A/D Conversion

INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT†	A/D CONVERSION RESULT
	d6	d7		
Differential configuration Analog input = IN+ – IN– = AUX IN+ – AUX IN–	1	1	± 6 V	Full scale
	0	0		
	1	0	± 3 V	Full scale
	0	1	± 1.5 V	Full scale
Single-ended configuration Analog input = IN+ – ANLG GND = AUX IN+ – ANLG GND	1	1	± 3 V	Half scale
	0	0		
	1	0	± 3 V	Full scale
	0	1	± 1.5 V	Full scale

† In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.



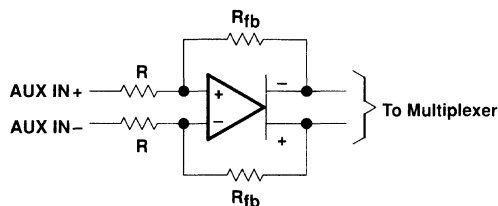
$$R_{fb} = R \text{ for } d6 = 1, d7 = 1$$

$$d6 = 0, d7 = 0$$

$$R_{fb} = 2R \text{ for } d6 = 1, d7 = 0$$

$$R_{fb} = 4R \text{ for } d6 = 0, d7 = 1$$

Figure 2. IN+ and IN– Gain Control Circuitry



$$R_{fb} = R \text{ for } d6 = 1, d7 = 1$$

$$d6 = 0, d7 = 0$$

$$R_{fb} = 2R \text{ for } d6 = 1, d7 = 0$$

$$R_{fb} = 4R \text{ for } d6 = 0, d7 = 1$$

Figure 3. AUX IN+ and AUX IN– Gain Control Circuitry

(sin x)/x correction section

The AIC does not have (sin x)/x correction circuitry after the digital-to-analog converter. The (sin x)/x correction can be accomplished easily and efficiently in digital signal processor (DSP) software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results, which are shown below, are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires only seven instruction cycles per sample on the TMS320 DSPs. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction adds a slight amount of group delay at the upper edge of the 300–3000-Hz band.

(sin x)/x roll-off for a zero-order hold function

The (sin x)/x roll-off for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in the table below.

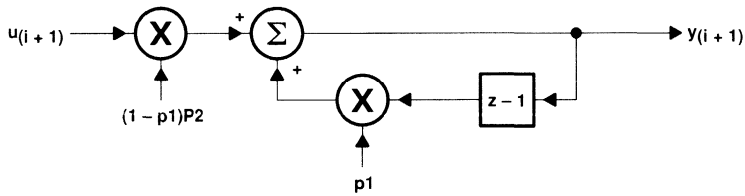
Table 3. (sin x)/x Roll-Off

f_s (Hz)	$20 \log \frac{\sin \pi f/f_s}{\pi f/f_s}$ ($f = 3000$ Hz) (dB)
7200	-2.64
8000	-2.11
9600	-1.44
14400	-0.63
19200	-0.35

The actual AIC (sin x)/x roll-off is slightly less than the above figures, because the AIC has less than a 100% duty cycle hold interval.

correction filter

To compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter shown below, is recommended.



The difference equation for this correction filter is:

$$y_i + 1 = p_2(1 - p_1) (u_{i+1}) + p_1 y_i$$

where the constant p_1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{p_2^2 (1 - p_1)^2}{1 - 2p_1 \cos(2\pi f/f_s) + p_1^2}$$

TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

correction results

Table 4 below shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates.

Table 4. Correction Results

f (Hz)	ERROR (dB)	
	$f_s = 8000$ Hz $p1 = -0.14813$ $p2 = 0.9888$	$f_s = 9600$ Hz $p1 = -0.1307$ $p2 = 0.9951$
300	-0.099	-0.043
600	-0.089	-0.043
900	-0.054	0
1200	-0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	-0.043	0
3000	-0.102	-0.043

TMS320 software requirements

The digital correction filter equation can be written in state variable form as follows:

$$Y = k1 \times Y + k2 \times U$$

where

$$k1 = p1$$

$$k2 = (1 - p1) \times p2$$

Y = filter state

U = next I/O sample

The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) will yield the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC+} (see Note 1)	–0.3 V to 15 V
Supply voltage range, V_{DD}	–0.3 V to 15 V
Output voltage range, V_O	–0.3 V to 15 V
Input voltage range, V_I	–0.3 V to 15 V
Digital ground voltage range	–0.3 V to 15 V
Operating free-air temperature range, T_A : TLC32040C, TLC32041C	0°C to 70°C
TLC32040I, TLC32041I	–40°C to 85°C
Storage temperature range, T_{stg}	–40°C to 125°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values for maximum ratings are with respect to V_{CC-} .

recommended operating conditions

	MIN	NOM	MAX	UNIT	
Supply voltage, V_{CC+} (see Note 2)	4.75	5	5.25	V	
Supply voltage, V_{CC-} (see Note 2)	–4.75	–5	–5.25	V	
Digital supply voltage, V_{DD} (see Note 2)	4.75	5	5.25	V	
Digital ground voltage with respect to ANLG GND, DGTL GND		0		V	
Reference input voltage, $V_{ref(ext)}$ (see Note 2)	2		4	V	
High-level input voltage, V_{IH}	2		$V_{DD} + 0.3$	V	
Low-level input voltage, V_{IL} (see Note 3)	–0.3		0.8	V	
Load resistance at OUT+ and/or OUT–, R_L	300			Ω	
Load capacitance at OUT+ and/or OUT–, C_L			100	pF	
MSTR CLK frequency (see Note 4)	0.075	5	10.368	MHz	
Analog input amplifier common mode input voltage (see Note 5)			± 1.5	V	
A/D or D/A conversion rate			20	kHz	
Operating free-air temperature, T_A	TLC32040C, TLC32041C		0	70	°C
	TLC32040I, TLC32041I		–40	85	

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+} , and V_{CC-} , are with respect to ANLG GND. Voltages at digital inputs and outputs and V_{DD} are with respect to DGTL GND.

3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

4. The bandpass low-pass switched-capacitor filter response specifications apply only when the switched-capacitor clock frequency is 288 kHz. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

5. This range applies when $(IN+ - IN-)$ or $(AUX IN+ - AUX IN-)$ equals ± 6 V.



TLC32040C, TLC32040I, TLC32041C, TLC32041I

ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

electrical characteristics over recommended operating free-air temperature range, $V_{CC+} = 5\text{ V}$, $V_{CC-} = -5\text{ V}$, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

total device, MSTR CLK frequency = 5.184 MHz, outputs not loaded

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$V_{DD} = 4.75\text{ V}$, $I_{OH} = -300\text{ }\mu\text{A}$	2.4			V
V_{OL}	Low-level output voltage	$V_{DD} = 4.75\text{ V}$, $I_{OL} = 2\text{ mA}$			0.4	V
I_{CC+}	Supply current from V_{CC+}	TLC3204_C			35	mA
		TLC3204_I			40	
I_{CC-}	Supply current from V_{CC-}	TLC3204_C			-35	mA
		TLC3204_I			-40	
I_{DD}	Supply current from V_{DD}	fMSTR CLK = 5.184 MHz			7	mA
V_{ref}	Internal reference output voltage		3		3.3	V
$\times V_{ref}$	Temperature coefficient of internal reference voltage			200		ppm/°C
r_o	Output resistance at REF			100		k Ω

receive amplifier input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters bypassed)			25	65	mV
	A/D converter offset error (filters in)			25	65	mV
CMRR	Common-mode rejection ratio at IN+, IN-, or AUX IN+, AUX IN-	See Note 6		55		dB
r_i	Input resistance at IN+, IN-, or AUX IN+, AUX IN-, REF			100		k Ω

transmit filter output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+, OUT-, (single-ended relative to ANLG GND)			15	75	mV
V_{OM}	Maximum peak output voltage swing across R_L at OUT+ or OUT-, (single ended)	$R_L \geq 300\text{ }\Omega$, Offset voltage = 0		± 3		V
V_{OM}	Maximum peak output voltage swing between R_L at OUT+ and OUT-, (differential output)	$R_L \geq 600\text{ }\Omega$		± 6		V

system distortion specifications, SCF clock frequency = 288 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	Single ended	$V_1 = -0.5\text{ dB}$ to -24 dB referred to V_{ref} , See Note 7		70		dB
	Differential		62	70		
Attenuation of third and higher harmonics of A/D input signal	Single ended	$V_1 = -0.5\text{ dB}$ to -24 dB referred to V_{ref} , See Note 7		65		dB
	Differential		57	65		
Attenuation of second harmonic of D/A input signal	Single ended	$V_1 = -0\text{ dB}$ to -24 dB referred to V_{ref} , See Note 7		70		dB
	Differential		62	70		
Attenuation of third and higher harmonics of D/A input signal	Single ended	$V_1 = -0\text{ dB}$ to -24 dB referred to V_{ref} , See Note 7		65		dB
	Differential		57	65		

† All typical values are at $T_A = 25\text{ }^\circ\text{C}$.

NOTES: 6. The test condition is a 0-dB,m, 1-kHz input signal with an 8-kHz conversion rate.

7. The test condition V_1 is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance for the DAC is 600 Ω .



TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

A/D channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 7)	$A_V = 1^\dagger$		$A_V = 2^\dagger$		$A_V = 4^\dagger$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio	$V_I = -6$ dB to -0.1 dB	58		$>58^\S$		$>58^\S$		dB
	$V_I = -12$ dB to -6 dB	58		58		$>58^\S$		
	$V_I = -18$ dB to -12 dB	56		58		58		
	$V_I = -24$ dB to -18 dB	50		56		58		
	$V_I = -30$ dB to -24 dB	44		50		56		
	$V_I = -36$ dB to -30 dB	38		44		50		
	$V_I = -42$ dB to -36 dB	32		38		44		
	$V_I = -48$ dB to -42 dB	26		32		38		
	$V_I = -54$ dB to -48 dB	20		26		32		

D/A channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 7)	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	$V_I = -6$ dB to 0 dB	58		dB
	$V_I = -12$ dB to -6 dB	58		
	$V_I = -18$ dB to -12 dB	56		
	$V_I = -24$ dB to -18 dB	50		
	$V_I = -30$ dB to -24 dB	44		
	$V_I = -36$ dB to -30 dB	38		
	$V_I = -42$ dB to -36 dB	32		
	$V_I = -48$ dB to -42 dB	26		
	$V_I = -54$ dB to -48 dB	20		

gain and dynamic range

PARAMETER	TEST CONDITIONS	MIN	TYP ‡	MAX	UNIT
Absolute transmit gain tracking error while transmitting into 600Ω	-48 -dB to 0-dB signal range. See Note 8		± 0.05	± 0.15	dB
Absolute receive gain tracking error	-48 -dB to 0-dB signal range. See Note 8		± 0.05	± 0.15	dB
Absolute gain of the A/D channel	Signal input is a -0.5 -dB, 1-kHz sinewave		0.2		dB
Absolute gain of the D/A channel	Signal input is a 0-dB, 1-kHz sinewave		-0.3		dB

power supply rejection and crosstalk attenuation

PARAMETER	TEST CONDITIONS	MIN	TYP ‡	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	$f = 0$ to 30 kHz		30		dB
	$f = 30$ kHz to 50 kHz		45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single ended)	$f = 0$ to 30 kHz		30		dB
	$f = 30$ kHz to 50 kHz		45		
Crosswalk attenuation, transmit-to-receive (single ended)			80		dB

$^\dagger A_V$ is the programmable gain of the input amplifier.

‡ All typical values are at $T_A = 25^\circ\text{C}$.

§ A value >58 is overrange and signal clipping occurs.

NOTES: 7. The test condition V_{IN} is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{REF}). The load impedance for the DAC is 600Ω .

8. Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 dB relative to V_{REF}).



TLC32040C, TLC32040I, TLC32041C, TLC32041I

ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

delay distortion, SCF clock frequency = 288 kHz \pm 2%, input (IN+ – IN–) is \pm 3-V sinewave

Refer to filter response graphs for delay distortion specifications.

TLC32040 and TLC32041 bandpass filter transfer function (see curves), SCF clock frequency = 288 kHz, \pm 2%, input (IN+ – IN–) is a \pm 3-V sinewave (see Note 9)

PARAMETER	TEST CONDITIONS	FREQUENCY RANGE	MIN	MAX	UNIT
Filter gain. (see Note 10)	Input signal reference is 0 dB	f = 100 Hz		-42	dB
		f = 170 Hz		-25	
		300 Hz \leq f \leq 3.4 kHz	-0.5	0.5	
		f = 4 kHz		-16	
		f \geq 4.6 kHz		-58	

low-pass filter transfer function, SCF clock frequency = 288 kHz \pm 2% (see Note 9)

PARAMETER	TEST CONDITIONS	FREQUENCY RANGE	MIN	MAX	UNIT
Filter gain. (see Note 10)	Output signal reference is 0 dB	f \leq 3.4 kHz	-0.5	0.5	dB
		f = 3.6 kHz		-4	
		f = 4 kHz		-30	
		f \geq 4.4 kHz		-58	

serial port

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH} High-level output voltage	I _{OH} = -300 μ A	2.4			V
V _{OL} Low-level output voltage	I _{OL} = 2 mA			0.4	V
I _I Input current				\pm 10	μ A
C _I Input capacitance			15		pF
C _O Output capacitance			15		pF

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = -5 V, V_{DD} = 5 V

noise (measurement includes low-pass and bandpass switched-capacitor filters)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit noise	Single ended DX input = 00 00 00 00 00 00 00, constant input code		200		μ V rms
			300	500	μ V rms
				20	dBrncO
Receive noise (see Note 11)	Inputs grounded. gain = 1		300	475	μ V rms
				20	dBrncO

† All typical values are at T_A = 25°C.

NOTES: 9. The above filter specifications are for a switched-capacitor filter clock range of 288 kHz \pm 2%. For switched-capacitor filter clocks at frequencies other than 288 kHz \pm 2%, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

10. The filter gain outside of the passband is measured with respect to the gain at 1 kHz. The filter gain within the passband is measured with respect to the average gain within the passband. The passbands are 300 to 3400 Hz and 0 to 3400 Hz for the bandpass and low-pass filters respectively.

11. The noise is referred to the input with a buffer gain of one. If the buffer gain is two or four, the noise figure is correspondingly reduced. The noise is computed by statistically evaluating the digital output of the A/D converter.



TLC32040C, TLC32040I, TLC32041C, TLC32041I

ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

timing requirements

serial port recommended input signals

	MIN	MAX	UNIT
$t_c(\text{MCLK})$ Master clock cycle time	95		ns
$t_r(\text{MCLK})$ Master clock rise time		10	ns
$t_f(\text{MCLK})$ Master clock fall time		10	ns
Master clock duty cycle	42%	58%	
RESET pulse duration (see Note 12)	800		ns
$t_{su}(\text{DX})$ DX setup time before SCLK↓	20		ns
$t_h(\text{DX})$ DX hold time after SCLK↓	$t_c(\text{SCLK})/4$		ns

serial port – AIC output signals, $C_L = 30$ pF for SHIFT CLK output, $C_L = 15$ pF for all other outputs

	MIN	TYP†	MAX	UNIT
$t_c(\text{SCLK})$ Shift clock (SCLK) cycle time	380			ns
$t_f(\text{SCLK})$ Shift clock (SCLK) fall time		3	8	ns
$t_r(\text{SCLK})$ Shift clock (SCLK) rise time		3	8	ns
Shift clock (SCLK) duty cycle	45		55	%
$t_d(\text{CH-FL})$ Delay from SCLK↑ to FSR/FSX/FSD↓		30		ns
$t_d(\text{CH-FH})$ Delay from SCLK↑ to FSR/FSX/FSD↑		35	90	ns
$t_d(\text{CH-DR})$ DR valid after SCLK↑			90	ns
$t_d(\text{CH-EL})$ Delay from SCLK↑ to EODX/EODR↓ in word mode			90	ns
$t_d(\text{CH-EH})$ Delay from SCLK↑ to EODX/EODR↑ in word mode			90	ns
$t_f(\text{EODX})$ EODX fall time		2	8	ns
$t_f(\text{EODR})$ EODR fall time		2	8	ns
$t_d(\text{CH-EL})$ Delay from SCLK↑ to EODX/EODR↓ in byte mode			90	ns
$t_d(\text{CH-EH})$ Delay from SCLK↑ to EODX/EODR↑ in byte mode			90	ns
$t_d(\text{MH-SL})$ Delay from MSTR CLK↑ to SCLK↓		65	170	ns
$t_d(\text{MH-SH})$ Delay from MSTR CLK↑ to SCLK↑		65	170	ns

† Typical values are at $T_A = 25^\circ\text{C}$.

NOTE 12: RESET pulse duration is the amount of time that the reset terminal is held below 0.8 V after the power supplies have reached their recommended values.



TLC32040C, TLC32040I, TLC32041C, TLC32041I

ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

serial port – AIC output signals

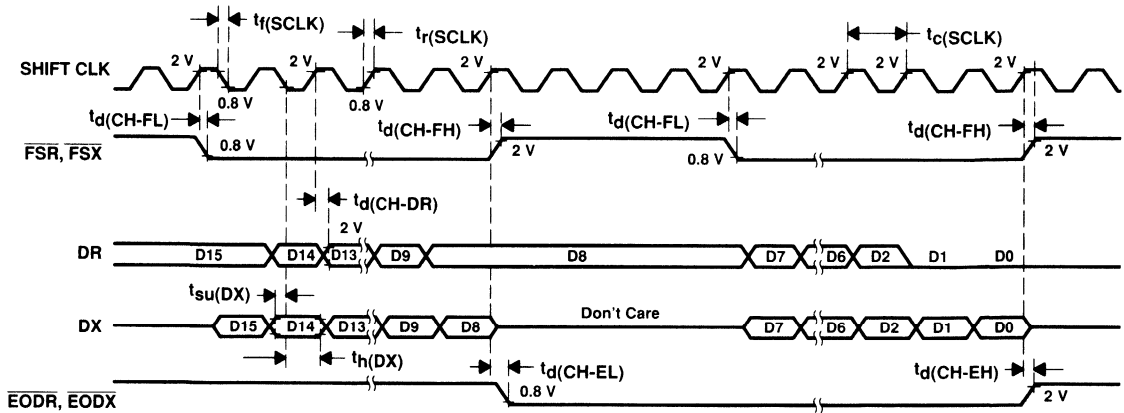
		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_c(\text{SCLK})$	Shift clock (SCLK) cycle time		380			ns
$t_f(\text{SCLK})$	Shift clock (SCLK) fall time				50	ns
$t_r(\text{SCLK})$	Shift clock (SCLK) rise time				50	ns
	Shift clock (SCLK) duty cycle		45		55	%
$t_d(\text{CH-FL})$	Delay from SCLK↑ to FSR/FSX↓	$C_L = 50 \text{ pF}$			52	ns
$t_d(\text{CH-FH})$	Delay from SCLK↑ to FSR/FSX↑	$C_L = 50 \text{ pF}$			52	ns
$t_d(\text{CH-DR})$	DR valid after SCLK↑				90	ns
$t_d(\text{CH-EL})$	Delay from SCLK↑ to EODX/EODR↓ in word mode				90	ns
$t_d(\text{CH-EH})$	Delay from SCLK↑ to EODX/EODR↑ in word mode				90	ns
$t_f(\text{EODX})$	EODX fall time				15	ns
$t_f(\text{EODR})$	EODR fall time				15	ns
$t_d(\text{CH-EL})$	Delay from SCLK↑ to EODX/EODR↓ in byte mode				100	ns
$t_d(\text{CH-EH})$	Delay from SCLK↑ to EODX/EODR↑ in byte mode				100	ns
$t_d(\text{MH-SL})$	Delay from MSTR CLK↑ to SCLK↓			65		ns
$t_d(\text{MH-SH})$	Delay from MSTR CLK↑ to SCLK↑			65		ns

† Typical values are at $T_A = 25^\circ\text{C}$.

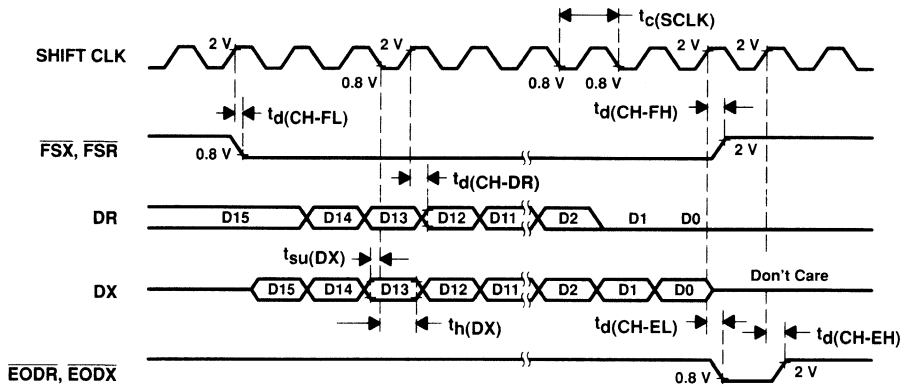
TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

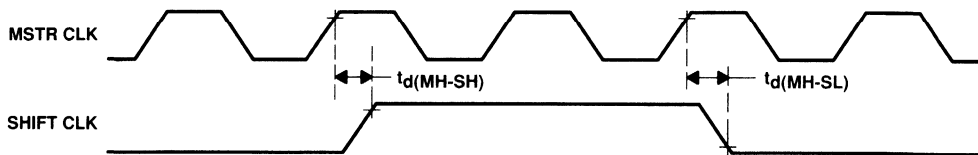
PARAMETER MEASUREMENT INFORMATION



(a) BYTE-MODE TIMING



(b) WORD-MODE TIMING



(c) SHIFT-CLOCK TIMING

Figure 4. Serial Port Timing



TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

PARAMETER MEASUREMENT INFORMATION

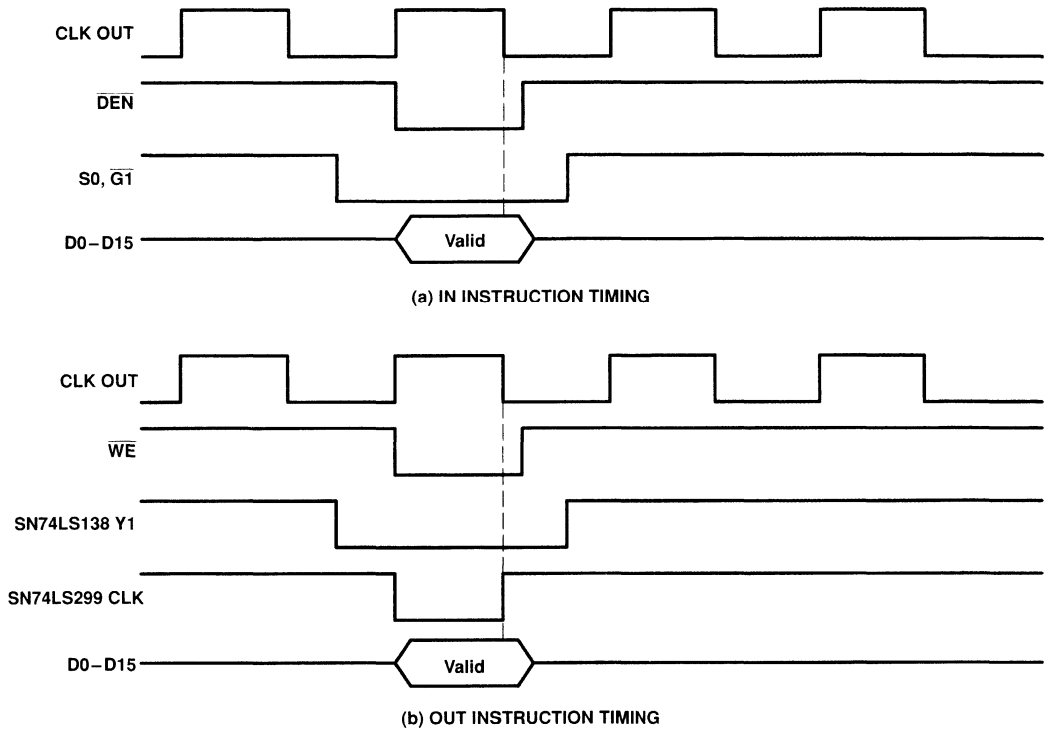
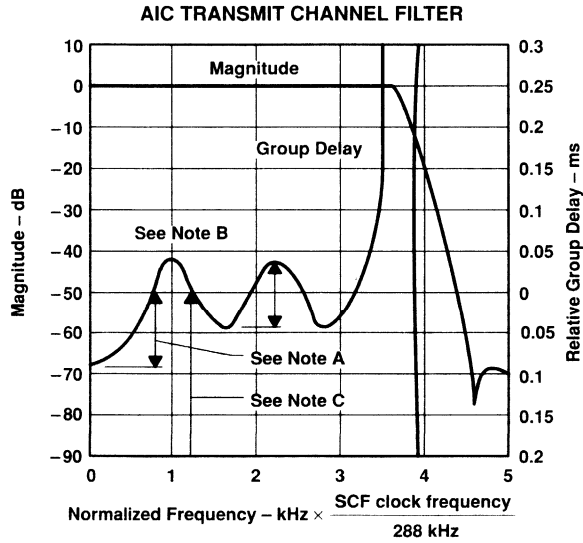


Figure 5. TMS32010-TLC32040/TLC32041 Interface Timing

TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

TYPICAL CHARACTERISTICS



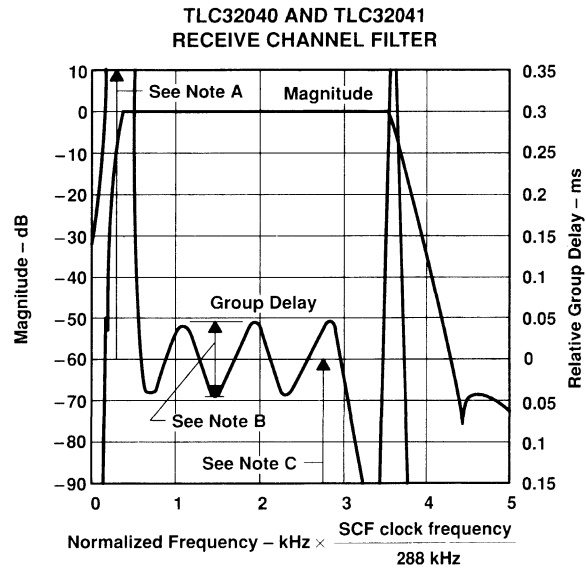
- NOTES: A. Maximum relative delay (0 Hz to 600 Hz) = 125 μ s
 B. Maximum relative delay (600 Hz to 3000 Hz) = \pm 50 μ s
 C. Absolute delay (600 Hz to 3000 Hz) = 700 μ s
 D. Test conditions are V_{CC+} , V_{CC-} , and V_{DD} within recommended operating conditions, SCF clock $f = 288$ kHz \pm 2% input = \pm 3-V sinewave, and $T_A = 25^\circ$ C.

Figure 6

TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

TYPICAL CHARACTERISTICS



- NOTES: A. Maximum relative delay (200 Hz to 600 Hz) = 3350 μ s
 B. Maximum relative delay (600 Hz to 3000 Hz) = \pm 50 μ s
 C. Absolute delay (600 Hz to 3000 Hz) = 1230 μ s
 D. Test conditions are V_{CC+} , V_{CC-} , and V_{DD} within recommended operating conditions, SCF clock f = 288 kHz \pm 2%, input = \pm 3-V sinewave, and T_A = 25 $^{\circ}$ C.

Figure 7

TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

TYPICAL CHARACTERISTICS

**A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL**

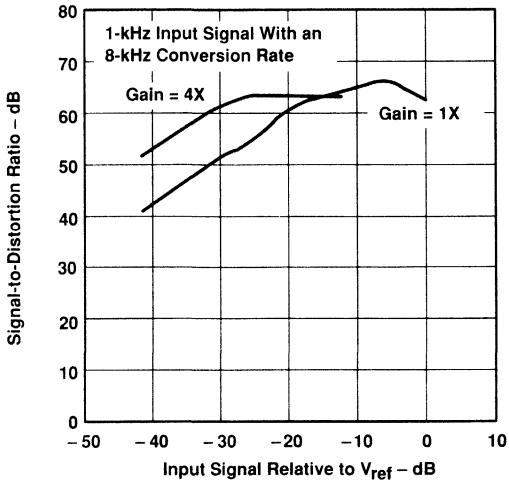


Figure 8

**A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN
AT 0-dB INPUT SIGNAL)**

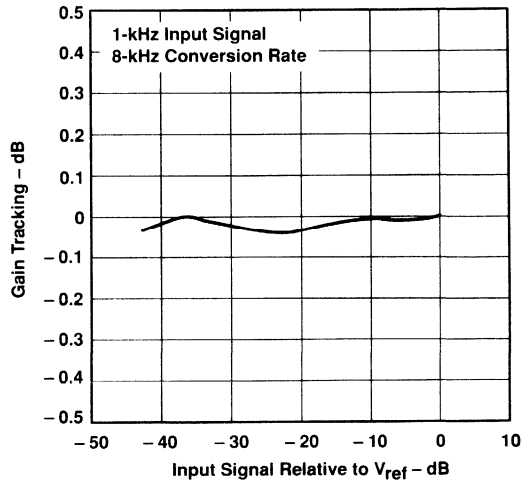


Figure 9

**D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL**

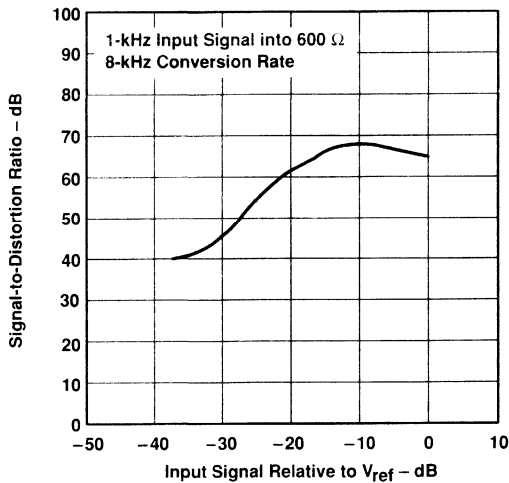


Figure 10

**D/A GAIN TRACKING
vs
(GAIN RELATIVE TO GAIN
AT 0 dB INPUT SIGNAL)**

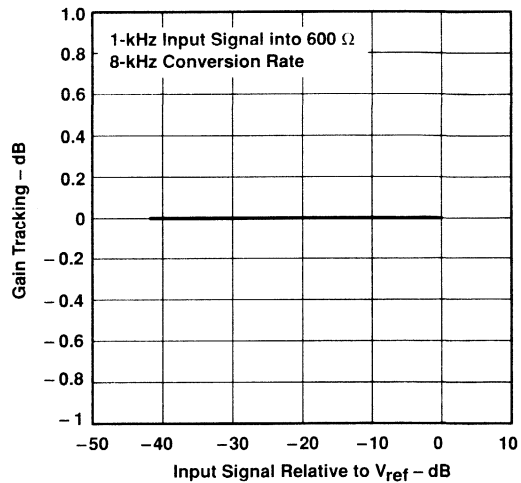


Figure 11

NOTE: Test conditions are V_{CC+} , V_{CC-} , V_{DD} and within recommended operating conditions set clock $f = 288 \text{ kHz} \pm 2\%$, and $T_A = 25^\circ\text{C}$.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

TYPICAL CHARACTERISTICS

ATTENUATION OF SECOND HARMONIC OF A/D INPUT
vs
INPUT SIGNAL

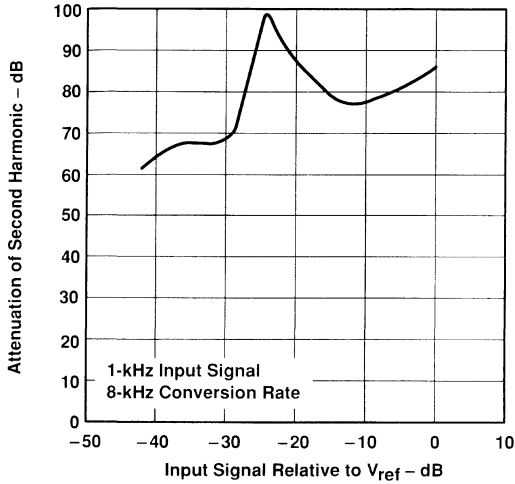


Figure 12

ATTENUATION OF THIRD HARMONIC OF A/D INPUT
vs
INPUT SIGNAL

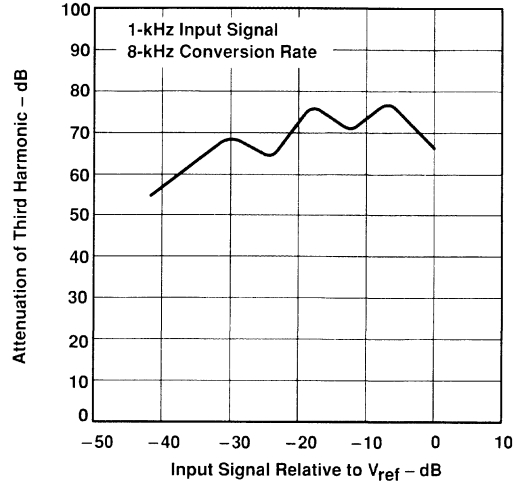


Figure 13

ATTENUATION OF SECOND HARMONIC OF D/A INPUT
vs
INPUT SIGNAL

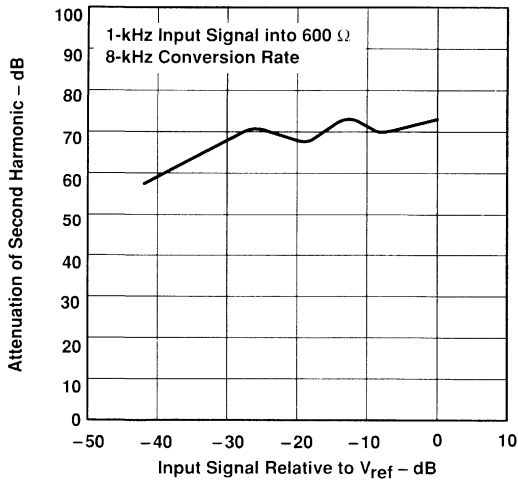


Figure 14

ATTENUATION OF THIRD HARMONIC OF D/A INPUT
vs
INPUT SIGNAL

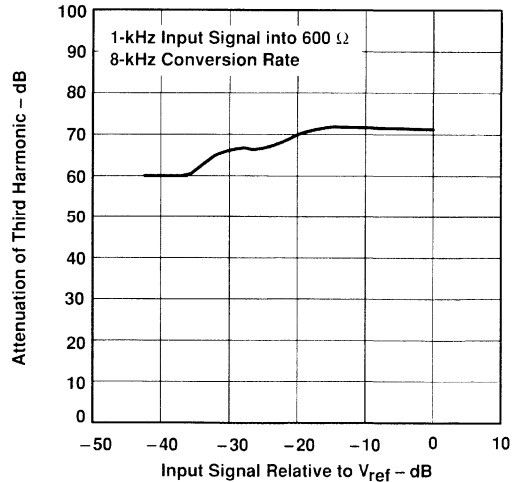


Figure 15

NOTE: Test conditions are V_{CC+} , V_{CC-} , and V_{DD} within recommended operating conditions set clock $f = 288 \text{ kHz} \pm 2\%$, and $T_A = 25 \text{ }^\circ\text{C}$.

TLC32040C, TLC32040I, TLC32041C, TLC32041I
ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

APPLICATION INFORMATION

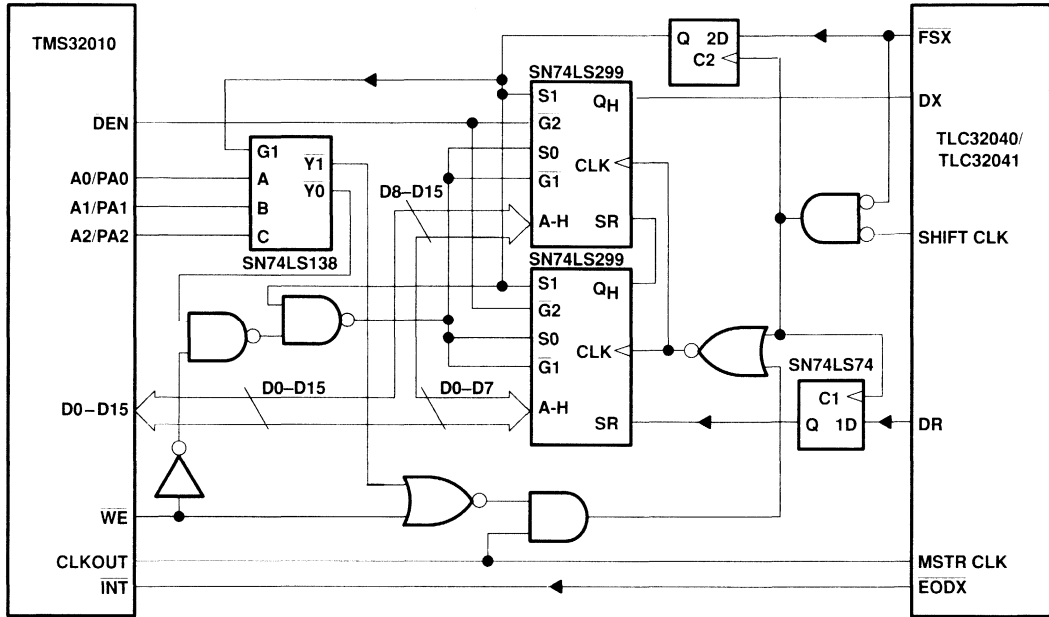


Figure 16. TMS32010-TLC32040/TLC32041 Interface Circuit

TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

APPLICATION INFORMATION

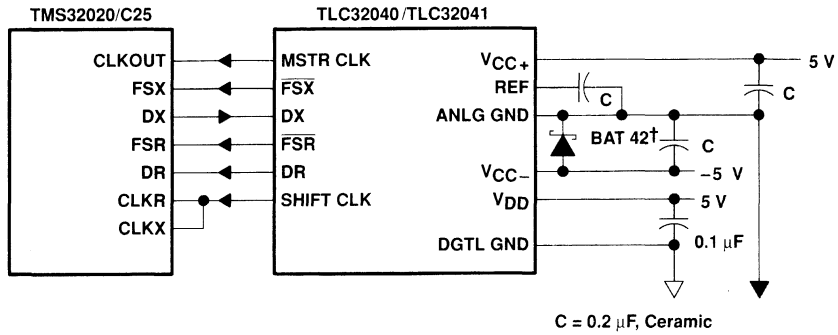


Figure 17. AIC Interface to the TMS32020/C25 Showing Decoupling Capacitors and Schottky Diode†

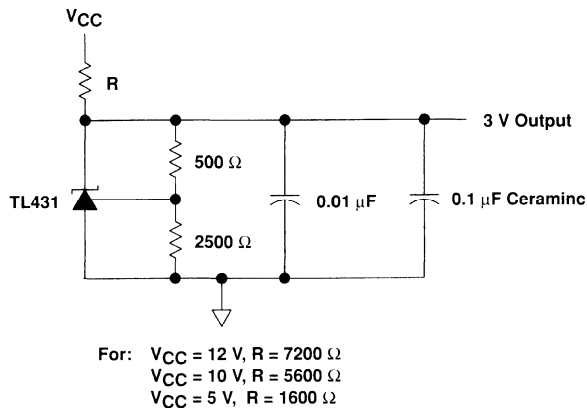


Figure 18. External Reference Circuit For TLC32045

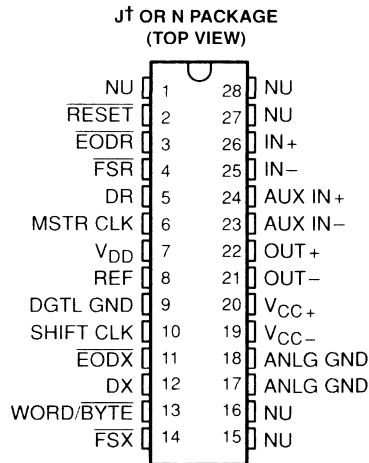
TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

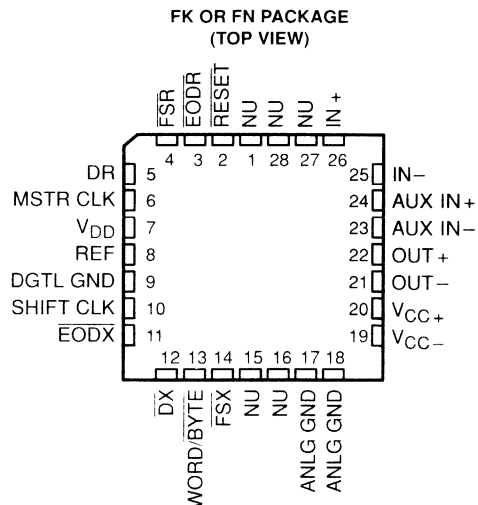
- 14-Bit Dynamic Range ADC and DAC
- 2's Complement Format
- Variable ADC and DAC Sampling Rate Up to 19,200 Samples per Second
- Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter
- Serial Port for Direct Interface to TMS(SMJ)320C17, TMS(SMJ)32020, TMS(SMJ)320C25, and TMS320C30 Digital Signal Processors
- Synchronous or Asynchronous ADC and DAC Conversion Rates With Programmable Incremental ADC and DAC Conversion Timing Adjustments
- Serial Port Interface to SN74(54)299 Serial-to-Parallel Shift Register for Parallel Interface to TMS(SMJ)32010, TMS(SMJ)320C15, or Other Digital Processors
- Internal Reference for Normal Operation and External Purposes, or Can Be Overridden by External Reference
- CMOS Technology

description

The TLC32044 and TLC32045 are complete analog-to-digital and digital-to-analog input and output systems on single monolithic CMOS chips. The TLC32044 and TLC32045 integrate a bandpass switched-capacitor antialiasing input filter, a 14-bit-resolution A/D converter, four microprocessor-compatible serial port modes, a 14-bit-resolution D/A converter, and a low-pass switched-capacitor output-reconstruction filter. The devices offer numerous combinations of master clock input frequencies and conversion/sampling rates, which can be changed via digital processor control.



† Refer to the mechanical data for the JT package.



NU – Nonusable: no external connection should be made to these terminals (see Table 2).

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

AVAILABLE OPTIONS

T _A	PACKAGE			
	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)	CERAMIC DIP (J)	CHIP CARRIER (FK)
0°C to 70°C	TLC32044CFN	TLC32044CN		
	TLC32045CFN	TLC32045CN		
-20°C to 85°C	TLC32044EFN			
-40°C to 85°C		TLC32044IN		
		TLC32045IN		
-55°C to 125°C			TLC32044MJ	TLC32044MFK

description (continued)

Typical applications for the TLC32044 and TLC32045 include speech encryption for digital transmission, speech recognition/ storage systems, speech synthesis, modems (7.2-, 8-, 9.6-, 14.4-, and 19.2-kHz sampling rate), analog interface for digital signal processors (DSPs), industrial process control, biomedical instrumentation, acoustical signal processing, spectral analysis, data acquisition, and instrumentation recorders. Four serial modes, which allow direct interface to the TMS(SMJ)320C17, TMS(SMJ)32020, TMS(SMJ)320C25, and TMS(SMJ)320C30 digital signal processors, are provided. Also, when the transmit and receive sections of the analog interface circuit (AIC) are operating synchronously, it will interface to two SN74(54)299 serial-to-parallel shift registers. These serial-to-parallel shift registers can then interface in parallel to the TMS(SMJ)32010, TMS(SMJ)320C15, and other digital signal processors, or external FIFO circuitry. Output data pulses are emitted to inform the processor that data transmission is complete or to allow the DSP to differentiate between two transmitted bytes. A flexible control scheme is provided so that the functions of the TLC32044 or TLC32045 can be selected and adjusted coincidentally with signal processing via software control.

The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When only low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable, auxiliary, differential analog input is provided for applications where more than one analog input is required.

The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the TLC32044 or TLC32045. The internal voltage reference is brought out to a terminal and is available to the designer. Separate analog and digital voltage supplies and grounds are provided to minimize noise and ensure a wide dynamic range. Also, the analog circuit path contains only differential circuitry to keep noise to an absolute minimum. The only exception is the DAC sample and hold, which utilizes pseudo-differential circuitry.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order $(\sin x)/x$ correction filter and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the digitally encoded signal. The on-board $(\sin x)/x$ correction filter can be switched out of the signal path using digital signal processor control, if desired.

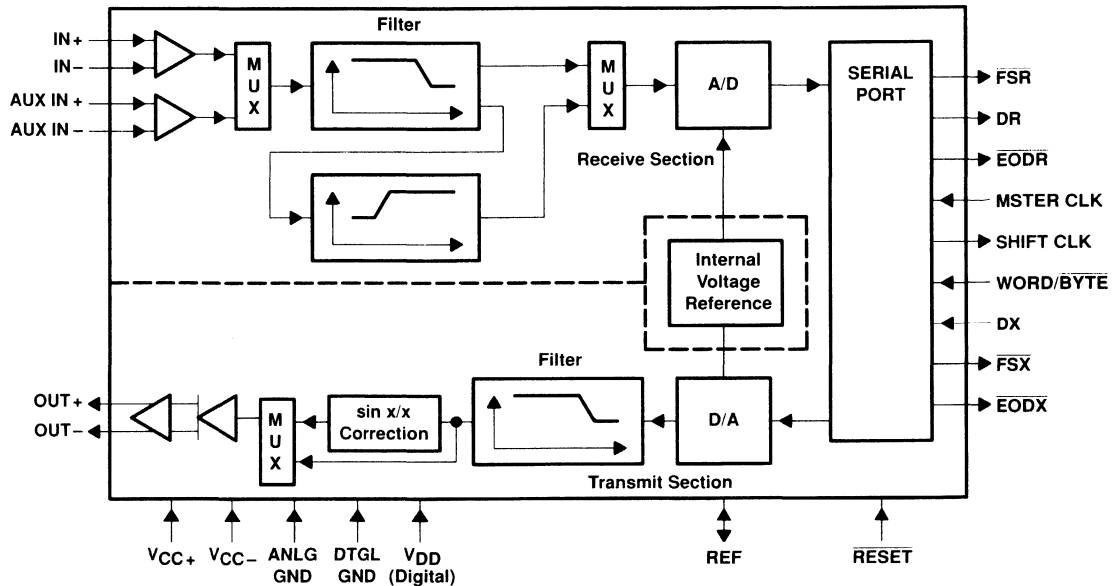
The TLC32044C and TLC32045C are characterized for operation from 0°C to 70°C. The TLC32044E is characterized for operation from -20°C to 85°C. The TLC32044I and TLC32045I are characterized for operation from -40°C to 85°C. The TLC32044M is characterized for operation from -55°C to 125°C.



TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN+	24	I	Noninverting auxiliary analog input stage. AUX IN+ can be switched into the bandpass filter and A/D converter path via software control. If the appropriate bit in the control register is a 1, the auxiliary inputs will replace the IN+ and IN- inputs. If the bit is a 0, the IN+ and IN- inputs will be used (see the AIC DX data word format section).
AUX IN-	23	I	Inverting auxiliary analog input (see the above AUX IN+ description).
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
DR	5	O	Data receive. DR is used to transmit the ADC output bits from the AIC to the TMS320 (SMJ320) serial port. This transmission of bits from the AIC to the TMS320 (SMJ320) serial port is synchronized with the SHIFT CLK signal.
DX	12	I	Data transmit. DX is used to receive the DAC input bits and timing and control information from the TMS320 (SMJ320). This serial transmission from the TMS320 (SMJ320) serial port to the AIC is synchronized with the SHIFT CLK signal.
EODR	3	O	End of data receive. (See the WORD/BYTE description and Serial Port Timing diagram.) During the word-mode timing, EODR is a low-going pulse that occurs immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 (SMJ320) serial port. EODR can be used to interrupt a microprocessor upon completion of serial communications. Also, EODR can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, EODR goes low after the first byte has been transmitted from the AIC to the TMS320 (SMJ320) serial port and is kept low until the second byte has been transmitted. The DSP can use this low-going signal to differentiate between the two bytes as to which is first and which is second. EODR does not occur after secondary communication.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I

VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

Terminal Functions (continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
EODX	11	O	End of data transmit. (See the WORD/BYTE description and Serial Port Timing diagram.) During the word-mode timing, EODX is a low-going pulse that occurs immediately after the 16 bits of D/A converter and control or register information have been transmitted from the TMS320 (SMJ320) serial port to the AIC. EODX can be used to interrupt a microprocessor upon the completion of serial communications. Also, EODX can be used to strobe and enable external serial-to-parallel shift registers, latches, or an external FIFO RAM, and to facilitate parallel data-bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, EODX goes low after the first byte has been transmitted from the TMS320 (SMJ320) serial port to the AIC and is kept low until the second byte has been transmitted. The DSP can use this low-going signal to differentiate between the two bytes as to which is first and which is second.
FSR	4	O	Frame sync receive. In the serial transmission modes, which are described in the WORD/BYTE description, FSR is held low during bit transmission. When FSR goes low, the TMS320 (SMJ320) serial port begins receiving bits from the AIC via DR of the AIC. The most significant DR bit is present on DR before FSR goes low. (See Serial Port Timing and Internal Timing Configuration diagrams.) FSR does not occur after secondary communications.
FSX	14	O	Frame sync transmit. When FSX goes low, the TMS320 (SMJ320) serial port begins transmitting bits to the AIC via DX of the AIC. In all serial transmission modes, which are described in the WORD/BYTE description, FSX is held low during bit transmission (see Serial Port Timing and Internal Timing Configuration diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN-	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	Master clock. MSTR CLK is used to derive all the key logic signals of the AIC, such as the shift clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these key signals are synchronous submultiples of the master clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the A/D and D/A converters (see the Internal Timing Configuration diagram).
OUT+	22	O	Noninverting output of analog output power amplifier. OUT+ can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
OUT-	21	O	Inverting output of analog output power amplifier. OUT- is functionally identical with and complementary to OUT+.
REF	8	I/O	Internal voltage reference. An internal reference voltage is brought out on REF. An external voltage reference can also be applied to REF.
RESET	2	I	Reset function. RESET is provided to initialize the TA, TA', TB, RA, RA', RB, and control registers. A reset initiates serial communications between the AIC and DSP. A reset initializes all AIC registers including the control register. After a negative-going pulse on RESET, the AIC registers are initialized to provide an 8-kHz data conversion rate for a 5.184-MHz master clock input signal. The conversion rate adjust registers, TA' and RA', are reset to 1. The control register bits are reset as follows (see AIC DX data word format section): d9 = 1, d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1. This initialization allows normal serial-port communication to occur between the AIC and DSP.
SHIFT CLK	10	O	Shift clock. SHIFT CLK is obtained by dividing the master clock signal frequency by four. SHIFT CLK is used to clock the serial data transfers of the AIC, described in the WORD/BYTE description below (see the Serial Port Timing and Internal Timing Configuration diagrams).
V _{DD}	7		Digital supply voltage, 5 V ±5%
V _{CC+}	20		Positive analog supply voltage, 5 V ±5%
V _{CC-}	19		Negative analog supply voltage, -5 V ±5%

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

Terminal Functions (continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
WORD/BYTE	13	I	<p>Used in conjunction with a bit in the control register, WORD/BYTE is used to establish one of four serial modes. These four serial modes are described below.</p> <p><i>AIC transmit and receive sections are operated asynchronously.</i></p> <p>The following description applies when the AIC is configured to have asynchronous transmit and receive sections. If the appropriate data bit in the control register is a 0 (see the AIC DX data word format section), the transmit and receive sections are asynchronous.</p> <ul style="list-style-type: none"> L Serial port directly interfaces with the serial port of the DSP and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams): <ol style="list-style-type: none"> 1. FSX or FSR is brought low. 2. One 8-bit byte is transmitted or one 8-bit byte is received. 3. EODX or EODR is brought low. 4. FSX or FSR emits a positive frame-sync pulse that is four shift clock cycles wide. 5. One 8-bit byte is transmitted or one 8-bit byte is received. 6. EODX or EODR is brought high. 7. FSX or FSR is brought high. H Serial port directly interfaces with the serial ports of the TMS(SMJ)32020, TMS(SMJ)320C25, or TMS(SMJ)320C30, and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): <ol style="list-style-type: none"> 1. FSX or FSR is brought low. 2. One 16-bit word is transmitted or one 16-bit word is received. 3. FSX or FSR is brought high. 4. EODX or EODR emits a low-going pulse. <p><i>AIC transmit and receive sections are operated synchronously.</i></p> <p>If the appropriate data bit in the control register is 1, the transmit and receive sections are configured to be synchronous. In this case, the bandpass switched-capacitor filter and the A/D conversion timing are derived from the TX counter A, TX counter B, and TA, TA', and TB registers, rather than the RX counter A, RX counter B, and RA, RA', and RB registers. In this case, the AIC FSX and FSR timing are identical during primary data communication; however, FSR is not asserted during secondary data communication since there is no new A/D conversion result. The synchronous operation sequences are as follows (see Serial Port Timing diagrams).</p> <ul style="list-style-type: none"> L Serial port directly interfaces with the serial port of the DSP and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams): <ol style="list-style-type: none"> 1. FSX and FSR are brought low. 2. One 8-bit byte is transmitted and one 8-bit byte is received. 3. EODX and EODR are brought low. 4. FSX and FSR emit positive frame-sync pulses that are four shift clock cycles wide. 5. One 8-bit byte is transmitted and one 8-bit byte is received. 6. EODX and EODR are brought high. 7. FSX and FSR are brought high. H Serial port directly interfaces with the serial port of the TMS(SMJ)32020, TMS(SMJ)320C25, or TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): <ol style="list-style-type: none"> 1. FSX and FSR are brought low. 2. One 16-bit word is transmitted and one 16-bit word is received. 3. FSX and FSR are brought high. 4. EODX or EODR emit low-going pulses. <p>Since the transmit and receive sections of the AIC are now synchronous, the AIC serial port with additional NOR and AND gates interface to two SN74(54)299 serial-to-parallel shift registers. Interfacing the AIC to the SN74(54)299 shift register allows the AIC to interface to an external FIFO RAM and facilitates parallel, data bus communications between the AIC and the digital signal processor. The operation sequence is the same as the above sequence (see Serial Port Timing diagrams).</p>



TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I

VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

PRINCIPLES OF OPERATION

analog input

Two sets of analog inputs are provided. Normally, the IN+ and IN– input set is used; however, the auxiliary input set, AUX IN + and AUX IN–, can be used if a second input is required. Each input set can be operated in either differential or single-ended modes, since sufficient common-mode range and rejection are provided. The gain for the IN +, IN–, AUX IN +, and AUX IN– inputs can be programmed to be either 1, 2, or 4 (see Table 2). Either input circuit can be selected via software control. It is important to note that a wide dynamic range is assured by the differential internal analog architecture and by the separate analog and digital voltage supplies and grounds.

A/D bandpass filter, A/D bandpass filter clocking, and A/D conversion timing

The A/D high-pass filter can be selected or bypassed via software control. The frequency response of this filter is presented in the following pages. This response results when the switched-capacitor filter clock frequency is 288 kHz and the A/D sample rate is 8 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the low-pass filter transfer function is frequency scaled by the ratio of the actual clock frequency to 288 kHz. The ripple bandwidth and 3-dB low-frequency roll-off points of the high-pass section are 150 Hz and 100 Hz, respectively. However, the high-pass section low-frequency roll-off is frequency scaled by the ratio of the A/D sample rate to 8 kHz.

The internal timing configuration and AIC DX data word format sections of this data sheet indicate the many options for attaining a 288-kHz bandpass switched-capacitor filter clock. These sections indicate that the RX counter A can be programmed to give a 288-kHz bandpass switched-capacitor filter clock for several master clock input frequencies.

The A/D conversion rate is then attained by frequency dividing the 288-kHz bandpass switched-capacitor filter clock with the RX counter B. Unwanted aliasing is prevented because the A/D conversion rate is an integral submultiple of the bandpass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

A/D converter performance specifications

Fundamental performance specifications for the A/D converter circuitry are presented in the A/D converter operating characteristics section of this data sheet. The realization of the A/D converter circuitry with switched-capacitor techniques provides an inherent sample-and-hold.

analog output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

D/A low-pass filter, D/A low-pass filter clocking, and D/A conversion timing

The frequency response of this filter is presented in the following pages. This response results when the low-pass switched-capacitor filter clock frequency is 288 kHz. Like the A/D filter, the transfer function of this filter is frequency scaled when the clock frequency is not 288 kHz. A continuous-time filter is provided on the output of the $(\sin x)/x$ correction filter to eliminate the periodic sample data signal information, which occurs at multiples of the 288-kHz switched-capacitor filter clock. The continuous time filter also greatly attenuates any switched-capacitor clock feedthrough.



PRINCIPLES OF OPERATION

D/A low-pass filter, D/A low-pass filter clocking, and D/A conversion timing (continued)

The D/A conversion rate is attained by frequency dividing the 288-kHz switched-capacitor filter clock with TX Counter B. Unwanted aliasing is prevented because the D/A conversion rate is an integral submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

asynchronous versus synchronous operation

If the transmit section of the AIC (low-pass filter and DAC) and receive section (bandpass filter and ADC) are operated asynchronously, the low-pass and bandpass filter clocks are independently generated from the master clock signal. Also, the D/A and A/D conversion rates are independently determined. If the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and bandpass filters. In synchronous operation, the A/D conversion timing is derived from, and is equal to, the D/A conversion timing (see description of the WORD/BYTE in the Terminal Functions table.)

D/A converter performance specifications

Fundamental performance specifications for the D/A converter circuitry are presented in the D/A converter operating characteristics section of the data sheet. The D/A converter has a sample-and-hold that is realized with a switched-capacitor ladder.

system frequency response correction

The $(\sin x)/x$ correction for the D/A converter zero-order sample-and-hold output can be provided by an on-board second-order $(\sin x)/x$ correction filter. This $(\sin x)/x$ correction filter can be inserted into or deleted from the signal path by digital signal processor control. When inserted, the $(\sin x)/x$ correction filter follows the switched-capacitor low-pass filter. When the TB register (see Internal Timing Configuration section) equals 36, the correction results of Figures 11 and 12 can be obtained.

The $(\sin x)/x$ correction can also be accomplished by deleting the on-board second-order correction filter and performing the $(\sin x)/x$ correction in digital signal processor software. The system frequency response can be corrected via DSP software to ± 0.1 -dB accuracy to a band edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, which requires only seven TMS320 (SMJ320) instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of only 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the $(\sin x)/x$ correction section for more details).

serial port

The serial port has four possible modes that are described in detail in the Terminal Functions table. These modes are briefly described below and in the functional description for WORD/BYTE.

- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the DSP.
- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS(SMJ)32020, TMS(SMJ)320C25, and the TMS(SMJ)320C30.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the DSP.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS(SMJ)32020, TMS(SMJ)320C25, TMS(SMJ)320C30, or two SN74(54)299 serial-to-parallel shift registers, which can then interface in parallel to the TMS(SMJ)32010, TMS(SMJ)320C15, and SMJ320E15 to any other digital signal processor or to external FIFO circuitry.

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

PRINCIPLES OF OPERATION

operation of TLC32044 or TLC32045 with internal voltage reference

The internal reference eliminates the need for an external voltage reference and provides overall circuit cost reduction. Thus, the internal reference eases the design task and provides complete control over device performance. The internal reference is brought out to a terminal and is available to the designer. To keep the amount of noise on the reference signal to a minimum, an external capacitor can be connected between REF and ANLG GND.

operation of TLC32044 or TLC32045 with external voltage reference

REF can be driven from an external reference circuit. This external circuit must be capable of supplying 250 μ A and must be adequately protected from noise such as crosstalk from the analog input.

reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on $\overline{\text{RESET}}$, the AIC is initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX data word format section).

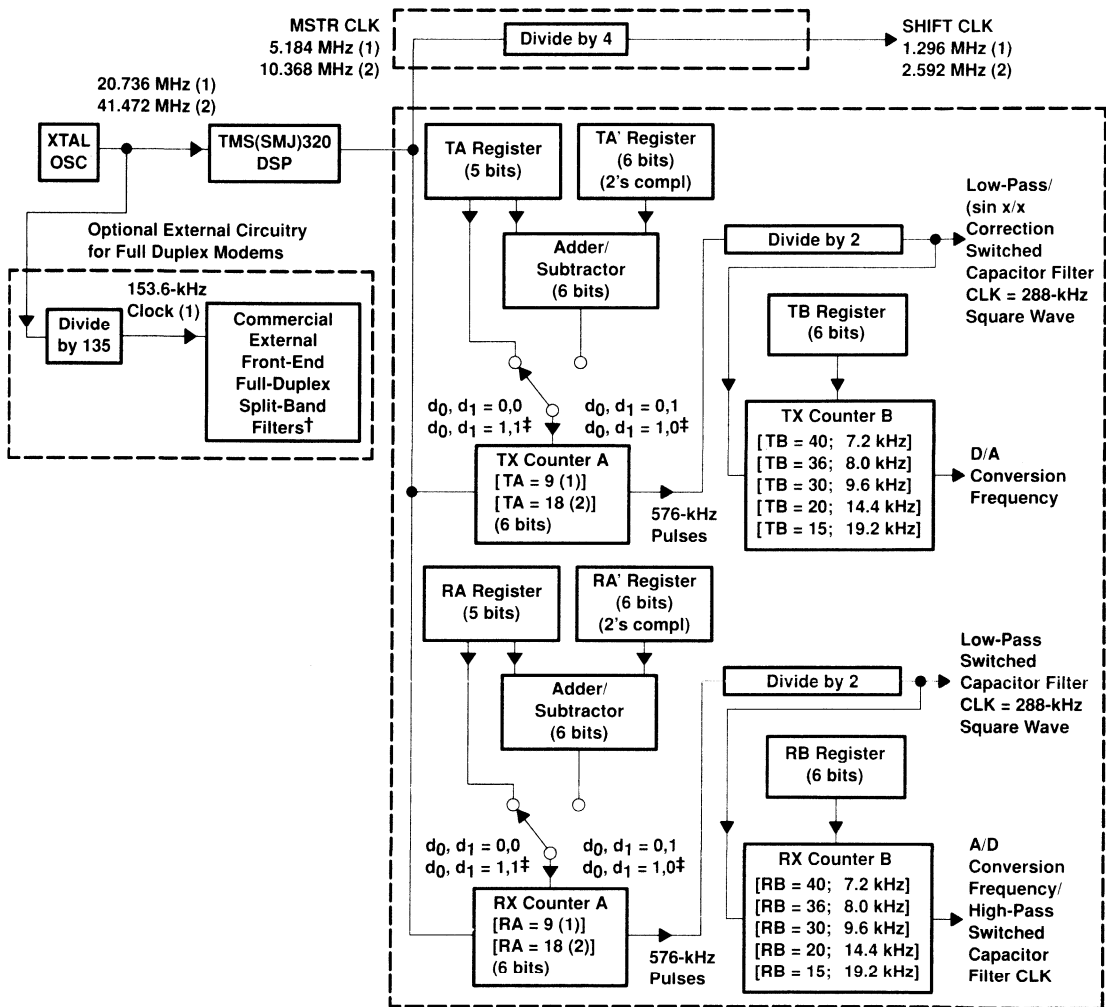
loopback

This feature allows the user to test the circuit remotely. In loopback, OUT+ and OUT– are internally connected to the IN+ and IN–. Thus, the DAC bits (d15 to d2), which are transmitted to DX, can be compared with the ADC bits (d15 to d2), which are received from DR. An ideal comparison would be that the bits on DR equal the bits on DX. However, there are some difference in these bits due to the ADC and DAC output offsets. The loopback feature is implemented with digital signal processor control by transmitting the appropriate serial port bit to the control register (see AIC DX data word format section).

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

INTERNAL TIMING CONFIGURATION



† Split-band filtering can alternatively be performed after the analog input function via software in the TMS(SMJ)320.

‡ These control bits are described in the AIC DX data word format section.

NOTE: Frequency 1 (20.736 MHz) is used to show how 153.6 kHz (for a commercially available modem split-band filter clock), popular speech and modem sampling signal frequencies, and an internal 288-kHz switched-capacitor filter clock can be derived synchronously and as submultiples of the crystal oscillator frequency. Since these derived frequencies are synchronous submultiples of the crystal frequency, aliasing does not occur as the sampled analog signal passes between the analog converter and switched-capacitor filter stages. Frequency 2 (41.472 MHz) is used to show that the AIC can work with high-frequency signals, which are used by high-speed digital signal processors.



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TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I

VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

explanation of internal timing configuration

All of the internal timing of the AIC is derived from the high-frequency clock signal that drives the master clock input. The shift clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the master clock input signal frequency by four.

Low-pass:

$$\text{SCF Clock Frequency (D/A or A/D path)} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

$$\text{Conversion Frequency} = \frac{\text{SCF Clock Frequency (D/A or A/D path)}}{\text{Contents of Counter B}}$$

High-pass:

$$\text{SCF Clock Frequency (A/D Path)} = \text{A/D Conversion Frequency}$$

$$\text{Shift Clock Frequency} = \frac{\text{Master Clock Frequency}}{4}$$

TX counter A and TX counter B, which are driven by the master clock, determine the D/A conversion timing. Similarly, RX counter A and RX counter B determine the A/D conversion timing. In order for the low-pass switched-capacitor filter in the D/A path to meet its transfer function specifications, the frequency of its clock input must be 288 kHz. If the clock frequency is not 288 kHz, the filter transfer function frequencies are frequency-scaled by the ratios of the clock frequency to 288 kHz. Thus, to obtain the specified filter response, the combination of master clock frequency and TX counter A and RX counter A values must yield a 288-kHz switched-capacitor clock signal. This 288-kHz clock signal can then be divided by the TX counter B to establish the D/A conversion timing.

The transfer function of the bandpass switched-capacitor filter in the A/D path is a composite of its high-pass and low-pass section transfer functions. The high-frequency roll-off of the low-pass section meets the bandpass filter transfer function specification when the low-pass section SCF is 288 kHz. Otherwise, the high-frequency roll-off will be frequency-scaled by the ratio of the high-pass section's SCF clock to 288 kHz. The low-frequency roll-off of the high-pass section meets the bandpass filter transfer function specification when the A/D conversion rate is 8 kHz. Otherwise, the low-frequency roll-off of the high-pass section is frequency-scaled by the ratio of the A/D conversion rate to 8 kHz.

TX counter A and TX counter B are reloaded every D/A conversion period, while RX counter A and RX counter B are reloaded every A/D conversion period. The TX counter B and RX counter B are loaded with the values in the TB and RB registers, respectively. Via software control, the TX counter A can be loaded with either the TA register, the TA register less the TA' register, or the TA register plus the TA' register. By selecting the TA register less the TA' register option, the upcoming conversion timing occurs earlier by an amount of time that equals TA' times the signal period of the master clock. By selecting the TA register plus the TA' register option, the upcoming conversion timing occurs later by an amount of time that equals TA' times the signal period of the master clock. The D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. In this case, however, the RX counter A can be programmed via software control with the RA register, the RA register less the RA' register, or the RA register plus the RA' register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing. This feature can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.



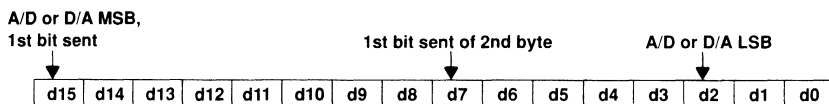
TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

explanation of internal timing configuration (continued)

If the transmit and receive sections are configured to be synchronous (see WORD/BYTE description), then both the low-pass and bandpass switched-capacitor filter clocks are derived from TX counter A. Also, both the D/A and A/D conversion timing are derived from the TX counter A and TX counter B. When the transmit and receive sections are configured to be asynchronous, the RX counter A, RX counter B, RA register, RA' register, and RB registers are not used.

AIC DR or DX word bit pattern



AIC DX data word format section

d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	Comments	
primary DX serial communication protocol																	
←d15 (MSB) through d2 go to the D/A converter register														→	0	0	The TX and RX counter As are loaded with the TA and RA register values. The TX and RX counter Bs are loaded with TB and RB register values.
←d15 (MSB) through d2 go to the D/A converter register														→	0	1	The TX and RX counter As are loaded with the TA + TA' and RA + RA' register values. The TX and RX counter Bs are loaded with the TB and RB register values. LSBs d1 = 0 and d0 = 1 cause the next D/A and A/D conversion periods to be changed by the addition of TA' and RA' master clock cycles, in which TA' and RA' can be positive or negative or zero (refer to Table 1).
←d15 (MSB) through d2 go to the D/A converter register														→	1	0	The TX and RX counter As are loaded with the TA – TA' and RA – RA' register values. The TX and RX counter Bs are loaded with the TB and RB register values. LSBs d1 = 1 and d0 = 0 cause the next D/A and A/D conversion periods to be changed by the subtraction of TA' and RA' master clock cycles, in which TA' and RA' can be positive or negative or zero (refer to Table 1).
←d15 (MSB) through d2 go to the D/A converter register														→	1	1	The TX and RX counter As are loaded with the TA and RA register converter register values. The TX and RX counter Bs are loaded with the TB and RB register values. After a delay of four shift clock cycles, a secondary transmission immediately follows to program the AIC to operate in the desired configuration.

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (primary communications) to the AIC initiates secondary communications upon completion of the primary communications. Upon completion of the primary communication, \overline{FSX} remains high for four shift clock cycles and then goes low and initiates the secondary communication. The timing specifications for the primary and secondary communications are identical. In this manner, the secondary communication, if initiated, is interleaved between successive primary communications. This interleaving prevents the secondary communication from interfering with the primary communications and DAC timing, thus preventing the AIC from skipping a DAC output. In the synchronous mode, \overline{FSR} is not asserted during secondary communications.



TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I

VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

secondary DX serial communication protocol

x x ← to TA register → x x ← to RA register →	0 0	d13 and d6 are MSBs (unsigned binary)
x ← to TA' register → x ← to RA' register →	0 1	d14 and d7 are 2's complement sign bits
x ← to TB register → x ← to RB register →	1 0	d14 and d7 are MSBs (unsigned binary)
x x x x x x x d9 x d7 d6 d5 d4 d3 d2 1 1		
		d2 = 0/1 deletes/inserts the A/D high-pass filter d3 = 0/1 disables/enables the loopback function d4 = 0/1 disables/enables the AUX IN+ and AUX IN- d5 = 0/1 asynchronous/synchronous transmit and receive sections d6 = 0/1 gain control bits (see gain control section) d7 = 0/1 gain control bits (see gain control section) d9 = 0/1 delete/insert on-board second-order (sin x)/x correction filter

reset function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on **RESET** initializes the AIC registers to provide an 8-kHz A/D and D/A conversion rate for a 5.184 MHz master clock input signal. The AIC, except the control register, is initialized as follows (see AIC DX data word format section):

REGISTER	INITIALIZED REGISTER VALUE (HEX)
TA	9
TA'	1
TB	24
RA	9
RA'	1
RB	24

The control register bits are reset as follows (see AIC DX data word format section):

$$d9 = 1, d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1$$

This initialization allows normal serial port communications to occur between AIC and DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA', and TB register need to be programmed, since both transmit and receive timing are synchronously derived from these registers (see the terminal functions table and AIC DX word format sections).

The circuit shown in Figure 1 provides a reset on power up when power is applied in the sequence given under power-up sequence. The circuit depends on the power supplies reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.

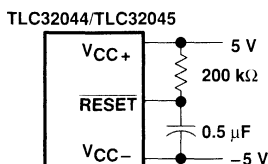


Figure 1. Power-Up Reset

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

power-up sequence

To ensure proper operation of the AIC and as a safeguard against latch-up, it is recommended that Schottky diodes with forward voltages less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND and from V_{CC-} to DGTL GND (see Figure 21). In the absence of such diodes, power should be applied in the following sequence: ANLG GND and DGTL GND, V_{CC-} , then V_{CC+} and V_{DD} . Also, no input signal should be applied until after power up.

AIC responses to improper conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 1 below.

AIC register constraints

The following constraints are placed on the contents of the AIC registers:

1. TA register must be ≥ 4 in word mode (WORD/ $\overline{\text{BYTE}}$ = high).
2. TA register must be ≥ 5 in byte mode (WORD/ $\overline{\text{BYTE}}$ = low).
3. TA' register can be either positive, negative, or zero.
4. RA register must be ≥ 4 in word mode (WORD/ $\overline{\text{BYTE}}$ = high).
5. RA register must be ≥ 5 in byte mode (WORD/ $\overline{\text{BYTE}}$ = low).
6. RA' register can be either positive, negative, or zero.
7. (TA register \pm TA' register) must be > 1 .
8. (RA register \pm RA' register) must be > 1 .
9. TB register must be > 1 .

Table 1. AIC Responses to Improper Conditions

IMPROPER CONDITION	AIC RESPONSE
TA register + TA' register = 0 or 1 TA register - TA' register = 0 or 1	Reprogram TX counter A with TA register value
TA register + TA' register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into the TX counter A. i.e., TA register + TA' register + 40 hex is loaded into TX counter A.
RA register + RA' register = 0 or 1 RA register - RA' register = 0 or 1	Reprogram RX counter A with RA register value
RA register + RA' register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX counter A. i.e., RA register + RA' register + 40 hex is loaded into RX counter A.
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down.
TA register < 4 in word mode TA register < 5 in byte mode RA register < 4 in word mode RA register < 5 in byte mode	The AIC serial port no longer operates.
TB register = 0 or 1	Reprogram TB register with 24 hex
RB register = 0 or 1	Reprogram RB register with 24 hex
AIC and DSP cannot communicate	Hold last DAC output



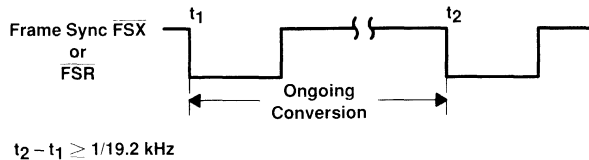
TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I

VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

improper operation due to conversion times being too close together

If the difference between two successive D/A conversion frame syncs is less than 1/19.2 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A' register or A - A' register result is too small. When incrementally adjusting the conversion period via the A + A' register options, the designer should be careful not to violate this requirement (see following diagram).



asynchronous operation — more than one receive frame sync occurring between two transmit frame syncs

When incrementally adjusting the conversion period via the A + A' or A - A' register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during a $\overline{\text{FSX}}$ frame sync. The ongoing conversion period is then adjusted. However, either receive conversion period A or B can be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. Therefore, if there is sufficient time between t_1 and t_2 , the receive conversion period adjustment is performed during receive conversion period A. Otherwise, the adjustment is performed during receive conversion period B. The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent FSX frame (see figure below).

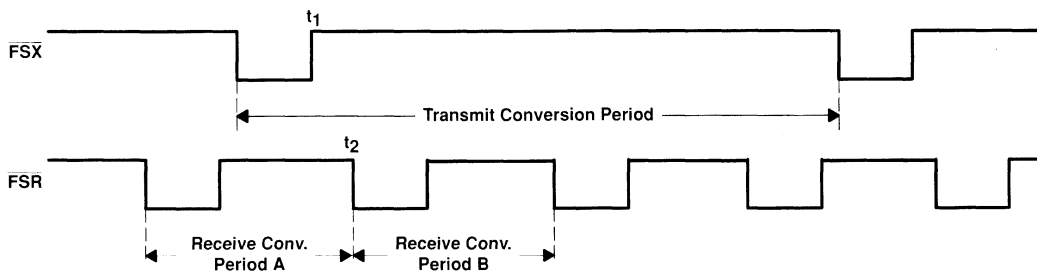


Figure 2. Adjusted Transmit and Receive Conversion Periods

asynchronous operation — more than one transmit frame sync occurring between two receive frame syncs

When incrementally adjusting the conversion period via the A + A' or A - A' register options, a specific protocol is followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during a $\overline{\text{FSX}}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment in the diagram as shown in the following figure. If the adjustment command is issued during transmit conversion period A, receive conversion period A is adjusted if there is sufficient time between t_1 and t_2 . If there is not sufficient time between t_1 and t_2 , receive conversion period B is adjusted. The receive portion of an adjustment command can be

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

ignored if the adjustment command is sent during a receive conversion period, which is already being or will be adjusted due to a prior adjustment command. For example, if adjustment commands are issued during transmit conversion periods A, B, and C, the first two commands can cause receive conversion periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during receive conversion period B, which already is adjusted via the transmit conversion period B adjustment command.

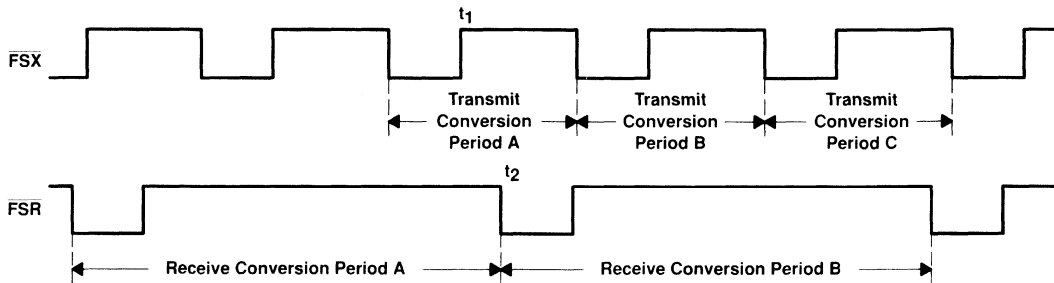


Figure 3. Receive and Transmit Conversion Period Adjustments

asynchronous operation — more than one set of primary and secondary DX serial communication occurring between two receive frame sync (see AIC DX data word format section)

The TA, TA', TB, and control register information that is transmitted in the secondary communications is always accepted and is applied during the ongoing transmit conversion period. If there is sufficient time between t_1 and t_2 , the TA, RA', and RB register information, which is sent during transmit conversion period A, is applied to receive conversion period A. Otherwise, this information is applied during receive conversion period B. If RA, RA', and RB register information has already been received and is being applied during an ongoing conversion period, any subsequent RA, RA', or RB information that is received during this receive conversion period is disregarded (see Figure 4).

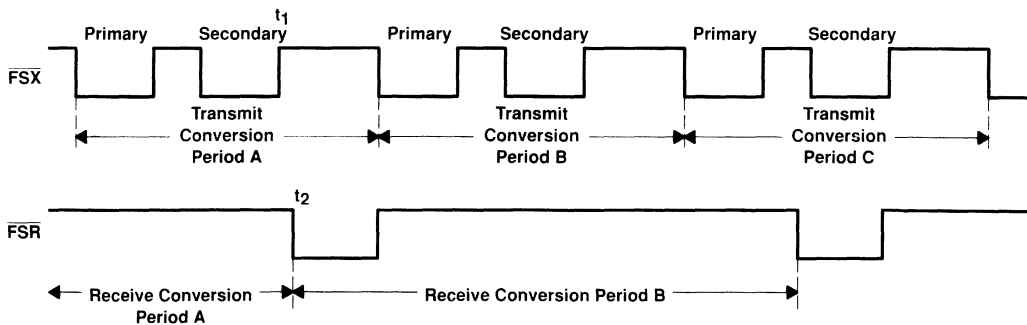


Figure 4. Receive and Transmit Periods for Primary and Secondary Data

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I

VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

test modes†

The TLC32044 or TLC32045 can be operated in special test modes. These test modes are used by Texas Instruments to facilitate testing of the device during manufacturing. They are not intended to be used in real applications; however, they allow the filters in the A/D and D/A paths to be used without using the A/D and D/A converters.

In normal operation, the nonusable (NU) terminals are left unconnected. These NU terminals are used by the factory to speed up testing of the TLC32044 or TLC32045 analog interface circuits (AIC). When the device is used in normal (non-test mode) operation, the NU terminal (terminal 1) has an internal pulldown to -5 V. Externally connecting 0 V or 5 V to terminal 1 puts the device in test-mode operation. Selecting one of the possible test modes is accomplished by placing a particular voltage on certain terminals. A description of these modes is provided in Table 2 and Figures 5 and 6.

Table 2. List of Test Modes

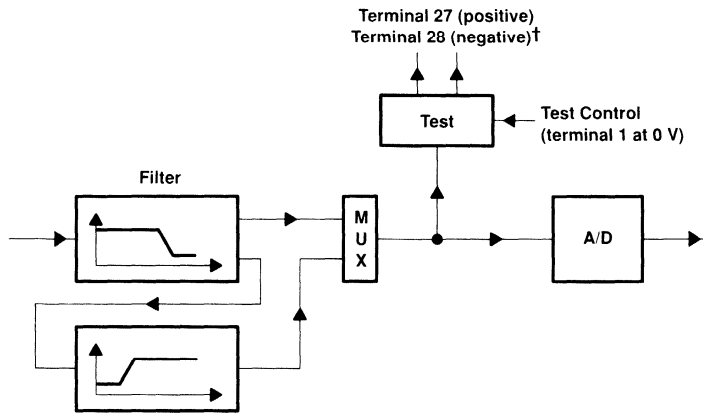
TEST TERMINALS	D/A PATH TEST (TERMINAL 1 to 5 V)	A/D PATH TEST (TERMINAL 1 to 0)
	TEST FUNCTION	TEST FUNCTION
5	The low-pass switched-capacitor filter clock is brought out to DR. This clock signal is normally internal.	The bandpass switched-capacitor filter clock is brought out to DR. This clock signal is normally internal.
11	No change from normal operation. The \overline{EODX} signal is brought out to EODX.	The pulse that initiates the A/D conversion is brought out here. This signal is normally internal.
3	The pulse that initiates the D/A conversion is brought out here.	No change from normal operation. The \overline{EODR} signal is brought out.
27 and 28	There are no test output signals provided on these terminals.	The outputs of the A/D path low-pass or bandpass filter (depending upon control bit d2 – see AIC DX data word format section) are brought out to these terminals. If the high-pass section is inserted, the output will have a $(\sin x)/x$ droop. The slope of the droop is determined by the ADC sampling frequency, which is the high-pass section clock frequency (see diagram of bandpass or low-pass filter test for receive section). These outputs drive small (30-pF) loads.
15 and 16	D/A PATH LOW-PASS FILTER TEST: (WORD/BYTE) to -5 V	
	TEST FUNCTION	
	The inputs of the D/A path low-pass filter are brought out to terminals 15 and 16. The D/A input to this filter is removed. If $(\sin x)/x$ correction filter is inserted, the OUT+ and OUT– signals have a flat response (see Figure 2). The common-mode range of these inputs must not exceed ± 0.5 V.	

† In the test mode, the AIC responds to the setting of WORD/BYTE to -5 V, as if WORD/BYTE were set to 0 V. Thus, the byte mode is selected for communicating between DSP and AIC. Either of the path tests (D/A or A/D) can be performed simultaneously with the D/A low-pass filter test. In this situation, WORD/BYTE must be connected to -5 V, which initiates byte-mode communications.



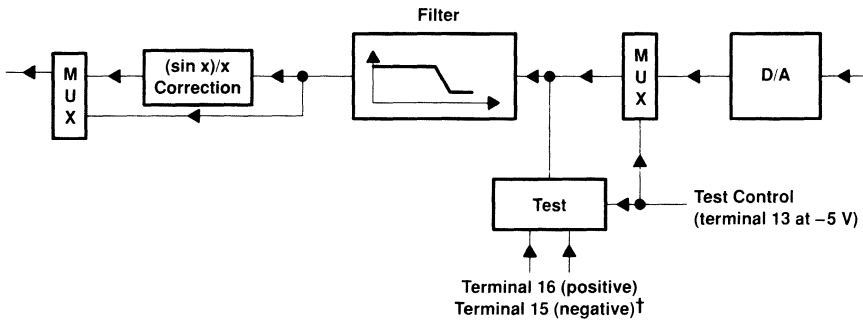
TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I
VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995



† All analog signal paths have differential architecture and hence have positive and negative components.

Figure 5. Bandpass or Low-Pass Filter Test for Receiver Section



† All analog signal paths have differential architecture and hence have positive and negative components.

Figure 6. Low-Pass Filter Test for Transmit Section

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I

VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC+} (see Note 1)	–0.3 V to 15 V
Supply voltage range, V_{DD}	–0.3 V to 15 V
Output voltage range, V_O	–0.3 V to 15 V
Input voltage range, V_I	–0.3 V to 15 V
Digital ground voltage range	–0.3 V to 15 V
Operating free-air temperature range: TLC32044C, TLC32045C	0°C to 70°C
TLC32044E	–20°C to 85°C
TLC32044I, TLC32045I	–40°C to 85°C
TLC32044M	–55°C to 125°C
Storage temperature range: TLC32044C, I, TLC32045C, I	–40°C to 125°C
TLC32044M	–65°C to 150°C
Case temperature for 10 seconds: FN or FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C
J package	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values for maximum ratings are with respect to V_{CC-} .

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)	4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)	–4.75	–5	–5.25	V
Digital supply voltage, V_{DD} (see Note 2)	4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND	0			V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)	2	4		V
High-level input voltage, V_{IH}	2	$V_{DD} + 0.3$		V
Low-level input voltage, V_{IL} (see Note 3)	–0.3	0.8		V
Load resistance at OUT+ and/or OUT–, R_L	300			Ω
Load capacitance at OUT+ and/or OUT–, C_L	100			pF
MSTR CLK frequency (see Note 4)	0.075	5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)	± 1.5			V
A/D or D/A conversion rate	20			kHz
Operating free-air temperature, T_A	TLC32044C, TLC32045C		0	°C
	TLC32044E		–20	
	TLC32044I, TLC32045I		–40	
	TLC32044M		–55	

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+} , and V_{CC-} , are with respect to the ANLG GND terminal. Voltages at digital inputs and outputs and V_{DD} are with respect to the DGTL GND terminal.

- The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.
- The bandpass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 288 kHz and the high-pass section SCF clock is 8 kHz. If the low-pass SCF clock is shifted from 288 kHz, the low-pass roll-off frequency will shift by the ratio of the low-pass SCF clock to 288 kHz. If the high-pass SCF is shifted from 8 kHz, the high-pass roll-off frequency will shift by the ratio of the high-pass SCF clock to 8 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 288 kHz. If the SCF clock is shifted from 288 kHz, the low-pass roll-off frequency will shift by the ratio of the SCF clock to 288 kHz.
- This range applies when (IN+ – IN–) or (AUX IN+ – AUX IN–) equals ± 6 V.

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

electrical characteristics over recommended operating free-air temperature range, $V_{CC+} = 5\text{ V}$, $V_{CC-} = -5\text{ V}$, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

total device, MSTR CLK frequency = 5.184 MHz, outputs not loaded

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$V_{DD} = 4.75\text{ V}$, $I_{OH} = -300\text{ }\mu\text{A}$	2.4			V
V_{OL}	Low-level output voltage	$V_{DD} = 4.75\text{ V}$, $I_{OL} = 2\text{ mA}$			0.4	
I_{CC+}	Supply current from V_{CC+}	TLC32044C, TLC32045C			35	mA
		TLC32044I, TLC32045I, TLC32044E, TLC32044M			40	
I_{CC-}	Supply current from V_{CC-}	TLC32044C, TLC32045C			-35	
		TLC32044I, TLC32045I, TLC32044E, TLC32044M			-40	
I_{DD}	Supply current from V_{DD}	TLC3204xC, E, I	$f_{\text{MSTR CLK}} = 5.184\text{ MHz}$			7
		TLC32044M				8
V_{ref}	Internal reference output voltage	TLC3204xC, E, I	3		3.3	V
		TLC32044M	2.9		3.3	
αV_{ref}	Temperature coefficient of internal reference voltage		200			ppm/°C
r_o	Output resistance at REF		100			k Ω

receive amplifier input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
A/D converter offset error (filters in)	TLC32044C, E, I			10	70	mV
	TLC32044M			10	85	
	TLC32045C, I			10	75	
CMRR	Common-mode rejection ratio at $IN+$, $IN-$, or $AUX\ IN+$, $AUX\ IN-$	TLC3204xC, E, I	See Note 6	55		dB
		TLC32044M		35	55	
r_i	Input resistance at $IN+$, $IN-$, or $AUX\ IN+$, $AUX\ IN-$, REF		100			k Ω

transmit filter output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at $OUT+$ or $OUT-$ (single-ended relative to ANLG GND)	TLC3204xC, E, I	15		80	mV
		TLC32044M	15		75	
V_{OM}	Maximum peak output voltage swing across R_L at $OUT+$ or $OUT-$ (single ended)	$R_L \geq 300\text{ }\Omega$, Offset voltage = 0	± 3			V
V_{OM}	Maximum peak output voltage swing between $OUT+$ and $OUT-$ (differential output)	$R_L \geq 600\text{ }\Omega$	± 6			

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with an 8-kHz conversion rate.



TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I

VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

system distortion specifications, SCF clock frequency = 288 kHz (see Note 7)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	Single ended	TLC3204xC, E, I	$V_I = -0.5 \text{ dB to } -24 \text{ dB referred to } V_{ref}$ $T_A = 25^\circ\text{C}$			70	dB
		TLC32044M		62	70		
	Differential	TLC32044C, E, I		62	70		
		TLC32045C, I		55	70		
Attenuation of third and higher harmonics of A/D input signal	Single ended	TLC3204xC, E, I	$V_I = -0.5 \text{ dB to } -24 \text{ dB referred to } V_{ref}$ $T_A = 25^\circ\text{C}$			65	
		TLC32044M		57	65		
	Differential	TLC32044C, E, I		57	65		
		TLC32045C, I		55	65		
Attenuation of second harmonic of D/A input signal	Single ended	TLC3204xC, I, M	$V_I = -0 \text{ dB to } -24 \text{ dB referred to } V_{ref}$			70	
	Differential	TLC32044C, E, I		62	70		
		TLC32045C, I		55	70		
Attenuation of third and higher harmonics of D/A input signal	Single ended	TLC3204xC, I, M	$V_I = -0 \text{ dB to } -24 \text{ dB referred to } V_{ref}$			65	
	Differential	TLC32044C, E, I		57	65		
		TLC32045C, I		55	65		

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 7: The test condition V_I is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance for the DAC is 600 Ω (300 Ω for TLC32044M).



TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

A/D channel signal-to-distortion ratio (see Note 7)

PARAMETER	TEST CONDITIONS	$A_V = 1^\dagger$		$A_V = 2^\dagger$		$A_V = 4^\dagger$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio, TLC32044C, TLC32044I, TLC32044E	$V_I = -6 \text{ dB to } -0.1 \text{ dB}$	58		$>58^\ddagger$		$>58^\ddagger$		dB
	$V_I = -12 \text{ dB to } -6 \text{ dB}$	58		58		$>58^\ddagger$		
	$V_I = -18 \text{ dB to } -12 \text{ dB}$	56		58		58		
	$V_I = -24 \text{ dB to } -18 \text{ dB}$	50		56		58		
	$V_I = -30 \text{ dB to } -24 \text{ dB}$	44		50		56		
	$V_I = -36 \text{ dB to } -30 \text{ dB}$	38		44		50		
	$V_I = -42 \text{ dB to } -36 \text{ dB}$	32		38		44		
	$V_I = -48 \text{ dB to } -42 \text{ dB}$	26		32		38		
	$V_I = -54 \text{ dB to } -48 \text{ dB}$	20		26		32		
A/D channel signal-to-distortion ratio, TLC32044M	$V_I = -6 \text{ dB to } -0.5 \text{ dB}$	58		$>58^\ddagger$		$>58^\ddagger$		dB
	$V_I = -12 \text{ dB to } -6 \text{ dB}$	58		58		$>58^\ddagger$		
	$V_I = -18 \text{ dB to } -12 \text{ dB}$	56		58		58		
	$V_I = -24 \text{ dB to } -18 \text{ dB}$	50		56		58		
	$V_I = -30 \text{ dB to } -24 \text{ dB}$	44		50		56		
	$V_I = -36 \text{ dB to } -30 \text{ dB}$	38		44		50		
	$V_I = -42 \text{ dB to } -36 \text{ dB}$	32		38		44		
	$V_I = -48 \text{ dB to } -42 \text{ dB}$	26		32		38		
A/D channel signal-to-distortion ratio, TLC32045C, TLC32045I	$V_I = -6 \text{ dB to } -0.1 \text{ dB}$	55		$>55^\ddagger$		$>55^\ddagger$		dB
	$V_I = -12 \text{ dB to } -6 \text{ dB}$	55		55		$>55^\ddagger$		
	$V_I = -18 \text{ dB to } -12 \text{ dB}$	53		55		55		
	$V_I = -24 \text{ dB to } -18 \text{ dB}$	47		53		55		
	$V_I = -30 \text{ dB to } -24 \text{ dB}$	41		47		53		
	$V_I = -36 \text{ dB to } -30 \text{ dB}$	35		41		47		
	$V_I = -42 \text{ dB to } -36 \text{ dB}$	29		35		41		
	$V_I = -48 \text{ dB to } -42 \text{ dB}$	23		29		35		
	$V_I = -54 \text{ dB to } -48 \text{ dB}$	17		23		29		

$^\dagger A_V$ is the programmable gain of the input amplifier.

‡ A value >60 is over range and signal clipping occurs.

NOTE 7: The test condition V_I is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{REF}). The load impedance for the DAC is 600 Ω (300 Ω for TLC32044M).



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

D/A channel signal-to-distortion ratio (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio, TLC32044C, TLC32044E, TLC32044I, TLC32044M	$V_I = -6$ dB to 0 dB	58		dB
	$V_I = -12$ dB to -6 dB	58		
	$V_I = -18$ dB to -12 dB	56		
	$V_I = -24$ dB to -18 dB	50		
	$V_I = -30$ dB to -24 dB	44		
	$V_I = -36$ dB to -30 dB	38		
	$V_I = -42$ dB to -36 dB	32		
	$V_I = -48$ dB to -42 dB	26		
$V_I = -54$ dB to -48 dB	20			
D/A channel signal-to-distortion ratio, TLC32045C, TLC32045I	$V_I = -6$ dB to 0 dB	55		
	$V_I = -12$ dB to -6 dB	55		
	$V_I = -18$ dB to -12 dB	53		
	$V_I = -24$ dB to -18 dB	47		
	$V_I = -30$ dB to -24 dB	41		
	$V_I = -36$ dB to -30 dB	35		
	$V_I = -42$ dB to -36 dB	29		
	$V_I = -48$ dB to -42 dB	23		
$V_I = -54$ dB to -48 dB	17			

NOTE 7: The test condition V_I is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance for the DAC is 600 Ω (300 Ω for TLC32044M).

gain and dynamic range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Absolute transmit gain tracking error while transmitting into 600 Ω	-48 -dB to 0-dB signal range. See Note 8	± 0.05	± 0.15		dB
Absolute transmit gain tracking error while transmitting into 300 Ω , TLC32044M	-48 -dB to 0-dB signal range. $T_A = 25^\circ\text{C}$. See Note 8	± 0.05	± 0.25		dB
Absolute transmit gain tracking error while transmitting into 300 Ω , TLC32044M	-48 -dB to 0-dB signal range. $T_A = -55^\circ\text{C}$ to 125°C . See Note 8		± 0.4		dB
Absolute receive gain tracking error	-48 -dB to 0-dB signal range. See Note 8	± 0.05	± 0.15		dB
Absolute receive gain tracking error, TLC32044M	-48 -dB to 0-dB signal range. $T_A = 25^\circ\text{C}$. See Note 8	± 0.05	± 0.25		dB
Absolute receive gain tracking error, TLC32044M	-48 -dB to 0-dB signal range. $T_A = -55^\circ\text{C}$ to 125°C . See Note 8		± 0.4		dB
Absolute gain of the A/D channel	Signal input is a -0.5 -dB, 1-kHz sinewave		0.2		dB
Absolute gain of the D/A channel	Signal input is a 0-dB, 1-kHz sinewave		-0.3		dB

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 8: Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 dB relative to V_{ref}).



TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I
VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

power supply rejection and crosstalk attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{CC+} or V _{CC-} supply voltage rejection ratio, receive channel	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)	30			dB
	f = 30 kHz to 50 kHz		45			
V _{CC+} or V _{CC-} supply voltage rejection ratio, transmit channel (single ended)	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT +	30			
	f = 30 kHz to 50 kHz		45			
Crosstalk attenuation, transmit-to-receive (single ended)	TLC3204xC, E, I		80			
	TLC32044M		65	80		
Crosstalk attenuation, receive-to-transmit, TLC32044M		Inputs grounded, Gain = 1, 2, 4	65			

† All typical values are at T_A = 25 °C.



TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

delay distortion

bandpass filter transfer function, SCF $f_{\text{clock}} = 288 \text{ kHz}$ $IN_+ - IN_-$ is a $\pm 3 \text{ V}$ sinewave† (see Note 9)

PARAMETER	TEST CONDITIONS	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP§	MAX	UNIT
Filter gain, TLC32044C, TLC32044E, TLC32044I	Input signal reference to 0 dB	$f \leq 50 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-33	-29	-25	dB
		$f = 100 \text{ Hz}$	$K1 \times -0.26 \text{ dB}$	-4	-2	-1	
		$f = 150 \text{ Hz to } 3100 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.25	0	0.25	
		$f = 3100 \text{ Hz to } 3300 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.3	0	0.3	
		$f = 3300 \text{ Hz to } 3650 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.5	0	0.5	
		$f = 3800 \text{ Hz}$	$K1 \times 2.3 \text{ dB}$		-3	-1	
		$f = 4000 \text{ Hz}$	$K1 \times 2.7 \text{ dB}$		-17	-16	
		$f \geq 4400 \text{ Hz}$	$K1 \times 3.2 \text{ dB}$			-40	
Filter gain, TLC32044M	Input signal reference to 0 dB	$f \leq 50 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-33	-29	-25	dB
		$f = 100 \text{ Hz}$	$K1 \times -0.26 \text{ dB}$	-4	-2	-1	
		$f = 150 \text{ Hz to } 3100 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.25	0	0.25	
		$f = 3100 \text{ Hz to } 3300 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.3	0	0.3	
		$f = 3300 \text{ Hz to } 3500 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.5	0	0.5	
		$f = 3800 \text{ Hz}$	$K1 \times 2.3 \text{ dB}$		-3	-0.5	
		$f = 4000 \text{ Hz}$	$K1 \times 2.7 \text{ dB}$		-17	-16	
		$f \geq 4400 \text{ Hz}$	$K1 \times 3.2 \text{ dB}$			-40	
Filter gain, TLC32045C, TLC32045I	Input signal reference to 0 dB	$f \leq 50 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-33	-29	-25	dB
		$f = 100 \text{ Hz}$	$K1 \times -0.26 \text{ dB}$	-4	-2	-1	
		$f = 150 \text{ Hz to } 3100 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.25	0	0.25	
		$f = 3100 \text{ Hz to } 3300 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.3	0	0.3	
		$f = 3300 \text{ Hz to } 3650 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.5	0	0.5	
		$f = 3800 \text{ Hz}$	$K1 \times 2.3 \text{ dB}$		-3	-1	
		$f = 4000 \text{ Hz}$	$K1 \times 2.7 \text{ dB}$		-17	-16	
		$f \geq 4400 \text{ Hz}$	$K1 \times 3.2 \text{ dB}$			-40	
		$f \geq 5000 \text{ Hz}$	$K1 \times 0 \text{ dB}$			-65	

† See filter curves in typical characteristics

‡ The MIN, TYP, and MAX specifications are given for a 288-kHz SCF clock frequency. A slight error in the 288-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where $K1 = 100 \cdot [(\text{SCF frequency} - 288 \text{ kHz}) / 288 \text{ kHz}]$. For errors greater than 0.25%, see Note 8.

§ All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 9: The filter gain outside of the passband is measured with respect to the gain at 1 kHz. The filter gain within the passband is measured with respect to the average gain within the passband. The passbands are 150 to 3600 Hz and 0 to 3600 Hz for the bandpass and low-pass filters respectively. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.



TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

low-pass filter transfer function†, SCF $f_{\text{clock}} = 288 \text{ kHz}$ (see Note 9)

PARAMETER	TEST CONDITIONS	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP§	MAX	UNIT
Filter gain, TLC32044C, TLC32044E, TLC32044I	Input signal reference is 0 dB	$f = 0 \text{ Hz to } 3100 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.25	0	0.25	dB
		$f = 3100 \text{ Hz to } 3300 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.3	0	0.3	
		$f = 3300 \text{ Hz to } 3650 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.5	0	0.5	
		$f = 3800 \text{ Hz}$	$K1 \times 2.3 \text{ dB}$		-3	-1	
		$f = 4000 \text{ Hz}$	$K1 \times 2.7 \text{ dB}$		-17	-16	
		$f \geq 4400 \text{ Hz}$	$K1 \times 3.2 \text{ dB}$			-40	
Filter gain, TLC32044M	Input signal reference is 0 dB	$f = 0 \text{ Hz to } 3100 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.25	0	0.25	dB
		$f = 3100 \text{ Hz to } 3300 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.3	0	0.3	
		$f = 3300 \text{ Hz to } 3500 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.5	0	0.5	
		$f = 3800 \text{ Hz}$	$K1 \times 2.3 \text{ dB}$		-3	-0.5	
		$f = 4000 \text{ Hz}$	$K1 \times 2.7 \text{ dB}$		-17	-16	
		$f \geq 4400 \text{ Hz}$	$K1 \times 3.2 \text{ dB}$			-40	
Filter gain, TLC32045C, TLC32045I	Input signal reference is 0 dB	$f = 0 \text{ Hz to } 3100 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.25	0	0.25	dB
		$f = 3100 \text{ Hz to } 3300 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.3	0	0.3	
		$f = 3300 \text{ Hz to } 3650 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.5	0	0.5	
		$f = 3800 \text{ Hz}$	$K1 \times 2.3 \text{ dB}$		-3	-1	
		$f = 4000 \text{ Hz}$	$K1 \times 2.7 \text{ dB}$		-17	-16	
		$f \geq 4400 \text{ Hz}$	$K1 \times 3.2 \text{ dB}$			-40	
		$f \geq 5000 \text{ Hz}$	$K1 \times 0 \text{ dB}$			-65	

† See filter curves in typical characteristics

‡ The MIN, TYP, and MAX specifications are given for a 288-kHz SCF clock frequency. A slight error in the 288-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where $K1 = 100 \cdot [(SCF \text{ frequency} - 288 \text{ kHz}) / 288 \text{ kHz}]$. For errors greater than 0.25%, see Note 8.

§ All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 9: The filter gain outside of the passband is measured with respect to the gain at 1 kHz. The filter gain within the passband is measured with respect to the average gain within the passband. The passbands are 150 to 3600 Hz and 0 to 3600 Hz for the bandpass and low-pass filters respectively. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

serial port

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH} High-level output voltage	$I_{OH} = -300 \mu\text{A}$	2.4			V
V_{OL} Low-level output voltage	$I_{OL} = 2 \text{ mA}$			0.4	V
I_I Input current				± 10	μA
C_i Input capacitance			15		pF
C_o Output capacitance			15		pF

† All typical values are at $T_A = 25^\circ\text{C}$.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

operating characteristics over recommended operating free-air temperature range, $V_{CC+} = 5\text{ V}$, $V_{CC-} = -5\text{ V}$, $V_{DD} = 5\text{ V}$

noise (measurement includes low-pass and bandpass switched-capacitor filters)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT		
Transmit noise	TLC32044C, E, I	DX input = 00 00 00 00 00 00 00, constant input code			550	$\mu\text{V rms}$		
	TLC32044M				575	$\mu\text{V rms}$		
	TLC32045C, I				600	$\mu\text{V rms}$		
	TLC32044C, E, I		Without sin x/x correction			325	425	$\mu\text{V rms}$
	TLC32044M					325	450	$\mu\text{V rms}$
	TLC32045C, I					450		$\mu\text{V rms}$
	TLC32044C, E, I					18		dBrncO
TLC32045C, I			24		dBrncO			
Receive noise (see Note 10)	TLC32044C, E, I, M	Inputs grounded, gain = 1			300	500	$\mu\text{V rms}$	
	TLC32045C, I				530		$\mu\text{V rms}$	
	TLC32044C, E, I, M				18		dBrncO	
	TLC32045C, I				24		dBrncO	

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 10: The noise is computed by statistically evaluating the digital output of the A/D converter.

timing requirements

serial port recommended input signals

		MIN	MAX	UNIT
$t_c(\text{MCLK})$	Master clock cycle time	95		ns
	Master clock cycle time, TLC32044M	100	192	ns
$t_r(\text{MCLK})$	Master clock rise time		10	ns
$t_f(\text{MCLK})$	Master clock fall time		10	ns
	Master clock duty cycle	25%	75%	
	Master clock duty cycle, TLC32044M	42%	58%	
	RESET pulse duration (see Note 11)	800		ns
$t_{su}(\text{DX})$	DX setup time before SCLK↓	20		ns
	DX setup time before SCLK↓, TLC32044M	28		ns
$t_h(\text{DX})$	DX hold time after SCLK↓	$t_c(\text{SCLK})/4$		ns

NOTE 11: RESET pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values.

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

serial port — AIC output signals

	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_c(\text{SCLK})$	Shift clock (SCLK) cycle time	380			ns
$t_f(\text{SCLK})$	Shift clock (SCLK) fall time				50
$t_r(\text{SCLK})$	Shift clock (SCLK) rise time				50
	Shift clock (SCLK) duty cycle	45		55	%
$t_d(\text{CH-FL})$	Delay from SCLK↑ to FSR/F $\bar{\text{S}}\bar{\text{X}}$ ↓	$C_L = 50$ pF		52	ns
$t_d(\text{CH-FH})$	Delay from SCLK↑ to FSR/F $\bar{\text{S}}\bar{\text{X}}$ ↑	$C_L = 50$ pF		52	ns
$t_d(\text{CH-DR})$	DR valid after SCLK↑			90	ns
$t_d(\text{CH-EL})$	Delay from SCLK↑ to E $\bar{\text{O}}\text{D}\bar{\text{X}}$ /E $\bar{\text{O}}\text{D}\bar{\text{R}}$ ↓ in word mode			90	ns
$t_d(\text{CH-EH})$	Delay from SCLK↑ to E $\bar{\text{O}}\text{D}\bar{\text{X}}$ /E $\bar{\text{O}}\text{D}\bar{\text{R}}$ ↑ in word mode			90	ns
$t_f(\text{E\bar{\text{O}}\text{D}\bar{\text{X}})$	E $\bar{\text{O}}\text{D}\bar{\text{X}}$ fall time			15	ns
$t_f(\text{E\bar{\text{O}}\text{D}\bar{\text{R}})$	E $\bar{\text{O}}\text{D}\bar{\text{R}}$ fall time			15	ns
$t_d(\text{CH-EL})$	Delay from SCLK↑ to E $\bar{\text{O}}\text{D}\bar{\text{X}}$ /E $\bar{\text{O}}\text{D}\bar{\text{R}}$ ↓ in byte mode			100	ns
$t_d(\text{CH-EH})$	Delay from SCLK↑ to E $\bar{\text{O}}\text{D}\bar{\text{X}}$ /E $\bar{\text{O}}\text{D}\bar{\text{R}}$ ↑ in byte mode			100	ns
$t_d(\text{MH-SL})$	Delay from MSTR CLK↑ to SCLK↓		65		ns
$t_d(\text{MH-SH})$	Delay from MSTR CLK↑ to SCLK↑		65		ns

serial port — AIC output signals, TLC32044M

	MIN	TYP†	MAX	UNIT
$t_c(\text{SCLK})$	400			ns
$t_f(\text{SCLK})$	50			ns
$t_r(\text{SCLK})$	50			ns
	50			%
$t_d(\text{CH-FL})$	260			ns
$t_d(\text{CH-FH})$	260			ns
$t_d(\text{CH-DR})$	316			ns
$t_d(\text{CH-EL})$	280			ns
$t_d(\text{CH-EH})$	280			ns
$t_f(\text{E\bar{\text{O}}\text{D}\bar{\text{X}})$	15			ns
$t_f(\text{E\bar{\text{O}}\text{D}\bar{\text{R}})$	15			ns
$t_d(\text{CH-EL})$	100			ns
$t_d(\text{CH-EH})$	100			ns
$t_d(\text{MH-SL})$	65			ns
$t_d(\text{MH-SH})$	65			ns

† Typical values are at $T_A = 25^\circ\text{C}$.

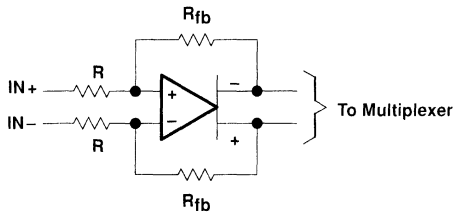
TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

Table 3. Gain Control Table (Analog Input Signal Required for Full-Scale A/D Conversion)

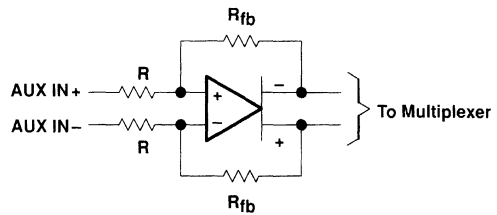
INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT [‡]	A/D CONVERSION RESULT
	d6	d7		
Differential configuration Analog input = IN+ – IN– = AUX IN+ – AUX IN–	1	1	± 6 V	Full-scale
	0	0		
	1	0	± 3 V	Full-scale
	0	1	± 1.5 V	Full-scale
Single-ended configuration Analog input = IN+ – ANLG GND = AUX IN+ – ANLG GND	1	1	± 3 V	Half-scale
	0	0		
	1	0	± 3 V	Full-scale
	0	1	± 1.5 V	Full-scale

[‡] In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.



$R_{fb} = R$ for $d6 = 1, d7 = 1$
 $d6 = 0, d7 = 0$
 $R_{fb} = 2R$ for $d6 = 1, d7 = 0$
 $R_{fb} = 4R$ for $d6 = 0, d7 = 1$

Figure 7. IN+ and IN– Gain Control Circuitry



$R_{fb} = R$ for $d6 = 1, d7 = 1$
 $d6 = 0, d7 = 0$
 $R_{fb} = 2R$ for $d6 = 1, d7 = 0$
 $R_{fb} = 4R$ for $d6 = 0, d7 = 1$

Figure 8. AUX IN+ and AUX IN– Gain Control Circuitry

(sin x)/x correction

The AIC does not have (sin x)/x correction circuitry after the digital-to-analog converter. (Sin x)/x correction can be accomplished easily and efficiently in digital signal processor (DSP) software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results, which are shown in Table 4, are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires only seven instruction cycles per sample on the TMS(SMJ)320 DSPs. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction adds a slight amount of group delay at the upper edge of the 300–3000-Hz band.

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I
VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

(sin x)/x roll-off for a zero-order hold function

The (sin x)/x roll-off for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in the table below.

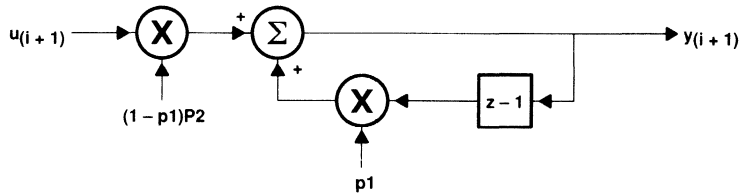
Table 4. (sin x)/x Roll-Off

f_s (Hz)	$20 \log \frac{\sin \pi f/f_s}{\pi f/f_s}$ ($f = 3000$ Hz) (dB)
7200	-2.64
8000	-2.11
9600	-1.44
14400	-0.63
19200	-0.35

The actual AIC (sin x)/x roll-off will be slightly less than the above figures because the AIC has less than a 100% duty cycle hold interval.

correction filter

To compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter (shown below) is recommended.



The difference equation for this correction filter is:

$$y_{i+1} = p_2(1-p_1)(u_{i+1}) + p_1 y_i$$

where the constant p_1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{p_2^2 (1-p_1)^2}{1 - 2p_1 \cos(2 \pi f/f_s) + p_1^2}$$

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

correction results

Table 5 shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates.

Table 5. Optimum P Values

f (Hz)	ERROR (dB)	ERROR (dB)
	$f_s = 8000$ Hz $p1 = -0.14813$ $p2 = 0.9888$	$f_s = 9600$ Hz $p1 = -0.1307$ $p2 = 0.9951$
300	-0.099	-0.043
600	-0.089	-0.043
900	-0.054	0
1200	-0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	-0.043	0
3000	-0.102	-0.043

TMS(SMJ)320 software requirements

The digital correction filter equation can be written in state variable form as follows:

$$Y = k1 \times Y + k2 \times U$$

where

$$k1 = p1$$

$$k2 = (1 - p1) \times p2$$

Y = filter state

U = next I/O sample

The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) yields the correct result. With the assumption that the TMS(SMJ)320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

PARAMETER MEASUREMENT INFORMATION

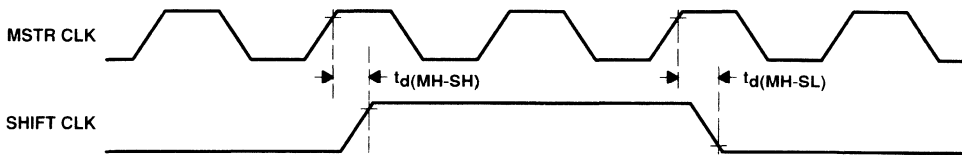
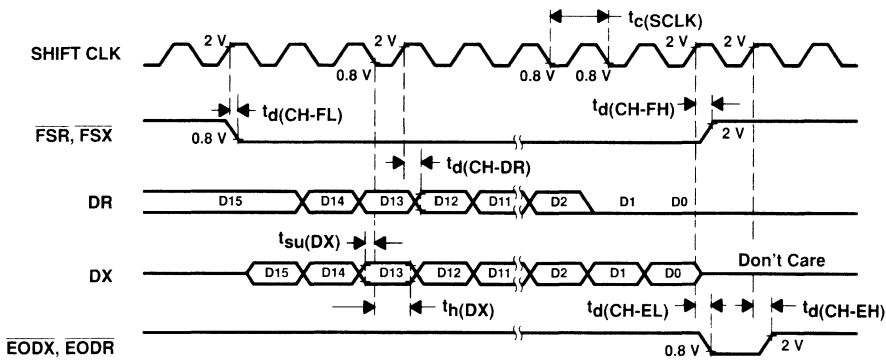
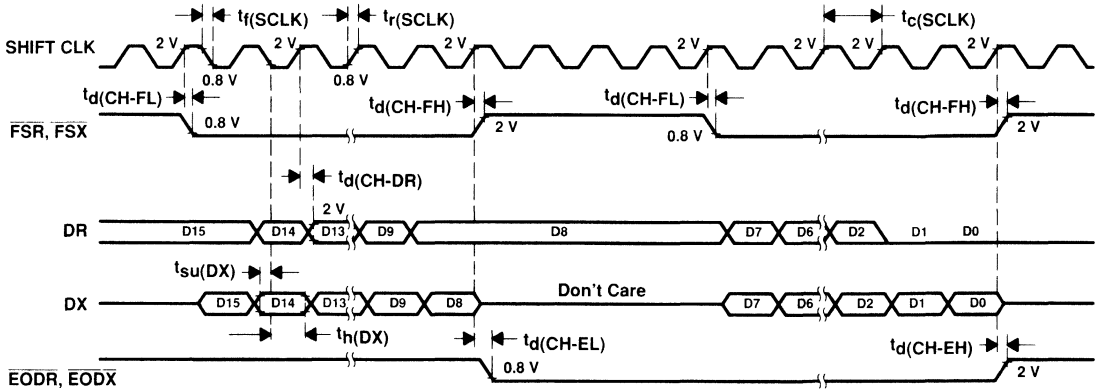


Figure 9. Serial-Port Timing

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F - MARCH 1988 - REVISED MAY 1995

PARAMETER MEASUREMENT INFORMATION

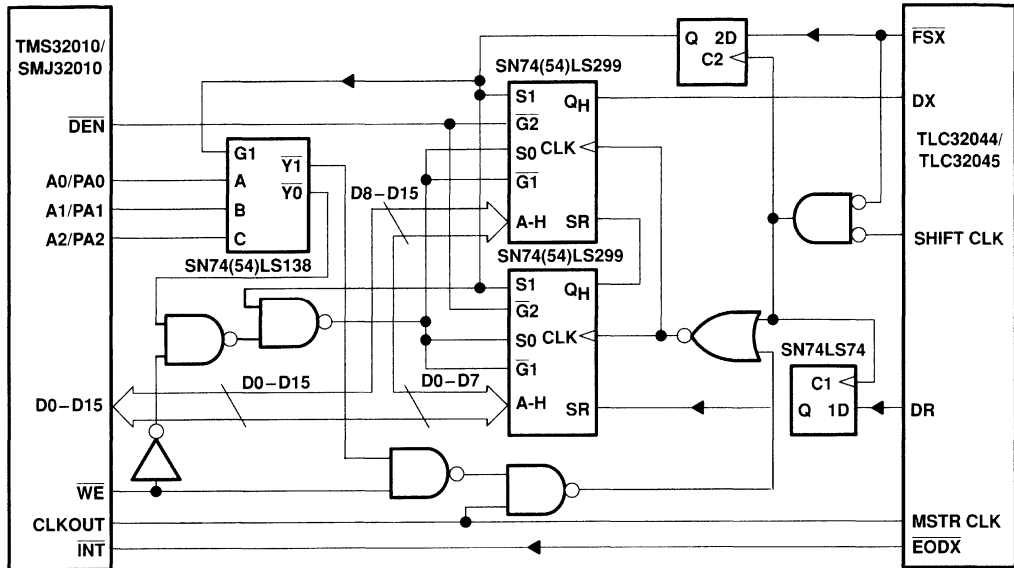


Figure 10. TMS(SMJ)32010/TMS(SMJ)320C15/(SMJ320E15)-TLC32044/45 Interface Circuit

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I
 VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

PARAMETER MEASUREMENT INFORMATION

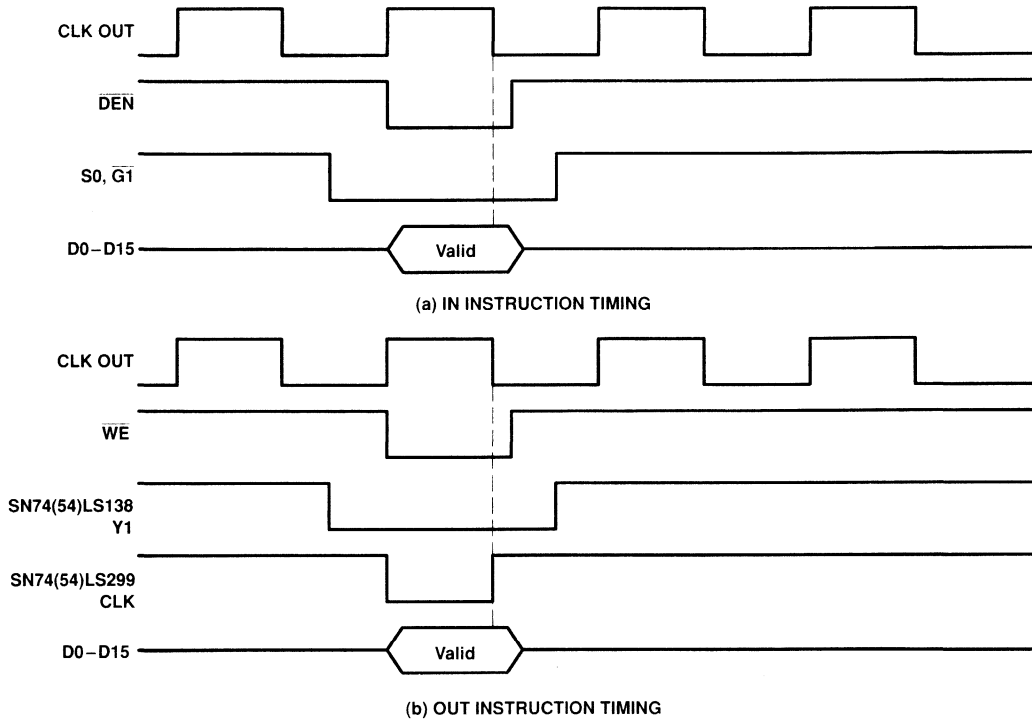


Figure 11. TMS(SMJ)32010/TMS(SMJ)320C15-TLC32044/TLC32045 Interface Timing

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

TYPICAL CHARACTERISTICS

**AIC TRANSMIT AND RECEIVE
LOW-PASS FILTER**

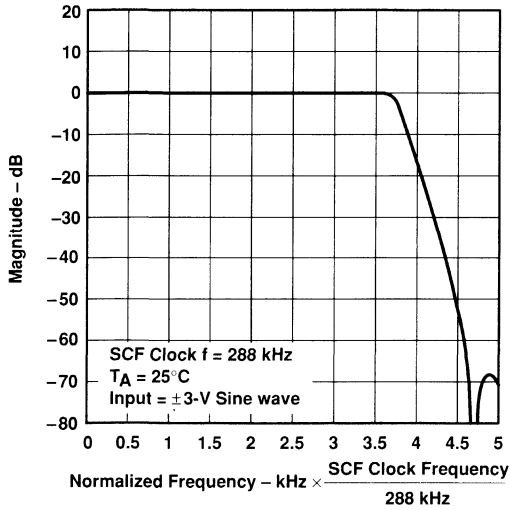


Figure 12

**AIC TRANSMIT AND RECEIVE
LOW-PASS FILTER**

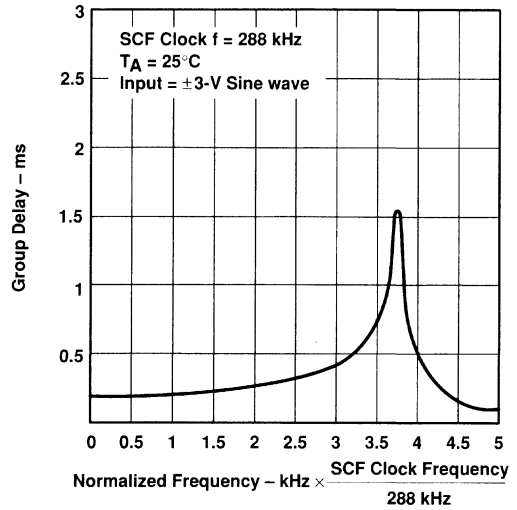


Figure 13

**AIC RECEIVE-CHANNEL
BANDPASS FILTER**

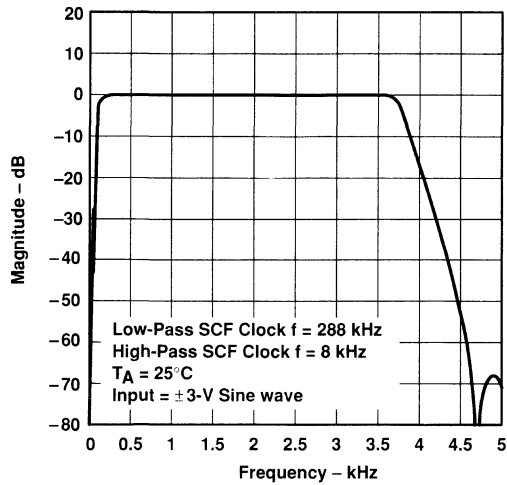


Figure 14

**AIC RECEIVE-CHANNEL
HIGH-PASS FILTER**

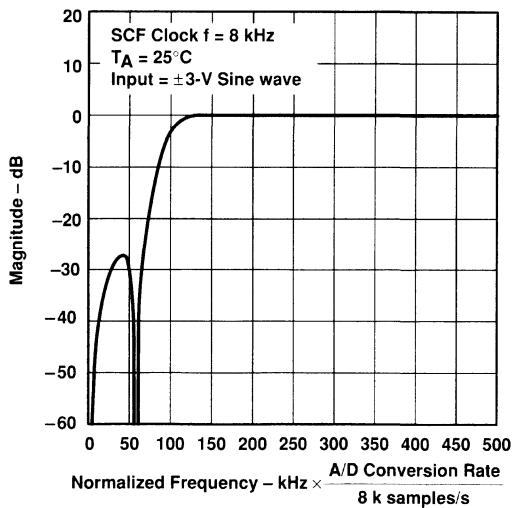


Figure 15

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I
VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

TYPICAL CHARACTERISTICS

AIC RECEIVE CHANNEL
BANDPASS FILTER

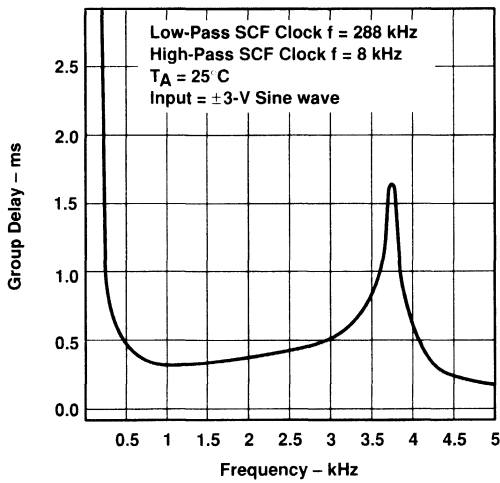


Figure 16

AIC (sin x)/x CORRECTION FILTER

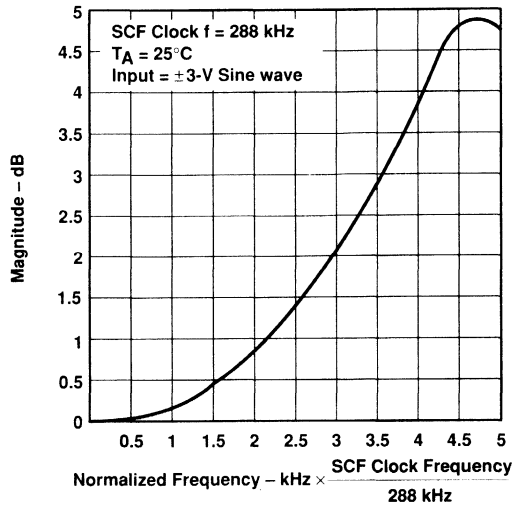


Figure 17

AIC (sin x)/x CORRECTION FILTER

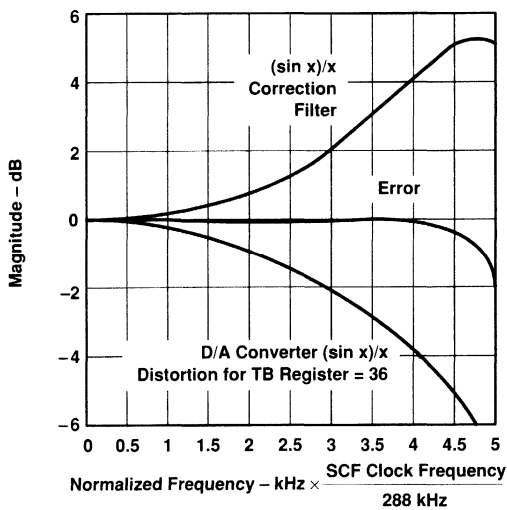


Figure 18

A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT-SIGNAL LEVEL

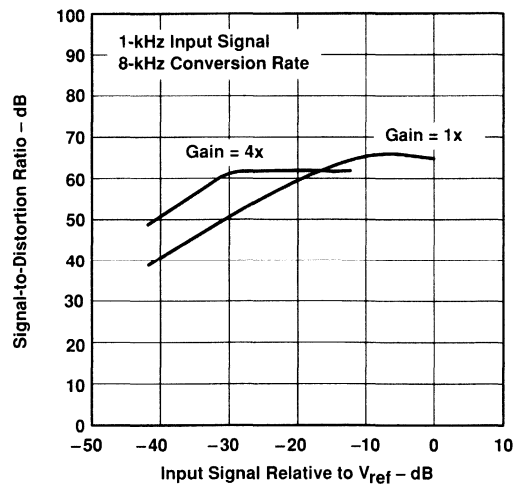


Figure 19

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

TYPICAL CHARACTERISTICS

A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN
AT 0-dB INPUT-SIGNAL LEVEL)

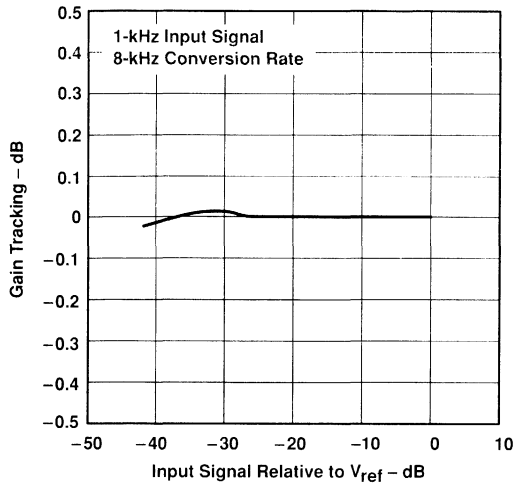


Figure 20

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT-SIGNAL LEVEL

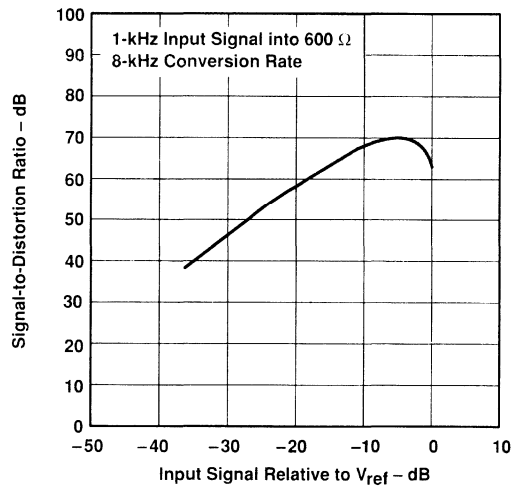


Figure 21

D/A GAIN TRACKING
(GAIN RELATIVE TO GAIN
AT 0-dB INPUT-SIGNAL LEVEL)

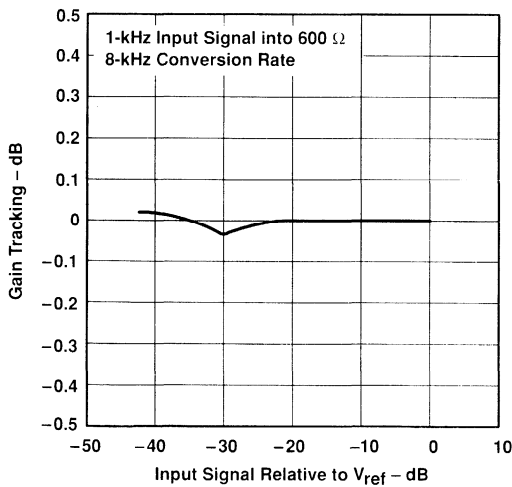


Figure 22

A/D SECOND HARMONIC DISTORTION
vs
INPUT-SIGNAL LEVEL

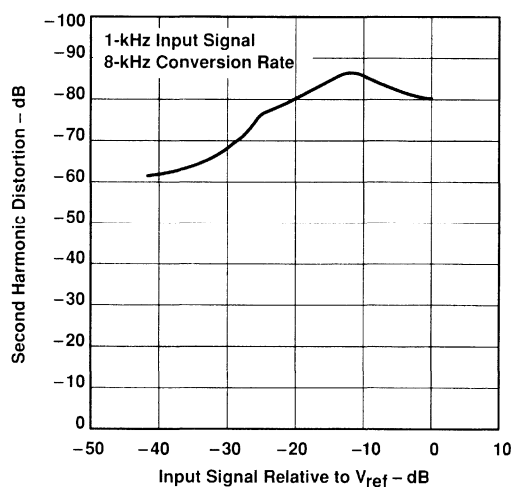


Figure 23

TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I
VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

TYPICAL CHARACTERISTICS

D/A SECOND HARMONIC DISTORTION
vs
INPUT-SIGNAL LEVEL

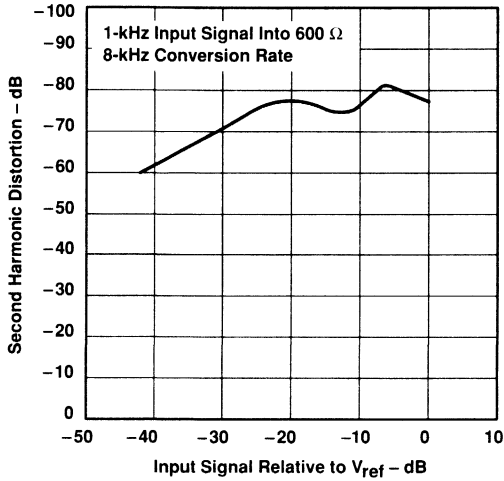


Figure 24

A/D THIRD HARMONIC DISTORTION
vs
INPUT-SIGNAL LEVEL

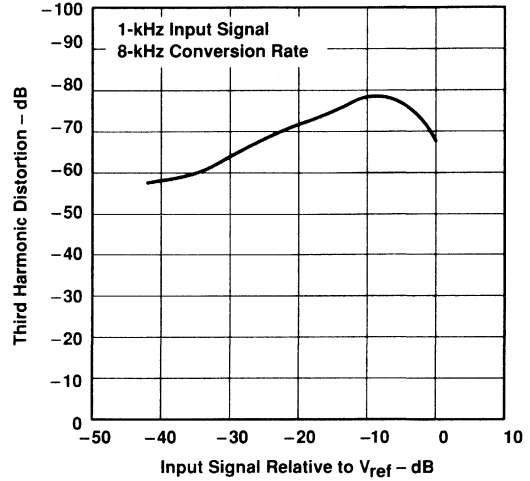


Figure 25

D/A THIRD HARMONIC DISTORTION
vs
INPUT-SIGNAL LEVEL

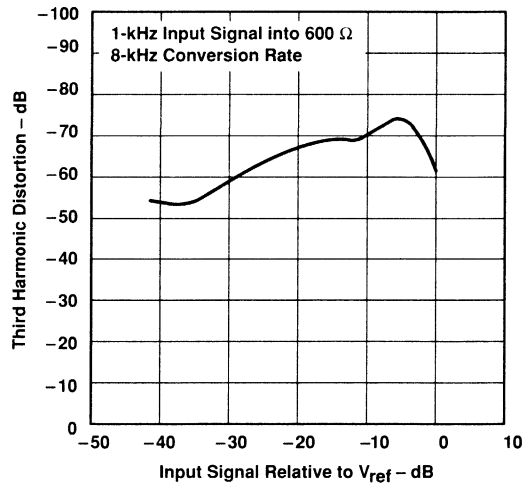


Figure 26



TLC32044C, TLC32044E, TLC32044I, TLC32044M, TLC32045C, TLC32045I VOICE-BAND ANALOG INTERFACE CIRCUITS

SLAS017F – MARCH 1988 – REVISED MAY 1995

APPLICATION INFORMATION

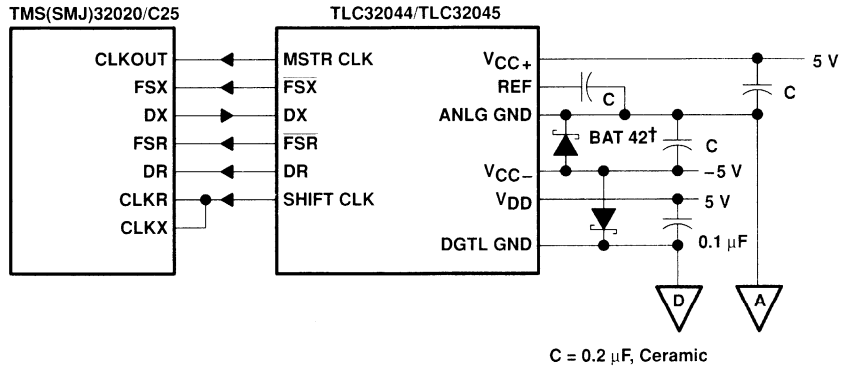


Figure 27. AIC Interface to the TMS(SMJ)32020/C25 Showing Decoupling Capacitors and Schottky Diode†

† Thomson Semiconductors

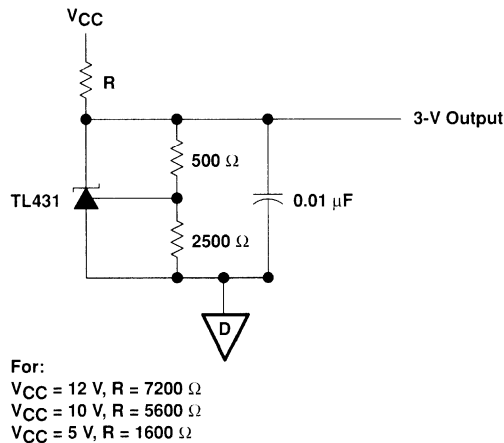


Figure 28. External Reference Circuit For TLC32044/TLC32045

TLC32046C, TLC32046I, TLC32046M Data Manual

Wide-Band Analog Interface Circuit

*SLAS028
May 1995*

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Contents

<i>Section</i>	<i>Title</i>	<i>Page</i>
1	Introduction	4-79
1.1	Features	4-80
1.2	Functional Block Diagrams	4-81
1.3	Terminal Assignments	4-84
1.4	Ordering Information	4-84
1.5	Terminal Functions	4-85
2	Detailed Description	4-87
2.1	Internal Timing Configuration	4-88
2.2	Analog Input	4-90
2.3	A/D Band-Pass Filter, Clocking, and Conversion Timing	4-90
2.4	A/D Converter	4-90
2.5	Analog Output	4-90
2.6	D/A Low-Pass Filter, Clocking, and Conversion Timing	4-90
2.7	D/A Converter	4-90
2.8	Serial Port	4-91
2.9	Synchronous Operation	4-91
2.9.1	One 16-Bit Word	4-91
2.9.2	Two 8-Bit Bytes	4-91
2.9.3	Synchronous Operating Frequencies	4-92
2.10	Asynchronous Operation	4-92
2.10.1	One 16-Bit Word	4-92
2.10.2	Two 8-Bit Bytes	4-92
2.10.3	Asynchronous Operating Frequencies	4-92
2.11	Operation of TLC32046C and TLC32046I With Internal Voltage Reference	4-93
2.12	Operation of TLC32046C AND TLC32046I With External Voltage Reference	4-93
2.13	Reset	4-93
2.14	Loopback	4-93
2.15	Communications Word Sequence	4-93
2.15.1	Primary DR Word Bit Pattern	4-94
2.15.2	Primary DX Word Bit Pattern	4-95
2.15.3	Secondary DX Word Bit Pattern	4-96
2.16	Reset Function	4-96
2.17	Power-Up Sequence	4-97
2.18	AIC Register Constraints	4-97
2.19	AIC Responses to Improper Conditions	4-97
2.20	Operation With Conversion Times Too Close Together	4-98
2.21	More Than One Receive Frame Sync Occurring Between Two Transmit Frame Syncs – Asynchronous Operation	4-98
2.22	More Than One Transmit Frame Sync Occurring Between Two Receive Frame Syncs – Asynchronous Operation	4-99

<i>Section</i>	<i>Title</i>	<i>Page</i>
2.23	More than One Set of Primary and Secondary DX Serial Communications Occurring Between Two Receive Frame Syncs – Asynchronous Operation . . .	4–99
2.24	System Frequency Response Correction	4–100
2.25	(Sin x)/x Correction	4–100
2.26	(Sin x)/x Roll-Off for a Zero-Order Hold Function	4–100
2.27	Correction Filter	4–101
2.28	Correction Results	4–101
2.29	TMS320 Software Requirements	4–102
3	Specifications	4–103
3.1	Absolute Maximum Ratings Over Operating Free-Air Temperature Range . . .	4–103
3.2	Recommended Operating Conditions	4–103
3.3	Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, $V_{CC+} = 5\text{ V}$, $V_{CC-} = -5\text{ V}$, $V_{DD} = 5\text{ V}$	4–104
3.3.1	Total Device, MSTR CLK Frequency = 5.184 MHz	4–104
3.3.2	Power Supply Rejection and Crosstalk Attenuation	4–104
3.3.3	Serial Port	4–104
3.3.4	Receive Amplifier Input	4–105
3.3.5	Transmit Filter Output	4–105
3.3.6	Receive and Transmit Channel System Distortion, SCF Clock Frequency = 288 kHz	4–105
3.3.7	Receive Channel Signal-to-Distortion Ratio	4–106
3.3.8	Transmit Channel Signal-to-Distortion Ratio	4–106
3.3.9	Receive and Transmit Gain and Dynamic Range	4–106
3.3.10	Receive Channel Band-Pass Filter Transfer Function, SCF $f_{\text{clock}} = 288\text{ kHz}$, Input (IN+ – IN–) Is A +3-V Sine Wave	4–107
3.3.11	Receive and Transmit Channel Low-Pass Filter Transfer Function, SCF $f_{\text{clock}} = 288\text{ kHz}$	4–107
3.4	Operating Characteristics Over Recommended Operating Free-Air Temperature Range, $V_{CC+} = 5\text{ V}$, $V_{CC-} = -5\text{ V}$, $V_{DD} = 5\text{ V}$	4–108
3.4.1	Receive and Transmit Noise	4–108
3.5	Timing Requirements	4–108
3.5.1	Serial Port Recommended Input Signals	4–108
3.5.2	Serial Port – AIC Output Signals, $C_L = 30\text{ pF}$ for SHIFT CLK Output, $C_L = 15\text{ pF}$ For All Other Outputs	4–109
4	Parameter Measurement Information	4–111
5	Typical Characteristics	4–117
6	Application Information	4–127

List of Illustrations

<i>Figure</i>	<i>Title</i>	<i>Page</i>
1-1	Dual-Word (Telephone Interface) Mode	4-83
1-2	Word Mode	4-83
1-3	Byte Mode	4-83
2-1	Asynchronous Internal Timing Configuration	4-89
2-2	Primary and Secondary Communications Word Sequence	4-84
2-3	DR Word Bit Pattern	4-84
2-4	Primary DX Word Blt Pattern	4-85
2-5	Secondary DX Word Blt Pattern	4-86
2-6	Reset on Power-Up Circuit	4-87
2-7	Conversion Times Too Close Together	4-88
2-8	More Than One Receive Frame Sync Between Two Transmit Frame Syncs ...	4-89
2-9	More Than One Transmit Frame Sync Between Two Receive Frame Syncs ...	4-89
2-10	More Than One Set of Primary and Secondary DX Serial Communications Between Two Receive Frame Syncs	4-90
2-11	First-Order Correction Filter	4-91
4-1	IN+ and IN- Gain Control Circuitry	4-111
4-2	Dual-Word (Telephone Interface) Mode Timing	4-112
4-3	Word Timing	4-112
4-4	Byte Mode Timing	4-113
4-5	Shift-Clock Timing	4-114
4-6	TMS32010/TMS320C15-TLC32046 Interface Timing	4-114
4-7	TMS32010/TMS320C15-TLC32046 Interface Circuit	4-115

List of Tables

<i>Table</i>	<i>Title</i>	<i>Page</i>
2-1	Mode-Selection Function Table	4-87
2-2	Primary DX Serial Communication Protocol	4-87
2-3	Secondary DX Serial Communication Protocol	4-87
2-4	AIC Responses to Improper Conditions	4-87
2-5	(sin x)/x Roll-Off Error	4-87
2-6	(sin x)/x Correction Table for $f_s = 8000$ Hz and $f_s = 9600$ Hz	4-87
4-1	Gain Control Table	4-111

1 Introduction

The TLC32046C, TLC32046I, and TLC32046M wide-band analog interface circuits (AIC) are a complete analog-to-digital and digital-to-analog interface system for advanced digital signal processors (DSPs) similar to the TMS32020, TMS320C25, and TMS320C30. The TLC32046C and TLC32046I offer a powerful combination of options under DSP control: three operating modes (dual-word [telephone interface], word, and byte) combined with two word formats (8 bits and 16 bits) and synchronous or asynchronous operation. It provides a high level of flexibility in that conversion and sampling rates, filter bandwidths, input circuitry, receive and transmit gains, and multiplexed analog inputs are under processor control.

This AIC features a

- band-pass switched-capacitor antialiasing input filter
- 14-bit-resolution A/D converter
- 14-bit-resolution D/A converter
- low-pass switched-capacitor output-reconstruction filter.

The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable auxiliary differential analog input is provided for applications where more than one analog input is required.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order $(\sin x)/x$ correction filter and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the sample data signal. The on-board $(\sin x)/x$ correction filter can be switched out of the signal path using digital signal processor control.

The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the IC. The internal voltage reference is brought out to REF. Separate analog and digital voltage supplies and ground are provided to minimize noise and ensure a wide dynamic range. The analog circuit path contains only differential circuitry to keep noise to a minimum. The exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The TLC32046C is characterized for operation from 0°C to 70°C, the TLC32046I is characterized for operation from -40°C to 85°C, and the TLC32046M is characterized for operation from -55°C to 125°C.

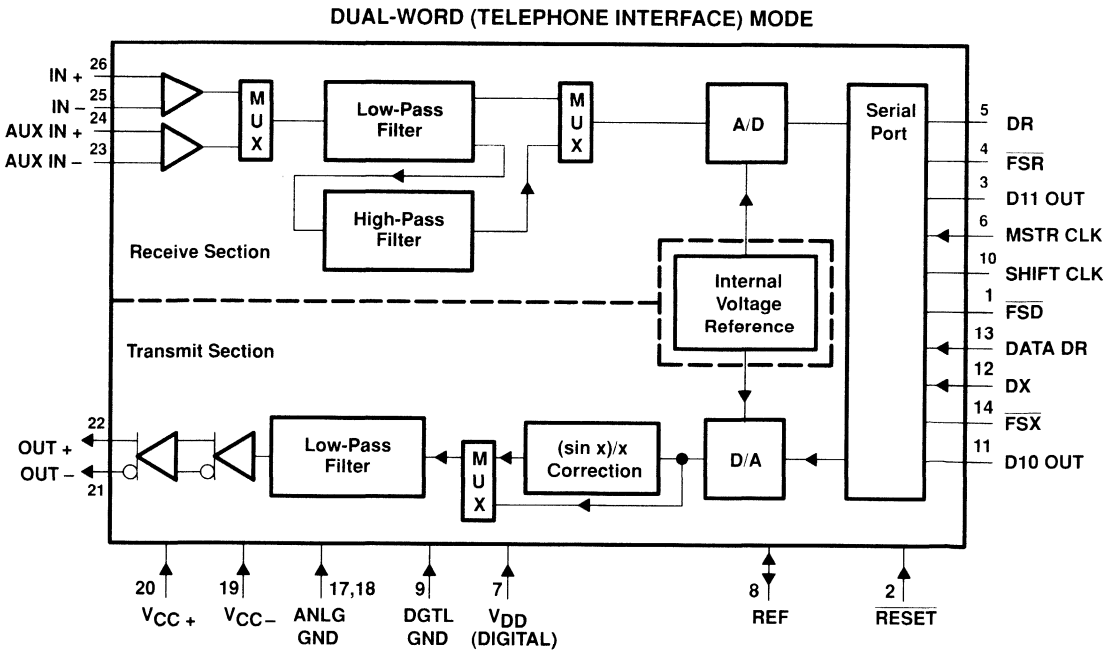
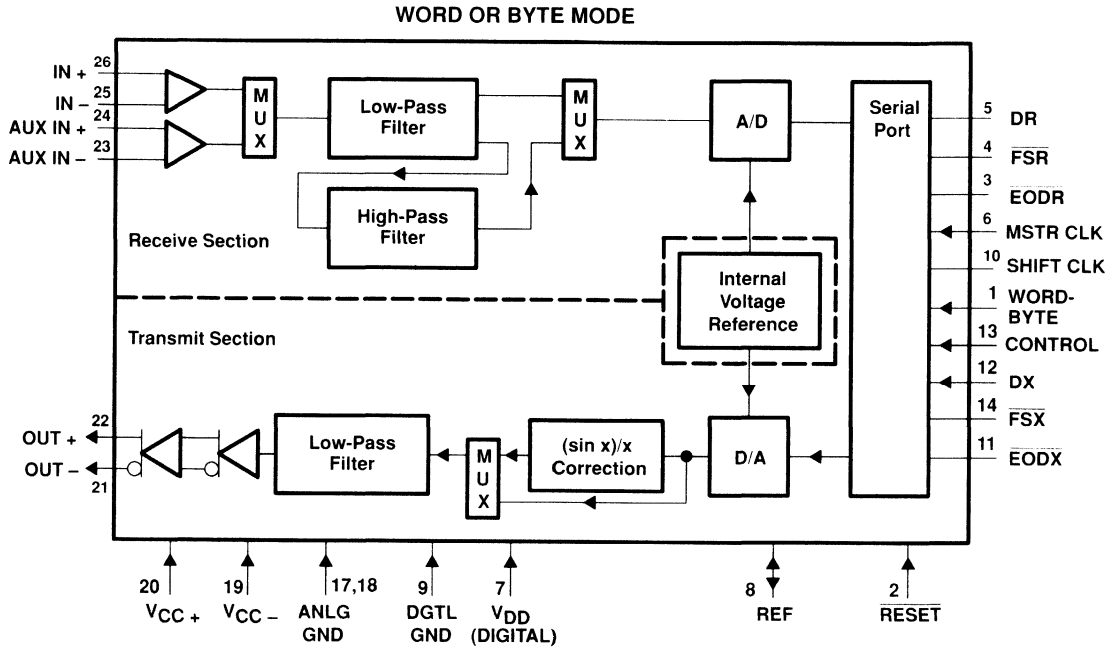
1.1 Features

- 14-Bit Dynamic Range ADC and DAC
- 16-Bit Dynamic Range Input With Programmable Gain
- Synchronous or Asynchronous ADC and DAC Sampling Rates Up to 25,000 Samples Per Second
- Programmable Incremental ADC and DAC Conversion Timing Adjustments
- Typical Applications
 - Speech Encryption for Digital Transmission
 - Speech Recognition and Storage Systems
 - Speech Synthesis
 - Modems at 8-kHz, 9.6-kHz, and 16-kHz Sampling Rates
 - Industrial Process Control
 - Biomedical Instrumentation
 - Acoustical Signal Processing
 - Spectral Analysis
 - Instrumentation Recorders
 - Data Acquisition
- Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter
- Three Fundamental Modes of Operation: Dual-Word (Telephone Interface), Word, and Byte
- 600-mil Wide N Package
- Digital Output in Twos Complement Format
- CMOS Technology

FUNCTION TABLE

DATA COMMUNICATIONS FORMAT	SYNCHRONOUS (CONTROL REGISTER BIT D5 = 1)	ASYNCHRONOUS (CONTROL REGISTER BIT D5 = 0)	FORCING CONDITION	DIRECT INTERFACE
16-bit format	Dual-word (telephone interface) mode	Dual-word (telephone interface) mode	Terminal 13 = 0 to 5 V Terminal 1 = 0 to 5 V	TMS32020, TMS320C25, TMS320C30
16-bit format	Word mode	Word mode	Terminal 13 = V_{CC-} (-5 V nom) Terminal 1 = V_{CC+} (5 V nom)	TMS32020, TMS320C25, TMS320C30, indirect interface to TMS320C10. (see Figure 7).
8-bit format (2 bytes required)	Byte mode	Byte mode	Terminal 13 = V_{CC-} (-5 V nom) Terminal 1 = V_{CC-} (-5 V nom)	TMS320C17

1.2 Functional Block Diagrams



FRAME SYNCHRONIZATION FUNCTIONS

Function	Frame Sync Output
Receiving serial data on DX from processor to internal DAC	$\overline{\text{FSX}}$ low
Transmitting serial data on DR from internal ADC to processor, primary communications	FSR low
Transmitting serial data on DR from Data-DR to processor, secondary communications in dual-word (telephone interface) mode only	$\overline{\text{FSD}}$ low

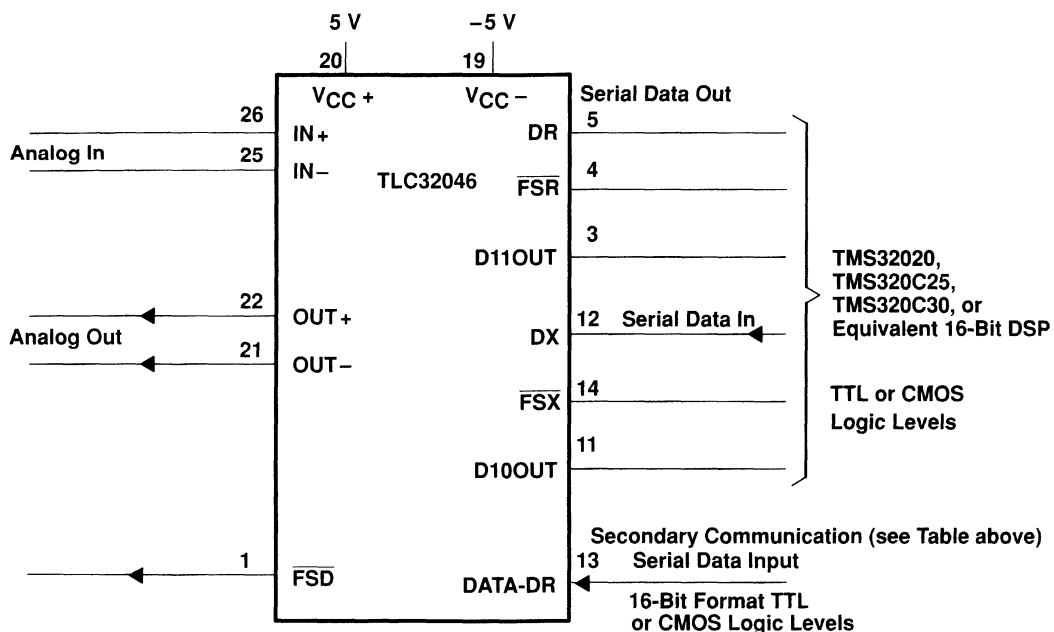


Figure 1-1. Dual-Word (Telephone Interface) Mode

When the DATA-DR/CONTROL input is tied to a logic signal source varying between 0 and 5 V, the TLC32046 is in the dual-word (telephone interface) mode. This logic signal is routed to the DR line for input to the DSP only when data frame synchronization ($\overline{\text{FSD}}$) outputs a low level. The $\overline{\text{FSD}}$ pulse duration is 16 shift clock pulses. Also, in this mode, the control register data bits D10 and D11 appear on D10OUT and D11OUT, respectively, as outputs.

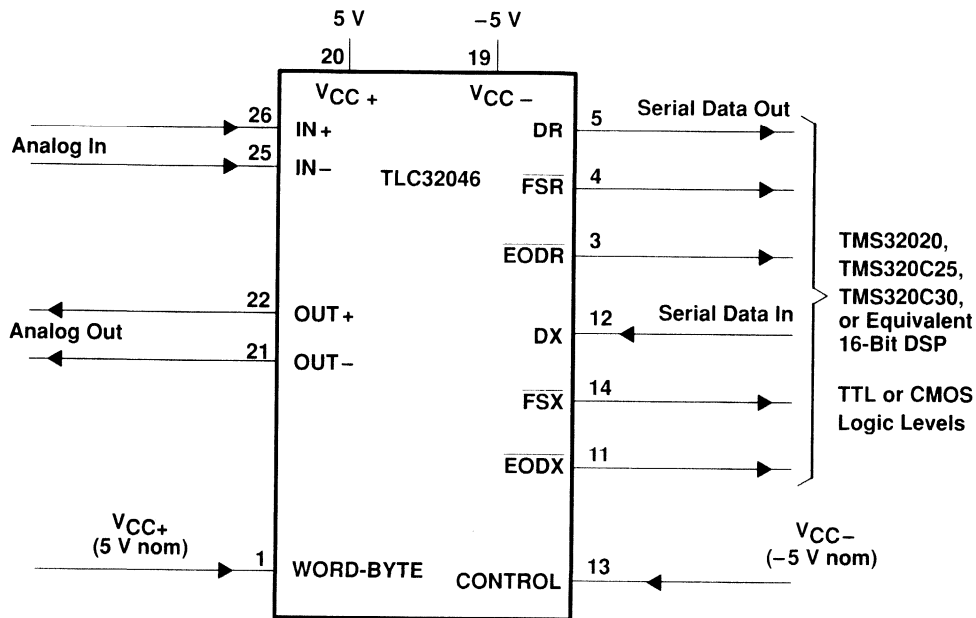


Figure 1-2. Word Mode

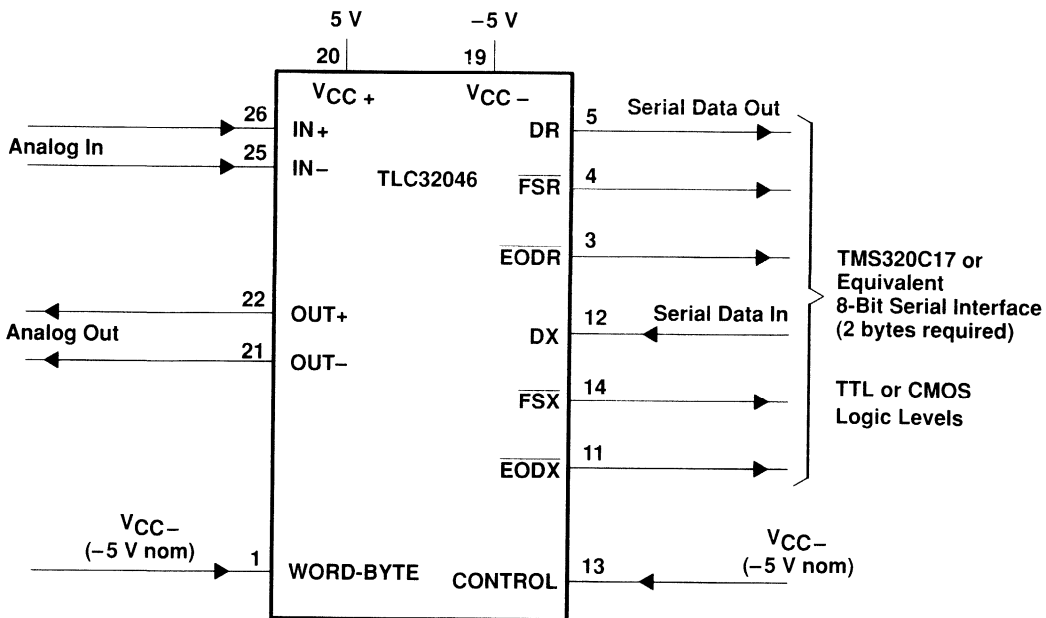
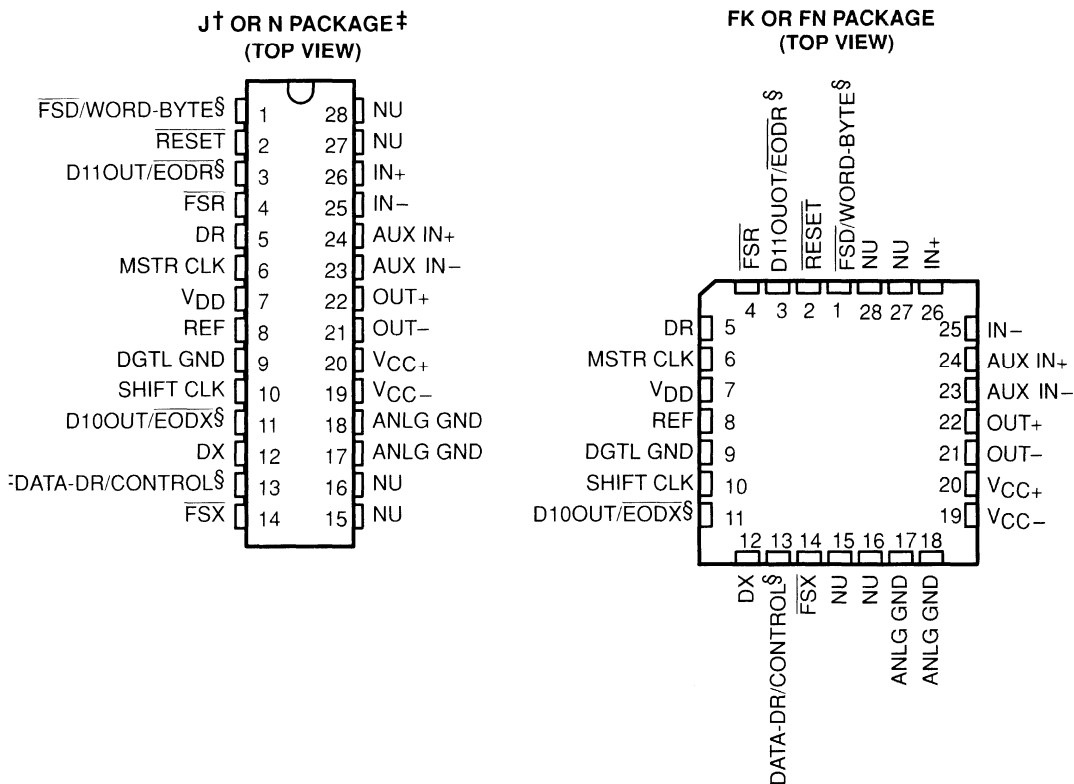


Figure 1-3. Byte Mode

The word or byte mode is selected by first connecting the DATA-DR/CONTROL input to V_{CC-} . \overline{FSD} /WORD-BYTE becomes an input and can then be used to select either word or byte transmission formats. The end-of-data transmit (EODX) and the end-of-data receive (EODR) signals respectively, are used to signal the end of word or byte communication (see the Terminal Functions section).

1.3 Terminal Assignments



NU - Nonusable; no external connection should be made to these terminals.

† Refer to the mechanical data for the JT package.

‡ 600-mil wide

§ The portion of the terminal name to the left of the slash is used for the dual-word (telephone interface) mode. The portion of the terminal name to the right of the slash is used for word-byte mode.

1.4 Ordering Information

AVAILABLE OPTIONS

TA	PACKAGE			
	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)	CERAMIC DIP (J)	CHIP CARRIER (FK)
0°C to 70°C	TLC32046CFN	TLC32046CN		
-40°C to 85°C	TLC32046IFN	TLC32046IN		
-55°C to 125°C			TLC32046MJ	TLC32046MFK

1.5 Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN+	24	I	Noninverting auxiliary analog input stage. AUX IN+ can be switched into the band-pass filter and ADC path via software control. If the appropriate bit in the control register is a 1, the auxiliary inputs replace the IN+ and IN- inputs. If the bit is a 0, the IN+ and IN- inputs are used (see the DX Serial Data Word Format).
AUX IN-	23	I	Inverting auxiliary analog input (see the above AUX IN+ description).
DATA-DR	13	I	The dual-word (telephone interface) mode, selected by applying an input logic level between 0 and 5 V to DATA-DR, allows this terminal to function as a data input. The data is then framed by the $\overline{\text{FSD}}$ signal and transmitted as an output to the DR line during secondary communication. The functions $\overline{\text{FSD}}$, D11OUT, and D10OUT are valid with this mode selection (see Table 2-1).
CONTROL			When CONTROL is tied to $\text{V}_{\text{CC-}}$, the device is in the word or byte mode. The functions WORD-BYTE, $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are valid in this mode. CONTROL is then used to select either the word or byte mode (see Function Table).
DR	5	O	DR is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with SHIFT CLK.
DX	12	I	DX is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port is synchronized with SHIFT CLK.
D10OUT	11	O	In the dual-word (telephone interface) mode, bit D10 of the control register is output to D10OUT. When the device is reset, bit D10 is initialized to 0 (see DX Serial Data Word Format). The output update is immediate upon changing bit D10.
$\overline{\text{EODX}}$			End-of-data transmit. During the word-mode timing, a low-going pulse occurs on $\overline{\text{EODX}}$ immediately after the 16 bits of DAC and control or register information have transmitted from the TMS320 serial port to the AIC. This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM and to facilitate parallel data bus communications between the DSP and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate first and second bytes.
D11OUT	3	O	In the dual-word (telephone interface) mode, bit D11 of the control register is output to D11OUT. When the device is reset, bit D11 is initialized to 0 (see DX Serial Data Word Format). The output update is immediate upon changing bit D11.
$\overline{\text{EODR}}$			End-of-data receive. During the word-mode timing, a low-going pulse occurs on $\overline{\text{EODR}}$ immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the DSP and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate between first and second bytes.

1.5 Terminal Functions (continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
DGTL	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
$\overline{\text{FSD}}$	1	O	Frame sync data. The $\overline{\text{FSD}}$ output remains high during primary communication. In the dual-word (telephone interface) mode, $\overline{\text{FSD}}$ is identical to $\overline{\text{FSX}}$ during secondary communication.
WORD-BYTE		I	WORD-BYTE allows differentiation between the word and byte data format (see DATA-DR/CONTROL and Table 2-1 for details).
FSR	4	O	Frame sync receive. $\overline{\text{FSR}}$ is held low during bit transmission. When $\overline{\text{FSR}}$ goes low, the TMS320 serial port begins receiving bits from the AIC via DR of the AIC. The most significant DR bit is present on DR before $\overline{\text{FSR}}$ goes low (see Serial Port Sections and Internal Timing Configuration Diagrams).
FSX	14	O	Frame sync transmit. When FSX goes low, the TMS320 serial port begins transmitting bits to the AIC via DX of the AIC. $\overline{\text{FSX}}$ is held low during bit transmission (see Serial Port Sections and Internal Timing Configuration Diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN-	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	The master clock signal is used to derive all the key logic signals of the AIC, such as the shift clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these signals are synchronous submultiples of the master clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the ADC and DAC converters (see the Internal Timing Configuration).
OUT+	22	O	Noninverting output of analog output power amplifier. OUT+ drives transformer hybrids or high-impedance loads directly in a differential or a single-ended configuration.
OUT-	21	O	Inverting output of analog output power amplifier. OUT- is functionally identical with and complementary to OUT+.
REF	8	I/O	The internal voltage reference is brought out on REF. An external voltage reference can be applied to REF to override the internal voltage reference.
RESET	2	I	A reset function is provided to initialize TA, TA', TB, RA, RA', RB (see Figure 2-1), and the control registers. This reset function initiates serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on $\overline{\text{RESET}}$, the AIC registers are initialized to provide a 16-kHz data conversion rate for a 10.368-MHz master clock input signal. The conversion rate adjust registers, TA' and RA', are reset to 1. The CONTROL register bits are reset as follows (see AIC DX Data Word Format section): D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1 The shift clock (SCLK) is held high during $\overline{\text{RESET}}$. This initialization allows normal serial-port communication to occur between the AIC and the DSP.
SHIFT CLK	10	O	The shift clock signal is obtained by dividing the master clock signal frequency by four. SHIFT CLK is used to clock the serial data transfers of the AIC.
VDD	7		Digital supply voltage, 5 V \pm 5%
VCC+	20		Positive analog supply voltage, 5 V \pm 5%
VCC-	19		Negative analog supply voltage, -5 V \pm 5%

2 Detailed Description

Table 2–1. Mode-Selection Function Table

DATA-DR/ CONTROL (Terminal 13)	FSD/ WORD-BYTE (Terminal 1)	CONTROL REGISTER BIT (D5)	OPERATING MODE	SERIAL CONFIGURATION	DESCRIPTION
Data in (0 V to 5 V)	FSD out (0 V to 5 V)	1	Dual Word (Telephone Interface)	Synchronous, One 16-Bit Word	Terminal functions DATA-DR [†] , FSD [†] , D11OUT, and D10OUT are applicable in this configuration. FSD is asserted during secondary communication, but FSR is not asserted. However, FSD remains high during primary communication.
Data in (0 V to 5 V)	FSD out (0 V to 5 V)	0	Dual Word (Telephone Interface)	Synchronous, One 16-Bit Word	Terminal functions DATA-DR [†] , FSD [†] , D11OUT, and D10OUT are applicable in this configuration. FSD is asserted during secondary communication, but FSR is not asserted. However, FSD remains high during primary communication. If secondary communications occur while the A/D conversion is being transmitted from DR, FSD cannot go low, and data from DATA-DR cannot go onto DR.
VCC–	VCC+	1	WORD	Synchronous, One 16-Bit Word	Terminal functions CONTROL [†] , WORD-BYTE [†] , EODR, and EODX are applicable in this configuration.
		0		Asynchronous, One 16-bit Word	Terminal functions CONTROL [†] , WORD-BYTE [†] , EODR, and EODX are applicable in this configuration.
	VCC–	1	BYTE	Synchronous, Two 8-Bit Bytes	Terminal functions CONTROL [†] , WORD-BYTE [†] , EODR, and EODX are applicable in this configuration.
		0		Asynchronous, Two 8-Bit Bytes	Terminal functions CONTROL [†] , WORD-BYTE [†] , EODR, and EODX are applicable in this configuration.

[†] DATA-DR/CONTROL has an internal pulldown resistor to –5 V, and FSD/WORD-BYTE has an internal pullup resistor to 5 V.

2.1 Internal Timing Configuration (see Figure 2–1)

All the internal timing of the AIC is derived from the high-frequency clock signal that drives the master clock input. The shift clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the master clock input signal frequency by four.

The TX(A) counter and the TX(B) counter, which are driven by the master clock signal, determine the D/A conversion timing. Similarly, the RX(A) counter and the RX(B) counter determine the A/D conversion timing. In order for the low-pass switched-capacitor filter in the D/A path (see Functional Block Diagram) to meet its transfer function specifications, the frequency of its clock input must be 288 kHz. If the clock frequency is not 288 kHz, the filter transfer function frequencies are frequency-scaled by the ratios of the clock frequency to 288 kHz:

$$\text{Absolute Frequency (kHz)} = \frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{288} \quad (1)$$

For Low-Pass SCF $f_{\text{clock}} > 288$ kHz, please call the factory.

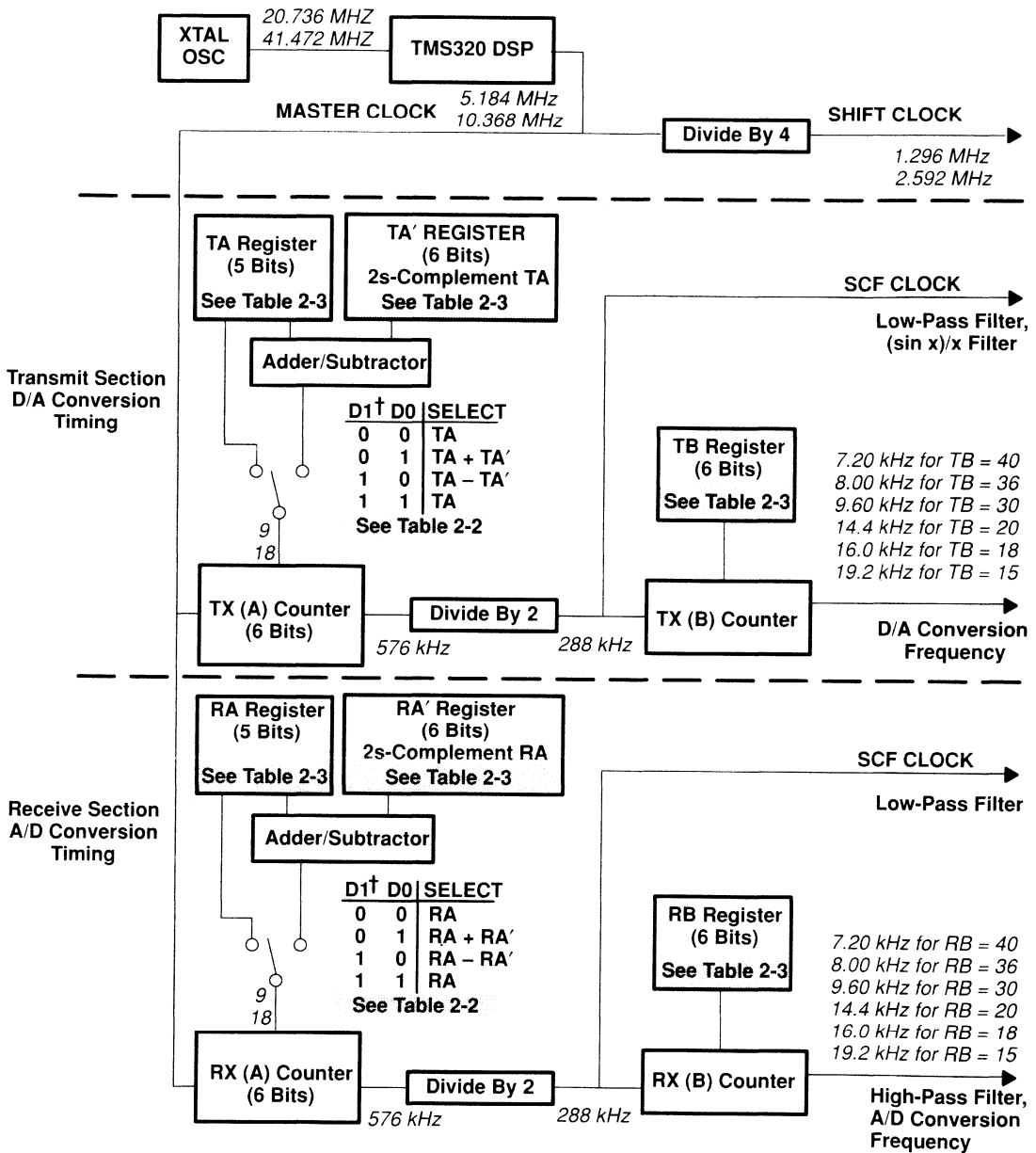
To obtain the specified filter response, the combination of master clock frequency and the TX(A) counter and the RX(A) counter values must yield a 288-kHz switched-capacitor clock signal. This 288-kHz clock signal can then be divided by the TX(B) counter to establish the D/A conversion timing.

The transfer function of the band-pass switched-capacitor filter in the A/D path (see Functional Block Diagram) is a composite of its high-pass and low-pass transfer functions. When the shift-clock frequency (SCF) is 288 kHz, the high-frequency roll-off of the low-pass section will meet the band-pass filter transfer function specification. Otherwise, the high-frequency roll-off is frequency-scaled by the ratio of the high-pass section SCF clock to 288 kHz (see Figure 5–5). The low-frequency roll-off of the high-pass section meets the band-pass filter transfer function specification when the A/D conversion rate is 16 kHz. If not, the low-frequency roll-off of the high-pass section is frequency-scaled by the ratio of the A/D conversion rate to 16 kHz.

The TX(A) counter and the TX(B) counter are reloaded each D/A conversion period, while the RX(A) counter and the RX(B) counter are reloaded every A/D conversion period. The TX(B) counter and the RX(B) counter are loaded with the values in the TB and RB registers, respectively. Via software control, the TX(A) counter can be loaded with the TA register, the TA register less the TA' register, or the TA register plus the TA' register. By selecting the TA register less the TA' register option, the upcoming conversion timing occurs earlier by an amount of time that equals TA' times the signal period of the master clock. If the TA register plus the TA' register option is executed, the upcoming conversion timing occurs later by an amount of time that equals TA' times the signal period of the master clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. However, the RX(A) counter can be programmed via software control with the RA register, the RA register less the RA' register, or the RA register plus the RA' register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing and can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous, then the low-pass and band-pass switched-capacitor filter clocks are derived from the TX(A) counter. Also, both the D/A and A/D conversion timings are derived from the TX(A) counter and the TX(B) counter. When the transmit and receive sections are configured to be asynchronous, the RX(A) counter, RX(B) counter, RA register, RA' register, and RB registers are not used.



† These control bits are described in the DX Serial Data Word Format section.

- NOTES: A. Tables 2–2 and 2–3 are primary and secondary communication protocols, respectively.
- B. In synchronous operation, RA, RA', RB, RX(A), and RX(B) are not used. TA, TA', TB, TX(A), and TX(B) are used instead.
- C. Items in italics refer only to frequencies and register contents, which are variable. A crystal oscillator driving 20.736 MHz into the TMS320-series DSP provides a master clock frequency of 5.184 MHz. The TLC32046 produces a shift clock frequency of 1.296 MHz. If the TX(A) register contents equal 9, the SCF clock frequency is 288 kHz, and the D/A conversion frequency is $288 \text{ kHz} \div T(B)$.

Figure 2–1. Asynchronous Internal Timing Configuration

2.2 Analog Input

Two pairs of analog inputs are provided. Normally, the IN+ and IN– input pair is used; however, the auxiliary input pair, AUX IN+ and AUX IN–, can be used if a second input is required. Since sufficient common-mode range and rejection are provided, each input set can be operated in differential or single-ended modes. The gain for the IN+, IN–, AUX IN+, and AUX IN– inputs can be programmed to 1, 2, or 4 (see Table 4–1). Either input circuit can be selected via software control. Multiplexing is controlled with the D4 bit (enable/disable AUX IN+ and AUX IN–) of the secondary DX word (see Table 2–3). The multiplexing requires a 2-ms wait at $SCF = 288\text{ kHz}$ (see Figure 5–3) for a valid output signal. A wide dynamic range is ensured by the differential internal analog architecture and the separate analog and digital voltage supplies and grounds.

2.3 A/D Band-Pass Filter, Clocking, and Conversion Timing

The receive-channel A/D high-pass filter can be selected or bypassed via software control (see Functional Block Diagram). The frequency response of this filter is found in the electrical characteristic section. This response results when the switched-capacitor filter clock frequency is 288 kHz and the A/D sample rate is 16 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the low-pass filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 288 kHz (see Typical Characteristics section). The ripple bandwidth and 3-dB low-frequency roll-off points of the high-pass section are 300 Hz and 200 Hz, respectively. However, the high-pass section low-frequency roll-off is frequency-scaled by the ratio of the A/D sample rate to 16 kHz.

Figure 2–1 and the DX serial data word format sections of this data manual indicate the many options for attaining a 288-kHz band-pass switched-capacitor filter clock. These sections indicate that the RX(A) counter can be programmed to give a 288-kHz band-pass switched-capacitor filter clock for several master clock input frequencies.

The A/D conversion rate is attained by frequency-dividing the band-pass switched-capacitor filter clock with the RX(B) counter. Unwanted aliasing is prevented because the A/D conversion rate is an integer submultiple of the band-pass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

2.4 A/D Converter

Fundamental performance specifications for the receive channel ADC circuitry are in the electrical characteristic section of this data manual. The ADC circuitry, using switched-capacitor techniques, provides an inherent sample-and-hold function.

2.5 Analog Output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

2.6 D/A Low-Pass Filter, Clocking, and Conversion Timing

The frequency response results when the low-pass switched-capacitor filter clock frequency is 288 kHz (see equation 1). Like the A/D filter, the transfer function of this filter is frequency-scaled when the clock frequency is not 288 kHz (see Typical Characteristics section). A continuous-time filter is provided on the output of the low-pass filter to eliminate the periodic sample data signal information, which occurs at multiples of the 288-kHz switched-capacitor clock feedthrough.

The D/A conversion rate is attained by frequency-dividing the 288-kHz switched-capacitor filter clock with the T(B) counter. Unwanted aliasing is prevented because the D/A conversion rate is an integer submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

2.7 D/A Converter

Fundamental performance specifications for the transmit channel DAC circuitry are in the electrical characteristic section. The DAC has a sample-and-hold function that is realized with a switched-capacitor ladder.

2.8 Serial Port

The serial port has four possible configurations summarized in the function table on page 1–2. These configurations are briefly described below.

- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS320C17. The communications protocol is two 8-bit bytes.
- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, and TMS320C30. The communications protocol is one 16-bit word.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS320C17. The communications protocol is two 8-bit bytes.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, TMS320C30, or two SN74299 serial-to-parallel shift registers, which can interface in parallel to the TMS32010, TMS320C15, to any other digital signal processor, or to external FIFO circuitry. The communications protocol is one 16-bit word.

2.9 Synchronous Operation

When the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and band-pass filters (see Functional Block Diagram). The A/D conversion timing is derived from and equal to the D/A conversion timing. When data bit D5 in the control register is a logic 1, transmit and receive sections are synchronous. The band-pass switched-capacitor filter and the A/D converter timing are derived from the TX(A) counter, the TX(B) counter, and the TA and TA' registers. In synchronous operation, both the A/D and the D/A channels operate from the same frequencies. The \overline{FSX} and the \overline{FSR} timing is identical during primary communication, but \overline{FSR} is not asserted during secondary communication because there is no new A/D conversion result.

2.9.1 One 16-Bit Word (Dual-Word [Telephone Interface] or Word Mode)

The serial port interfaces directly with the serial ports of the TMS32020, TMS320C25, and the TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows:

1. The \overline{FSX} and \overline{FSR} pins are brought low by the TLC32046 AIC.
2. One 16-bit word is transmitted and one 16-bit word is received.
3. \overline{FSX} and \overline{FSR} are brought high.
4. \overline{EODX} and \overline{EODR} emit low-going pulses one shift clock wide. \overline{EODX} and \overline{EODR} are valid in the word or byte mode only.

If the device is in the dual-word (telephone interface) mode, \overline{FSD} goes low during the secondary communication period and enables the data word received at the DATA-DR/CONTROL input to be routed to the DR line. The secondary communication period occurs four shift clocks after completion of primary communications.

2.9.2 Two 8-Bit Bytes (Byte Mode)

The serial port interfaces directly with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows:

1. \overline{FSX} and \overline{FSR} are brought low.
2. One 8-bit word is transmitted and one 8-bit word is received.
3. \overline{EODX} and \overline{EODR} are brought low.
4. \overline{FSX} and \overline{FSR} emit positive frame-sync pulses that are four shift clock cycles wide.
5. One 8-bit byte is transmitted and one 8-bit byte is received.
6. \overline{FSX} and \overline{FSR} are brought high.
7. \overline{EODX} and \overline{EODR} are brought high.

2.9.3 Synchronous Operating Frequencies

The synchronous operating frequencies are determined by the following equations.

Switched capacitor filter (SCF) frequencies (see Figure 2–1):

$$\text{Low-pass SCF clock frequency (D/A and A/D channels)} = \frac{\text{master clock frequency}}{T(A) \times 2}$$

$$\text{High-pass SCF clock frequency (A/D channel)} = \text{A/D conversion frequency}$$

$$\begin{aligned} \text{Conversion frequency (A/D and D/A channels)} &= \frac{\text{low-pass SCF clock frequency}}{T(B)} \\ &= \frac{\text{master clock frequency}}{T(A) \times 2 \times T(B)} \end{aligned}$$

NOTE: T(A), T(B), R(A), and R(B) are the contents of the TA, TB, RA, and RB registers, respectively.

2.10 Asynchronous Operation

When the transmit and the receive sections are operated asynchronously, the low-pass and band-pass filter clocks are independently generated from the master clock. The D/A and the A/D conversion timing is also determined independently.

D/A timing is set by the counters and registers described in synchronous operation, but the RA and RB registers are substituted for the TA and TB registers to determine the A/D channel sample rate and the A/D path switched-capacitor filter frequencies. Asynchronous operation is selected by control register bit D5 being zero.

2.10.1 One 16-Bit Word (Word Mode)

The serial port interfaces directly with the serial ports of the TMS32020, TMS320C25, and TMS320C30 and communicates with 16-bit word formats. The operation sequence is as follows:

1. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought low by the TLC32046 AIC.
2. One 16-bit word is transmitted or one 16-bit word is received.
3. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought high.
4. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ emit low-going pulses one shift clock wide. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are valid in either the word or byte mode only.

2.10.2 Two 8-Bit Bytes (Byte Mode)

The serial port interfaces directly with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operating sequence is as follows:

1. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought low by the TLC32046 AIC.
2. One byte is transmitted or received.
3. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ are brought low.
4. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought high for four shift clock periods and then brought low.
5. The second byte is transmitted or received.
6. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought high.
7. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ are brought high.

2.10.3 Asynchronous Operating Frequencies

The asynchronous operating frequencies are determined by the following equations.

Switched-capacitor filter frequencies (see Figure 2–1):

$$\text{Low-pass D/A SCF clock frequency} = \frac{\text{master clock frequency}}{T(A) \times 2}$$

$$\text{Low-pass A/D SCF clock frequency} = \frac{\text{master clock frequency}}{R(A) \times 2}$$

$$\text{High-pass SCF clock frequency (A/D channel)} = \text{A/D conversion frequency} \quad (2)$$

Conversion frequency:

$$\text{D/A conversion frequency} = \frac{\text{low-pass D/A SCF clock frequency}}{T(B)}$$

$$\text{A/D conversion frequency} = \frac{\text{low-pass A/D SCF clock frequency (for low pass receive filter)}}{R(B)} \quad (3)$$

NOTE: T(A), T(B), R(A), and R(B) are the contents of the TA, TB, RA, and RB registers, respectively.

2.11 Operation of TLC32046 With Internal Voltage Reference

The internal reference of the TLC32046 eliminates the need for an external voltage reference and provides overall circuit cost reduction. The internal reference eases the design task and provides complete control of the IC performance. The internal reference is brought out to REF. To keep the amount of noise on the reference signal to a minimum, an external capacitor can be connected between REF and ANLG GND.

2.12 Operation of TLC32046 With External Voltage Reference

REF can be driven from an external reference circuit. This external circuit must be capable of supplying 250 μ A and must be protected adequately from noise and crosstalk from the analog input.

2.13 Reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on RESET, the AIC is initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX Data Word Format section). After RESET, TA=TB=RA=RB=18 (or 12 hexadecimal), TA'=RA'=01 (hexadecimal), the A/D high-pass filter is inserted, the loop-back function is deleted, AUX IN+ and AUX IN- are disabled, transmit and receive sections are in synchronous operation, programmable gain is set to 1, the on-board (sin x)/x correction filter is not selected, D10OUT is set to 0, and D11OUT is set to 0.

2.14 Loopback

This feature allows the circuit to be tested remotely. In loopback, OUT+ and OUT- are internally connected to IN+ and IN-. The DAC bits (D15 to D2), which are transmitted to DX, can be compared with the ADC bits (D15 to D2), received from DR. The bits on DR equal the bits on DX. However, there is some difference in these bits due to the ADC and DAC output offsets.

The loopback feature is implemented with digital signal processor control by transmitting a logic 1 for data bit D3 in the DX secondary communication to the control register (see Table 2-3).

2.15 Communications Word Sequence

In the dual-word (telephone interface) mode, there are two data words that are presented to the DSP or μP from the DR terminal. The first data word is the ADC conversion result occurring during the FSR time, and the second is the serial data applied to DATA-DR during the FSD time. FSR is not asserted during secondary communications and FSD is not asserted during primary communications.

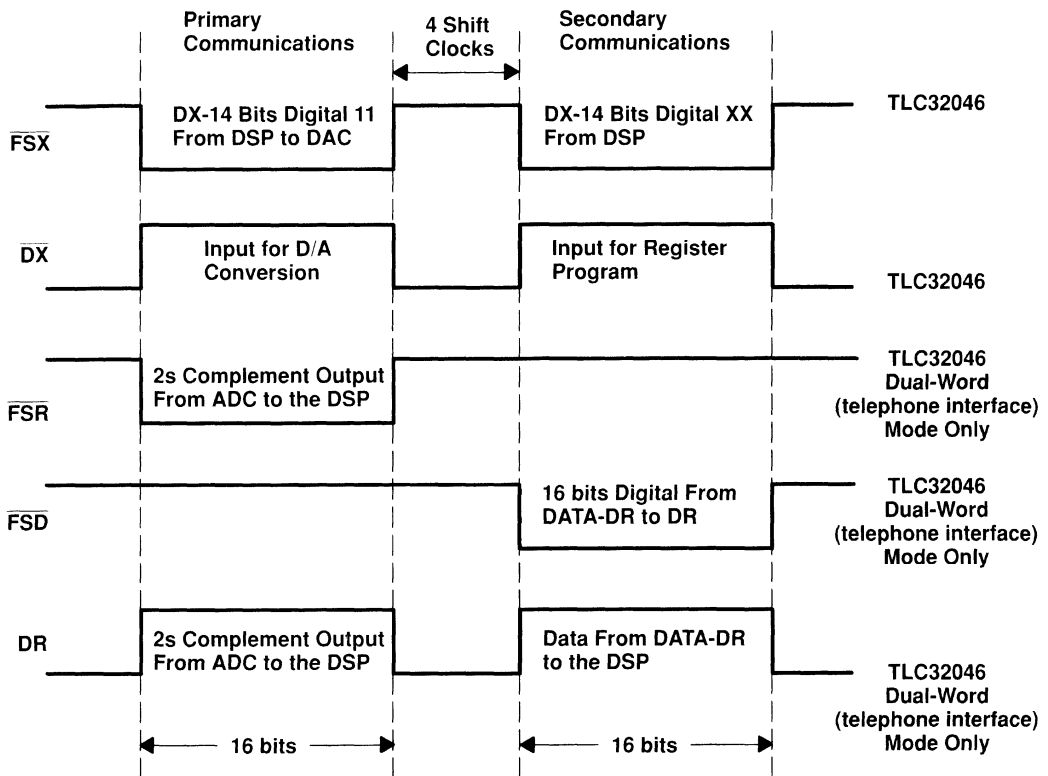
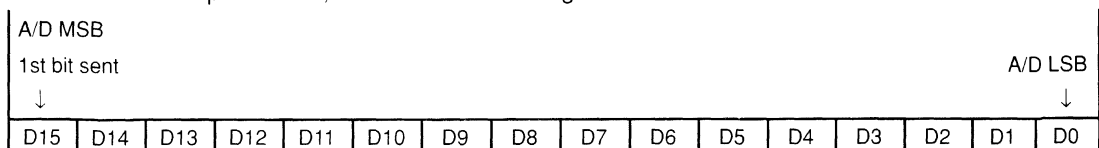


Figure 2-2. Primary and Secondary Communications Word Sequence

2.15.1 DR Word Bit Pattern

The data word is the 14-bit conversion result of the receive channel to the processor in 2s complement format. With 16-bit processors, the data is 16 bits long with the two LSBs at zero.



2.15.2 Primary DX Word Bit Pattern

Using 8-bit processors, the data word is transmitted in the same order as one 16-bit word, but as two bytes with the two LSBs of the second byte set to zero.

A/D OR D/A MSB															
1st bit sent				1st bit sent of 2nd byte								A/D or D/A LSB			
↓				↓								↓			
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 2–2. Primary DX Serial Communication Protocol

FUNCTIONS	D1	D0
D15 (MSB)-D2 → DAC Register. TA → TX(A), RA → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1).	0	0
D15 (MSB)-D2 → DAC Register. TA+TA' → TX(A), RA+RA' → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1). The next D/A and A/D conversion period is changed by the addition of TA' and RA' master clock cycles, in which TA' and RA' can be positive, negative, or zero (refer to Table 2–4).	0	1
D15 (MSB)-D2 → DAC Register. TA-TA' → TX(A), RA-RA' → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1). The next D/A and A/D conversion period is changed by the subtraction of TA' and RA' master clock cycles, in which TA' and RA' can be positive, negative, or zero (refer to Table 2–4).	1	0
D15 (MSB)-D2 → DAC Register. TA → TX(A), RA → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1). After a delay of four shift cycles, a secondary transmission follows to program the AIC to operate in the desired configuration. In the telephone interface mode, data on DATA DR is routed to DR during secondary transmission.	1	1

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (primary communications) to the AIC initiates secondary communications upon completion of the primary communications. When the primary communication is complete, FSR remains high for four SHIFT CLOCK cycles and then goes low and initiates the secondary communication. The timing specifications for the primary and secondary communications are identical. In this manner, the secondary communication, if initiated, is interleaved between successive primary communications. This interleaving prevents the secondary communication from interfering with the primary communications and DAC timing. This prevents the AIC from skipping a DAC output. FSR is not asserted during secondary communications activity. However, in the dual-word (telephone interface) mode, FSD is asserted during secondary communications but not during primary communications.

2.15.3 Secondary DX Word Bit Pattern

D/A MSB															1st bit sent															1st bit sent of 2nd byte															D/A LSB																		
↓															↓															↓																																	
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 2–3. Secondary DX Serial Communication Protocol

FUNCTIONS	D1	D0
D13 (MSB)-D9 → TA , 5 bits unsigned binary (see Figure 2–1). D6 (MSB)-D2 → RA, 5 bits unsigned binary (see Figure 2–1). D15, D14, D8, and D7 are unassigned.	0	0
D14 (sign bit)-D9 → TA', 6 bits 2s complement (see Figure 2–1). D7 (sign bit)-D2 → RA', 6 bits 2s complement (see Figure 2–1). D15 and D8 are unassigned.	0	1
D14 (MSB)-D9 → TB, 6 bits unsigned binary (see Figure 2–1). D7 (MSB)-D2 → RB, 6 bits unsigned binary (see Figure 2–1). D15 and D8 are unassigned.	1	0
D2 = 0/1 deletes/inserts the A/D high-pass filter. D3 = 0/1 deletes/inserts the loopback function. D4 = 0/1 disables/enables AUX IN+ and AUX IN–. D5 = 0/1 asynchronous/synchronous transmit and receive sections. D6 = 0/1 gain control bits (see Table 4–1). D7 = 0/1 gain control bits (see Table 4–1). D9 = 0/1 delete/insert on-board second-order (sinx)/x correction filter D10 = 0/1 output to D10OUT (dual-word (telephone interface) mode) D11 = 0/1 output to D11OUT (dual-word (telephone interface) mode) D8, D12–D15 are unassigned.	1	1

2.16 Reset Function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on $\overline{\text{RESET}}$ initializes the AIC registers to provide a 16-kHz A/D and D/A conversion rate for a 10.368-MHz master clock input signal. Also, the pass-bands of the A/D and D/A filters are 300 Hz to 7200 Hz and 0 Hz to 7200 Hz, respectively; therefore, the filter bandwidths are half those shown in the filter transfer function specification section. The AIC, except the CONTROL register, is initialized as follows (see AIC DX Data Word Format section):

REGISTER	TA	TA'	TB	RA	RA'	RB
INITIALIZED VALUE (HEX)	12	01	12	12	01	12

The CONTROL register bits are reset as follows (see Table 2–3):

$$D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1$$

This initialization allows normal serial port communications to occur between the AIC and the DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA', and TB register need to be programmed. Both transmit and receive timing are synchronously derived from these registers (see the Terminal Functions and DX Serial Data Word Format sections).

Figure 2–3 shows a circuit that provides a reset on power-up when power is applied in the sequence given in the power-up sequence section. The circuit depends on the power supplies reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.

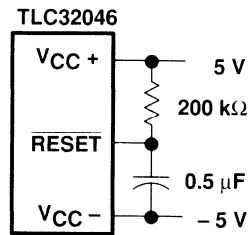


Figure 2–3. Reset on Power-Up Circuit

2.17 Power-Up Sequence

To ensure proper operation of the AIC and as a safeguard against latch-up, it is recommended that Schottky diodes with forward voltages less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND and from V_{CC-} to DGTL GND. In the absence of such diodes, power is applied in the following sequence: ANLG GND and DGTL GND, V_{CC-} , then V_{CC+} and V_{DD} . Also, no input signal is applied until after power-up.

2.18 AIC Register Constraints

The following constraints are placed on the contents of the AIC registers:

1. TA register must be ≥ 4 in word mode (WORD/BYTE= high).
2. TA register must be ≥ 5 in byte mode (WORD/BYTE= low).
3. TA' register can be either positive, negative, or zero.
4. RA register must be ≥ 4 in word mode (WORD/BYTE = high).
5. RA register must be ≥ 5 in byte mode (WORD/BYTE = low).
6. RA' register can be either positive, negative, or zero.
7. (TA register \pm TA' register) must be > 1 .
8. (RA register \pm RA' register) must be > 1 .
9. TB register must be ≥ 15 .
10. RB register must be ≥ 15 .

2.19 AIC Responses to Improper Conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 2–4.

Table 2–4. AIC Responses to Improper Conditions

IMPROPER CONDITION	AIC RESPONSE
TA register + TA' register = 0 or 1 TA register – TA' register = 0 or 1	Reprogram TX(A) counter with TA register value
TA register + TA' register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into TX(A) counter, i.e., TA register + TA' register + 40 HEX is loaded into TX(A) counter.
RA register + RA' register = 0 or 1 RA register – RA' register = 0 or 1	Reprogram RX(A) counter with RA register value
RA register + RA' register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX(A) counter, i.e., RA register + RA' register + 40 HEX is loaded into RX(A) counter.
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down. Reprogram TA or RA registers after a reset.
TA register < 4 in word mode TA register < 5 in byte mode RA register < 4 in word mode RA register < 5 in byte mode	The AIC serial port no longer operates. Reprogram TA or RA registers after a reset.
TB register < 15	Reprogram TB register with 12 HEX
RB register < 15	Reprogram RB register with 12 HEX
AIC and DSP cannot communicate	Hold last DAC output

2.20 Operation With Conversion Times Too Close Together

If the difference between two successive D/A conversion frame syncs is less than 1/25 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly, and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A' register result is too small. When incrementally adjusting the conversion period via the A + A' register options, the designer should not violate this requirement (see Figure 2–4).

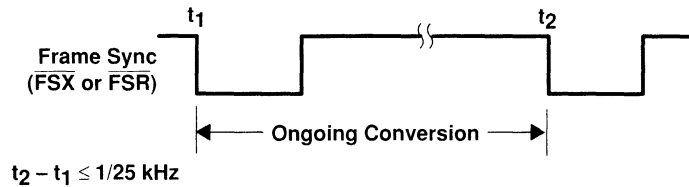


Figure 2–4. Conversion Times Too Close Together

2.21 More Than One Receive Frame Sync Occurring Between Two Transmit Frame Syncs – Asynchronous Operation

When incrementally adjusting the conversion period via the A + A' or A – A' register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during an FSX frame sync. The ongoing conversion period is then adjusted; however, either receive conversion period A or conversion period B can be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. If there is sufficient time between t_1 and t_2 , the receive conversion period adjustment is performed during receive conversion period A. Otherwise, the adjustment is performed during receive conversion period B.

The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent FSX frame (see Figure 2–5).

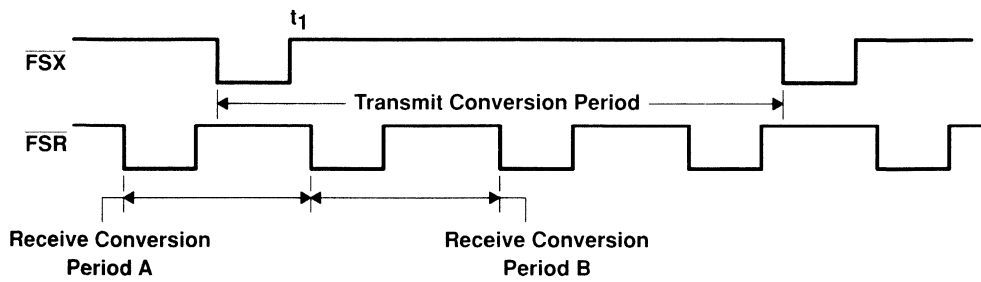


Figure 2-5. More Than One Receive Frame Sync Between Two Transmit Frame Syncs

2.22 More Than One Transmit Frame Sync Occurring Between Two Receive Frame Syncs – Asynchronous Operation

When incrementally adjusting the conversion period via the $A + A'$ or $A - A'$ register options, a specific protocol must be followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during an \overline{FSX} frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment as shown in Figure 2-6. When the adjustment command is issued during transmit conversion period A, receive conversion period A is adjusted if there is sufficient time between t_1 and t_2 . If there is not sufficient time between t_1 and t_2 , receive conversion period B is adjusted. The third option is that the receive portion of an adjustment command can be ignored if the adjustment command is sent during a receive conversion period, which is adjusted due to a prior adjustment command. For example, if adjustment commands are issued during transmit conversion periods A, B, and C, the first two commands may cause receive conversion periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during receive conversion period B, which already is adjusted via the transmit conversion period B adjustment command.

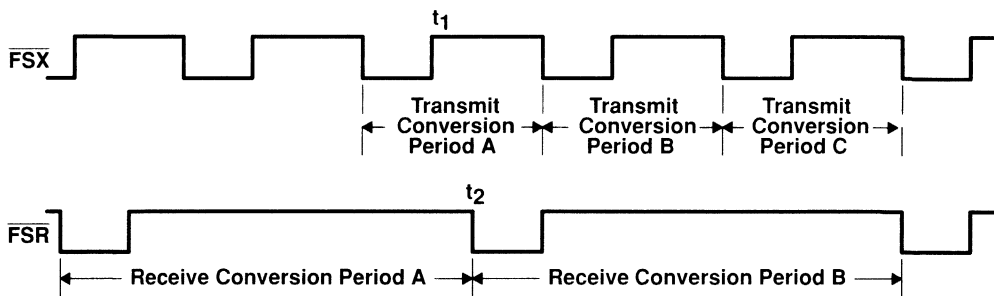


Figure 2-6. More Than One Transmit Frame Sync Between Two Receive Frame Syncs

2.23 More than One Set of Primary and Secondary DX Serial Communications Occurring Between Two Receive Frame Syncs (See DX Serial Data Word Format section) – Asynchronous Operation

The TA, TA', TB, and control register information that is transmitted in the secondary communication is accepted and applied during the ongoing transmit conversion period. If there is sufficient time between t_1 and t_2 , the TA, RA', and RB register information, sent during transmit conversion period A, is applied to receive conversion period A; otherwise, this information is applied during receive conversion period B. If RA, RA', and RB register information has been received and is being applied during an ongoing conversion period, any subsequent RA, RA', or RB information received during this receive conversion period is disregarded (see Figure 2-7).

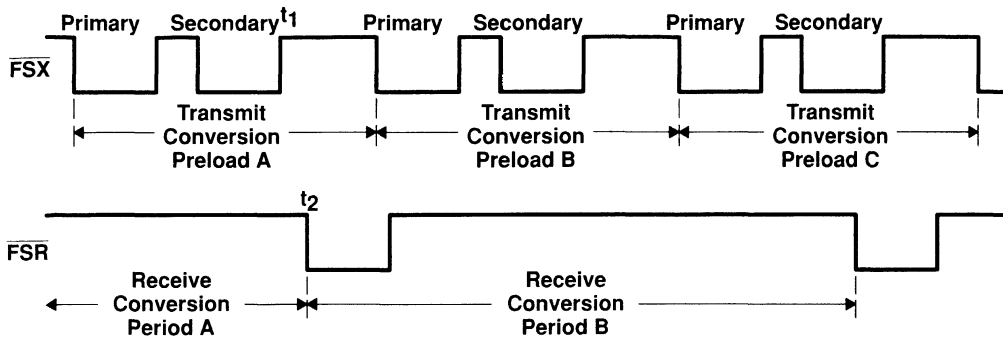


Figure 2–7. More Than One Set of Primary and Secondary DX Serial Communications Between Two Receive Frame Syncs

2.24 System Frequency Response Correction

The $(\sin x)/x$ correction for the DAC zero-order sample-and-hold output can be provided by an on-board second-order $(\sin x)/x$ correction filter (see Functional Block Diagram). This $(\sin x)/x$ correction filter can be inserted into or omitted from the signal path by digital-signal-processor control (data bit D9 in the DX secondary communications). When inserted, the $(\sin x)/x$ correction filter precedes the switched-capacitor low-pass filter. When the TB register (see Figure 2–1) equals 15, the correction results of Figures 5–5, 5–6, and 5–7 can be obtained.

The $(\sin x)/x$ correction [see section $(\sin x)/x$] can also be accomplished by disabling the on-board second-order correction filter and performing the $(\sin x)/x$ correction in digital signal processor software. The system frequency response can be corrected via DSP software to ± 0.1 dB accuracy to a band edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, that requires seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the $(\sin x)/x$ Correction Section for more details).

2.25 $(\sin x)/x$ Correction

If the designer does not wish to use the on-board second-order $(\sin x)/x$ correction filter, correction can be accomplished in digital signal processor (DSP) software. $(\sin x)/x$ correction can be accomplished easily and efficiently in digital signal processor software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results shown are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires seven instruction cycles per sample on the TMS320 DS. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction adds a slight amount of group delay at the upper edge of the 300-Hz to 3000-Hz band.

2.26 $(\sin x)/x$ Roll-Off for a Zero-Order Hold Function

The $(\sin x)/x$ roll-off error for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in Table 2–5 (see Figure 5–7).

Table 2-5. (sin x)/x Roll-Off Error

f_s (Hz)	Error = $20 \log \frac{\sin \pi f/f_s}{\pi f/f_s}$ $f = 3000$ Hz (dB)
7200	-2.64
8000	-2.11
9600	-1.44
14400	-0.63
16000	-0.50
19200	-0.35
25000	-0.21

The actual AIC (sin x)/x roll-off is slightly less than the figures in Table 2-5 because the AIC has less than 100% duty cycle hold interval.

2.27 Correction Filter

To externally compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter can be implemented as shown in Figure 2-8.

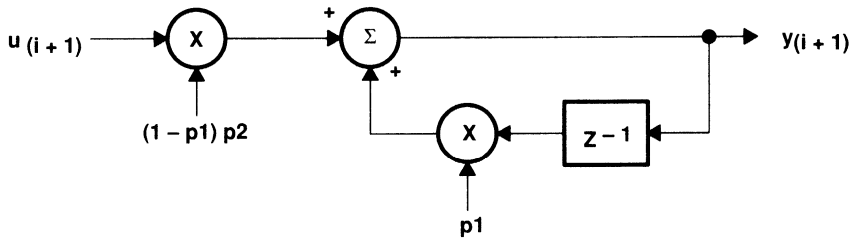


Figure 2-8. First-Order Correction Filter

The difference equation for this correction filter is:

$$y(i+1) = p2 \cdot (1 - p1) \cdot u(i+1) + p1 \cdot y(i) \quad (4)$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{(p2)^2 \cdot (1-p1)^2}{1 - 2 \cdot p1 \cdot \cos(2\pi f/f_s) + (p1)^2} \quad (5)$$

2.28 Correction Results

Table 2-6 shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates (see Figures 5-8, 5-9, and 5-10).

Table 2–6. (Sin x)/x Correction Table for $f_s = 8000$ Hz and $f_s = 9600$ Hz

f (Hz)	ROLL-OFF ERROR (dB)	ROLL-OFF ERROR (dB)
	$f_s = 8000$ Hz $p1 = -0.14813$ $p2 = 0.9888$	$f_s = 9600$ Hz $p1 = -0.1307$ $p2 = 0.9951$
300	-0.099	-0.043
600	-0.089	-0.043
900	-0.054	0
1200	-0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	-0.043	0
3000	-0.102	-0.043

2.29 TMS320 Software Requirements

The digital correction filter equation can be written in state variable form as follows:

$$y_{(i+1)} = y_{(i)} \cdot k1 + u_{(i+1)} \cdot k2$$

Where

$$k1 = p1$$

$$k2 = (1 - p1) p2$$

$y(i)$ = filter state

$u(i+1)$ = next I/O sample

The coefficients $k1$ and $k2$ must be represented as 16-bit integers. The SACH instruction (with the proper shift) yields the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)

Supply voltage range, V_{CC+} (see Note 1)	−0.3 V to 15 V
Supply voltage range, V_{DD}	−0.3 V to 15 V
Output voltage range, V_O	−0.3 V to 15 V
Input voltage range, V_I	−0.3 V to 15 V
Digital ground voltage range	−0.3 V to 15 V
Operating free-air temperature range: TLC32046C	0°C to 70°C
TLC32046I	−40°C to 85°C
TLC32046M	−55°C to 125°C
Storage temperature range: TLC32046C, TLC32046I	−40°C to 125°C
TLC32046M	−65°C to 150°C
Case temperature for 10 seconds: FN or FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N or J package	260°C

NOTE 1: Voltage values for maximum ratings are with respect to V_{CC-} .

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)	4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)	−4.75	−5	−5.25	V
Digital supply voltage, V_{DD} (see Note 2)	4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND		0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)	2		4	V
High-level input voltage, V_{IH}	2		$V_{DD}+0.3$	V
Low-level input voltage, V_{IL} (see Note 3)	−0.3		0.8	V
Load resistance at OUT+ and/or OUT−, R_L	300			Ω
Load capacitance at OUT+ and/or OUT−, C_L			100	pF
MSTR CLK frequency (see Note 4)		5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)			± 1.5	V
A/D or D/A conversion rate			25	kHz
Operating free-air temperature range, T_A	TLC32046C	0	70	°C
	TLC32046I	−40	85	
	TLC32046M	−55	125	

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+} , and V_{CC-} are with respect to ANLG GND. Voltages at digital inputs and outputs and V_{DD} are with respect to DGTL GND.

- The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data manual for logic voltage levels only.
- The band-pass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 288 kHz and the high-pass section SCF clock is 16 kHz. If the low-pass SCF clock is shifted from 288 kHz, the low-pass roll-off frequency shifts by the ratio of the low-pass SCF clock to 288 kHz. If the high-pass SCF clock is shifted from 16 kHz, the high-pass roll-off frequency shifts by the ratio of the high-pass SCF clock to 16 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 288 kHz. If the SCF clock is shifted from 288 kHz, the low-pass roll-off frequency shifts by the ratio of the SCF clock to 288 kHz.
- This range applies when $(IN+ - IN-)$ or $(AUX IN+ - AUX IN-)$ equals ± 6 V.

3.3 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, $V_{CC+} = 5\text{ V}$, $V_{CC-} = -5\text{ V}$, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted)

3.3.1 Total Device, MSTR CLK Frequency = 5.184 MHz, Outputs Not Loaded

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$V_{DD} = 4.75\text{ V}$, $I_{OH} = -300\text{ }\mu\text{A}$	2.4			V
V_{OL}	Low-level output voltage	$V_{DD} = 4.75\text{ V}$, $I_{OL} = 2\text{ mA}$			0.4	V
I_{CC+}	Supply current from V_{CC+}	TLC32046C			35	mA
		TLC32046I			40	
		TLC32046M			45	
I_{CC-}	Supply current from V_{CC-}	TLC32046C			-35	mA
		TLC32046I			-40	
		TLC32046M			-45	
I_{DD}	Supply current from V_{DD}				7	mA
V_{ref}	Internal reference output voltage	TLC32046M	2.9		3.3	V
α_{Vref}	Temperature coefficient of internal reference voltage			250		ppm/°C
r_o	Output resistance at REF			100		k Ω

3.3.2 Power Supply Rejection and Crosstalk Attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	$f = 0\text{ kHz to }30\text{ kHz}$	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)		30		dB
	$f = 30\text{ kHz to }50\text{ kHz}$			45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single-ended)	$f = 0\text{ kHz to }30\text{ kHz}$	Idle channel, supply signal at 200 mV p-p measured at OUT+		30		dB
	$f = 30\text{ kHz to }50\text{ kHz}$			45		
Crosstalk attenuation, transmit-to-receive (single-ended)	TLC32046C, I			80		dB
	TLC32046M		60	80		
Crosstalk attenuation, receive-to-transmit (single-ended)	TLC32046M		70	80		dB

3.3.3 Serial Port

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -300\text{ }\mu\text{A}$	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.4	V
I_I	Input current				± 10	μA
I_I	Input current, DATA-DR/CONTROL				± 100	μA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

† All typical values are at $T_A = 25^\circ\text{C}$.

3.3.4 Receive Amplifier Input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
A/D converter offset error (filters in)				10	70	mV
CMRR	Common-mode rejection ratio at IN+, IN–, or AUX IN+, AUX IN–	See Note 6		55		dB
r_i	Input resistance at IN+, IN– or AUX IN+, AUX IN+, AUX IN–, REF			100		k Ω

NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with a 16-kHz conversion rate.

3.3.5 Transmit Filter Output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+ or OUT– (single-ended relative to ANLG GND)	TLC32046C, I		15	80	mV
		TLC32046M		15	85	mV
V_{OM}	Maximum peak output voltage swing across R_L at OUT+ or OUT– (single-ended)	TLC32046C, I	$R_L \geq 300 \Omega$, Offset voltage = 0	± 3		V
	Maximum peak output voltage swing between OUT+ and OUT– (differential output)		$R_L \geq 600 \Omega$	± 6		V

† All typical values are at $T_A = 25^\circ\text{C}$.

3.3.6 Receive and Transmit Channel System Distortion, SCF Clock Frequency = 288 kHz (see Note 7)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	Single-ended	$V_I = -0.1 \text{ dB to } -24 \text{ dB}$		70		dB
	Differential		62	70		
Attenuation of third and higher harmonics of A/D input signal	Single-ended			65		dB
	Differential		57	65		
Attenuation of second harmonic of D/A input signal	Single-ended	$V_I = -0 \text{ dB to } -24 \text{ dB}$		70		dB
	Differential		62	70		
Attenuation of third and higher harmonics of D/A input signal	Single-ended			65		dB
	Differential		57	65		

† All typical values are at $T_A = 25^\circ\text{C}$.

3.3.7 Receive Channel Signal-to-Distortion Ratio (see Note 7)

PARAMETER	TEST CONDITIONS	$A_V = 1\ddagger$		$A_V = 2\ddagger$		$A_V = 4\ddagger$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio	$V_I = -6 \text{ dB to } -0.1 \text{ dB}$	58		§		§		dB
	$V_I = -12 \text{ dB to } -6 \text{ dB}$	58		58		§		
	$V_I = -18 \text{ dB to } -12 \text{ dB}$	56		58		58		
	$V_I = -24 \text{ dB to } -18 \text{ dB}$	50		56		58		
	$V_I = -30 \text{ dB to } -24 \text{ dB}$	44		50		56		
	$V_I = -36 \text{ dB to } -30 \text{ dB}$	38		44		50		
	$V_I = -42 \text{ dB to } -36 \text{ dB}$	32		38		44		
	$V_I = -48 \text{ dB to } -42 \text{ dB}$	26		32		38		
$V_I = -54 \text{ dB to } -48 \text{ dB}$	20		26		32			

‡ A_V is the programmable gain of the input amplifier.

§ Measurements under these conditions are unreliable due to overrange and signal clipping.

NOTE 7: The test condition is a 1-kHz input signal with a 16-kHz conversion rate. The load impedance for the DAC is 600 Ω . Input and output voltages are referred to V_{ref} .

3.3.8 Transmit Channel Signal-to-Distortion Ratio (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	$V_I = -6 \text{ dB to } -0.1 \text{ dB}$	58		dB
	$V_I = -12 \text{ dB to } -6 \text{ dB}$	58		
	$V_I = -18 \text{ dB to } -12 \text{ dB}$	56		
	$V_I = -24 \text{ dB to } -18 \text{ dB}$	50		
	$V_I = -30 \text{ dB to } -24 \text{ dB}$	44		
	$V_I = -36 \text{ dB to } -30 \text{ dB}$	38		
	$V_I = -42 \text{ dB to } -36 \text{ dB}$	32		
	$V_I = -48 \text{ dB to } -42 \text{ dB}$	26		
$V_I = -54 \text{ dB to } -48 \text{ dB}$	20			

NOTE 7: The test condition is a 1-kHz input signal with a 16-kHz conversion rate. The load impedance for the DAC is 600 Ω . Input and output voltages are referred to V_{ref} .

3.3.9 Receive and Transmit Gain and Dynamic Range (see Note 8)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit gain tracking error	C, I	$V_O = -48 \text{ dB to } 0 \text{ dB}$ signal range		± 0.05	± 0.15	dB
Receive gain tracking error	C, I	$V_I = -48 \text{ dB to } 0 \text{ dB}$ signal range		± 0.05	± 0.15	dB
Transmit gain tracking error	M	$V_O = -48 \text{ dB to } 0 \text{ dB}$ signal range, $T_A = 25^\circ\text{C}$		± 0.05	± 0.25	dB
Receive gain tracking error	M	$V_I = -48 \text{ dB to } 0 \text{ dB}$ signal range, $T_A = 25^\circ\text{C}$		± 0.05	± 0.25	dB
Transmit gain tracking error	M	$V_O = -48 \text{ dB to } 0 \text{ dB}$ signal range, $T_A = -55^\circ\text{C TO } 125^\circ\text{C}$			± 0.4	dB
Receive gain tracking error	M	$V_I = -48 \text{ dB to } 0 \text{ dB}$ signal range, $T_A = -55^\circ\text{C TO } 125^\circ\text{C}$			± 0.4	dB

NOTE 8: Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 dB relative to V_{ref}).

3.3.10 Receive Channel Band-Pass Filter Transfer Function, SCF $f_{\text{clock}} = 288 \text{ kHz}$, Input ($IN_+ - IN_-$) Is A $\pm 3\text{-V}$ Sine Wave \ddagger (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY	ADJUSTMENT	MIN	TYP \dagger	MAX	UNIT
Filter gain	Input signal reference is 0 dB	$f \leq 100 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-33	-29	-25	dB
		$f = 200 \text{ Hz}$	$K1 \times -0.26 \text{ dB}$	-4	-2	-1	
		$f = 300 \text{ Hz to } 6200 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.25	0	0.25	
		$f = 6200 \text{ Hz to } 6600 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.3	0	0.3	
		$f = 6600 \text{ Hz to } 7300 \text{ Hz}$	$K1 \times 0 \text{ dB}$		0	0.5	
		$f = 7600 \text{ Hz}$	$K1 \times 2.3 \text{ dB}$		-2	-0.5	
		$f = 8000 \text{ Hz}$	$K1 \times 2.7 \text{ dB}$		-16	-14	
		$f \geq 8800 \text{ Hz}$	$K1 \times 3.2 \text{ dB}$			-40	
		$f \geq 10000 \text{ Hz}$	$K1 \times 0 \text{ dB}$			-65	

3.3.11 Receive and Transmit Channel Low-Pass Filter Transfer Function, SCF $f_{\text{clock}} = 288 \text{ kHz}$ (see Note 9)

	TEST CONDITION	FREQUENCY RANGE	ADJUSTMENT ADDEND \ddagger	MIN	TYP \dagger	MAX	UNIT
Filter gain	Input signal reference is 0 dB	$f = 0 \text{ Hz to } 6200 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.25	0	0.25	dB
		$f = 6200 \text{ Hz to } 6600 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.3	0	0.3	
		$f = 6600 \text{ Hz to } 7300 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.5	0	0.5	
		$f = 7600 \text{ Hz}$	$K1 \times 2.3 \text{ dB}$		-2	-0.5	
		$f = 8000 \text{ Hz}$	$K1 \times 2.7 \text{ dB}$		-16	-14	
		$f \geq 8800 \text{ Hz}$	$K1 \times 3.2 \text{ dB}$			-40	
		$f \geq 10000 \text{ Hz}$	$K1 \times 0 \text{ dB}$			-65	

\dagger All typical values are at $T_A = 25^\circ\text{C}$.

\ddagger The MIN, TYP, and MAX specifications are given for a 288-kHz SCF clock frequency. A slight error in the 288-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where $K1 = 100 \cdot [(SCF \text{ frequency} - 288 \text{ kHz})/288 \text{ kHz}]$. For errors greater than 0.25%, see Note 9.

NOTE 9: The filter gain outside of the pass band is measured with respect to the gain at 1 kHz (2 kHz for M version). The filter gain within the pass band is measured with respect to the average gain within the pass band. The pass bands are 300 Hz to 7200 Hz and 0 to 7200 Hz for the band-pass and low-pass filters, respectively. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

3.4 Operating Characteristics Over Recommended Operating Free-Air Temperature Range, $V_{CC+} = 5\text{ V}$, $V_{CC-} = -5\text{ V}$, $V_{DD} = 5\text{ V}$

3.4.1 Receive and Transmit Noise (measurement includes low-pass and band-pass switched-capacitor filters)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit noise	Broadband with (sin x)/x	DX input = 00000000000000, Constant input code		250	500	μVrms
	Broadband without (sin x)/x			200	450	
	0 to 30 kHz with (sin x)/x			200	400	
	0 to 30 kHz without (sin x)/x			200	400	
	0 to 3.4 kHz with (sin x)/x			180	300	
	0 to 3.4 kHz without (sin x)/x			160	300	
	0 to 6.8 kHz with (sin x)/x (wide-band operation with 7.2 kHz roll-off)			180	350	
	0 to 6.8 kHz without (sin x)/x (wide-band operation with 7.2 kHz roll-off)			160	350	
Receive noise (see Note 10)		Inputs grounded, Gain = 1		300	500	μVrms
				18		dBrnc0

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 10: The noise is computed by statistically evaluating the digital output of the A/D converter.

3.5 Timing Requirements

3.5.1 Serial Port Recommended Input Signals, TLC32046C and TLC32046I

PARAMETER		MIN	MAX	UNIT
$t_c(\text{MCLK})$	Master clock cycle time	95		ns
$t_r(\text{MCLK})$	Master clock rise time		10	ns
$t_f(\text{MCLK})$	Master clock fall time		10	ns
	Master clock duty cycle	25%	75%	
	RESET pulse duration (see Note 11)	800		ns
$t_{su}(\text{DX})$	DX setup time before SCLK↓	20		ns
$t_h(\text{DX})$	DX hold time after SCLK↓		$t_c(\text{SCLK})/4$	ns

NOTE 11: RESET pulse duration is the amount of time that the RESET is held below 0.8 V after the power supplies have reached their recommended values.

3.5.2 Serial Port Recommended Input Signals, TLC32046M

PARAMETER		MIN	TYP†	MAX	UNIT
$t_c(\text{MCLK})$	Master clock cycle time	95			ns
$t_r(\text{MCLK})$	Master clock rise time		10		ns
$t_f(\text{MCLK})$	Master clock fall time		10		ns
	Master clock duty cycle		50%		
	RESET pulse duration (see Note 11)	800			ns
$t_{su}(\text{DX})$	DX setup time before SCLK↓	28			ns
$t_h(\text{DX})$	DX hold time after SCLK↓			$t_c(\text{SCLK})/4$	ns

NOTE 11: RESET pulse duration is the amount of time that the RESET is held below 0.8 V after the power supplies have reached their recommended values.

3.5.3 Serial Port – AIC Output Signals, $C_L = 30$ pF for SHIFT CLK Output, $C_L = 15$ pF For All Other Outputs, TLC32046C and TLC32046I

PARAMETER		MIN	TYP†	MAX	UNIT
$t_c(\text{SCLK})$	Shift clock (SCLK) cycle time	380			ns
$t_f(\text{SCLK})$	Shift clock (SCLK) fall time		3	8	ns
$t_r(\text{SCLK})$	Shift clock (SCLK) rise time		3	8	ns
	Shift clock (SCLK) duty cycle	45%		55%	
$t_d(\text{CH-FL})$	Delay from SCLK↑ to $\overline{\text{FSR}}/\overline{\text{FSX}}/\overline{\text{FSD}}\downarrow$		30		ns
$t_d(\text{CH-FH})$	Delay from SCLK↑ to $\overline{\text{FSR}}/\overline{\text{FSX}}/\overline{\text{FSD}}\uparrow$		35	90	ns
$t_d(\text{CH-DR})$	DR valid after SCLK↑			90	ns
$t_d(\text{CH-EL})$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}\downarrow$ in word mode			90	ns
$t_d(\text{CH-EH})$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}\uparrow$ in word mode			90	ns
$t_f(\text{EODX})$	$\overline{\text{EODX}}$ fall time		2	8	ns
$t_f(\text{EODR})$	$\overline{\text{EODR}}$ fall time		2	8	ns
$t_d(\text{CH-EL})$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}\downarrow$ in byte mode			90	ns
$t_d(\text{CH-EH})$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}\uparrow$ in byte mode			90	ns
$t_d(\text{MH-SL})$	Delay from MSTR CLK↑ to SCLK↓		65	170	ns
$t_d(\text{MH-SH})$	Delay from MSTR CLK↑ to SCLK↑		65	170	ns

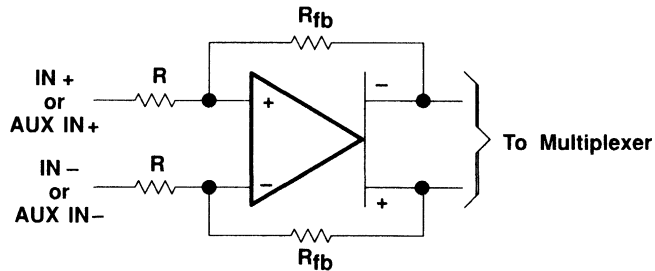
† Typical values are at $T_A = 25^\circ\text{C}$.

3.5.4 Serial Port – AIC Output Signals, $C_L = 30$ pF for SHIFT CLK Output, $C_L = 15$ pF For All Other Outputs, TLC32046M

PARAMETER		MIN	TYP†	MAX	UNIT
$t_c(\text{SCLK})$	Shift clock (SCLK) cycle time	400			ns
$t_f(\text{SCLK})$	Shift clock (SCLK) fall time		3		ns
$t_r(\text{SCLK})$	Shift clock (SCLK) rise time		3		ns
	Shift clock (SCLK) duty cycle	45%		55%	
$t_d(\text{CH-FL})$	Delay from SCLK↑ to $\overline{\text{FSR}}/\overline{\text{FSX}}/\overline{\text{FSD}}\downarrow$		30	250	ns
$t_d(\text{CH-FH})$	Delay from SCLK↑ to $\overline{\text{FSR}}/\overline{\text{FSX}}/\overline{\text{FSD}}\uparrow$		35	250	ns
$t_d(\text{CH-DR})$	DR valid after SCLK↑			250	ns
$t_d(\text{CH-EL})$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}\downarrow$ in word mode			250	ns
$t_d(\text{CH-EH})$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}\uparrow$ in word mode			250	ns
$t_f(\text{EODX})$	$\overline{\text{EODX}}$ fall time		2		ns
$t_f(\text{EODR})$	$\overline{\text{EODR}}$ fall time		2		ns
$t_d(\text{CH-EL})$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}\downarrow$ in byte mode			250	ns
$t_d(\text{CH-EH})$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}\uparrow$ in byte mode			250	ns
$t_d(\text{MH-SL})$	Delay from MSTR CLK↑ to SCLK↓		65	170	ns
$t_d(\text{MH-SH})$	Delay from MSTR CLK↑ to SCLK↑		65	170	ns

† Typical values are at $T_A = 25^\circ\text{C}$.

4 Parameter Measurement Information



$$R_{fb} = R \text{ for } D6 = 1 \text{ and } D7 = 1$$

$$D6 = 0 \text{ and } D7 = 0$$

$$R_{fb} = 2R \text{ for } D6 = 1 \text{ and } D7 = 0$$

$$R_{fb} = 4R \text{ for } D6 = 0, \text{ and } D7 = 1$$

Figure 4–1. IN+ and IN– Gain Control Circuitry

Table 4–1. Gain Control Table (Analog Input Signal Required for Full-Scale Bipolar A/D Conversion Twos Complement)[†]

INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT [‡] §	A/D CONVERSION RESULT
	D6	D7		
Differential configuration Analog input = IN+ – IN– = AUX IN+ – AUX IN–	1	1	$V_{ID} = \pm 6 \text{ V}$	±full scale
	0	0	$V_{ID} = \pm 3 \text{ V}$	±full scale
	1	0	$V_{ID} = \pm 1.5 \text{ V}$	±full scale
Single-ended configuration Analog input = IN+ – ANLG GND = AUX IN+ – ANLG GND	0	1	$V_I = \pm 3 \text{ V}$	±half scale
	1	0	$V_I = \pm 3 \text{ V}$	±full scale
	0	1	$V_I = \pm 1.5 \text{ V}$	±full scale

[†] $V_{CC+} = 5 \text{ V}$, $V_{CC-} = -5 \text{ V}$, $V_{DD} = 5 \text{ V}$

[‡] V_{ID} = Differential Input Voltage, V_I = Input voltage referenced to ground with IN– or AUX IN– connected to GND.

[§] In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.

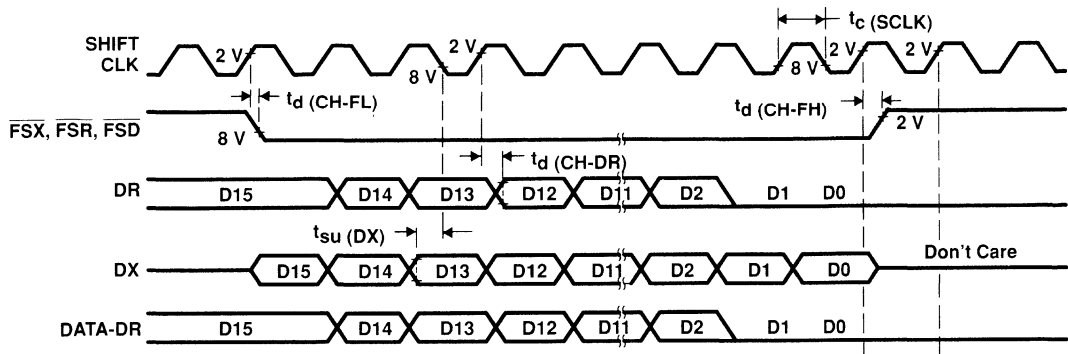


Figure 4–2. Dual-Word (Telephone Interface) Mode Timing

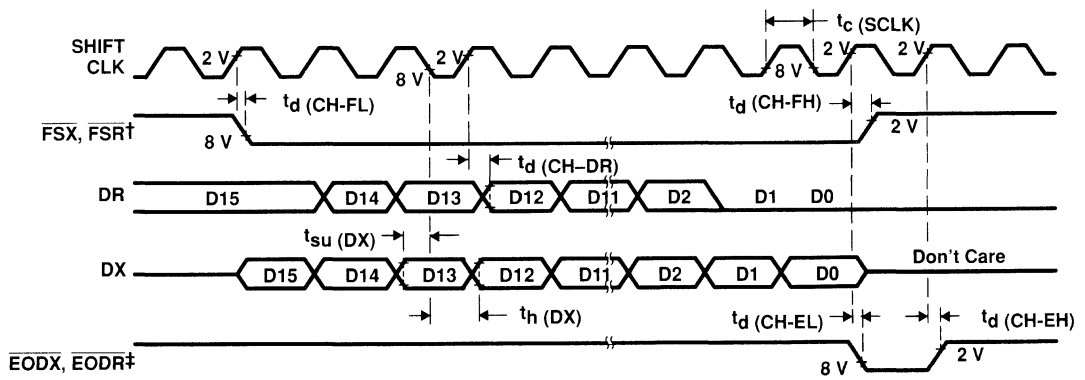


Figure 4–3. Word Timing

† The time between falling edges of $\overline{\text{FSR}}$ is the A/D conversion period and the time between falling edges of $\overline{\text{FSX}}$ is the D/A conversion period.

‡ In the word format, $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ go low to signal the end of a 16-bit data word to the processor. The word-cycle is 20 shift-clocks wide, giving a four-clock period setup time between data words.

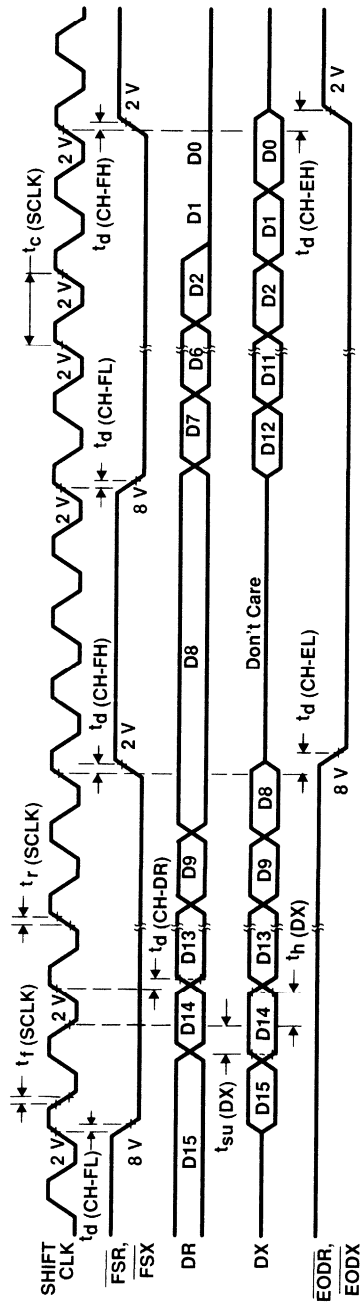


Figure 4-4. Byte-Mode Timing

† The time between falling edges of FSR is the A/D conversion period, and the time between falling edges of FSX is the D/A conversion period.
 ‡ In the byte mode, when EODX or EODR is high, the first byte is transmitted or received, and when these signals are low, the second byte is transmitted or received. Each byte-cycle is 12 shift-clocks long, allowing for a four-shift-clock setup time between byte transmissions.

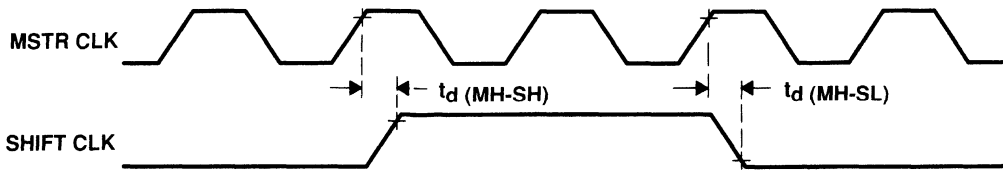


Figure 4-5. Shift-Clock Timing

4.1 TMS32010/TMS320C15 – TLC32046 Interface Circuit

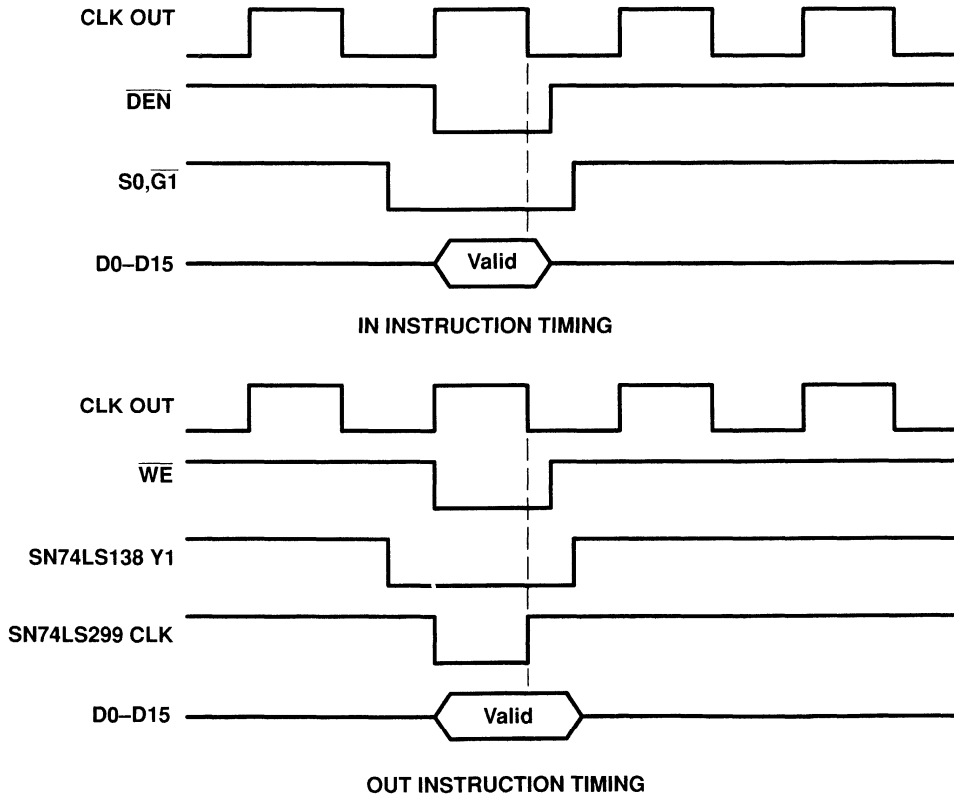


Figure 4-6. TMS32010/TMS320C15–TLC32046 Interface Timing

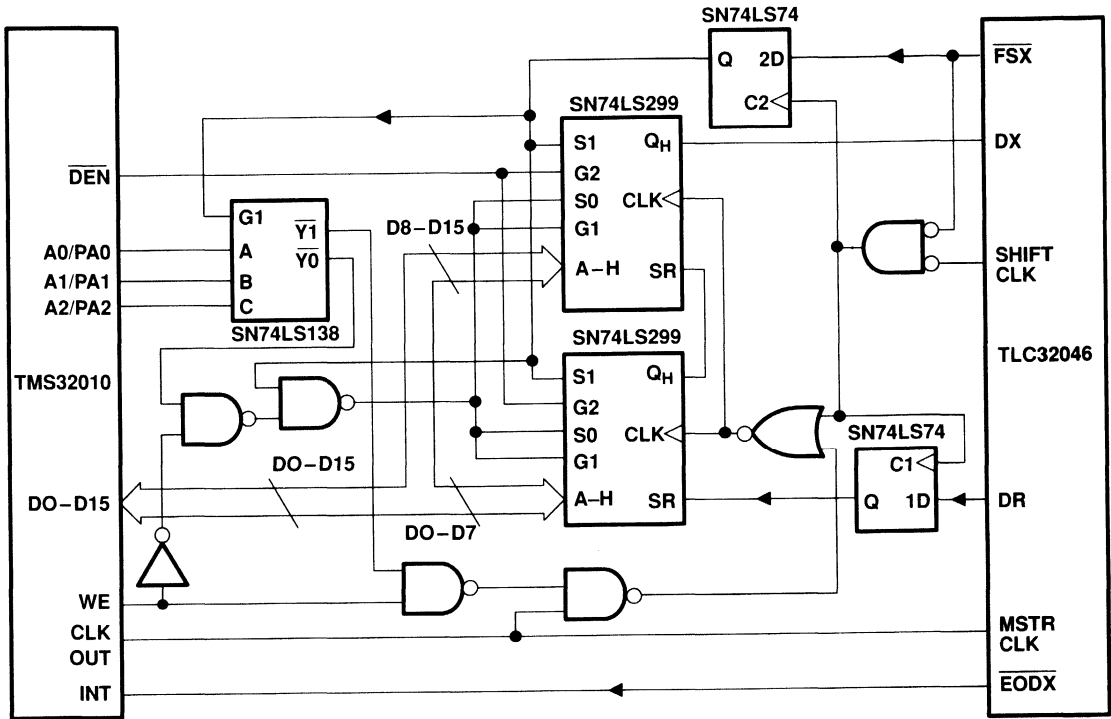


Figure 4-7. TMS32010/TMS320C15 - TLC32046 Interface Circuit

5 Typical Characteristics

D/A AND A/D LOW-PASS FILTER RESPONSE SIMULATION

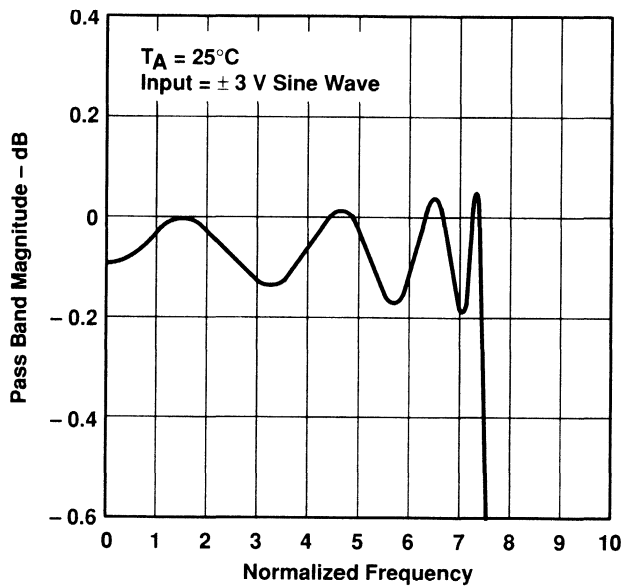


Figure 5-1

D/A AND A/D LOW-PASS FILTER RESPONSE

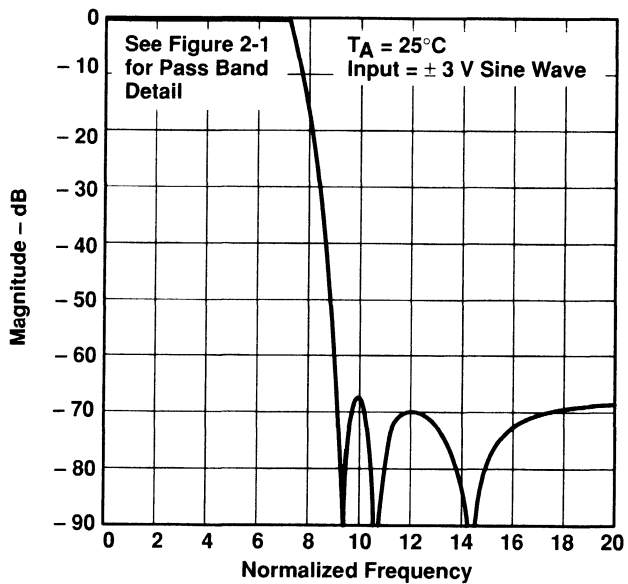


Figure 5-2

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{288}$
 For Low-Pass SCF $f_{\text{clock}} > 288$ kHz, please call the factory.

D/A AND A/D LOW-PASS GROUP DELAY

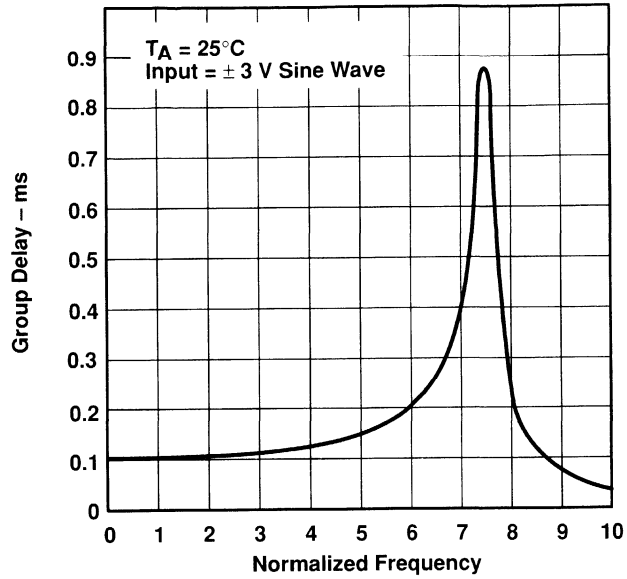


Figure 5-3

A/D BAND-PASS RESPONSE

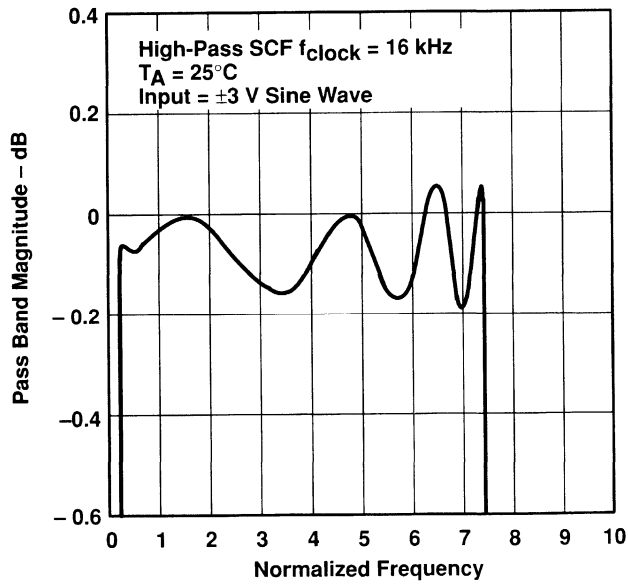


Figure 5-4

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{288}$

For Low-Pass SCF $f_{\text{clock}} > 288$ kHz, please call the factory.

A/D BAND-PASS FILTER RESPONSE SIMULATION

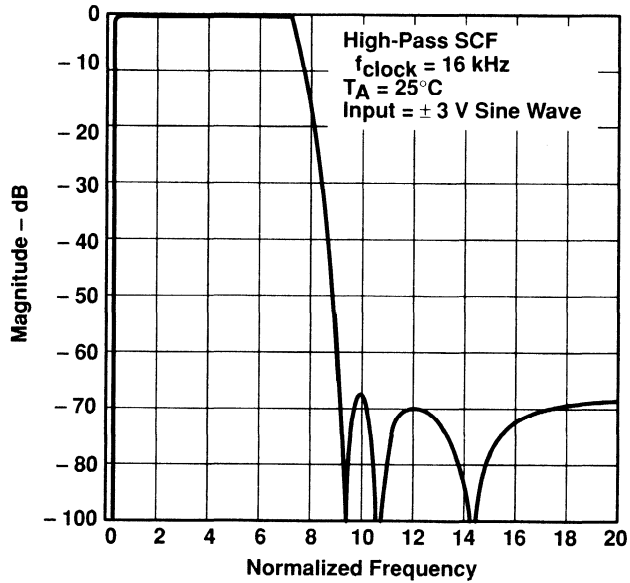


Figure 5-5

A/D BAND-PASS FILTER GROUP DELAY

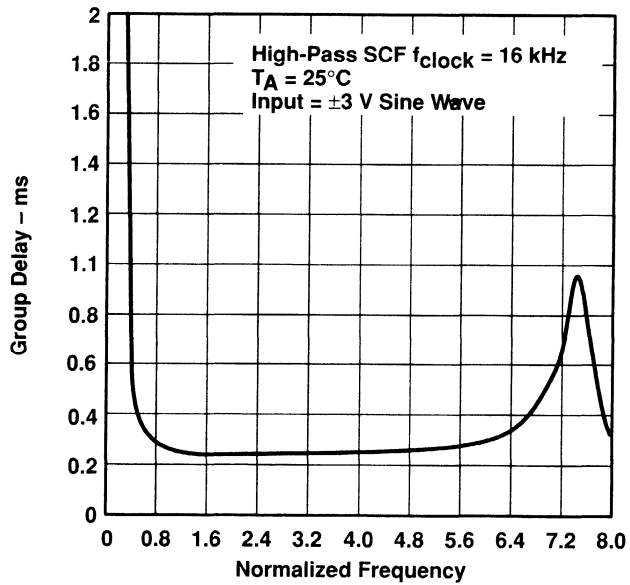


Figure 5-6

NOTE : Absolute Frequency (kHz) =
$$\frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{288}$$

For Low-Pass SCF $f_{\text{clock}} > 288 \text{ kHz}$, please call the factory.

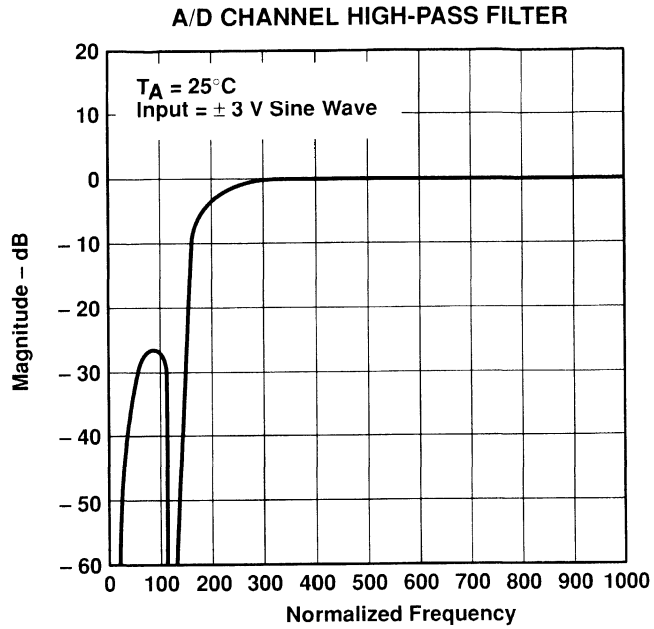


Figure 5-7

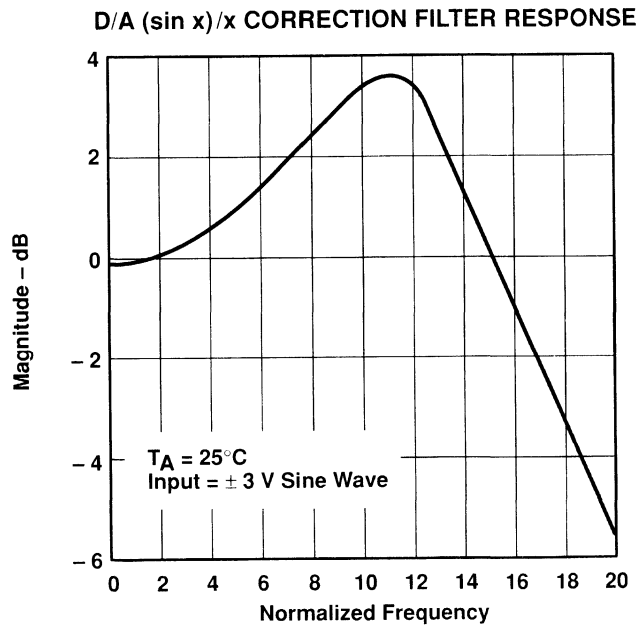


Figure 5-8

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{288}$

For Low-Pass SCF $f_{\text{clock}} > 288$ kHz, please call the factory.

D/A (sin x)/x CORRECTION FILTER RESPONSE

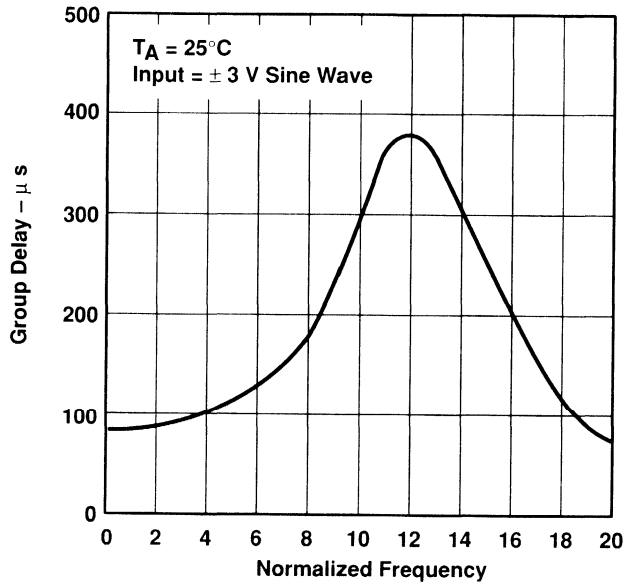


Figure 5-9

D/A (sin x)/x CORRECTION ERROR

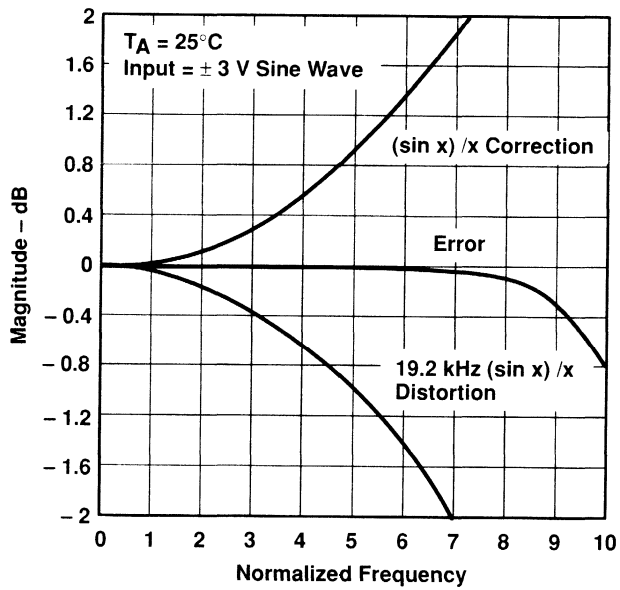


Figure 5-10

NOTE : Absolute Frequency (kHz) =
$$\frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{288}$$

For Low-Pass SCF $f_{\text{clock}} > 288\text{ kHz}$, please call the factory.

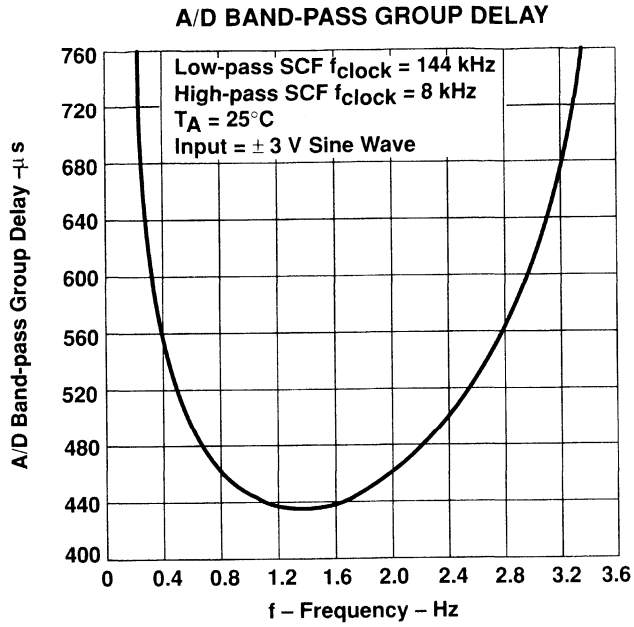


Figure 5-11

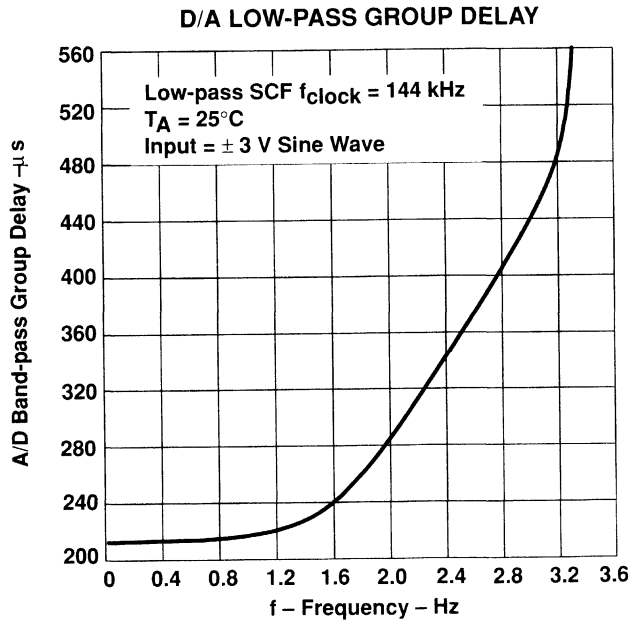


Figure 5-12

**A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL**

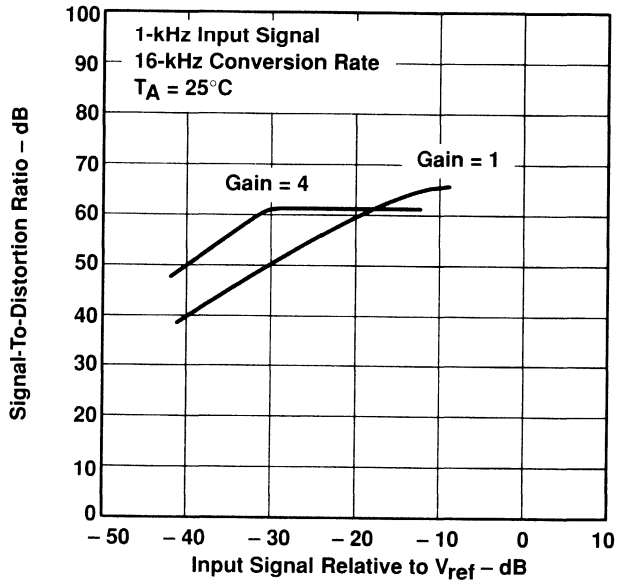


Figure 5-13

**A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN AT 0-dB INPUT SIGNAL)**

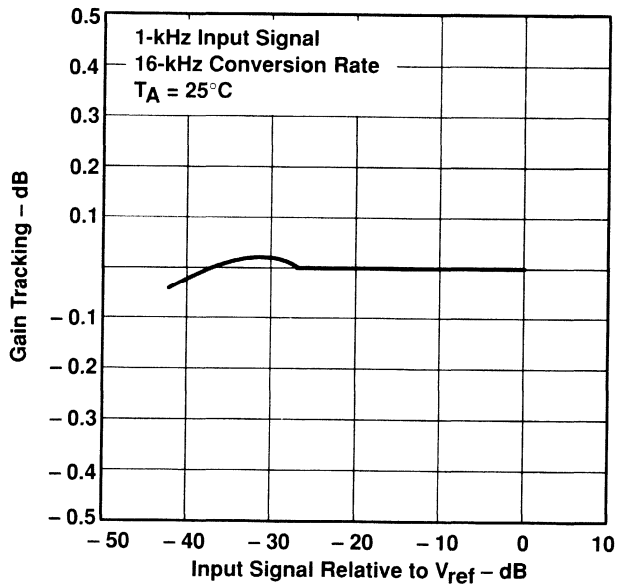


Figure 5-14

**D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL**

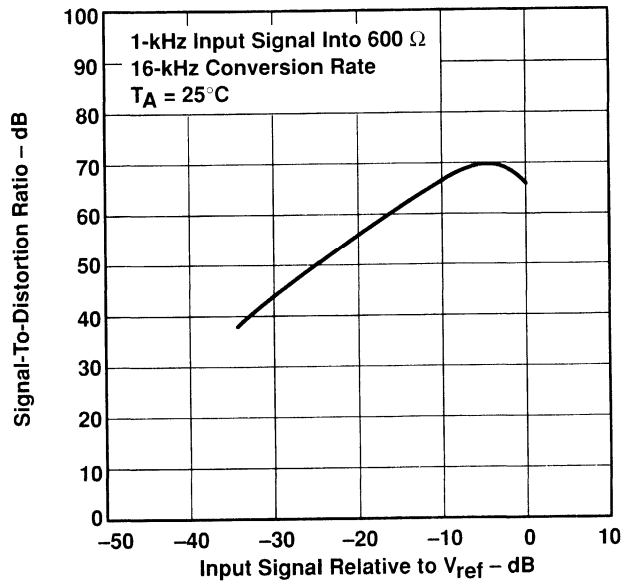


Figure 5-15

**D/A GAIN TRACKING (GAIN RELATIVE TO GAIN
AT 0-dB INPUT SIGNAL)**

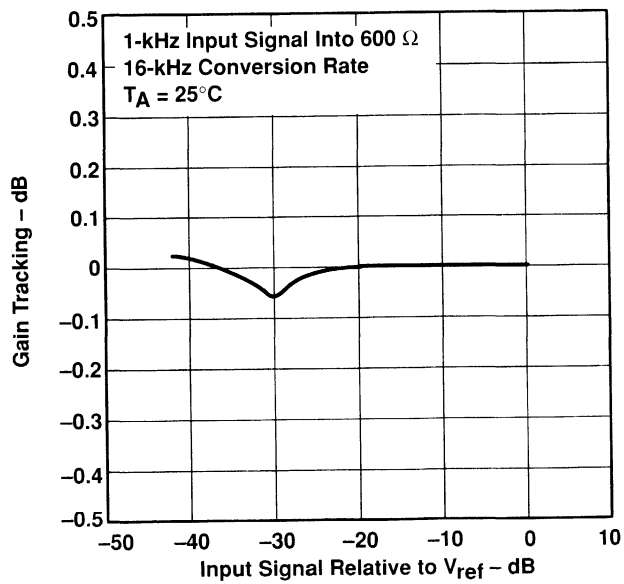


Figure 5-16

**A/D SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL**

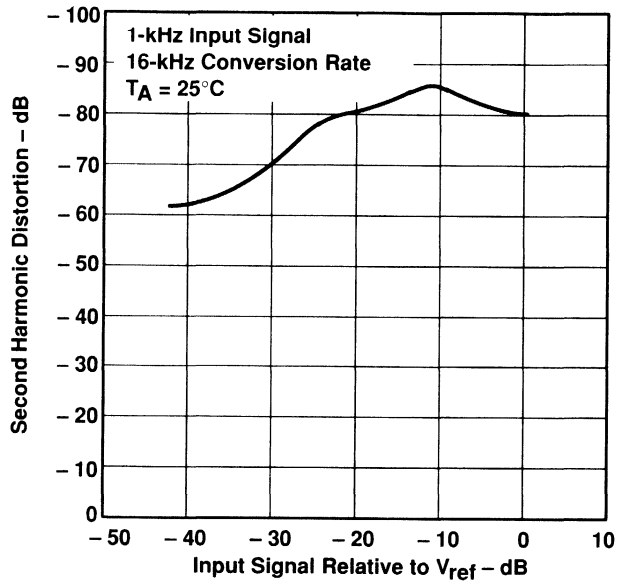


Figure 5-17

**D/A SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL**

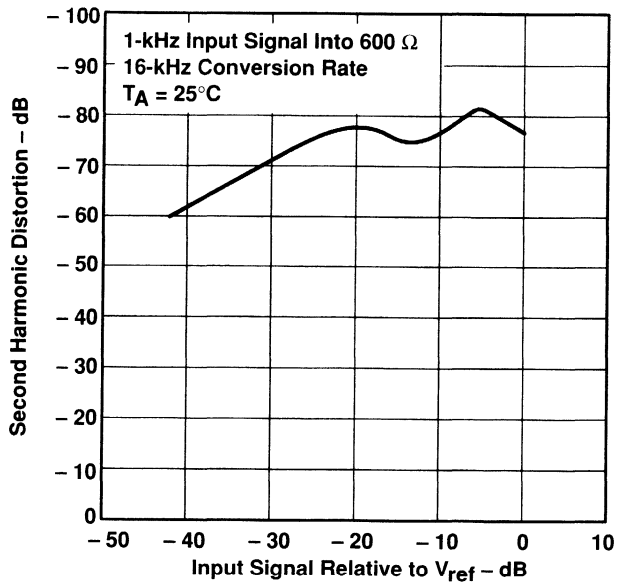


Figure 5-18

**A/D THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL**

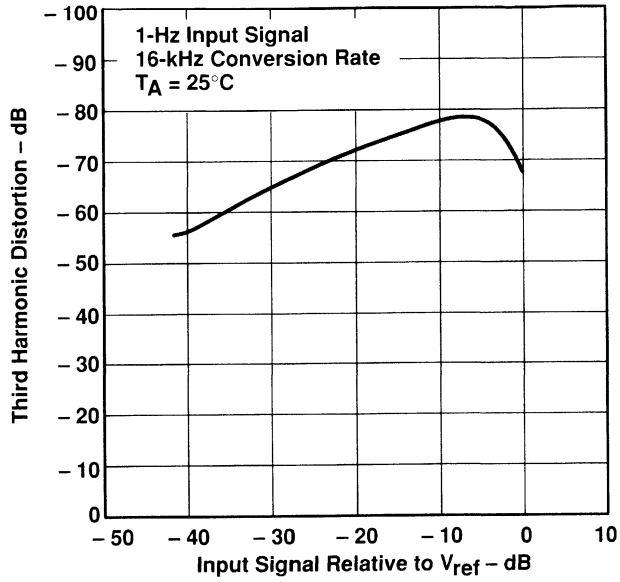


Figure 5-19

**D/A THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL**

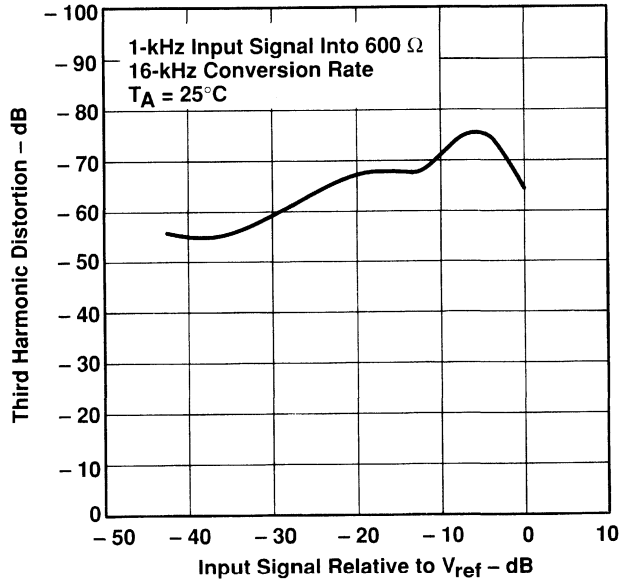


Figure 5-20

6 Application Information

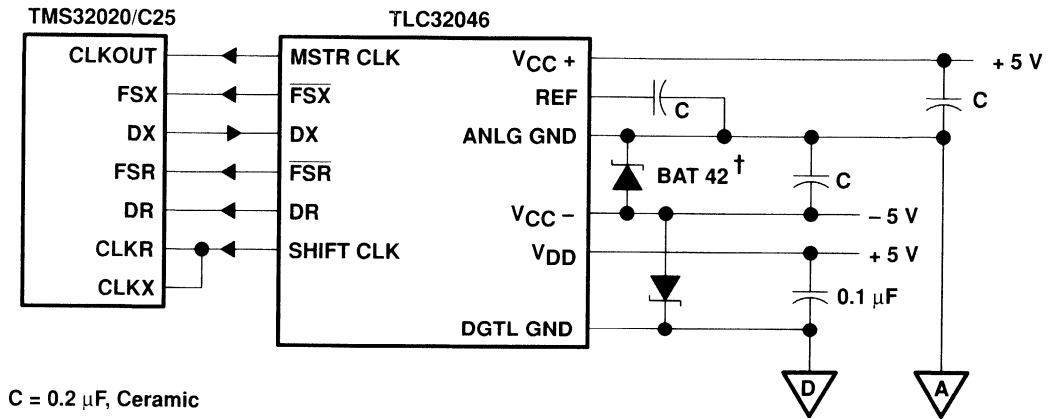


Figure 6-1. AIC Interface to the TMS32020/C25 Showing Decoupling Capacitors and Schottky Diode†

† Thomson Semiconductors

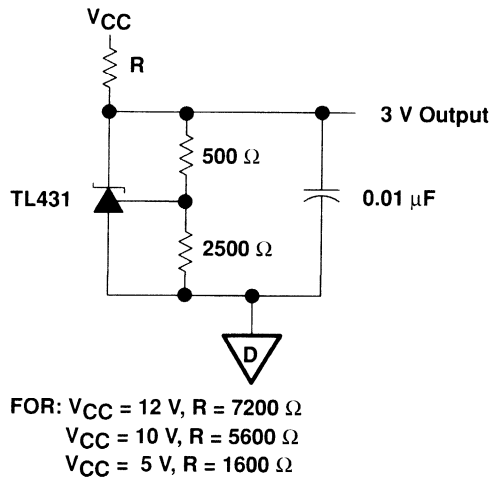


Figure 6-2. External Reference Circuit for TLC32046

TLC32047C, TLC32047I ***Data Manual***

Wide-Band Analog Interface Circuit

SLAS049A
April 1995



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Contents

<i>Section</i>	<i>Title</i>	<i>Page</i>
1	Introduction	4-135
1.1	Features	4-136
1.2	Functional Block Diagrams	4-137
1.3	Terminal Assignments	4-140
1.4	Ordering Information	4-140
1.5	Terminal Functions	4-141
2	Detailed Description	4-145
2.1	Internal Timing Configuration	4-146
2.2	Analog Input	4-148
2.3	A/D Band-Pass Filter, Clocking, and Conversion Timing	4-148
2.4	A/D Converter	4-148
2.5	Analog Output	4-148
2.6	D/A Low-Pass Filter, Clocking, and Conversion Timing	4-148
2.7	D/A Converter	4-149
2.8	Serial Port	4-149
2.9	Synchronous Operation	4-149
2.9.1	One 16-Bit Word	4-149
2.9.2	Two 8-Bit Bytes	4-149
2.9.3	Synchronous Operating Frequencies	4-150
2.10	Asynchronous Operation	4-150
2.10.1	One 16-Bit Word	4-150
2.10.2	Two 8-Bit Bytes	4-150
2.10.3	Asynchronous Operating Frequencies	4-151
2.11	Operation of TLC32047 With Internal Voltage Reference	4-151
2.12	Operation of TLC32047 With External Voltage Reference	4-151
2.13	Reset	4-151
2.14	Loopback	4-151
2.15	Communications Word Sequence	4-152
2.15.1	DR Word Bit Pattern	4-152
2.15.2	Primary DX Word Bit Pattern	4-153
2.15.3	Secondary DX Word Bit Pattern	4-154
2.16	Reset Function	4-154
2.17	Power-Up Sequence	4-155
2.18	AIC Register Constraints	4-155
2.19	AIC Responses to Improper Conditions	4-155
2.20	Operation With Conversion Times Too Close Together	4-156
2.21	More Than One Receive Frame Sync Occurring Between Two Transmit Frame Syncs – Asynchronous Operation	4-156

2.22	More than One Transmit Frame Sync Occurring Between Two Receive Frame Syncs – Asynchronous Operation	4-157
2.23	More than One Set of Primary and Secondary DX Serial Communications Occurring Between Two Receive Frame Syncs – Asynchronous Operation	4-157
2.24	System Frequency Response Correction	4-158
2.25	(sin x)/x Correction	4-158
2.26	(sin x)/x Roll-Off for a Zero-Order Hold Function	4-158
2.27	Correction Filter	4-159
2.28	Correction Results	4-159
2.29	TMS320 Software Requirements	4-160
Specifications		4-161
3.1	Absolute Maximum Ratings Over Operating Free-Air Temperature Range	4-161
3.2	Recommended Operating Conditions	4-161
3.3	Electrical Characteristics	4-162
3.3.1	total device	4-162
3.3.2	power supply rejection and crosstalk attenuation	4-162
3.3.3	serial port	4-162
3.3.4	receive amplifier input	4-162
3.3.5	transmit filter output	4-163
3.3.6	receive and transmit system distortion specifications	4-163
3.3.7	receive channel signal-to-distortion ratio	4-163
3.3.8	transmit channel signal-to-distortion ratio	4-164
3.3.9	receive and transmit gain and dynamic range	4-164
3.3.10	receive channel band-pass filter transfer function	4-164
3.3.11	receive and transmit channel low-pass filter transfer function	4-165
3.4	Operating Characteristics (Noise)	4-165
3.4.1	Timing Requirements	4-166
3.4.1	Receive and Transmit Noise (Measurement Includes Low-Pass and Band-Pass Switched-Capacitor Filters)	4-166
3.5	Timing Requirements	4-167
3.5.1	Serial Port Recommended Input Signals	4-167
3.5.2	Serial Port – AIC Output Signals For All Other Outputs	4-167
4	Parameter Measurement Information – Timing Diagrams	4-169
4.1	TMS32047 – Processor Interface	4-169
5	Typical Characteristics	4-175
6	Applications Information	4-185

List of Illustrations

<i>Figure</i>	<i>Title</i>	<i>Page</i>
1-1	Dual-Word (Telephone Interface) Mode	4-138
1-2	Word Mode	4-139
1-3	Byte Mode	4-139
2-1	Asynchronous Internal Timing Configuration	4-147
2-2	Primary and Secondary Communications Word Sequence	4-152
2-3	Reset on Power-Up Circuit	4-155
2-4	Conversion Times Too Close Together	4-156
2-5	More Than One Receive Frame Sync Between Two Transmit Frame Syncs	4-157
2-6	More Than One Transmit Frame Sync Between Two Receive Frame Syncs	4-157
2-7	More Than One Set of Primary and Secondary DX Serial Communications Between Two Receive Frame Syncs	4-158
2-8	First-Order Correction Filter	4-159
4-1	IN+ and IN- Gain Control Circuitry	4-159
4-2	Dual-Word (Telephone Interface) Mode Timing	4-170
4-3	Word Timing	4-170
4-4	Byte-Mode Timing	4-171
4-5	Shift-Clock Timing	4-172
4-6	TMS32010/TMS320C15-TLC32047 Interface Circuit	4-172
4-7	TMS32010/TMS320C15-TLC32047 Interface Timing	4-173
5-1	D/A and A/D Low-Pass Filter Response Simulation	4-175
5-2	D/A and A/D Low-Pass Filter Response	4-175
5-3	D/A and A/D Low-Pass Group Delay	4-176
5-4	A/D Band-Pass Response	4-176
5-5	A/D Band-Pass Filter Response Simulation	4-177
5-6	A/D Band-Pass Filter Group Delay	4-177
5-7	A/D Channel High-Pass Filter	4-178
5-8	D/A (sin x)/x Correction Filter Response	4-178
5-9	D/A (sin x)/x Correction Filter Response	4-179
5-10	D/A (sin x)/x Correction Error	4-179
5-11	A/D Band-Pass Group Delay	4-180
5-12	D/A Low-Pass Group Delay	4-180
5-13	A/D Signal-to-Distortion Ratio vs Input Signal	4-181
5-14	A/D Gain Tracking	4-181
5-15	D/A Converter Signal-to-Distortion Ratio vs Input Signal	4-182
5-16	D/A Gain Tracking	4-182
5-17	A/D Second Harmonic Distortion vs Input Signal	4-183
5-18	D/A Second Harmonic Distortion vs Input Signal	4-183
5-19	A/D Third Harmonic Distortion vs Input Signal	4-184
5-20	D/A Third Harmonic Distortion vs Input Signal	4-184
6-1	AIC Interface to the TMS32020/C25 Showing Decoupling Capacitors and Schottky Diode	4-185
6-2	External Reference Circuit for TLC32047	4-185

List of Tables

<i>Table</i>	<i>Title</i>	<i>Page</i>
2-1	Mode-Selection Function Table	4-145
2-2	Primary DX Serial Communication Protocol	4-153
2-3	Secondary DX Serial Communication Protocol	4-154
2-4	AIC Responses to Improper Conditions	4-156
2-5	(sin x)/x Roll-Off Error	4-159
2-6	(sin x)/x Correction Table for $f_s = 8000$ Hz and $f_s = 9600$ Hz	4-160
4-1	Gain Control Table	4-169

1 Introduction

The TLC32047 wide-band analog interface circuit (AIC) is a complete analog-to-digital and digital-to-analog interface system for advanced digital signal processors (DSPs) similar to the TMS32020, TMS320C25, and TMS320C30. The TLC32047 offers a powerful combination of options under DSP control: three operating modes [dual-word (telephone interface), word, and byte] combined with two word formats (8 bits and 16 bits) and synchronous or asynchronous operation. It provides a high level of flexibility in that conversion and sampling rates, filter bandwidths, input circuitry, receive and transmit gains, and multiplexed analog inputs are under processor control.

This AIC features a

- band-pass switched-capacitor antialiasing input filter
- 14-bit-resolution A/D converter
- 14-bit-resolution D/A converter
- low-pass switched-capacitor output-reconstruction filter

The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable auxiliary differential analog input is provided for applications where more than one analog input is required.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order $(\sin x)/x$ correction filter and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the sample data signal. The on-board $(\sin x)/x$ correction filter can be switched out of the signal path using digital signal processor control.

The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the IC. The internal voltage reference is brought out to REF. Separate analog and digital voltage supplies and ground are provided to minimize noise and ensure a wide dynamic range. The analog circuit path contains only differential circuitry to keep noise to a minimum. The exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The TLC32047C is characterized for operation from 0°C to 70°C, and the TLC32047I is characterized for operation from -40°C to 85°C.

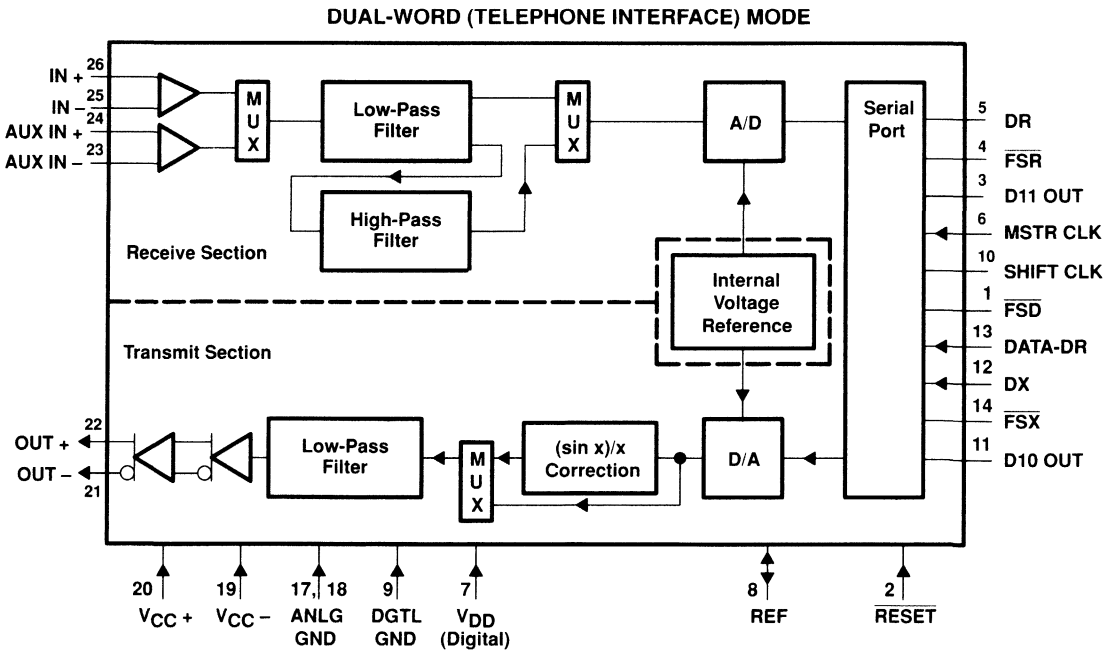
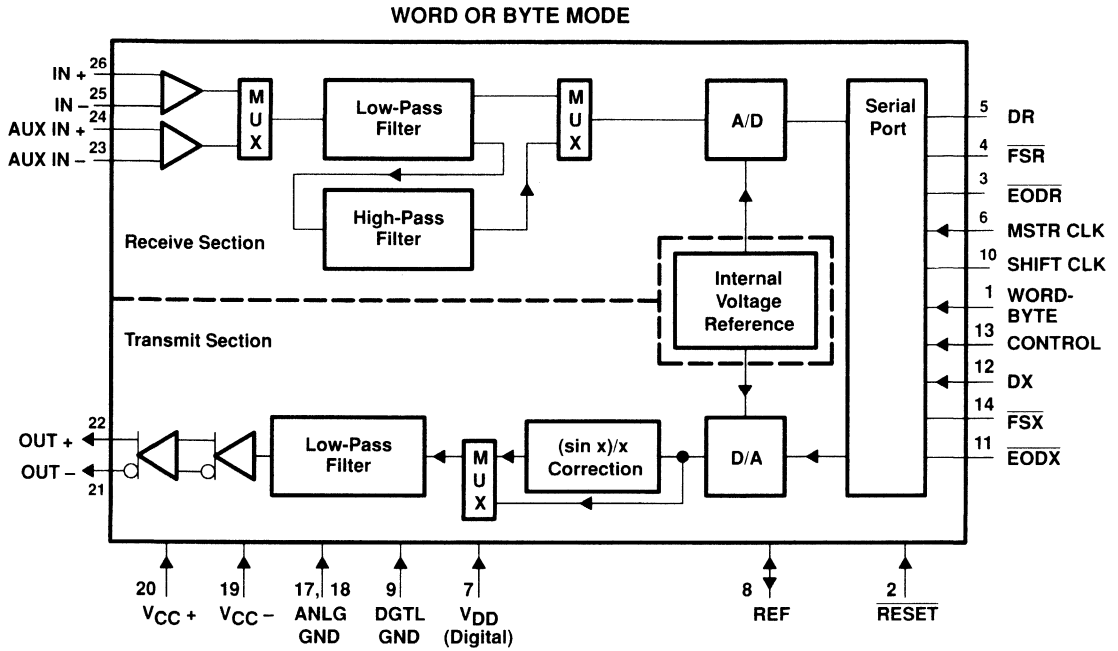
1.1 Features

- 14-Bit Dynamic Range ADC and DAC
- 16-Bit Dynamic Range Input With Programmable Gain
- Synchronous or Asynchronous ADC and DAC Sampling Rates Up to 25,000 Samples Per Second
- Programmable Incremental ADC and DAC Conversion Timing Adjustments
- Typical Applications
 - Speech Encryption for Digital Transmission
 - Speech Recognition and Storage Systems
 - Speech Synthesis
 - Modems at 8-kHz, 9.6-kHz, and 16-kHz Sampling Rates
 - Industrial Process Control
 - Biomedical Instrumentation
 - Acoustical Signal Processing
 - Spectral Analysis
 - Instrumentation Recorders
 - Data Acquisition
- Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter
- Three Fundamental Modes of Operation: Dual-Word (Telephone Interface), Word, and Byte
- 600-mil Wide N Package
- Digital Output in Twos Complement Format
- CMOS Technology

FUNCTION TABLE

DATA FORMAT	SYNCHRONOUS (CONTROL REGISTER BIT D5 = 1)	ASYNCHRONOUS (CONTROL REGISTER BIT D5 = 0)	FORCING CONDITION	DIRECT INTERFACE
16-bit format	Dual-word (telephone interface) mode	Dual-word (telephone interface) mode	DATA-DR/CONTROL = 0 to 5 V FSD/WORD-BYTE = 0 to 5 V	TMS32020, TMS320C25, TMS320C30
16-bit format	Word mode	Word mode	DATA-DR/CONTROL = V_{CC-} (-5 V nom) FSD/WORD-BYTE = V_{CC+} (5 V nom)	TMS32020, TMS320C25, TMS320C30, indirect interface to TMS320C10 (see Figure 7)
8-bit format (2 bytes required)	Byte mode	Byte mode	DATA-DR/CONTROL = V_{CC-} (-5 V nom) FSD/WORD-BYTE = V_{CC-} (-5 V nom)	TMS320C17

1.2 Functional Block Diagrams



FRAME SYNCHRONIZATION FUNCTIONS

TLC32047 Function	Frame Sync Output
Receiving serial data on DX from processor to internal DAC	FSX low
Transmitting serial data on DR from internal ADC to processor, primary communications	FSR low
Transmitting serial data on DR from DATA-DR to processor, secondary communications in dual-word (telephone interface) mode only	FSD low

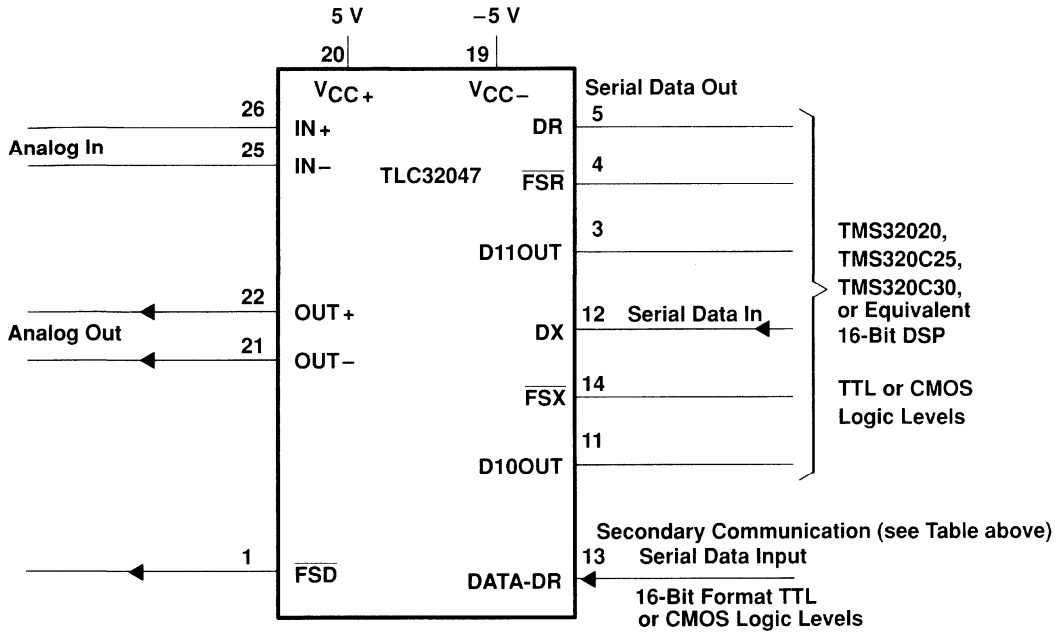


Figure 1–1. Dual-Word (Telephone Interface) Mode

When the DATA-DR/CONTROL input is tied to a logic signal source varying between 0 and 5 V, the TLC32047 is in the dual-word (telephone interface) mode. This logic signal is routed to the DR line for input to the DSP only when terminal 1, data frame synchronization (FSD), outputs a low level. The FSD pulse duration is 16 shift clock pulses. Also, in this mode, the control register data bits D10 and D11 appear on D10OUT and D11OUT, respectively, as outputs.

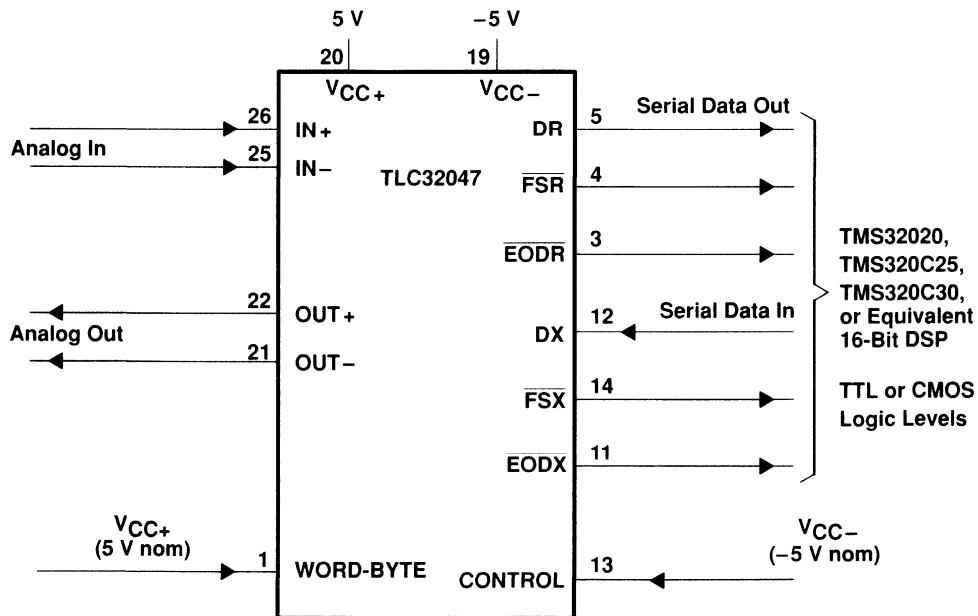


Figure 1-2. Word Mode

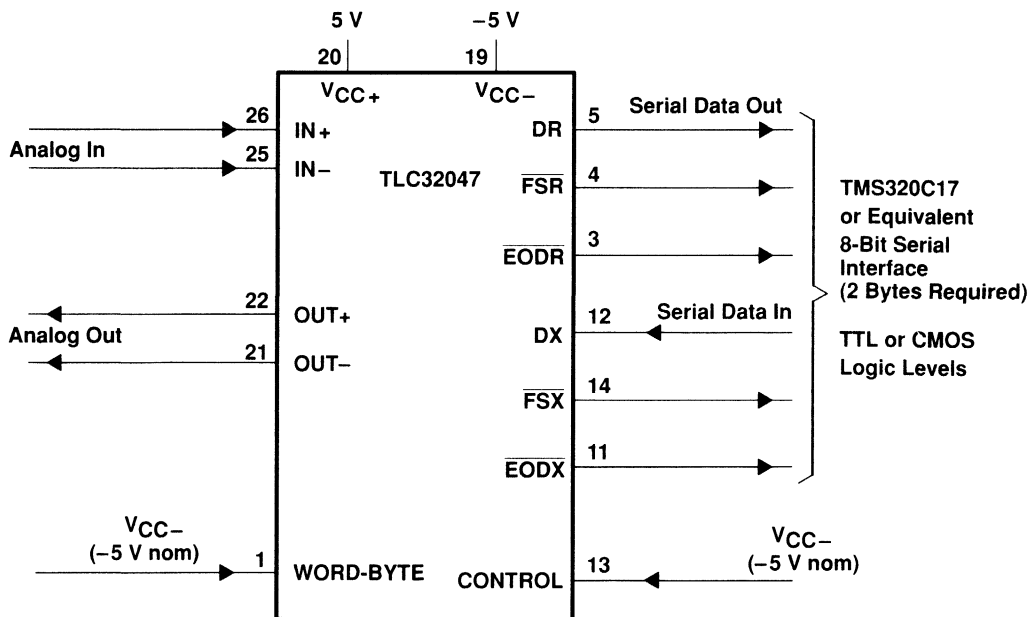
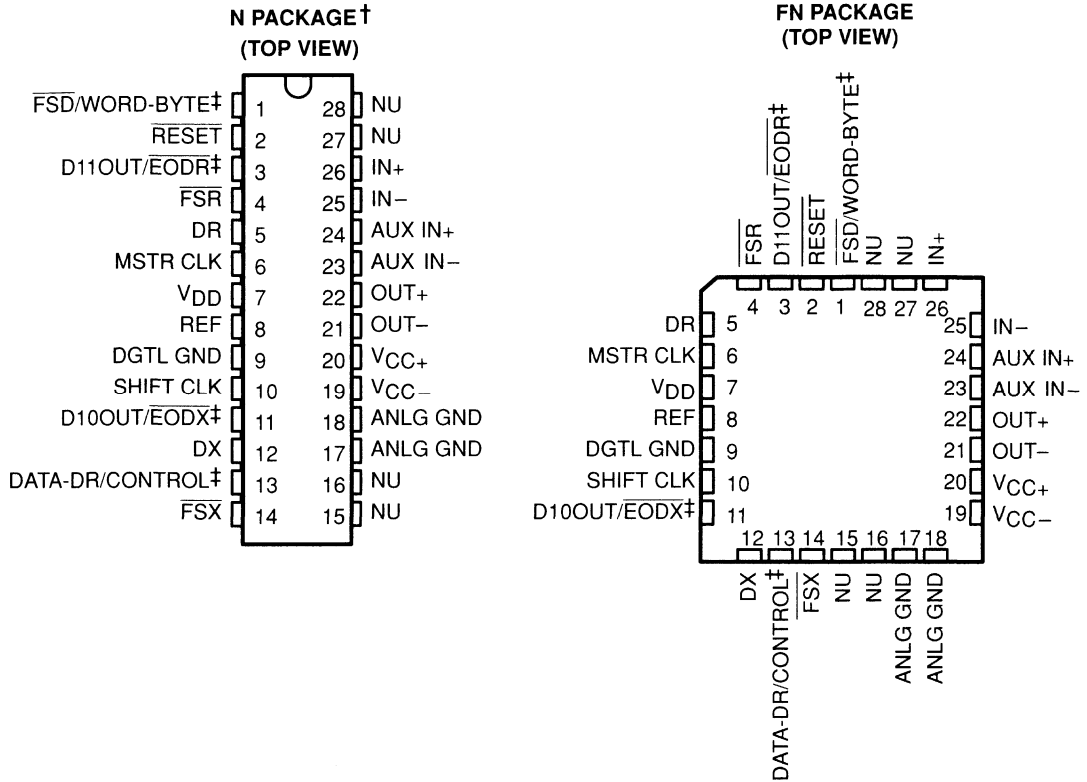


Figure 1-3. Byte Mode

The word or byte mode is selected by first connecting the DATA-DR/CONTROL input to V_{CC-} . FSD/WORD-BYTE becomes an input and can then be used to select either word or byte transmission formats. The end-of-data transmit (EODX) and the end-of-data receive (EODR) signals on terminals 11 and 3, respectively, are used to signal the end of word or byte communication (see the Terminal Functions section).

1.3 Terminal Assignments



NU - Nonusable; no external connection should be made to these pins.

† 600-mil wide

‡ The portion of the terminal name to the left of the slash is used for the dual-word (telephone interface) mode. The portion of the terminal name to the right of the slash is used for word-byte mode.

1.4 Ordering Information

AVAILABLE OPTIONS

T _A	PACKAGED DEVICES	
	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC32047CFN	TLC32047CN
-40°C to 85°C	TLC32047IFN	TLC32047IN

1.5 Terminal Functions

TERMINAL NAME NO.		I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. ANLG GND is internally connected to DGTL GND.
AUX IN+	24	I	Noninverting auxiliary analog input stage. AUX IN+ can be switched into the band-pass filter and ADC path via software control. If the appropriate bit in the control register is a 1, the auxiliary inputs replace the IN+ and IN– inputs. If the bit is a 0, the IN+ and IN– inputs are used (see the DX Serial Data Word Format).
AUX IN–	23	I	Inverting auxiliary analog input (see the above AUX IN+ description).
DATA-DR	13	I	The dual-word (telephone interface) mode, selected by applying an input logic level between 0 and 5 V to DATA-DR, allows DATA-DR to function as a data input. The data is then framed by the FSD signal and transmitted as an output to DR during secondary communication. The functions FSD, D11OUT, and D10OUT are valid with this mode selection (see Table 2–1).
CONTROL			When CONTROL is tied to V_{CC-} , the device is in the word or byte mode. The functions WORD-BYTE, EODR, and EODX are valid in this mode. FSD/WORD-BYTE is then used to select either the word or byte mode (see Function Table).
DR	5	O	DR is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with the SHIFT CLK signal.
DX	12	I	DX is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port is synchronized with the SHIFT CLK signal.
D10OUT	11	O	In the dual-word (telephone interface) mode, bit D10 of the control register is output to D10OUT. When the device is reset, bit D10 is initialized to 0 (see DX Serial Data Word Format). The output update is immediate upon changing bit D10.
EODX			End of data transmit. During the word-mode timing, a low-going pulse occurs on EODX immediately after the 16 bits of DAC and control or register information have been transmitted from the TMS320 serial port to the AIC. EODX can be used to interrupt a microprocessor upon completion of serial communications. Also, EODX can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM and to facilitate parallel data bus communications between the DSP and the serial-to-parallel shift registers. During the byte-mode timing, EODX goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate first and second bytes.

1.5 Terminal Functions (continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
D11OUT	3	O	In the dual-word (telephone interface) mode, bit D11 of the control register is output to D11OUT. When the device is reset, bit D11 is initialized to 0 (see DX Serial Data Word Format). The output update is immediate upon changing bit D11.
EODR			End of data receive. During the word-mode timing, a low-going pulse occurs on EODR immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. EODR can be used to interrupt a microprocessor upon completion of serial communications. Also, EODR can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the DSP and the serial-to-parallel shift registers. During the byte-mode timing, EODR goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate between first and second bytes.
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
FSD	1	O	Frame sync data. The $\overline{\text{FSD}}$ output remains high during primary communication. In the dual-word (telephone interface) mode, the $\overline{\text{FSD}}$ output is identical to the $\overline{\text{FSX}}$ output during secondary communication.
WORD-BYTE		I	WORD-BYTE allows differentiation between the word and byte data format (see DATA-DR/CONTROL and Table 2-1 for details).
FSR	4	O	Frame sync receive. $\overline{\text{FSR}}$ is held low during bit transmission. When $\overline{\text{FSR}}$ goes low, the TMS320 serial port begins receiving bits from the AIC via DR of the AIC. The most significant DR bit is present on DR before $\overline{\text{FSR}}$ goes low (see Serial Port Sections and Internal Timing Configuration Diagrams).
FSX	14	O	Frame sync transmit. When $\overline{\text{FSX}}$ goes low, the TMS320 serial port begins transmitting bits to the AIC via DX of the AIC. $\overline{\text{FSX}}$ is held low during bit transmission (see Serial Port Sections and Internal Timing Configuration Diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN-	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	Master clock. MSTR CLK is used to derive all the key logic signals of the AIC, such as the shift clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The internal timing configuration diagram shows how these key signals are derived. The frequencies of these signals are synchronous submultiples of the master clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the ADC and DAC converters (see the Internal Timing Configuration).
OUT+	22	O	Noninverting output of analog output power amplifier. OUT+ drives transformer hybrids or high-impedance loads directly in a differential or a single-ended configuration.
OUT-	21	O	Inverting output of analog output power amplifier. OUT- is functionally identical with and complementary to OUT+.
REF	8	I/O	Internal voltage reference is brought out on REF. An external voltage reference can be applied to REF to override the internal voltage reference.

1.5 Terminal Functions (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
RESET	2	I	<p>Reset. A reset function is provided to initialize TA, TA', TB, RA, RA', RB (see Figure 2-1), and the control registers. This reset function initiates serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on RESET, the AIC registers are initialized to provide a 16-kHz data conversion rate for a 10.368-MHz master clock input signal. The conversion rate adjust registers, TA' and RA', are reset to 1. The CONTROL register bits are reset as follows (see AIC DX Data Word Format section):</p> <p style="padding-left: 2em;">D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1</p> <p>The shift clock (SCLK) is held high during RESET.</p> <p>This initialization allows normal serial-port communication to occur between the AIC and the DSP.</p>
SHIFT CLK	10	O	<p>Shift clock. SHIFT CLK is obtained by dividing the master clock signal frequency by four. SHIFT CLK is used to clock the serial data transfers of the AIC.</p>
V _{DD}	7		Digital supply voltage, 5 V ±5%
V _{CC+}	20		Positive analog supply voltage, 5 V ±5%
V _{CC-}	19		Negative analog supply voltage, -5 V ±5%

2 Detailed Description

Table 2–1. Mode-Selection Function Table

DATA-DR/ CONTROL	$\overline{\text{FSD}}$ / WORD-BYTE	CONTROL REGISTER BIT (D5)	OPERATING MODE	SERIAL CONFIGURATION	DESCRIPTION
Data in (0 to 5 V)	$\overline{\text{FSD}}$ out (0 to 5 V)	1	Dual-Word (Telephone Interface)	Synchronous, One 16-Bit Word	Terminal functions DATA-DR [†] , $\overline{\text{FSD}}$ [†] , D11OUT, and D10OUT are applicable in this configuration. $\overline{\text{FSD}}$ is asserted during secondary communication, but the FSR is not asserted. However, $\overline{\text{FSD}}$ remains high during primary communication.
Data in (0 to 5 V)	$\overline{\text{FSD}}$ out (0 to 5 V)	0	Dual-Word (Telephone Interface)	Asynchronous, One 16-bit Word	Terminal functions DATA-DR [†] , $\overline{\text{FSD}}$ [†] , D11OUT, and D10OUT are applicable in this configuration. $\overline{\text{FSD}}$ is asserted during secondary communication, but the $\overline{\text{FSR}}$ is not asserted. However, $\overline{\text{FSD}}$ remains high during primary communication. If secondary communications occur while the A/D conversion is being transmitted from DR, $\overline{\text{FSD}}$ cannot go low, and data from DATA-DR cannot go onto DR.
$V_{\text{CC-}}$	$V_{\text{CC+}}$	1	WORD	Synchronous, One 16-Bit Word	Terminal functions CONTROL [†] , WORD-BYTE [†] , $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are applicable in this configuration.
		0		Asynchronous, One 16-bit Word	Terminal functions CONTROL [†] , WORD-BYTE [†] , $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are applicable in this configuration.
	$V_{\text{CC-}}$	1	BYTE	Synchronous, Two 8-Bit Bytes	Terminal functions CONTROL [†] , WORD-BYTE [†] , $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are applicable in this configuration.
		0		Asynchronous, Two 8-Bit Bytes	Terminal functions CONTROL [†] , WORD-BYTE [†] , $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are applicable in this configuration.

[†] DATA-DR/CONTROL has an internal pulldown resistor to -5 V, and $\overline{\text{FSD}}$ /WORD-BYTE has an internal pullup resistor to 5 V.

2.1 Internal Timing Configuration (see Figure 2–1)

All the internal timing of the AIC is derived from the high-frequency clock signal that drives the master clock input. The shift clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the master clock input signal frequency by four.

The TX(A) counter and the TX(B) counter, which are driven by the master clock signal, determine the D/A conversion timing. Similarly, the RX(A) counter and the RX(B) counter determine the A/D conversion timing. In order for the low-pass switched-capacitor filter in the D/A path (see Functional Block Diagram) to meet its transfer function specifications, the frequency of its clock input must be 432 kHz. If the clock frequency is not 432 kHz, the filter transfer function frequencies are frequency-scaled by the ratios of the clock frequency to 432 kHz:

$$\text{Absolute Frequency (kHz)} = \frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{432} \quad (1)$$

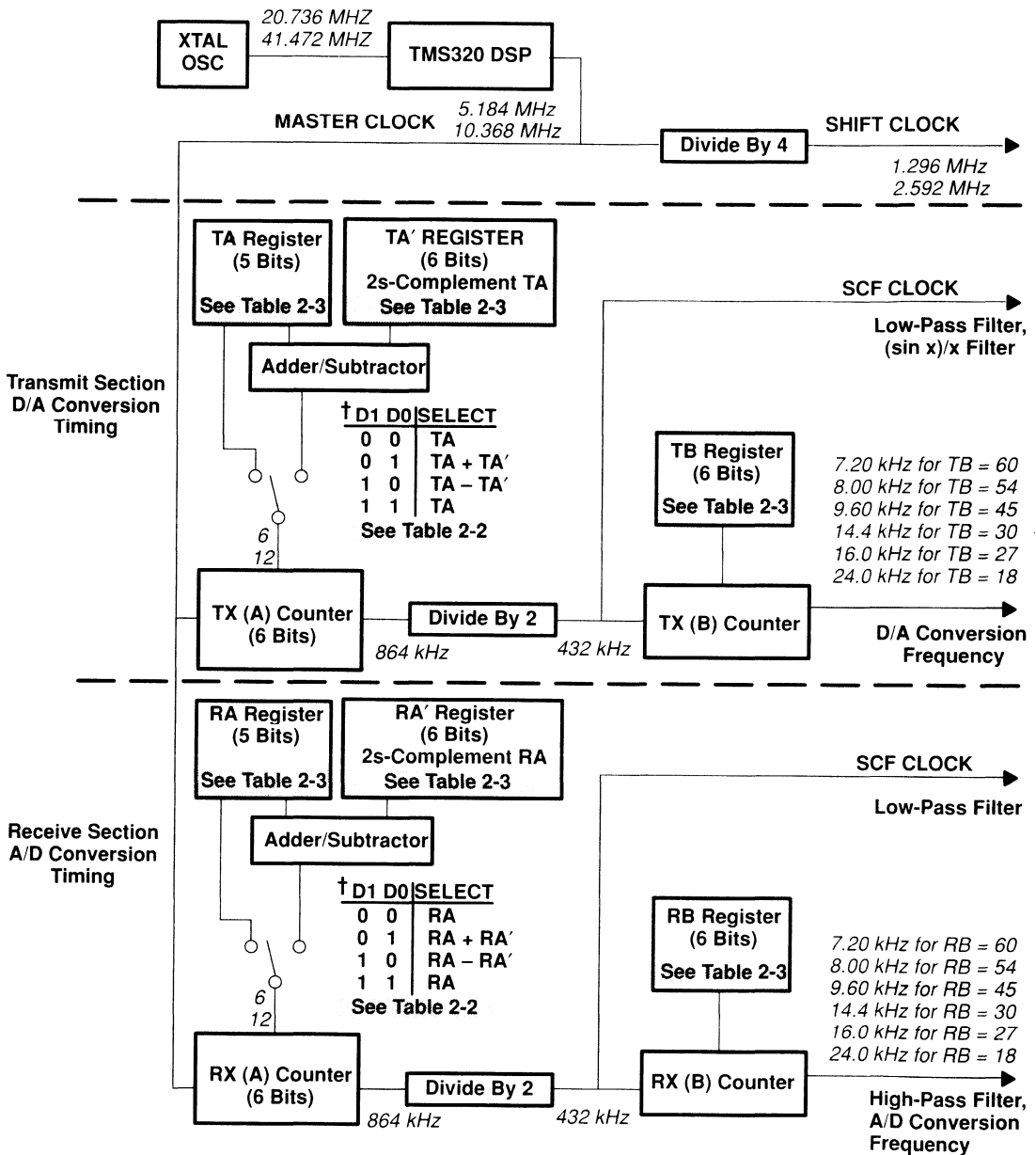
To obtain the specified filter response, the combination of master clock frequency and the TX(A) counter and the RX(A) counter values must yield a 432-kHz switched-capacitor clock signal. This 432-kHz clock signal can then be divided by the TX(B) counter to establish the D/A conversion timing.

The transfer function of the band-pass switched-capacitor filter in the A/D path (see Functional Block Diagram) is a composite of its high-pass and low-pass transfer functions. When the shift clock frequency (SCF) is 432 kHz, the high-frequency roll-off of the low-pass section meets the band-pass filter transfer function specification. Otherwise, the high-frequency roll-off is frequency-scaled by the ratio of the high-pass section's SCF clock to 432 kHz (see Figure 5–5). The low-frequency roll-off of the high-pass section meets the band-pass filter transfer function specification when the A/D conversion rate is 24 kHz. If not, the low-frequency roll-off of the high-pass section is frequency-scaled by the ratio of the A/D conversion rate to 24 kHz.

The TX(A) counter and the TX(B) counter are reloaded each D/A conversion period, while the RX(A) counter and the RX(B) counter are reloaded every A/D conversion period. The TX(B) counter and the RX(B) counter are loaded with the values in the TB and RB registers, respectively. Via software control, the TX(A) counter can be loaded with the TA register, the TA register less the TA' register, or the TA register plus the TA' register. By selecting the TA register less the TA' register option, the upcoming conversion timing occurs earlier by an amount of time that equals TA' times the signal period of the master clock. If the TA register plus the TA' register option is executed, the upcoming conversion timing occurs later by an amount of time that equals TA' times the signal period of the master clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. However, the RX(A) counter can be programmed via software control with the RA register, the RA register less the RA' register, or the RA register plus the RA' register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing and can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous, then the low-pass and band-pass switched-capacitor filter clocks are derived from the TX(A) counter. Also, both the D/A and A/D conversion timings are derived from the TX(A) counter and the TX(B) counter. When the transmit and receive sections are configured to be asynchronous, the RX(A) counter, RX(B) counter, RA register, RA' register, and RB registers are not used.



† These control bits are described in the DX Serial Data Word Format section.

NOTES: D. Tables 2-2 and 2-3 (pages 2-9 and 2-10) are primary and secondary communication protocols, respectively.

E. In synchronous operation, RA, RA', RB, RX(A), and RX(B) are not used. TA, TA', TB, TX(A), and TX(B) are used instead.

F. Items in italics refer only to frequencies and register contents, which are variable. A crystal oscillator driving 20.736 MHz into the TMS320-series DSP provides a master clock frequency of 5.184 MHz. The TLC32047 produces a shift clock frequency of 1.296 MHz. If the TX(A) register contents equal 6, the SCF clock frequency is then 432 kHz, and the D/A conversion frequency is $432 \text{ kHz} \div T(B)$.

Figure 2-1. Asynchronous Internal Timing Configuration

2.2 Analog Input

Two pairs of analog inputs are provided. Normally, the IN+ and IN– input pair is used; however, the auxiliary input pair, AUX IN+ and AUX IN–, can be used if a second input is required. Since sufficient common-mode range and rejection are provided, each input set can be operated in differential or single-ended modes. The gain for the IN+, IN–, AUX IN+, and AUX IN– inputs can be programmed to 1, 2, or 4 (see Table 4–1). Either input circuit can be selected via software control. Multiplexing is controlled with the D4 bit (enable/disable AUX IN+ and AUX IN–) of the secondary DX word (see Table 2–3). The multiplexing requires a 2-ms wait at SCF = 432 kHz (see Figure 5–3) for a valid output signal. A wide dynamic range is ensured by the differential internal analog architecture and the separate analog and digital voltage supplies and grounds.

2.3 A/D Band-Pass Filter, A/D Band-Pass Filter Clocking, and A/D Conversion Timing

The receive-channel A/D high-pass filter can be selected or bypassed via software control (see Functional Block Diagram). The frequency response of this filter is on page 3-5. This response results when the switched-capacitor filter clock frequency is 432 kHz and the A/D sample rate is 24 kHz. Several possible options can be used to attain a 432-kHz switched-capacitor filter clock. When the filter clock frequency is not 432 kHz, the low-pass filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 432 kHz (see Typical Characteristics section). The ripple bandwidth and 3-dB low-frequency roll-off points of the high-pass section are 450 Hz and 300 Hz, respectively. However, the high-pass section low-frequency roll-off is frequency-scaled by the ratio of the A/D sample rate to 24 kHz.

Figure 2–1 and the DX Serial Data Word Format sections of this data manual indicate the many options for attaining a 432-kHz band-pass switched-capacitor filter clock. These sections indicate that the RX(A) counter can be programmed to give a 432-kHz band-pass switched-capacitor filter clock for several master clock input frequencies.

The A/D conversion rate is attained by frequency-dividing the band-pass switched-capacitor filter clock with the RX(B) counter. Unwanted aliasing is prevented because the A/D conversion rate is an integer submultiple of the band-pass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

2.4 A/D Converter

Fundamental performance specifications for the receive channel ADC circuitry are on pages 3-2 and 3-3 of this data manual. The ADC circuitry, using switched-capacitor techniques, provides an inherent sample-and-hold function.

2.5 Analog Output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

2.6 D/A Low-Pass Filter, D/A Low-Pass Filter Clocking, and D/A Conversion Timing

The frequency response of these filters is on page 3-5. This response results when the low-pass switched-capacitor filter clock frequency is 432 kHz (see Equation 1). Like the A/D filter, the transfer function of this filter is frequency-scaled when the clock frequency is not 432 kHz (see Typical Characteristics section). A continuous-time filter is provided on the output of the low-pass filter to eliminate the periodic sample data signal information, which occurs at multiples of the 432-kHz switched-capacitor clock feedthrough.

The D/A conversion rate is attained by frequency-dividing the 432-kHz switched-capacitor filter clock with the T(B) counter. Unwanted aliasing is prevented because the D/A conversion rate is an integer submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

2.7 D/A Converter

Fundamental performance specifications for the transmit channel DAC circuitry are on pages 3-3 and 3-4. The DAC has a sample-and-hold function that is realized with a switched-capacitor ladder.

2.8 Serial Port

The serial port has four possible configurations summarized in the function table on page 1-2. These configurations are briefly described below.

- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS320C17. The communications protocol is two 8-bit bytes.
- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, and TMS320C30. The communications protocol is one 16-bit word.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS320C17. The communications protocol is two 8-bit bytes.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, TMS320C30, or two SN74299 serial-to-parallel shift registers, which can interface in parallel to the TMS32010, TMS320C15, to any other digital signal processor, or to external FIFO circuitry. The communications protocol is one 16-bit word.

2.9 Synchronous Operation

When the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and band-pass filters (see Functional Block Diagram). The A/D conversion timing is derived from and equal to the D/A conversion timing. When data bit D5 in the control register is a logic 1, transmit and receive sections are synchronous. The band-pass switched-capacitor filter and the A/D converter timing are derived from the TX(A) counter, the TX(B) counter, and the TA and TA' registers. In synchronous operation, both the A/D and the D/A channels operate from the same frequencies. The \overline{FSX} and the \overline{FSR} timing is identical during primary communication, but \overline{FSR} is not asserted during secondary communication because there is no new A/D conversion result.

2.9.1 One 16-Bit Word [Dual-Word (Telephone Interface) or Word Mode]

The serial port interfaces directly with the serial ports of the TMS32020, TMS320C25, and the TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows:

1. \overline{FSX} and \overline{FSR} are brought low by the TLC32047 AIC.
2. One 16-bit word is transmitted and one 16-bit word is received.
3. \overline{FSX} and \overline{FSR} are brought high.
4. \overline{EODX} and \overline{EODR} emit low-going pulses one shift clock wide. \overline{EODX} and \overline{EODR} are valid in the word or byte mode only.

If the device is in the dual-word (telephone interface) mode, \overline{FSD} goes low during the secondary communication period and enables the data word received at the DATA-DR/CONTROL input to be routed to the DR line. The secondary communication period occurs four shift clocks after completion of primary communications.

2.9.2 Two 8-Bit Bytes (Byte Mode)

The serial port interfaces directly with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows:

1. \overline{FSX} and \overline{FSR} are brought low.
2. One 8-bit word is transmitted and one 8-bit word is received.
3. \overline{EODX} and \overline{EODR} are brought low.
4. \overline{FSX} and \overline{FSR} emit positive frame-sync pulses that are four shift clock cycles wide.
5. One 8-bit byte is transmitted and one 8-bit byte is received.
6. \overline{FSX} and \overline{FSR} are brought high.
7. \overline{EODX} and \overline{EODR} are brought high.

2.9.3 Synchronous Operating Frequencies

The synchronous operating frequencies are determined by the following equations.

Switched capacitor filter (SCF) frequencies (see Figure 2–1):

$$\text{Low-pass SCF clock frequency (D/A and A/D channels)} = \frac{\text{master clock frequency}}{T(A) \times 2}$$

$$\text{High-pass SCF clock frequency (A/D channel)} = \text{A/D conversion frequency}$$

$$\begin{aligned} \text{Conversion frequency (A/D and D/A channels)} &= \frac{\text{Low pass SCF clock frequency}}{T(B)} \\ &= \frac{\text{master clock frequency}}{T(A) \times 2 \times T(B)} \end{aligned}$$

NOTE: T(A), T(B), R(A), and R(B) are the contents of the TA, TB, RA, and RB registers, respectively.

2.10 Asynchronous Operation

When the transmit and the receive sections are operated asynchronously, the low-pass and band-pass filter clocks are independently generated from the master clock. The D/A and the A/D conversion timing is also determined independently.

D/A timing is set by the counters and registers described in synchronous operation, but the RA and RB registers are substituted for the TA and TB registers to determine the A/D channel sample rate and the A/D path switched-capacitor filter frequencies. Asynchronous operation is selected by control register bit D5 being zero.

2.10.1 One 16-Bit Word (Word Mode)

The serial port interfaces directly with the serial ports of the TMS32020, TMS320C25, and TMS320C30 and communicates with 16-bit word formats. The operation sequence is as follows:

1. \overline{FSX} or \overline{FSR} are brought low by the TLC32047 AIC.
2. One 16-bit word is transmitted or one 16-bit word is received.
3. \overline{FSX} or \overline{FSR} are brought high.
4. \overline{EODX} or \overline{EODR} emit low-going pulses one shift clock wide. \overline{EODX} and \overline{EODR} are valid in either the word or byte mode only.

2.10.2 Two 8-Bit Bytes (Byte Mode)

The serial port interfaces directly with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operating sequence is as follows:

1. \overline{FSX} or \overline{FSR} are brought low by the TLC32047 AIC.
2. One byte is transmitted or received.

3. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ are brought low.
4. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought high for four shift clock periods and then brought low.
5. The second byte is transmitted or received.
6. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought high.
7. EODX or EODR are brought high.

2.10.3 Asynchronous Operating Frequencies

The asynchronous operating frequencies are determined by the following equations.

Switched-capacitor filter frequencies (see Figure 2–1):

$$\text{Low pass D/A SCF clock frequency} = \frac{\text{master clock frequency}}{T(A) \times 2}$$

$$\text{Low pass A/D SCF clock frequency} = \frac{\text{master clock frequency}}{R(A) \times 2}$$

$$\text{High pass SCF clock frequency (A/D channel)} = \text{A/D conversion frequency} \quad (2)$$

Conversion frequency:

$$\text{D/A conversion frequency} = \frac{\text{Low pass D/A SCF clock frequency}}{T(B)}$$

$$\text{A/D conversion frequency} = \frac{\text{Low pass A/D SCF clock frequency (for low pass receive filter)}}{R(B)} \quad (3)$$

NOTE: T(A), T(B), R(A), and R(B) are the contents of the TA, TB, RA, and RB registers, respectively.

2.11 Operation of TLC32047 With Internal Voltage Reference

The internal reference of the TLC32047 eliminates the need for an external voltage reference and provides overall circuit cost reduction. The internal reference eases the design task and provides complete control of the IC performance. The internal reference is brought out to REF. To keep the amount of noise on the reference signal to a minimum, an external capacitor can be connected between REF and ANLG GND.

2.12 Operation of TLC32047 With External Voltage Reference

REF can be driven from an external reference circuit. This external circuit must be capable of supplying 250 μA and must be protected adequately from noise and crosstalk from the analog input.

2.13 Reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on $\overline{\text{RESET}}$, the AIC is initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX Data Word Format section). After a reset, TA=TB=RA=RB=18 (or 12 hexadecimal), TA'=RA'=01 (hexadecimal), the A/D high-pass filter is inserted, the loop-back function is deleted, AUX IN+ and AUX IN– are disabled, the transmit and receive sections are in synchronous operation, programmable gain is set to 1, the on-board (sin x)/x correction filter is not selected, D10 OUT is set to 0, and D11 OUT is set to 0.

2.14 Loopback

This feature allows the circuit to be tested remotely. In loopback, OUT+ and OUT– are internally connected to IN+ and IN–. The DAC bits (D15 to D2), which are transmitted to DX, can be compared with the ADC bits (D15 to D2) received from DR. The bits on DR equal the bits on DX. However, there is some difference in these bits due to the ADC and DAC output offsets.

The loopback feature is implemented with digital signal processor control by transmitting a logic 1 for data bit D3 in the DX secondary communication to the control register (see Table 2–3).

2.15 Communications Word Sequence

In the dual-word (telephone interface) mode, there are two data words that are presented to the DSP or μP from DR. The first data word is the ADC conversion result occurring during the FSR time, and the second is the serial data applied to DATA-DR during the FSD time. FSR is not asserted during secondary communications and FSD is not asserted during primary communications.

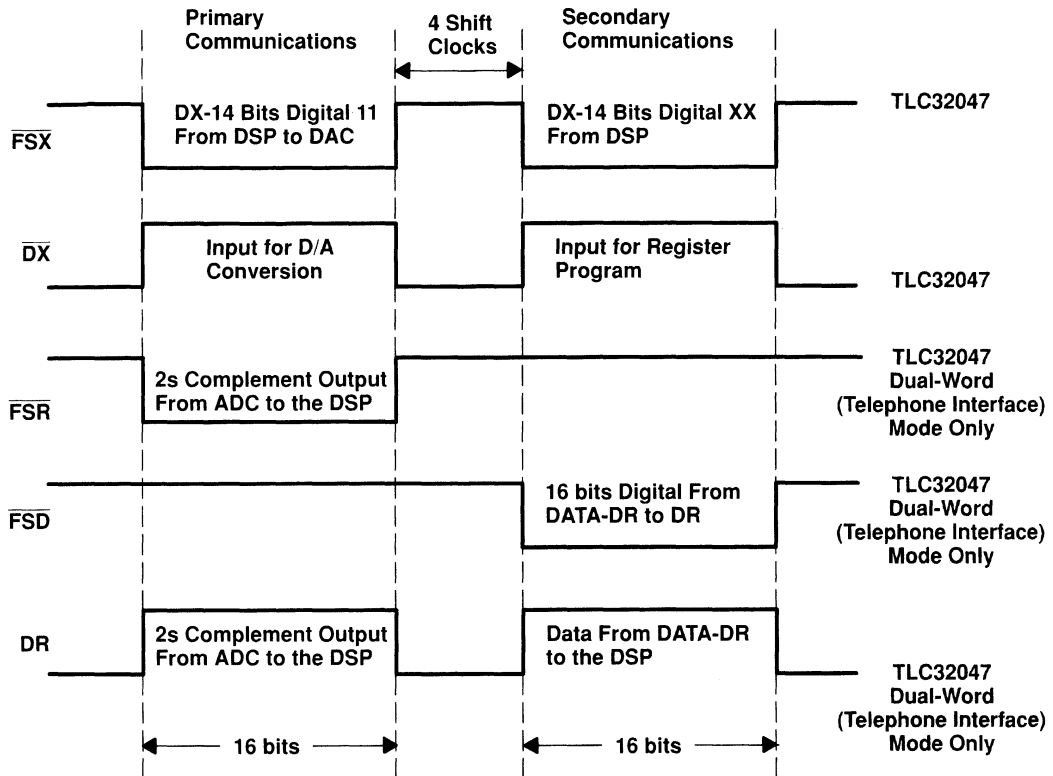
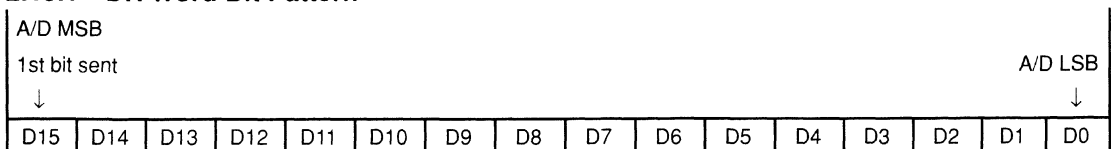


Figure 2–2. Primary and Secondary Communications Word Sequence

2.15.1 DR Word Bit Pattern



The data word is the 14-bit conversion result of the receive channel to the processor in 2s complement format. With 16-bit processors, the data is 16 bits long with the two LSBs at zero. Using 8-bit processors, the data word is transmitted in the same order as one 16-bit word, but as two bytes with the two LSBs of the second byte set to zero.

2.15.2 Primary DX Word Bit Pattern

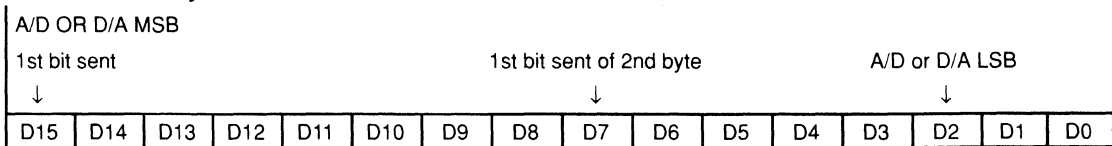


Table 2–2. Primary DX Serial Communication Protocol

FUNCTIONS	D1	D0
D15 (MSB)-D2 → DAC Register. TA → TX(A), RA → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1).	0	0
D15 (MSB)-D2 → DAC Register. TA+TA' → TX(A), RA+RA' → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1). The next D/A and A/D conversion period is changed by the addition of TA' and RA' master clock cycles, in which TA' and RA' can be positive, negative, or zero (refer to Table 2–4, AIC Responses to Improper Conditions).	0	1
D15 (MSB)-D2 → DAC Register. TA-TA' → TX(A), RA-RA' → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1). The next D/A and A/D conversion period is changed by the subtraction of TA' and RA' master clock cycles, in which TA' and RA' can be positive, negative, or zero (refer to Table 2–4, AIC Responses to Improper Conditions).	1	0
D15 (MSB)-D2 → DAC Register. TA → TX(A), RA → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1). After a delay of four shift cycles, a secondary transmission follows to program the AIC to operate in the desired configuration. In the telephone interface mode, data on DATA-DR is routed to DR (Serial Data Output) during secondary transmission.	1	1

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (primary communications) to the AIC initiates secondary communications upon completion of the primary communications. When the primary communication is complete, \overline{FSX} remains high for four shift clock cycles and then goes low and initiates the secondary communication. The timing specifications for the primary and secondary communications are identical. In this manner, the secondary communication, if initiated, is interleaved between successive primary communications. This interleaving prevents the secondary communication from interfering with the primary communications and DAC timing. This prevents the AIC from skipping a DAC output. \overline{FSR} is not asserted during secondary communications activity. However, in the dual-word (telephone interface) mode, \overline{FSD} is asserted during secondary communications but not during primary communications.

2.15.3 Secondary DX Word Bit Pattern

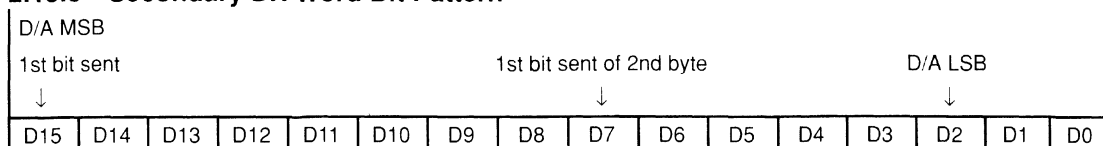


Table 2–3. Secondary DX Serial Communication Protocol

FUNCTIONS	D1	D0
D13 (MSB)-D9 → TA , 5 bits unsigned binary (see Figure 2–1). D6 (MSB)-D2 → RA, 5 bits unsigned binary (see Figure 2–1). D15, D14, D8, and D7 are unassigned.	0	0
D14 (sign bit)-D9 → TA', 6 bits 2s complement (see Figure 2–1). D7 (sign bit)-D2 → RA', 6 bits 2s complement (see Figure 2–1). D15 and D8 are unassigned.	0	1
D14 (MSB)-D9 → TB, 6 bits unsigned binary (see Figure 2–1). D7 (MSB)-D2 → RB, 6 bits unsigned binary (see Figure 2–1). D15 and D8 are unassigned.	1	0
D2 = 0/1 deletes/inserts the A/D high-pass filter. D3 = 0/1 deletes/inserts the loopback function. D4 = 0/1 disables/enables AUX IN+ and AUX IN–. D5 = 0/1 asynchronous/synchronous transmit and receive sections. D6 = 0/1 gain control bits (see Table 4–1). D7 = 0/1 gain control bits (see Table 4–1). D9 = 0/1 delete/insert on-board second-order (sin x)/x correction filter D10 = 0/1 output to D10OUT [dual-word (telephone interface) mode] D11 = 0/1 output to D11OUT [dual-word (telephone interface) mode] D8, D12–D15 are unassigned.	1	1

2.16 Reset Function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on RESET initializes the AIC registers to provide a 16-kHz A/D and D/A conversion rate for a 10.368-MHz master clock input signal. Also, the pass-bands of the A/D and D/A filters are 300 Hz to 7200 Hz and 0 Hz to 7200 Hz, respectively. Therefore, the filter bandwidths are 66% of those shown in the filter transfer function specification section. The AIC, excepting the control register, is initialized as follows (see AIC DX Data Word Format section):

REGISTER	TA	TA'	TB	RA	RA'	RB
INITIALIZED VALUE (HEX)	12	01	12	12	01	12

The control register bits are reset as follows (see Table 2–3):

$$D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1$$

This initialization allows normal serial port communications to occur between the AIC and the DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA', and TB register need to be programmed. Both transmit and receive timing are synchronously derived from these registers (see the Terminal Functions and DX Serial Data Word Format sections).

Figure 2–3 shows a circuit that provides a reset on power-up when power is applied in the sequence given in the Power-Up Sequence section. The circuit depends on the power supplies reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.

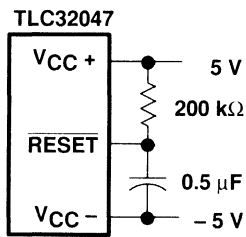


Figure 2–3. Reset on Power-Up Circuit

2.17 Power-Up Sequence

To ensure proper operation of the AIC and as a safeguard against latch-up, it is recommended that Schottky diodes with forward voltages less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND and from V_{CC-} to DGTL GND. In the absence of such diodes, power is applied in the following sequence: ANLG GND and DGTL GND, V_{CC-} , then V_{CC+} and V_{DD} . Also, no input signal is applied until after power-up.

2.18 AIC Register Constraints

The following constraints are placed on the contents of the AIC registers:

1. TA register must be ≥ 4 in word mode (WORD/BYTE= High).
2. TA register must be ≥ 5 in byte mode (WORD/BYTE= Low).
3. TA' register can be either positive, negative, or zero.
4. RA register must be ≥ 4 in word mode (WORD/BYTE = High).
5. RA register must be ≥ 5 in byte mode (WORD/BYTE = Low).
6. RA' register can be either positive, negative, or zero.
7. (TA register \pm TA' register) must be > 1 .
8. (RA register \pm RA' register) must be > 1 .
9. TB register must be ≥ 15 .
10. RB register must be ≥ 15 .

2.19 AIC Responses to Improper Conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 2–4. The general procedure for correcting any improper operation is to apply a reset and reprogram the registers to the proper value.

Table 2–4. AIC Responses to Improper Conditions

IMPROPER CONDITION	AIC RESPONSE
TA register + TA' register = 0 or 1 TA register – TA' register = 0 or 1	Reprogram TX(A) counter with TA register value
TA register + TA' register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into TX(A) counter, i.e., TA register + TA' register + 40 hex is loaded into TX(A) counter.
RA register + RA' register = 0 or 1 RA register – RA' register = 0 or 1	Reprogram RX(A) counter with RA register value
RA register + RA' register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX(A) counter, i.e., RA register + RA' register + 40 hex is loaded into RX(A) counter.
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down. Reprogram TA or RA registers after a reset.
TA register < 4 in word mode TA register < 5 in byte mode RA register < 4 in word mode RA register < 5 in byte mode	The AIC serial port no longer operates. Reprogram TA or RA registers after a reset.
TB register < 15	ADC no longer operates
RB register < 15	DAC no longer operates
AIC and DSP cannot communicate	Hold last DAC output

2.20 Operation With Conversion Times Too Close Together

If the difference between two successive D/A conversion frame syncs is less than 1/25 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly, and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A' register result is too small. When incrementally adjusting the conversion period via the A + A' register options, the designer should not violate this requirement. See Figure 2–4.

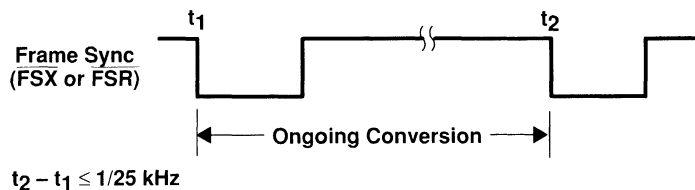


Figure 2–4. Conversion Times Too Close Together

2.21 More Than One Receive Frame Sync Occurring Between Two Transmit Frame Syncs – Asynchronous Operation

When incrementally adjusting the conversion period via the A + A' or A – A' register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during an FSX frame sync. The ongoing conversion period is then adjusted; however, either receive conversion period A or conversion period B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. If there is sufficient time between t_1 and t_2 , the receive conversion period adjustment is performed during receive conversion period A. Otherwise, the adjustment is performed during receive conversion period B. The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent FSX frame (see Figure 2–5).

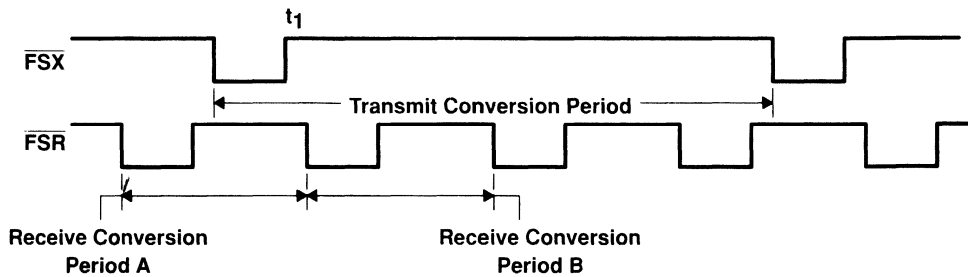


Figure 2-5. More Than One Receive Frame Sync Between Two Transmit Frame Syncs

2.22 More Than One Transmit Frame Sync Occurring Between Two Receive Frame Syncs – Asynchronous Operation

When incrementally adjusting the conversion period via the $A + A'$ or $A - A'$ register options, a specific protocol must be followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during an \overline{FSX} frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment as shown in Figure 2-6. When the adjustment command is issued during transmit conversion period A, receive conversion period A is adjusted if there is sufficient time between t_1 and t_2 . If there is not sufficient time between t_1 and t_2 , receive conversion period B is adjusted. The third option is that the receive portion of an adjustment command can be ignored if the adjustment command is sent during a receive conversion period, which is adjusted due to a prior adjustment command. For example, if adjustment commands are issued during transmit conversion periods A, B, and C, the first two commands may cause receive conversion periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during receive conversion period B, which already is adjusted via the transmit conversion period B adjustment command.

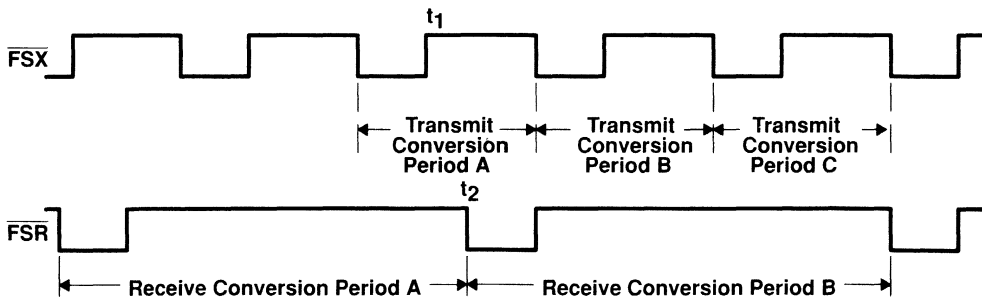


Figure 2-6. More Than One Transmit Frame Sync Between Two Receive Frame Syncs

2.23 More than One Set of Primary and Secondary DX Serial Communications Occurring Between Two Receive Frame Syncs (See DX Serial Data Word Format section) – Asynchronous Operation

The TA, TA', TB, and control register information that is transmitted in the secondary communication is accepted and applied during the ongoing transmit conversion period. If there is sufficient time between t_1 and t_2 , the TA, RA', and RB register information, sent during transmit conversion period A, is applied to receive conversion period A. Otherwise, this information is applied during receive conversion period B. If RA, RA', and RB register information has been received and is being applied during an ongoing conversion period, any subsequent RA, RA', or RB information received during this receive conversion period is disregarded. See Figure 2-7.

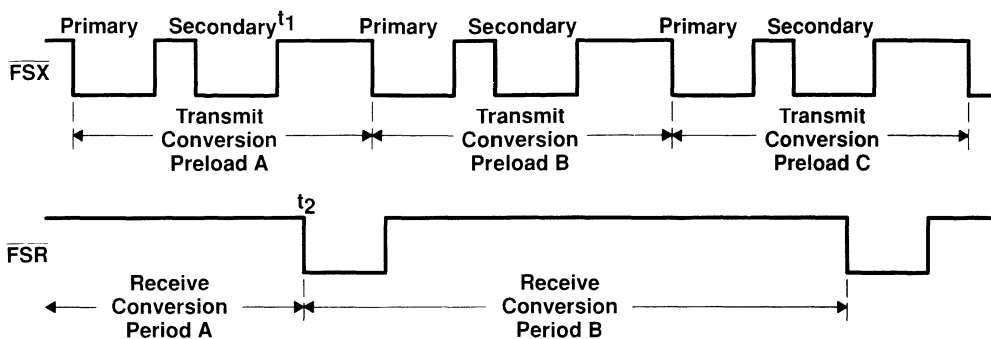


Figure 2–7. More Than One Set of Primary and Secondary DX Serial Communications Between Two Receive Frame Syncs

2.24 System Frequency Response Correction

The $(\sin x)/x$ correction for the DAC zero-order sample-and-hold output can be provided by an on-board second-order $(\sin x)/x$ correction filter (see Functional Block Diagram). This $(\sin x)/x$ correction filter can be inserted into or omitted from the signal path by digital-signal-processor control (data bit D9 in the DX secondary communications). When inserted, the $(\sin x)/x$ correction filter precedes the switched-capacitor low-pass filter. When the TB register (see Figure 2–1) equals 15, the correction results of Figures 5–8, 5–9, and 5–10 can be obtained.

The $(\sin x)/x$ correction can also be accomplished by disabling the on-board second-order correction filter and performing the $(\sin x)/x$ correction in digital signal processor software. The system frequency response can be corrected via DSP software to ± 0.1 dB accuracy to a band edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, that requires seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the $(\sin x)/x$ Correction Section for more details).

2.25 $(\sin x)/x$ Correction

If the designer does not wish to use the on-board second-order $(\sin x)/x$ correction filter, correction can be accomplished in digital signal processor (DSP) software. $(\sin x)/x$ correction can be accomplished easily and efficiently in digital signal processor software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results shown below are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires seven instruction cycles per sample on the TMS320 DSP. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction adds a slight amount of group delay at the upper edge of the 300-Hz to 3000-Hz band.

2.26 $(\sin x)/x$ Roll-Off for a Zero-Order Hold Function

The $(\sin x)/x$ roll-off error for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in Table 2–5 (see Figure 5–10).

Table 2–5. (sin x)/x Roll-Off Error

f_s (Hz)	Error = $20 \log \frac{\sin \pi f/f_s}{\pi f/f_s}$ $f = 3000$ Hz (dB)
7200	-2.64
8000	-2.11
9600	-1.44
14400	-0.63
16000	-0.50
19200	-0.35
25000	-0.21

The actual AIC (sin x)/x roll-off is slightly less than the figures above because the AIC has less than 100% duty cycle hold interval.

2.27 Correction Filter

To externally compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter can be implemented as shown in Figure 2–8.

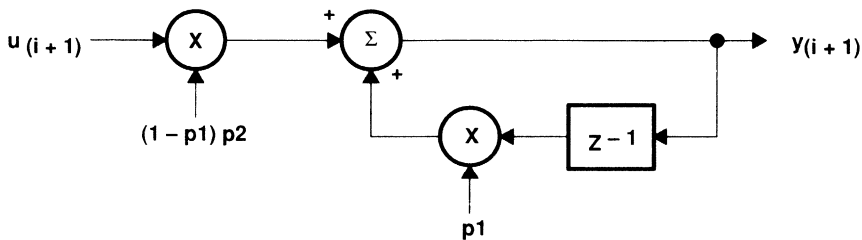


Figure 2–8. First-Order Correction Filter

The difference equation for this correction filter is:

$$y(i+1) = p2 \cdot (1-p1) \cdot u(i+1) + p1 \cdot y(i) \quad (4)$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{(p2)^2 \cdot (1-p1)^2}{1-2 \cdot p1 \cdot \cos(2\pi f/f_s) + (p1)^2} \quad (5)$$

2.28 Correction Results

Table 2-6 shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates (see Figures 5–8, 5–9, and 5–10).

Table 2–6. (sin x)/x Correction Table for $f_s = 8000$ Hz and $f_s = 9600$ Hz

f (Hz)	ROLL-OFF ERROR (dB)	
	$f_s = 8000$ Hz $p1 = -0.14813$ $p2 = 0.9888$	$f_s = 9600$ Hz $p1 = -0.1307$ $p2 = 0.9951$
300	-0.099	-0.043
600	-0.089	-0.043
900	-0.054	0
1200	-0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	-0.043	0
3000	-0.102	-0.043

2.29 TMS320 Software Requirements

The digital correction filter equation can be written in state variable form as follows:

$$Y_{(i+1)} = Y_{(i)} \times k1 + u_{(i+1)} \times k2$$

where

$$k1 = p1$$

$$k2 = (1 - p1)p2$$

$y(i)$ is the filter state

$u(i+1)$

The coefficients $k1$ and $k2$ must be represented as 16-bit integers. The SACH instruction (with the proper shift) yields the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, V_{CC+} (see Note 1)	-0.3 V to 15 V
Supply voltage range, V_{CC-} (see Note 1)	-0.3 V to 15 V
Supply voltage range, V_{DD}	-0.3 V to 15 V
Output voltage range, V_O	-0.3 V to 15 V
Input voltage range, V_I	-0.3 V to 15 V
Digital ground voltage range	-0.3 V to 15 V
Operating free-air temperature range: TLC32047C	0°C to 70°C
TLC32047I	-40°C to 85°C
Storage temperature range	-40°C to 125°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	...	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values for maximum ratings are with respect to V_{CC-} .

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)	4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)	-4.75	-5	-5.25	V
Digital supply voltage, V_{DD} (see Note 2)	4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND		0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)	2		4	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL} (see Note 3)	0		0.8	V
Load resistance at OUT+ and/or OUT-, R_L	300			Ω
Load capacitance at OUT+ and/or OUT-, C_L			100	pF
MSTR CLK frequency (see Note 4)		5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)			± 1.5	V
A/D or D/A conversion rate			25	kHz
Operating free-air temperature range, T_A	TLC32047C	0	70	$^{\circ}\text{C}$
	TLC32047I	-40	85	

- NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+} , and V_{CC-} are with respect to ANLG GND. Voltages at digital inputs and outputs and V_{DD} are with respect to DGTL GND.
3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data manual for logic voltage levels only.
4. The band-pass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 432 kHz and the high-pass section SCF clock is 24 kHz. If the low-pass SCF clock is shifted from 432 kHz, the low-pass roll-off frequency shifts by the ratio of the low-pass SCF clock to 432 kHz. If the high-pass SCF clock is shifted from 24 kHz, the high-pass roll-off frequency shifts by the ratio of the high-pass SCF clock to 24 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 432 kHz. If the SCF clock is shifted from 432 kHz, the low-pass roll-off frequency shifts by the ratio of the SCF clock to 432 kHz.
5. This range applies when $(IN+ - IN-)$ or $(AUX IN+ - AUX IN-)$ equals ± 6 V.

3.3 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $V_{DD} = 5$ V (Unless Otherwise Noted)

3.3.1 Total Device, MSTR CLK Frequency = 5.184 MHz, Outputs Not Loaded

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$V_{DD} = 4.75$ V, $I_{OH} = -300$ μA	2.4			V
V_{OL}	Low-level output voltage	$V_{DD} = 4.75$ V, $I_{OL} = 2$ mA			0.4	V
I_{CC+}	Supply current from V_{CC+}	TLC32047C			35	mA
		TLC32047I			40	
I_{CC-}	Supply current from V_{CC-}	TLC32047C			-35	mA
		TLC32047I			-40	
I_{DD}	Supply current from V_{DD}				7	mA
V_{ref}	Internal reference output voltage		3		3.3	V
αV_{ref}	Temperature coefficient of internal reference voltage			250		ppm/ $^{\circ}\text{C}$
r_o	Output resistance at REF			100		k Ω

† All typical values are at $T_A = 25^{\circ}\text{C}$.

3.3.2 Power Supply Rejection and Crosstalk Attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{CC+} or V _{CC-} supply voltage rejection ratio, receive channel	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)	30			dB
	f = 30 kHz to 50 kHz		45			
V _{CC+} or V _{CC-} supply voltage rejection ratio, transmit channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT+	30			dB
	f = 30 kHz to 50 kHz		45			
Crosstalk attenuation, transmit-to-receive (single-ended)			80			dB

† All typical values are at T_A = 25°C.

3.3.3 Serial Port

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -300 μA	2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 2 mA	0.4			V
I _I	Input current		±10			μA
I _I	Input current, DATA-DR/CONTROL		±100			μA
C _i	Input capacitance		15			pF
C _o	Output capacitance		15			pF

† All typical values are at T_A = 25°C.

3.3.4 Receive Amplifier Input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
A/D converter offset error (filters in)			10 70			mV
CMRR	Common-mode rejection ratio at IN+, IN-, or AUX IN+, AUX IN-	See Note 6	55			dB
r _i	Input resistance at IN+, IN- or AUX IN+, AUX IN-, REF		100			kΩ

† All typical values are at T_A = 25°C.

NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with a 24-kHz conversion rate.

3.3.5 Transmit Filter Output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OO}	Output offset voltage at OUT+ or OUT- (single-ended relative to ANLG GND)		15 80			mV
V _{OM}	Maximum peak output voltage swing across R _L at OUT+ or OUT- (single-ended)	R _L ≥ 300 Ω, Offset voltage = 0	±3			V
	Maximum peak output voltage swing between OUT+ and OUT- (differential output)	R _L ≥ 600 Ω,	±6			V

† All typical values are at T_A = 25°C.

3.3.6 Receive and Transmit Channel System Distortion, SCF Clock Frequency = 432 kHz (see Note 7)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	single-ended	$V_I = -0.1 \text{ dB to } -24 \text{ dB}$	70		dB	
	differential		62	70		
Attenuation of third and higher harmonics of A/D input signal	single-ended		65		dB	
	differential		57	65		
Attenuation of second harmonic of D/A input signal	single-ended		$V_I = -0 \text{ dB to } -24 \text{ dB}$	70		dB
	differential			62	70	
Attenuation of third and higher harmonics of D/A input signal	single-ended	65		dB		
	differential	57			65	

† All typical values are at $T_A = 25^\circ\text{C}$.

3.3.7 Receive Channel Signal-to-Distortion Ratio (see Note 7)

PARAMETER	TEST CONDITIONS	$A_V = 1 \text{ V/V}^\ddagger$		$A_V = 2 \text{ V/V}^\ddagger$		$A_V = 4 \text{ V/V}^\ddagger$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio	$V_I = -6 \text{ dB to } -0.1 \text{ dB}$	56		§		§		dB
	$V_I = -12 \text{ dB to } -6 \text{ dB}$	56		56		§		
	$V_I = -18 \text{ dB to } -12 \text{ dB}$	53		56		56		
	$V_I = -24 \text{ dB to } -18 \text{ dB}$	47		53		56		
	$V_I = -30 \text{ dB to } -24 \text{ dB}$	41		47		53		
	$V_I = -36 \text{ dB to } -30 \text{ dB}$	35		41		47		
	$V_I = -42 \text{ dB to } -36 \text{ dB}$	29		35		41		
	$V_I = -48 \text{ dB to } -42 \text{ dB}$	23		29		35		
$V_I = -54 \text{ dB to } -48 \text{ dB}$	17		23		29			

‡ A_V is the programmable gain of the input amplifier.

§ Measurements under these conditions are unreliable due to overrange and signal clipping.

NOTE 7: The test condition is a 1-kHz input signal with a 24-kHz conversion rate. The load impedance for the DAC is 600 Ω . Input and output voltages are referred to V_{ref} .

3.3.8 Transmit Channel Signal-to-Distortion Ratio (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	$V_I = -6 \text{ dB to } -0.1 \text{ dB}$	58		dB
	$V_I = -12 \text{ dB to } -6 \text{ dB}$	58		
	$V_I = -18 \text{ dB to } -12 \text{ dB}$	56		
	$V_I = -24 \text{ dB to } -18 \text{ dB}$	50		
	$V_I = -30 \text{ dB to } -24 \text{ dB}$	44		
	$V_I = -36 \text{ dB to } -30 \text{ dB}$	38		
	$V_I = -42 \text{ dB to } -36 \text{ dB}$	32		
	$V_I = -48 \text{ dB to } -42 \text{ dB}$	26		
	$V_I = -54 \text{ dB to } -48 \text{ dB}$	20		

NOTE 7: The test condition is a 1-kHz input signal with a 24-kHz conversion rate. The load impedance for the DAC is 600 Ω . Input and output voltages are referred to V_{ref} .

3.3.9 Receive and Transmit Gain and Dynamic Range (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit gain tracking error	$V_O = -48 \text{ dB to } 0 \text{ dB}$ signal range	± 0.05	± 0.25		dB
Receive gain tracking error	$V_I = -48 \text{ dB to } 0 \text{ dB}$ signal range	± 0.05	± 0.25		dB

NOTE 8: Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 dB relative to V_{ref}).

3.3.10 Receive Channel Band-Pass Filter Transfer Function, SCF $f_{clock} = 432 \text{ kHz}$, Input ($IN+$ – $IN-$) is a $\pm 3\text{-V}$ Sine Wave‡ (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY	ADJUSTMENT	MIN	TYP†	MAX	UNIT
Filter gain	Input signal reference is 0 dB	$f \leq 150 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-33	-29	-25	dB
		$f = 300 \text{ Hz}$	$K1 \times -0.26 \text{ dB}$	-4	-2	-1	
		$f = 450 \text{ Hz to } 9300 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.25	0	0.25	
		$f = 9300 \text{ Hz to } 9900 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.3	0	0.3	
		$f = 9900 \text{ Hz to } 10950 \text{ Hz}$	$K1 \times 0 \text{ dB}$	-0.5	0	0.5	
		$f = 11.4 \text{ kHz}$	$K1 \times 2.3 \text{ dB}$		-2	-0.5	
		$f = 12 \text{ kHz}$	$K1 \times 2.7 \text{ dB}$		-16	-14	
		$f \geq 13.2 \text{ kHz}$	$K1 \times 3.2 \text{ dB}$			-40	
		$f \geq 15 \text{ kHz}$	$K1 \times 0 \text{ dB}$			-60	

† All typical values are at $T_A = 25^\circ\text{C}$.

‡ The MIN, TYP, and MAX specifications are given for a 432-kHz SCF clock frequency. A slight error in the 432-kHz SCF can result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where $K1 = 100 \times [(SCF \text{ frequency} - 432 \text{ kHz})/432 \text{ kHz}]$. For errors greater than 0.25%, see Note 9.

NOTE 9: The filter gain outside of the pass band is measured with respect to the gain at 1 kHz. The filter gain within the pass band is measured with respect to the average gain within the pass band. The pass bands are 450 Hz to 10.95 kHz and 0 to 10.95 kHz for the band-pass and low-pass filters, respectively. For switched-capacitor filter clocks at frequencies other than 432 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 432 kHz.

3.3.11 Receive and Transmit Channel Low-Pass Filter Transfer Function, SCF $f_{\text{clock}} = 432 \text{ kHz}$ (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY RANGE	ADJUSTMENT ADDEND [‡]	MIN	TYP [†]	MAX	UNIT
Filter gain	Input signal reference is 0 dB	f = 0 Hz to 9300 Hz	$K1 \times 0 \text{ dB}$	-0.25	0	0.25	dB
		f = 9300 Hz to 9900 Hz	$K1 \times 0 \text{ dB}$	-0.3	0	0.3	
		f = 9900 Hz to 10950 Hz	$K1 \times 0 \text{ dB}$	-0.5	0	0.5	
		f = 11.4 kHz	$K1 \times 2.3 \text{ dB}$	-5	-2	-0.5	
		f = 12 kHz	$K1 \times 2.7 \text{ dB}$		-16	-14	
		f ≥ 13.2 kHz	$K1 \times 3.2 \text{ dB}$			-40	
		f ≥ 15 kHz	$K1 \times 0 \text{ dB}$			-60	

[†] All typical values are at $T_A = 25^\circ\text{C}$.

[‡] The MIN, TYP, and MAX specifications are given for a 432-kHz SCF clock frequency. A slight error in the 432-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where $K1 = 100 \times [(\text{SCF frequency} - 432 \text{ kHz})/432 \text{ kHz}]$. For errors greater than 0.25%, see Note 9.

NOTE 9: The filter gain outside of the pass band is measured with respect to the gain at 1 kHz. The filter gain within the pass band is measured with respect to the average gain within the pass band. The pass bands are 450 Hz to 10.95 kHz and 0 to 10.95 kHz for the band-pass and low-pass filters, respectively. For switched-capacitor filter clocks at frequencies other than 432 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 432 kHz.

3.4 Operating Characteristics Over Recommended Operating Free-Air Temperature Range, $V_{CC+} = 5 \text{ V}$, $V_{CC-} = -5 \text{ V}$, $V_{DD} = 5 \text{ V}$

3.4.1 Receive and Transmit Noise (Measurement Includes Low-Pass and Band-Pass Switched-Capacitor Filters)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
Transmit noise	broadband with (sin x)/x	DX = input = 00000000000000, constant input code		280	500	$\mu\text{V rms}$
	broadband without (sin x)/x			250	450	
	0 to 12 kHz with (sin x)/x			250	400	
	0 to 12 kHz without (sin x)/x			240	400	
Receive noise (see Note 10)		Inputs grounded, gain = 1		300	500	$\mu\text{V rms}$
				18		dBrnc0

[†] All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 10: The noise is computed by statistically evaluating the digital output of the A/D converter.

3.5 Timing Requirements

3.5.1 Serial Port Recommended Input Signals

PARAMETER		MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	95		ns
$t_{r(MCLK)}$	Master clock rise time		10	ns
$t_{f(MCLK)}$	Master clock fall time		10	ns
	Master clock duty cycle	25%	75%	
	RESET pulse duration (see Note 11)	800		ns
$t_{su(DX)}$	DX setup time before SCLK↓	20		ns
$t_{h(DX)}$	DX hold time after SCLK↓		$t_{c(SCLK)}/4$	ns

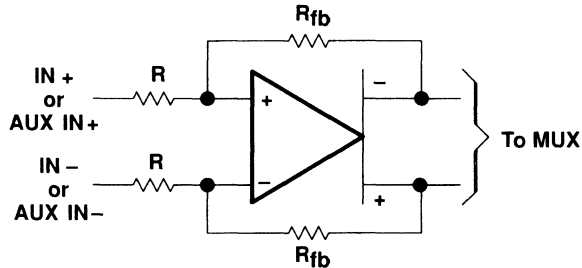
NOTE 11: RESET pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values.

3.5.2 Serial Port – AIC Output Signals, $C_L = 30$ pF for SHIFT CLK Output, $C_L = 15$ pF For All Other Outputs

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time	380			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		3	8	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		3	8	ns
	Shift clock (SCLK) duty cycle	45		55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}/\overline{FSD}$ ↓		30		ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}/\overline{FSD}$ ↑		35	90	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑			90	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$ ↓ in word mode			90	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$ ↑ in word mode			90	ns
$t_{f(EODX)}$	\overline{EODX} fall time		2	8	ns
$t_{f(EODR)}$	\overline{EODR} fall time		2	8	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$ ↓ in byte mode			90	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$ ↑ in byte mode			90	ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓		65	170	ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑		65	170	ns

† Typical values are at $T_A = 25^\circ\text{C}$.

4 Parameter Measurement Information



$$R_{fb} = R \text{ for } D6 = 1 \text{ and } D7 = 1$$

$$D6 = 0 \text{ and } D7 = 0$$

$$R_{fb} = 2R \text{ for } D6 = 1 \text{ and } D7 = 0$$

$$R_{fb} = 4R \text{ for } D6 = 0, \text{ and } D7 = 1$$

Figure 4–1. IN+ and IN– Gain Control Circuitry

Table 4–1. Gain Control Table (Analog Input Signal Required for Full-Scale Bipolar A/D Conversion Twos Complement)[†]

INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT [‡] [§]	A/D CONVERSION RESULT
	D6	D7		
Differential configuration Analog input = IN+ – IN– = AUX IN+ – AUX IN–	1	1	$V_{ID} = \pm 6 \text{ V}$	\pm full scale
	0	0	$V_{ID} = \pm 3 \text{ V}$	\pm full scale
	1	0	$V_{ID} = \pm 1.5 \text{ V}$	\pm full scale
Single-ended configuration Analog input = IN+ – ANLG GND = AUX IN+ – ANLG GND	1	1	$V_I = \pm 3 \text{ V}$	\pm half scale
	0	0	$V_I = \pm 3 \text{ V}$	\pm full scale
	1	0	$V_I = \pm 1.5 \text{ V}$	\pm full scale

[†] $V_{CC+} = 5 \text{ V}$, $V_{CC-} = -5 \text{ V}$, $V_{DD} = 5 \text{ V}$

[‡] V_{ID} = Differential Input Voltage, V_I = Input voltage referenced to ground with IN– or AUX IN– connected to ground.

[§] In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.

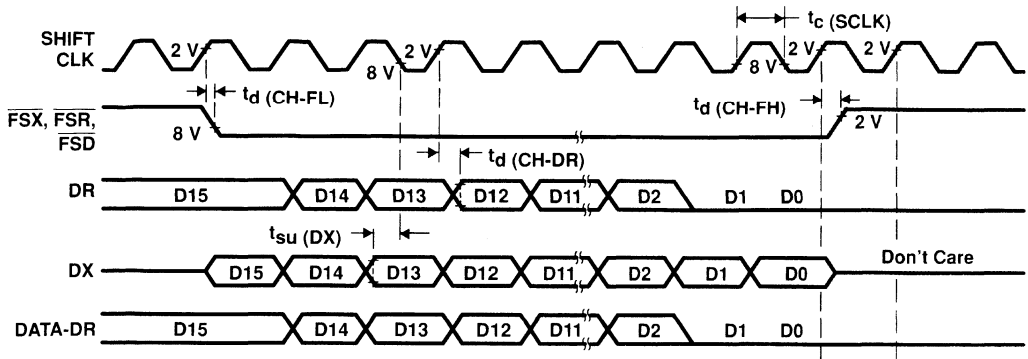


Figure 4-2. Dual-Word (Telephone Interface) Mode Timing

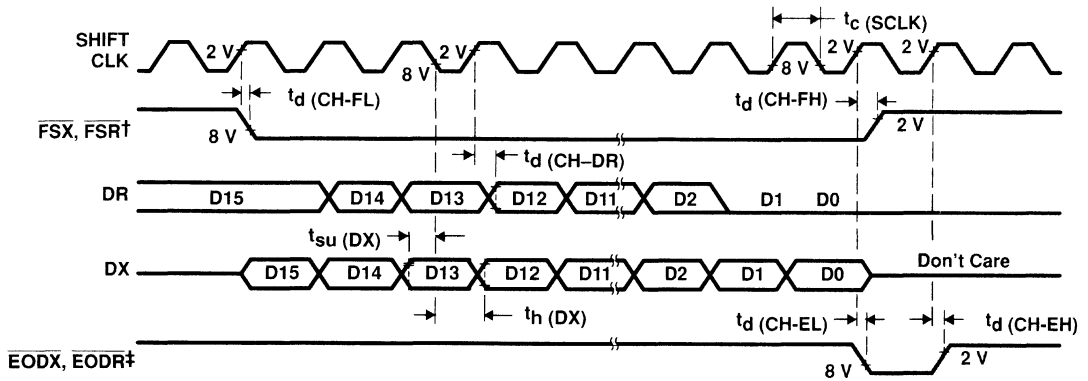


Figure 4-3. Word Timing

† The time between falling edges of $\overline{\text{FSR}}$ is the A/D conversion period and the time between falling edges of $\overline{\text{FSX}}$ is the D/A conversion period.

‡ In the word format, $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ go low to signal the end of a 16-bit data word to the processor. The word-cycle is 20 shift-clacks wide, giving a four-clock period setup time between data words.

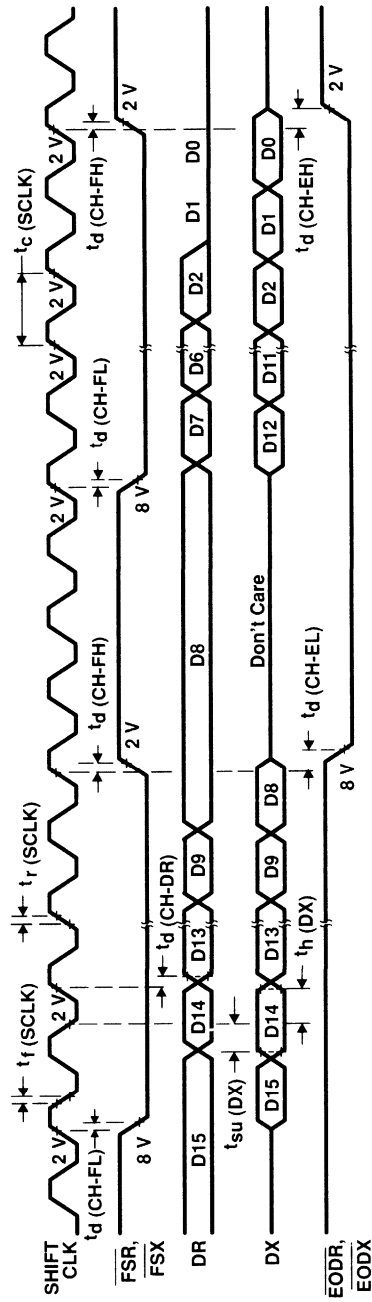


Figure 4-4. Byte-Mode Timing

† The time between falling edges of FSR is the A/D conversion period, and the time between falling edges of FSX is the D/A conversion period.
 ‡ In the byte mode, when EODX or EODR is high, the first byte is transmitted or received, and when these signals are low, the second byte is transmitted or received. Each byte-cycle is 12 shift-clocks long, allowing for a four-shift-clock setup time between byte transmissions.

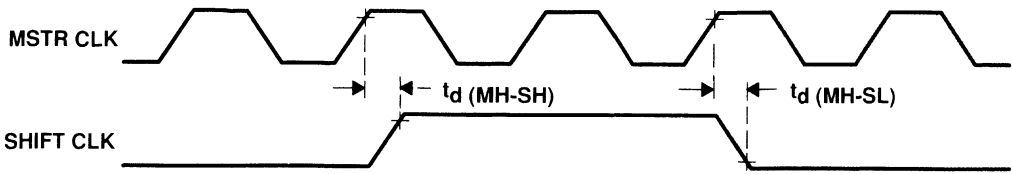


Figure 4-5. Shift-Clock Timing

4.1 TMS32047 – Processor Interface

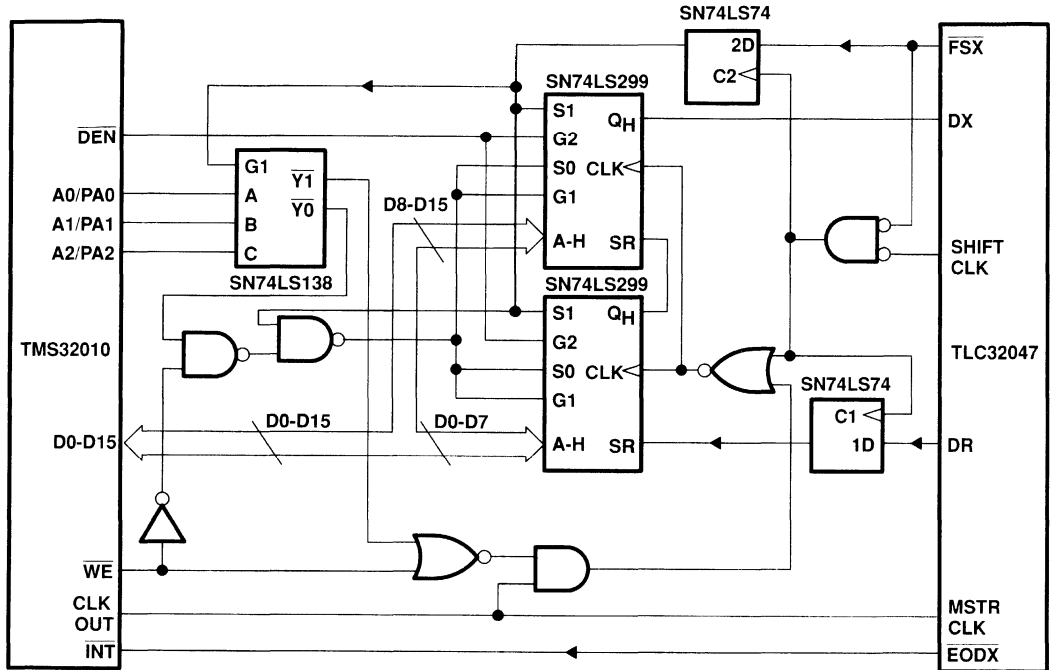
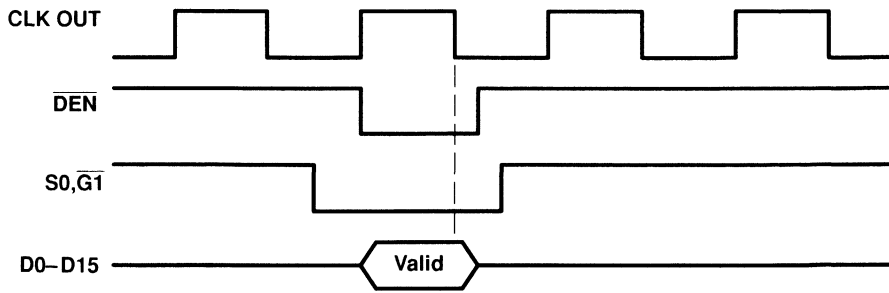
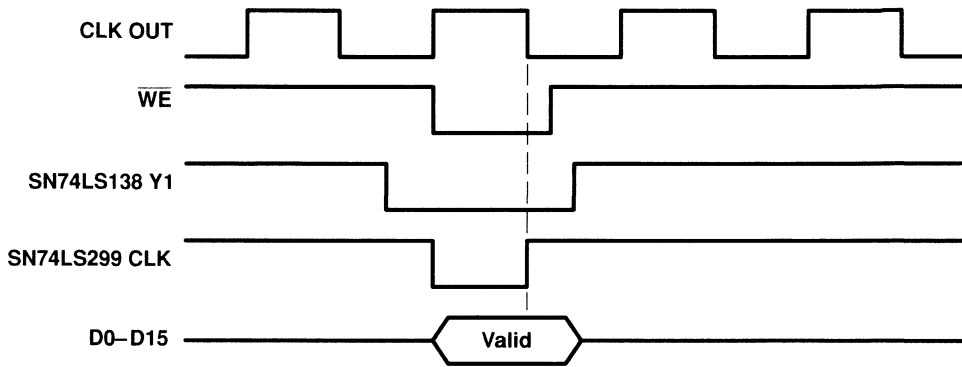


Figure 4-6. TMS32010/TMS320C15-TLC32047 Interface Circuit



(a) IN INSTRUCTION TIMING



(b) OUT INSTRUCTION TIMING

Figure 4-7. TMS32010/TMS320C15-TLC32047 Interface Timing

5 Typical Characteristics

**D/A AND A/D LOW-PASS FILTER
RESPONSE SIMULATION**

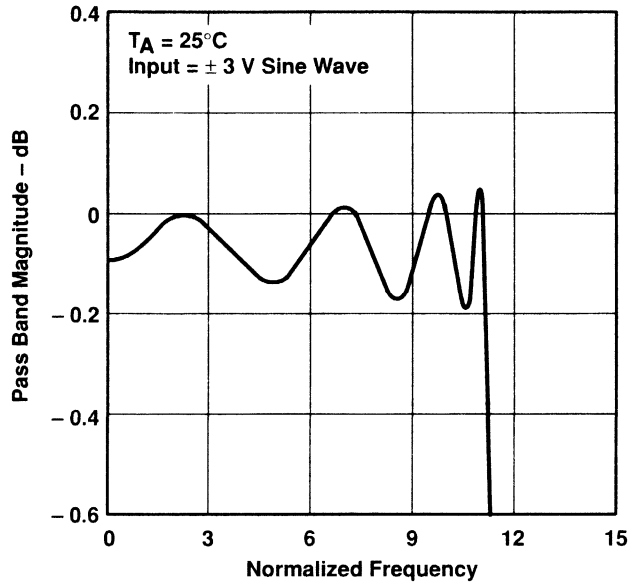


Figure 5-1

**D/A AND A/D LOW-PASS FILTER
RESPONSE SIMULATION**

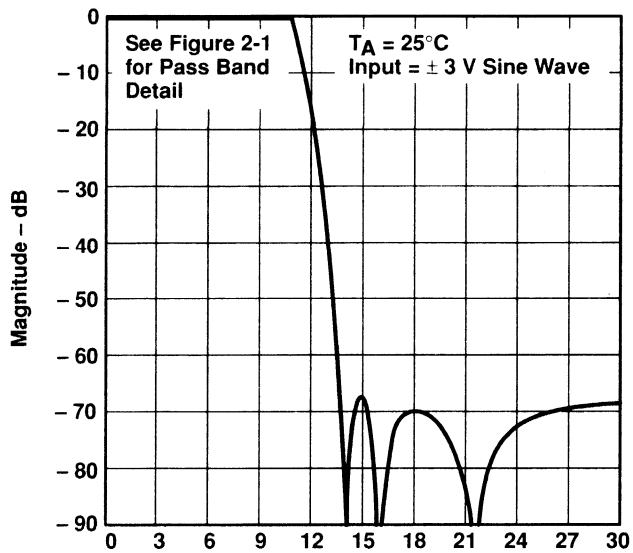


Figure 5-2

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{432}$

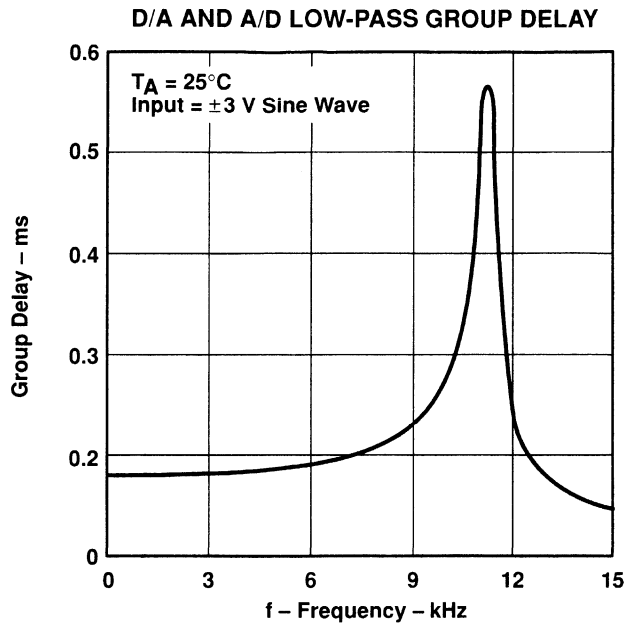


Figure 5–3

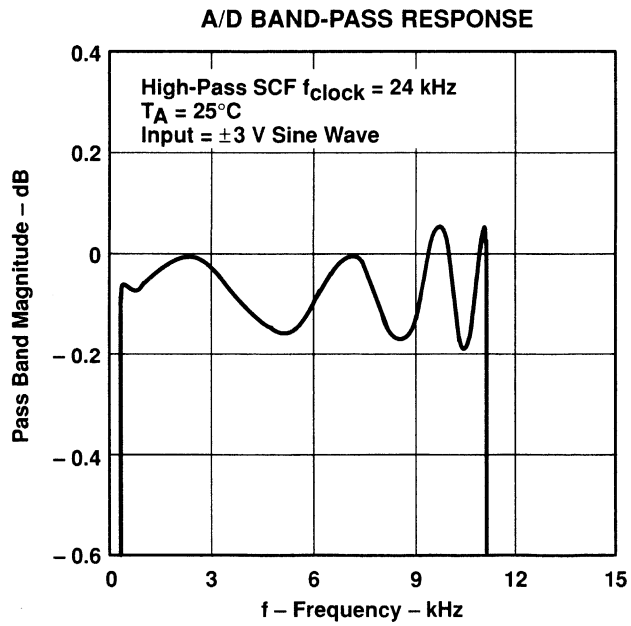


Figure 5–4

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{432}$

A/D BAND-PASS FILTER RESPONSE SIMULATION

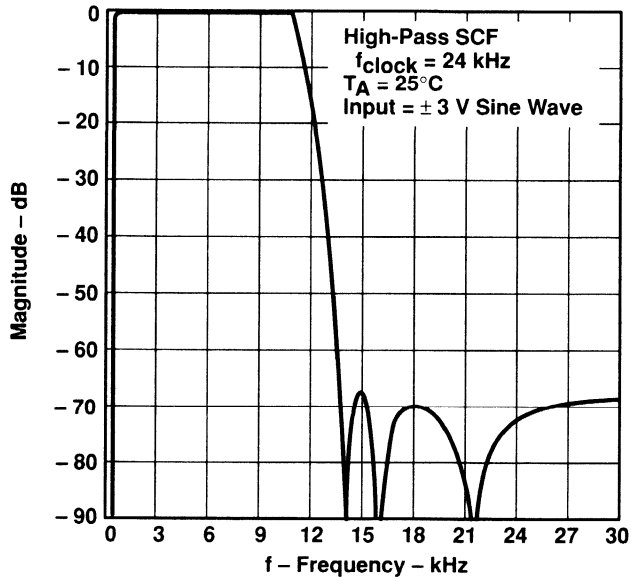


Figure 5-5

A/D BAND-PASS FILTER GROUP DELAY

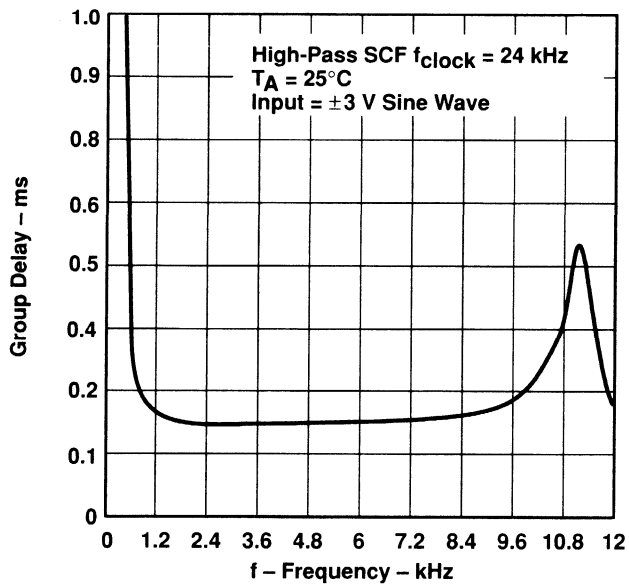


Figure 5-6

NOTE : Absolute Frequency (kHz) =
$$\frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{432}$$

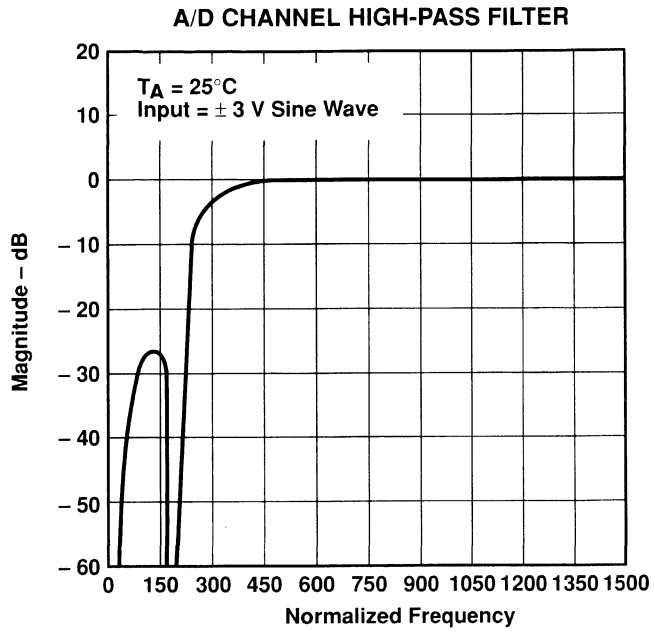


Figure 5-7

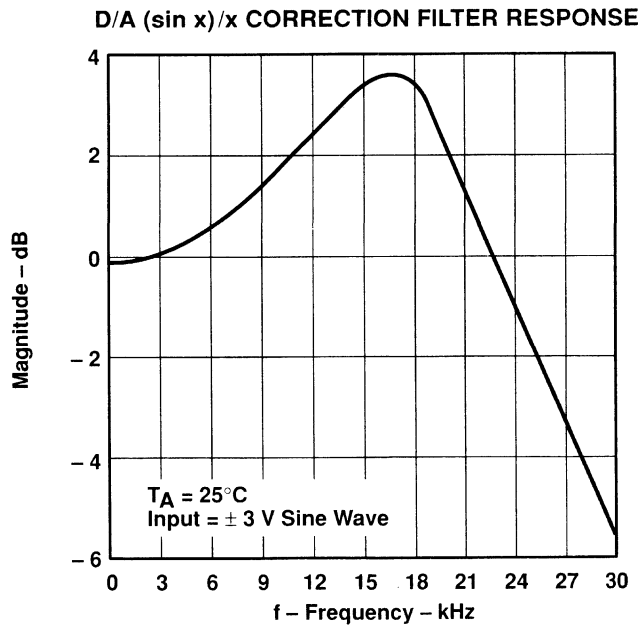
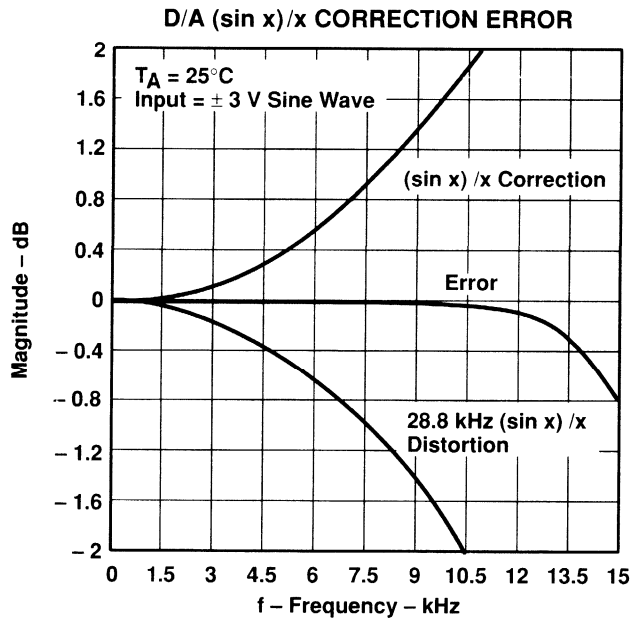
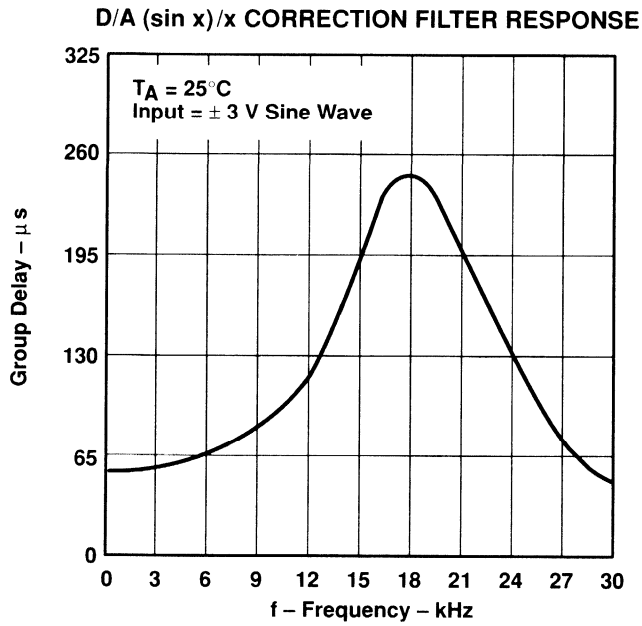


Figure 5-8

NOTE : Absolute Frequency (kHz) =
$$\frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{432}$$



NOTE : Absolute Frequency (kHz) =
$$\frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{432}$$

A/D BAND-PASS GROUP DELAY

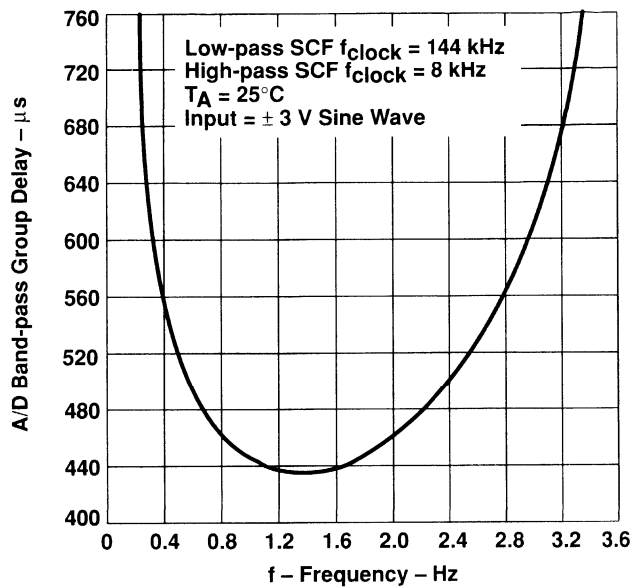


Figure 5-11

D/A LOW-PASS GROUP DELAY

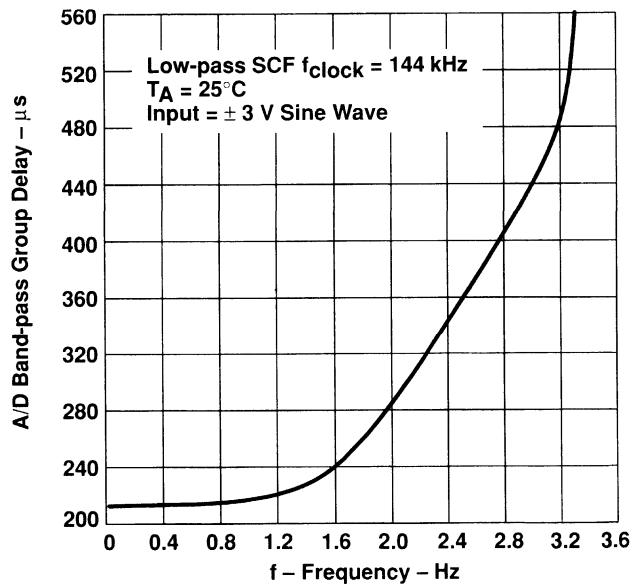


Figure 5-12

**A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL**

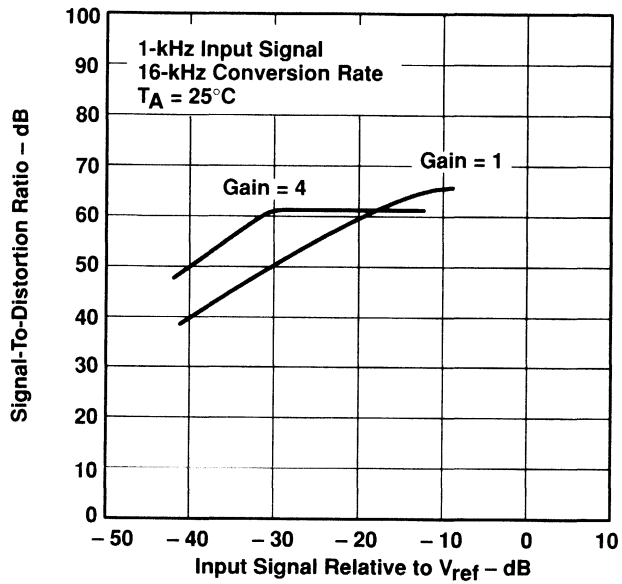


Figure 5-13

**A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN AT 0-dB INPUT SIGNAL)**

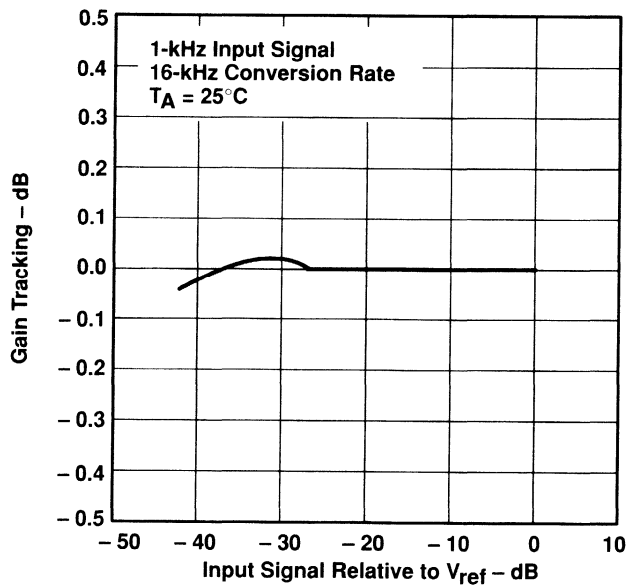


Figure 5-14

**D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL**

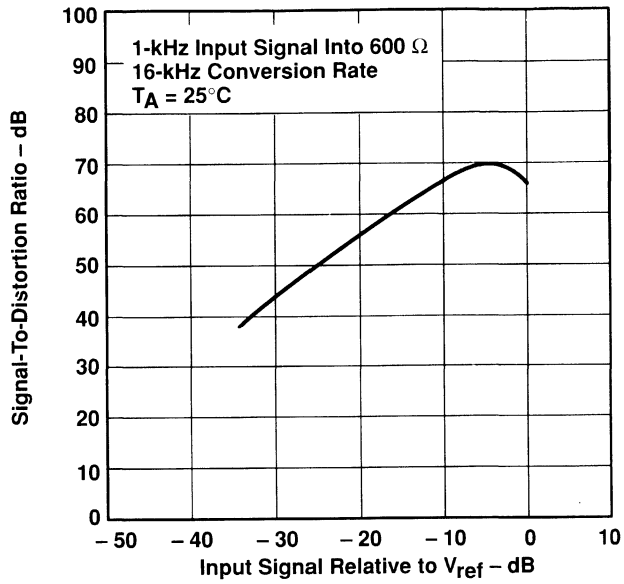


Figure 5-15

**D/A GAIN TRACKING (GAIN RELATIVE TO GAIN
AT 0-dB INPUT SIGNAL)**

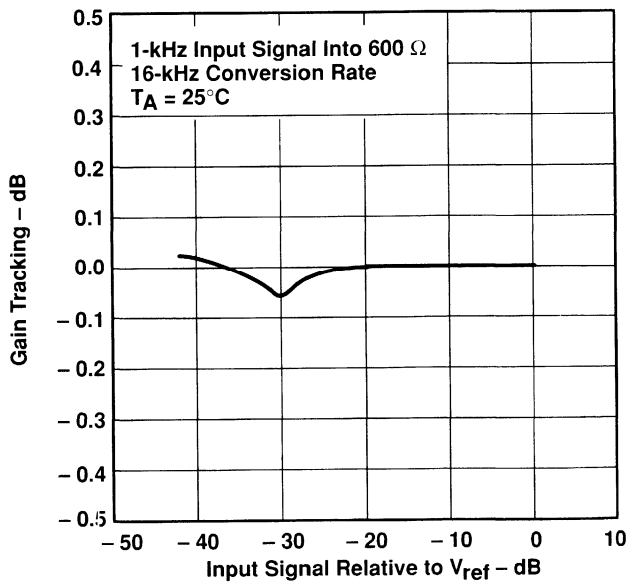


Figure 5-16

**A/D SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL**

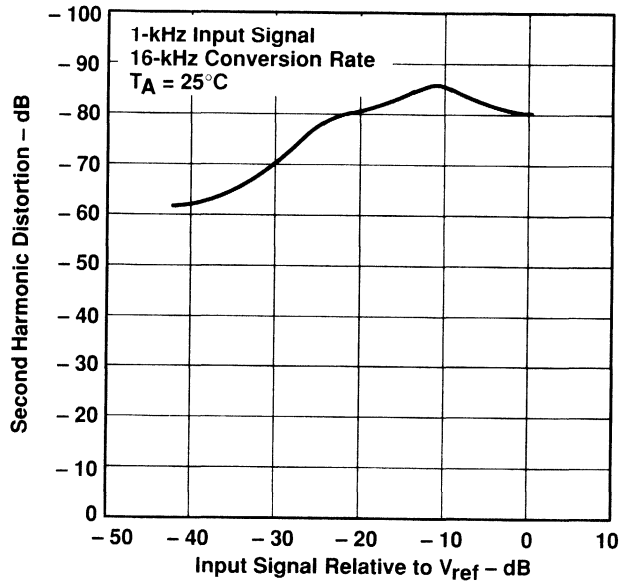


Figure 5-17

**D/A SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL**

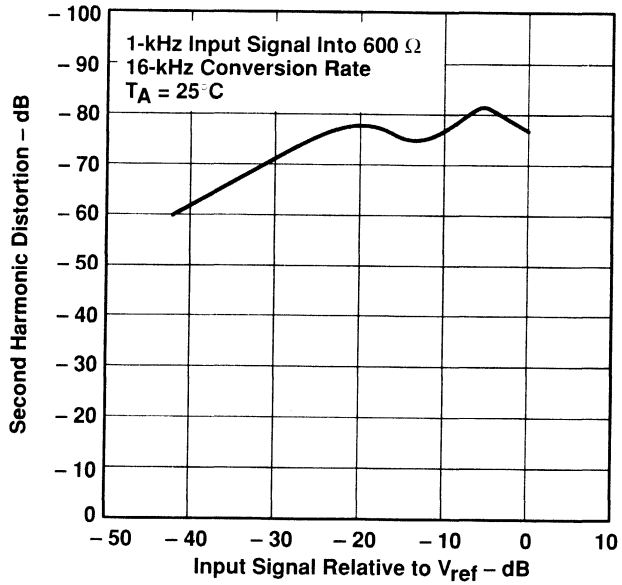


Figure 5-18

**A/D THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL**

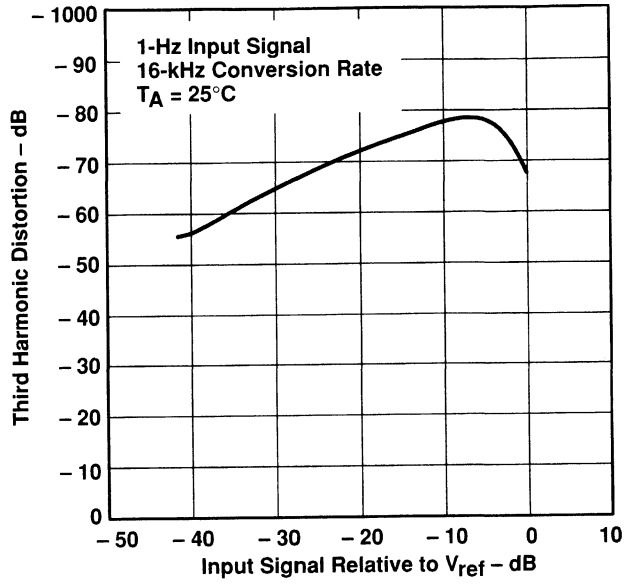


Figure 5-19

**D/A THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL**

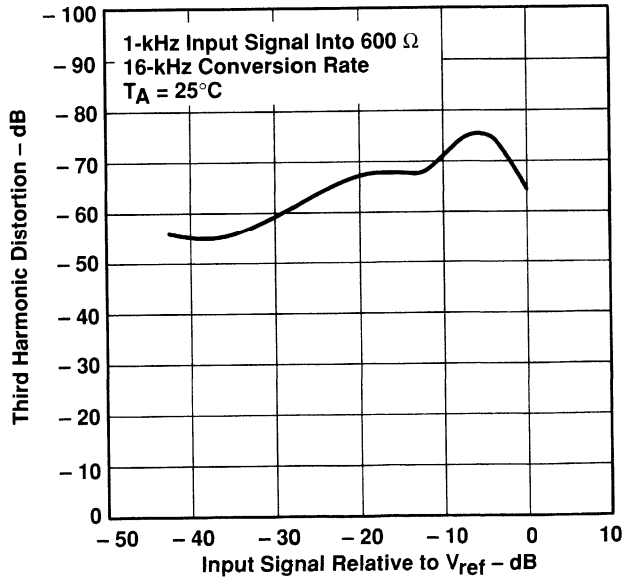
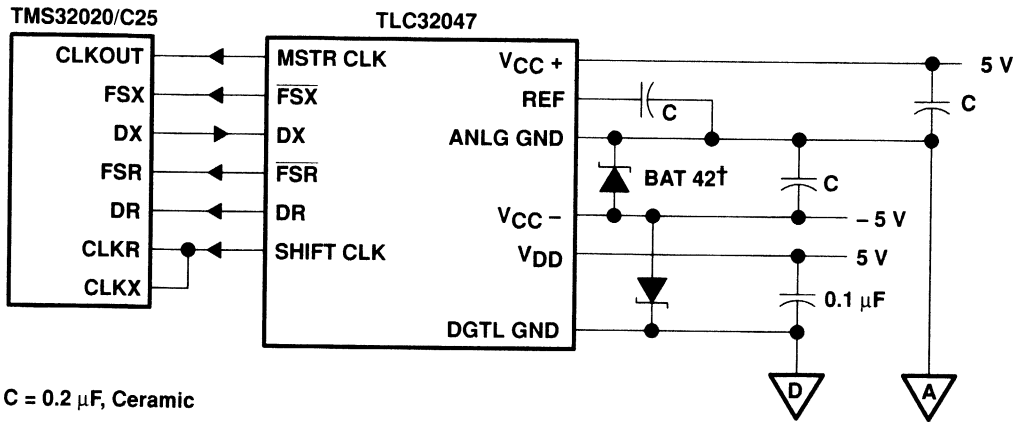


Figure 5-20

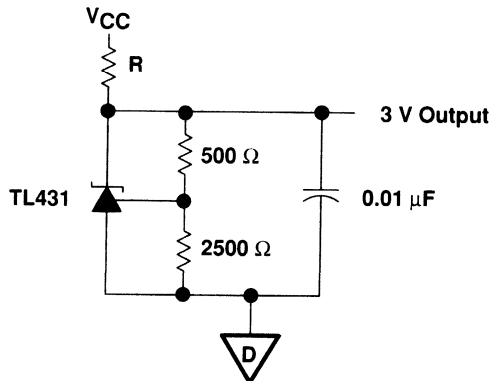
6 Application Information



C = 0.2 μ F, Ceramic

Figure 6-1. AIC Interface to the TMS32020/C25 Showing Decoupling Capacitors and Schottky Diode†

† Thomson Semiconductors



FOR: $V_{CC} = 12 \text{ V}$, $R = 7200 \Omega$
 $V_{CC} = 10 \text{ V}$, $R = 5600 \Omega$
 $V_{CC} = 0 \text{ V}$, $R = 1600 \Omega$

Figure 6-2. External Reference Circuit for TLC32047

TLC320AC01C ***Data Manual***

Single-Supply Analog Interface Circuit

SLAS057D
October 1996



Printed on Recycled Paper

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Contents

<i>Section</i>	<i>Title</i>	<i>Page</i>
1	Introduction	4–193
1.1	Features	4–194
1.2	Functional Block Diagram	4–195
1.3	Terminal Assignments	4–195
1.4	Terminal Functions	4–197
1.5	Register Functional Summary	4–200
2	Detailed Description	4–201
2.1	Definitions and Terminology	4–201
2.2	Reset and Power-Down Functions	4–202
2.2.1	Reset	4–202
2.2.2	Conditions of Reset	4–202
2.2.3	Software and Hardware Power-Down	4–202
2.2.4	Register Default Values After POR, Software Reset, or $\overline{\text{RESET}}$ Is Applied	4–202
2.3	Master-Slave Terminal Function	4–204
2.4	ADC Signal Channel	4–204
2.5	DAC Signal Channel	4–204
2.6	Serial Interface	4–204
2.7	Number of Slaves	4–205
2.8	Required Minimum Number of MCLK Periods	4–206
2.8.1	TLC320AC01 AIC Master-Slave Summary	4–206
2.8.2	Notes on TLC320AC01/02 AIC Master-Slave Operation	4–207
2.9	Operating Frequencies	4–209
2.9.1	Master and Stand-Alone Operating Frequencies	4–209
2.9.2	Slave and Codec Operating Frequencies	4–209
2.10	Switched-Capacitor Filter Frequency (FCLK)	4–209
2.11	Filter Bandwidths	4–209
2.12	Master and Stand-Alone Modes	4–209
2.12.1	Register Programming	4–209
2.12.2	Master and Stand-Alone Functional Sequence	4–210
2.13	Slave and Codec Modes	4–210
2.13.1	Slave and Codec Functional Sequence	4–211
2.13.2	Slave Register Programming	4–211
2.14	Terminal Functions	4–211
2.14.1	Frame-Sync Function	4–211
2.14.2	Data Out (DOUT)	4–212
2.14.3	Data In (DIN)	4–212
2.14.4	Hardware Program Terminals (FC1 and FC0)	4–212
2.14.5	Midpoint Voltages (ADC V_{MID} and DAC V_{MID})	4–213
2.15	Device Functions	4–213
2.15.1	Phase Adjustment	4–213
2.15.2	Analog Loopback	4–214

Contents (Continued)

<i>Section</i>	<i>Title</i>	<i>Page</i>
2.15.3	16-Bit Mode	4-214
2.15.4	Free-Run Mode	4-214
2.15.5	Force Secondary Communication	4-214
2.15.6	Enable Analog Input Summing	4-215
2.15.7	DAC Channel (sin x)/x Error Correction	4-215
2.16	Serial Communications	4-215
2.16.1	Stand-Alone and Master-Mode Word Sequence and Information Content During Primary and Secondary Communications	4-215
2.16.2	Slave and Codec-Mode Word Sequence and Information Content During Primary and Secondary Communications	4-216
2.17	Request for Secondary Serial Communication and Phase Shift	4-217
2.17.1	Initiating a Request	4-217
2.17.2	Normal Combinations of Control	4-217
2.17.3	Additional Control Options	4-217
2.18	Primary Serial Communications	4-218
2.18.1	Primary Serial Communications Data Format	4-219
2.18.2	Data Format From DOUT During Primary Serial Communications	4-219
2.19	Secondary Serial Communications	4-219
2.19.1	Data Format to DIN During Secondary Serial Communications	4-219
2.19.2	Control Data-Bit Function in Secondary Serial Communication	4-219
2.20	Internal Register Format	4-220
2.20.1	Pseudo-Register 0 (No-Op Address)	4-220
2.20.2	Register 1 (A Register)	4-220
2.20.3	Register 2 (B Register)	4-221
2.20.4	Register 3 (A' Register)	4-221
2.20.5	Register 4 (Amplifier Gain-Select Register)	4-222
2.20.6	Register 5 (Analog Configuration Register)	4-222
2.20.7	Register 6 (Digital Configuration Register)	4-223
2.20.8	Register 7 (Frame-Sync Delay Register)	4-223
2.20.9	Register 8 (Frame-Sync Number Register)	4-224
3	Specifications	4-225
3.1	Absolute Maximum Ratings Over Operating Free-Air Temperature Range	4-225
3.2	Recommended Operating Conditions	4-225
3.3	Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, MCLK = 5.184 MHz, V _{DD} = 5 V, Outputs Unloaded, Total Device	4-226
3.4	Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, V _{DD} = 5 V, Digital I/O Terminals (DIN, DOUT, EOC, FC0, FC1, \overline{FS} , \overline{FSD} , MCLK, M/ \overline{S} , SCLK)	4-226

Contents (Continued)

<i>Section</i>	<i>Title</i>	<i>Page</i>
3.5	Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, $V_{DD} = 5\text{ V}$, ADC and DAC Channels	4-226
3.5.1	ADC Channel Filter Transfer Function, $F_{CLK} = 144\text{ kHz}$, $f_s = 8\text{ kHz}$	4-226
3.5.2	ADC Channel Input, $V_{DD} = 5\text{ V}$, Input Amplifier Gain = 0 dB	4-227
3.5.3	ADC Channel Signal-to-Distortion Ratio, $V_{DD} = 5\text{ V}$, $f_s = 8\text{ kHz}$	4-227
3.5.4	DAC Channel Filter Transfer Function, $F_{CLK} = 144\text{ kHz}$, $f_s = 9.6\text{ kHz}$, $V_{DD} = 5\text{ V}$	4-227
3.5.5	DAC Channel Signal-to-Distortion Ratio, $V_{DD} = 5\text{ V}$, $f_s = 8\text{ kHz}$	4-228
3.5.6	System Distortion, $V_{DD} = 5\text{ V}$, $f_s = 8\text{ kHz}$, $F_{CLK} = 144\text{ kHz}$	4-228
3.5.7	Noise, Low-Pass and Band-Pass Switched-Capacitor Filters Included, $V_{DD} = 5\text{ V}$	4-229
3.5.8	Absolute Gain Error, $V_{DD} = 5\text{ V}$, $f_s = 8\text{ kHz}$	4-229
3.5.9	Relative Gain and Dynamic Range, $V_{DD} = 5\text{ V}$, $f_s = 8\text{ kHz}$	4-229
3.5.10	Power-Supply Rejection, $V_{DD} = 5\text{ V}$	4-230
3.5.11	Crosstalk Attenuation, $V_{DD} = 5\text{ V}$	4-230
3.5.12	Monitor Output Characteristics, $V_{DD} = 5\text{ V}$	4-231
3.6	Timing Requirements and Specifications in Master Mode	4-232
3.6.1	Recommended Input Timing Requirements for Master Mode, $V_{DD} = 5\text{ V}$	4-242
3.6.2	Operating Characteristics Over Recommended Range of Operating Free-Air Temperature, $V_{DD} = 5\text{ V}$	4-232
3.7	Timing Requirements and Specifications in Slave Mode and Codec Emulation Mode	4-233
3.7.1	Recommended Input Timing Requirements for Slave Mode, $V_{DD} = 5\text{ V}$	4-233
3.7.2	Operating Characteristics Over Recommended Range of Operating Free-Air Temperature, $V_{DD} = 5\text{ V}$	4-233
4	Parameter Measurement Information	4-235
5	Typical Characteristics	4-241
6	Application Information	4-255
A	Primary Control Bits	4-259
B	Secondary Communications	4-261
C	TLC320AC01C/TLC320AC02C Specification Comparisons	4-263
D	Multiple TLC320AC01/TLC320AC02 Analog Interface Circuits on One TMS320C5X DSP Serial Port	4-267

List of Illustrations

<i>Figure</i>	<i>Title</i>	<i>Page</i>
1-1	Control Flow Diagram	4-199
2-1	Functional Sequence for Primary and Secondary Communication	4-205
2-2	Timing Sequence	4-206
2-3	Master and Stand-Alone Functional Sequence	4-216
2-4	Slave and Codec Functional Sequence	4-216
4-1	IN+ and IN- Gain-Control Circuitry	4-235
4-2	AIC Stand-Alone and Master-Mode Timing	4-236
4-3	AIC Slave and Codec Emulation Mode	4-236
4-4	Master or Stand-Alone \overline{FS} and \overline{FSD} Timing	4-237
4-5	Slave \overline{FS} to \overline{FSD} Timing	4-237
4-6	Slave SCLK to \overline{FSD} Timing	4-237
4-7	DOUT Enable Timing From Hi-Z	4-238
4-8	DOUT Delay Timing to Hi-Z	4-238
4-9	EOC Frame Timing	4-238
4-10	Master-Slave Frame-Sync Timing After a Delay Has Been Programmed Into the FSD Registers	4-239
4-11	Master and Slave Frame-Sync Sequence with One Slave	4-239
6-1	Stand-Alone Mode (to DSP Interface)	4-255
6-2	Codec Mode (to DSP Interface)	4-255
6-3	Master With Slave (to DSP Interface)	4-256
6-4	Single-Ended Input (Ground Referenced)	4-256
6-5	Single-Ended to Differential Input (Ground Referenced)	4-257
6-6	Differential Load	4-257
6-7	Differential Output Drive (Ground Referenced)	4-257
6-8	Low-Impedance Output Drive	4-258
6-9	Single-Ended Output Drive (Ground Referenced)	4-258

List of Tables

<i>Table</i>	<i>Title</i>	<i>Page</i>
1-1	Operating Frequencies	4-199
2-1	Master-Slave Selection	4-204
2-2	Sampling Variation With A'	4-213
2-3	Software and Hardware Requests for Secondary Serial-Communication and Phase-Shift Truth Table	4-218
4-1	Gain Control (Analog Input Signal Required for Full-Scale Bipolar A/D-Conversion 2s Complement)	4-235

1 Introduction

The TLC320AC01† analog interface circuit (AIC) is an audio-band processor that provides an analog-to-digital and digital-to-analog input/output interface system on a single monolithic CMOS chip. This device integrates a band-pass switched-capacitor antialiasing input filter, a 14-bit-resolution analog-to-digital converter (ADC), a 14-bit-resolution digital-to-analog converter (DAC), a low-pass switched-capacitor output-reconstruction filter, $(\sin x)/x$ compensation, and a serial port for data and control transfers.

The internal circuit configuration and performance parameters are determined by reading control information into the eight available data registers. The register data sets up the device for a given mode of operation and application.

The major functions of the TLC320AC01 are:

1. To convert audio-signal data to digital format by the ADC channel
2. To provide the interface and control logic to transfer data between its serial input and output terminals and a digital signal processor (DSP) or microprocessor
3. To convert received digital data back to an audio signal through the DAC channel

The antialiasing input low-pass filter is a switched-capacitor filter with a sixth-order elliptic characteristic. The high-pass filter is a single-pole filter to preserve low-frequency response as the low-pass filter cutoff is adjusted. There is a three-pole continuous-time filter that precedes this filter to eliminate any aliasing caused by the filter clock signal.

The output-reconstruction switched-capacitor filter is a sixth-order elliptic transitional low-pass filter followed by a second-order $(\sin x)/x$ correction filter. This filter is followed by a three-pole continuous-time filter to eliminate images of the filter clock signal.

The TLC320AC01 consists of two signal-processing channels, an ADC channel and a DAC channel, and the associated digital control. The two channels operate synchronously; data reception at the DAC channel and data transmission from the ADC channel occur during the same time interval. The data transfer is in 2s-complement format.

There are three basic modes of operation available: the stand-alone analog-interface mode, the master-slave mode, and the linear-codec mode. In the stand-alone mode, the TLC320AC01 generates the shift clock and frame synchronization for the data transfers and is the only AIC used. The master-slave mode has one TLC320AC01 as the master that generates the master-shift clock and frame synchronization; the remaining AICs are slaves to these signals. In the linear-codec mode, the shift clock and the frame-synchronization signals are externally generated and the timing can be any of the standard codec-timing patterns.

Typical applications for this device include modems, speech processing, analog interface for DSPs, industrial-process control, acoustical-signal processing, spectral analysis, data acquisition, and instrumentation recorders.

The TLC320AC01C is characterized for operation from 0°C to 70°C.

† The TLC320AC01 is functionally equivalent to the TLC320AC02 and differs in the electrical specifications as shown in Appendix C.

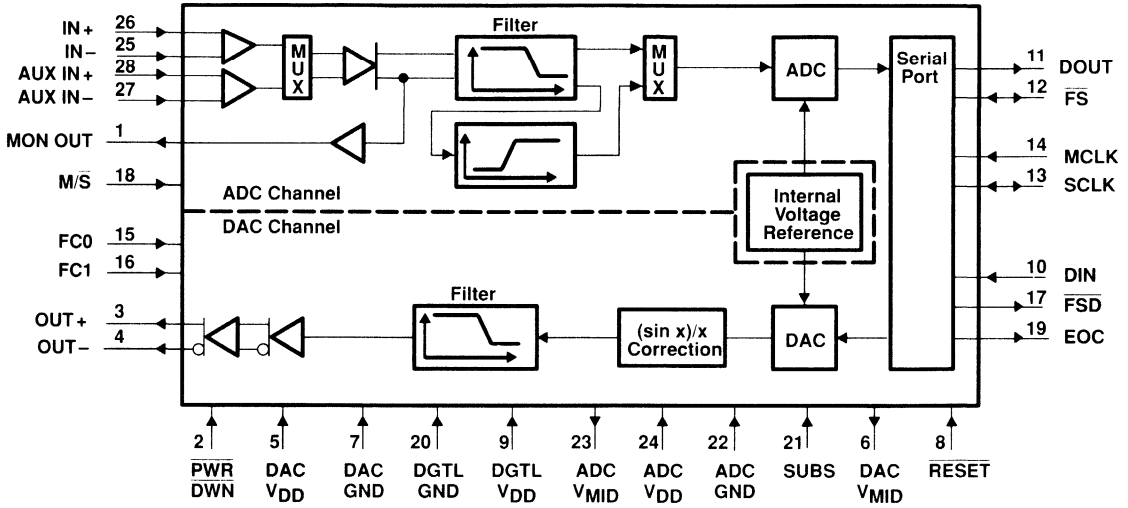
1.1 Features

- General-Purpose Signal-Processing Analog Front End (AFE)
- Single 5-V Power Supply
- Power Dissipation . . . 100 mW Typ
- Signal-to-Distortion Ratio . . . 70 dB Typ
- Programmable Filter Bandwidths (Up to 10.8 kHz) and Synchronous ADC and DAC Sampling
- Serial-Port Interface
- Monitor Output With Programmable Gains of 0 dB, –8 dB, –18 dB, and Squelch
- Two Sets of Differential Inputs With Programmable Gains of 0 dB, 6 dB, 12 dB, and Squelch
- Differential or Single-Ended Analog Output With Programmable Gains of 0 dB, –6 dB, –12 dB, and Squelch
- Differential Outputs Drive 3-V Peak Into a 600- Ω Differential Load
- Differential Architecture Throughout
- 1- μm Advanced LinEPIC™ Process
- 14-Bit Dynamic-Range ADC and DAC
- 2s-Complement Data Format
- Application Report Available†

† Designing with the TLC320AC01 Analog Interface for DSPs (SLAA006)

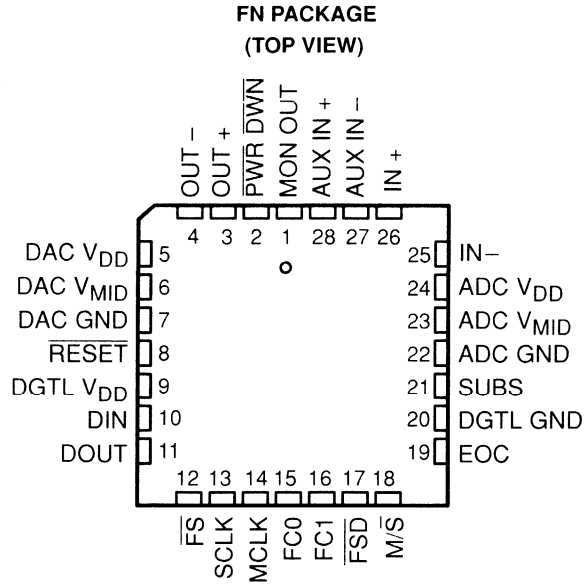
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1.2 Functional Block Diagram

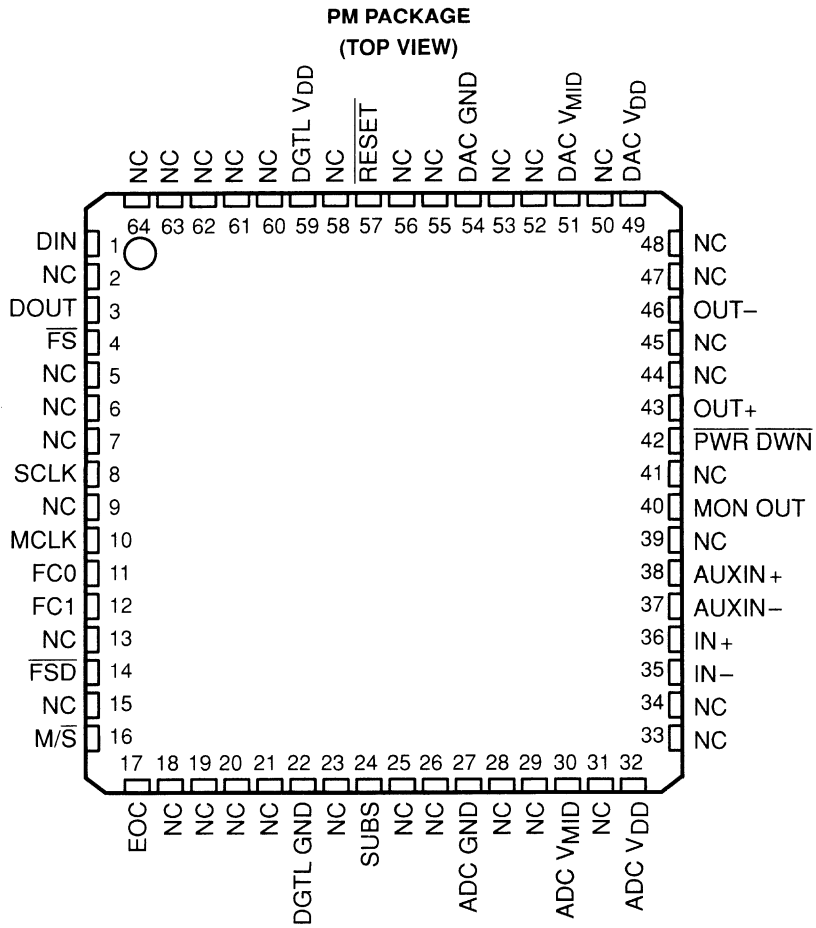


Terminal numbers shown are for the FN package.

1.3 Terminal Assignments



1.3 Terminal Assignments (Continued)



NC – No internal connection

1.4 Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.†	NO.‡		
ADC V _{DD}	24	32	I	Analog supply voltage for the ADC channel
ADC V _{MID}	23	30	O	Midsupply for the ADC channel (requires a bypass capacitor). ADC V _{MID} must be buffered when used as an external reference.
ADC GND	22	27	I	Analog ground for the ADC channel
AUX IN+	28	38	I	Noninverting input to auxiliary analog input amplifier
AUX IN-	27	37	I	Inverting input to auxiliary analog input amplifier
DAC V _{DD}	5	49	I	Digital supply voltage for the DAC channel
DAC V _{MID}	6	51	O	Midsupply for the DAC channel (requires a bypass capacitor). DAC V _{MID} must be buffered when used as an external reference.
DAC GND	7	54	I	Analog ground for the DAC channel
DIN	10	1	I	Data input. DIN receives the DAC input data and command information and is synchronized with SCLK.
DOUT	11	3	O	Data output. DOUT outputs the ADC data results and register read contents. DOUT is synchronized with SCLK.
DGTL V _{DD}	9	59	I	Digital supply voltage for control logic
DGTL GND	20	22	I	Digital ground for control logic
EOC	19	17	O	End-of-conversion output. EOC goes high at the start of the ADC conversion period and low when conversion is complete. EOC remains low until the next ADC conversion period begins and indicates the internal device conversion period.
FC0	15	11	I	Hardware control input. FC0 is used in conjunction with FC1 to request secondary communication and phase adjustments. FC0 should be tied low if it is not used.
FC1	16	12	I	Hardware control input. FC1 is used in conjunction with FC0 to request secondary communication and phase adjustments. FC1 should be tied low if it is not used.
FS	12	4	I/O	Frame synchronization. When FS goes low, DIN begins receiving data bits and DOUT begins transmitting data bits. In master mode, FS is low during the simultaneous 16-bit transmission to DIN and from DOUT. In slave mode, FS is externally generated and must be low for one shift-clock period minimum to initiate the data transfer.
FSD	17	14	O	Frame-synchronization delayed output. This active-low output synchronizes a slave device to the frame synchronization timing of the master device. FSD is applied to the slave FS input and is the same duration as the master FS signal but delayed in time by the number of shift clocks programmed in the FSD register.
IN+	26	36	I	Noninverting input to analog input amplifier
IN-	25	35	I	Inverting input to analog input amplifier
MCLK	14	10	I	The master-clock input drives all the key logic signals of the AIC.
MON OUT	1	40	O	The monitor output allows monitoring of analog input and is a high-impedance output.
M/S	18	16	I	Master/slave select input. When M/S is high, the device is the master and when low, it is a slave.

† Terminal numbers shown are for the FN package.

‡ Terminal numbers shown are for the PM package.

1.4 Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.†	NO.‡		
OUT+	3	43	O	Noninverting output of analog output power amplifier. OUT+ can drive transformer hybrids or high-impedance loads directly in a differential connection or a single-ended configuration with a buffered VMID.
OUT-	4	46	O	Inverting output of analog output power amplifier. OUT- is functionally identical with and complementary to OUT+.
PWR DWN	2	42	I	Power-down input. When PWR DWN is taken low, the device is powered down such that the existing internally programmed state is maintained. When PWR DWN is brought high, full operation resumes.
RESET	8	57	I	Reset input that initializes the internal counters and control registers. RESET initiates the serial data communications, initializes all of the registers to their default values, and puts the device in a preprogrammed state. After a low-going pulse on RESET, the device registers are initialized to provide a 16-kHz data-conversion rate and 7.2-kHz filter bandwidth for a 10.368-MHz master clock input signal.
SCLK	13	8	I/O	Shift clock. SCLK clocks the digital data into DIN and out of DOUT during the frame-synchronization interval. When configured as an output (M/S high), SCLK is generated internally by dividing the master clock signal frequency by four. When configured as an input (M/S low), SCLK is generated externally and synchronously to the master clock. This signal clocks the serial data into and out of the device.
SUBS	21	24	I	Substrate connection. SUBS should be tied to ADC GND.

† Terminal numbers shown are for the FN package.

‡ Terminal numbers shown are for the PM package.

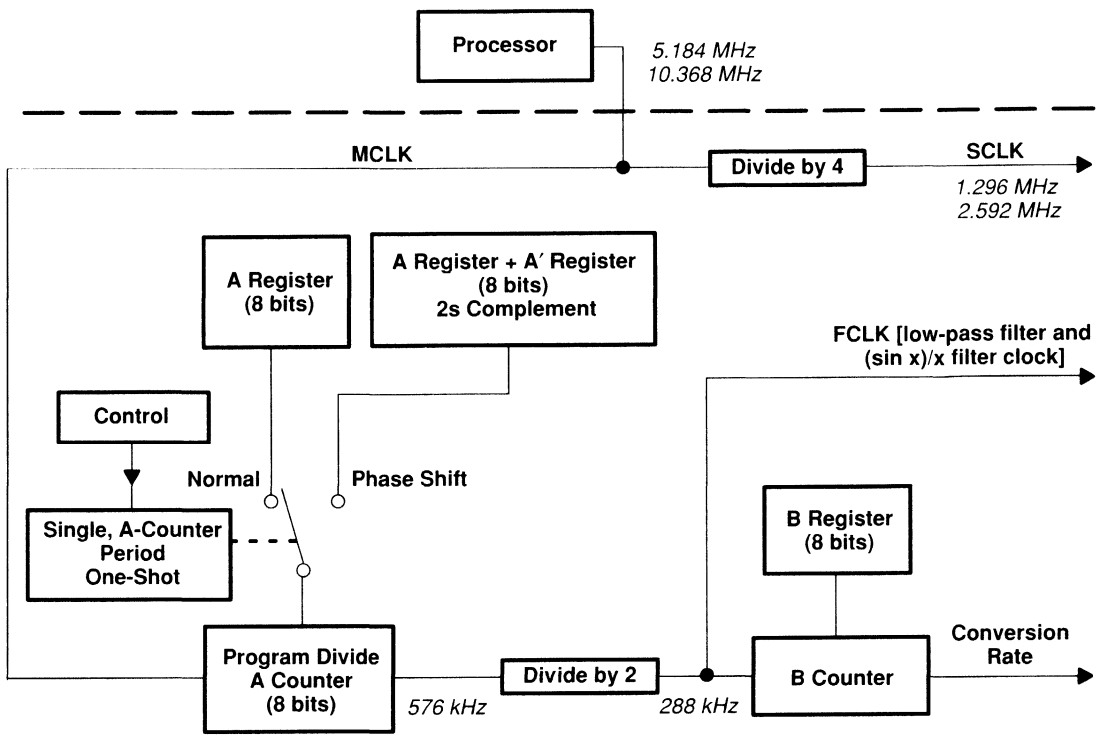


Figure 1-1. Control Flow Diagram

Table 1-1. Operating Frequencies

FCLK (kHz)	LOW-PASS FILTER BANDWIDTH (kHz)	B REGISTER CONTENTS (Program No. of Filter Clocks) (Decimal)	CONVERSION RATE (kHz)	HIGH-PASS POLE FREQUENCY (Hz)
144	3.6	20 (see Note 1)	7.2	36
		18	8	40
		15	9.6	48
		10 (see Note 2)	14.4	72
288	7.2	20 (see Note 1)	14.4	72
		18	16	80
		15	19.2	96
		10 (see Notes 2 and 3)	28.8	144
432	10.8	20 (see Note 1)	21.6	108
		18	24	120
		15 (see Note 3)	28.8	144
		10 (see Notes 2 and 3)	43.2	216

- NOTES: 1. The B register can be programmed for values greater than 20; however, since the sample rate is lower than 7.2 kHz and the internal filter remains at 3.6 kHz, an external antialiasing filter is required.
2. When the B register is programmed for a value less than 10, the ADC and the DAC conversions are not completed before the next frame-sync signal and the results are in error.
3. The maximum sampling rate for the ADC channel is 43.2 kHz. The maximum rate for the DAC channel is 25 kHz.

1.5 Register Functional Summary

There are nine data registers that are used as follows:

- Register 0 The No-op register. The 0 address allows phase adjustments to be made without reprogramming a data register.
- Register 1 The A register controls the count of the A counter.
- Register 2 The B register controls the count of the B counter.
- Register 3 The A' register controls the phase adjustment of the sampling period. The adjustment is equal to the register value multiplied by the input master period.
- Register 4 The amplifier gain register controls the gains of the input, output, and monitor amplifiers.
- Register 5 The analog configuration register controls:
- The addition/deletion of the high-pass filter to the ADC signal path
 - The enable/disable of the analog loopback
 - The selection of the regular inputs or auxiliary inputs
 - The function that allows processing of signals that are the sum of the regular inputs and the auxiliary inputs ($V_{IN} + V_{AUX IN}$)
- Register 6 The digital configuration register controls:
- Selection of the free-run function
 - \overline{FSD} [frame-synchronization (sync) delay] output enable/disable
 - Selection of 16-bit function
 - Forcing secondary communications
 - Software reset
 - Software power down
- Register 7 The frame-sync delay register controls the time delay between the master-device frame sync and slave-device frame sync. Register 7 must be the last register programmed when using slave devices since all register data is latched and valid on the sixteenth falling edge of SCLK. On the sixteenth falling edge of SCLK, all delayed frame-sync intervals are shifted by this programmed amount.
- Register 8 The frame-sync number register informs the master device of the number of slaves that are connected in the chain. The frame-sync number is equal to the number of slaves plus one.

2 Detailed Description

2.1 Definitions and Terminology

ADC Channel	All signal processing circuits between the analog input and the digital conversion results at DOUT
Codec Mode	The operating mode under which the device receives shift clock and frame-sync signals from a host processor. The device has no slaves.
d	The d represents valid programmed or default data in the control register format (see Section 2.19) when discussing other data-bit portions of the register.
Dxx	Bit position in the primary data word (xx is the bit number)
DAC Channel	All signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUT+ and OUT–
Data Transfer Interval	The time during which data is transferred from DOUT and to DIN. This interval is 16 shift clocks regardless of whether the shift clock is internally or externally generated. The data transfer is initiated by the falling edge of the frame-sync signal.
DSxx	Bit position in the secondary data word (xx is the bit number)
FCLK	An internal clock frequency that is a division of MCLK that controls the low-pass filter and (sinx)/x filter clock (see Figure 1–1 and Table 1-1).
f _i	The analog input frequency of interest
Frame Sync	The falling edge of the signal that initiates the data-transfer interval. The primary frame sync starts the primary communications, and the secondary frame sync starts the secondary communications.
Frame Sync and Sampling Period	The time between falling edges of successive primary frame-sync signals
Frame-Sync Interval	The time period occupied by 16 shift clocks. Regardless of the mode of operation, there is always an internal frame-sync interval signal that goes low on the rising edge of SCLK and remains low for 16 shift clocks. It is used for synchronization of the serial-port internal signals. It goes high on the seventeenth rising edge of SCLK.
f _s	The sampling frequency that is the reciprocal of the sampling period.
Host	Any processing system that interfaces to DIN, DOUT, SCLK, or \overline{FS} .
Master Mode	The operating mode under which the device generates and uses its own shift clock and frame-sync signal and generates all delayed frame-sync signals necessary to support slave devices.
Phase Adjustment	The programmed time variation from the falling edge of one frame-sync signal to the falling edge of the next frame sync signal. The time variation is determined by the contents of the A' register. Since the time between falling edges of successive frame-sync signals is the the sampling period, the sampling period is adjusted.
Primary (Serial) Communications	The digital data-transfer interval. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.
Secondary (Serial) Communications	The digital control and configuration data-transfer interval into DIN and the register read-data cycle from DOUT. The data-transfer interval occurs when requested by hardware or software.
Signal Data	The input signal and all of the converted representations through the ADC channel and return through the DAC channel to the analog output. This is contrasted with the purely digital software-control data.
Slave Mode	The operating mode under which the device receives shift clock and frame-sync signals from a master device.

- Stand-Alone Mode The operating mode under which the device generates and uses its own shift clock and frame-synch signal. The device has no slave devices.
- X The X represents a don't-care bit position within the control register format.

2.2 Reset and Power-Down Functions

2.2.1 Reset

The TLC320AC01 resets both the internal counters and registers, including the programmed registers, by any of the following:

- Applying power to the device, causing a power-on reset (POR)
- Applying a low reset pulse to $\overline{\text{RESET}}$
- Reading in the programmable software reset bit (DS01 in register 6)

$\overline{\text{PWR DWN}}$ resets the counters only and preserves the programmed register contents.

2.2.2 Conditions of Reset

The two internal reset signals used for the reset and synchronization functions are as follows:

1. Counter reset: This signal resets all flip-flops and latches that are not externally programmed with the exception of those generating the reset pulse itself. In addition, this signal resets the software power-down bit.

$$\text{Counter reset} = \text{power-on reset} + \overline{\text{RESET}} + \text{RESET bit} + \overline{\text{PWR DWN}}$$

2. Register reset: This signal resets all flip-flops and latches that are not reset by the counter reset except those generating the reset pulse itself.

$$\text{Register reset} = \text{power-on reset} + \overline{\text{RESET}} + \text{RESET bit}$$

Both reset signals are at least one master-clock period long and release on the falling edge of the master clock.

2.2.3 Software and Hardware Power-Down

Given the definitions and conditions of $\overline{\text{RESET}}$, the software-programmed power-down condition is cleared by resetting the software bit (DS00 in register 6) to zero. It is also cleared by either cycling the power to the device, bringing $\overline{\text{PWR DWN}}$ low, or bringing $\overline{\text{RESET}}$ low.

$\overline{\text{PWR DWN}}$ powers down the entire chip (< 1 mA). The software-programmable power-down bit only powers down the analog section of the chip (< 3 mA), which allows a software power-up function. Cycling $\overline{\text{PWR DWN}}$ high to low and back to high resets all flip-flops and latches that are not externally programmed, thereby preserving the register contents.

When $\overline{\text{PWR DWN}}$ is not used, it should be tied high.

2.2.4 Register Default Values After POR, Software Reset, or $\overline{\text{RESET}}$ Is Applied

Register 1 – The A Register

The default value of the A-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

Register 2 – The B Register

The default value of the B-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

Register 3 – The A' Register

The default value of the A'-register data is decimal 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

Register 4 – The Amplifier Gain-Select Register

The default value of the amplifier gain-select register data is shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	1	0	1

Register 5 – The Analog Control-Configuration Register

The power-up and reset conditions are as shown below. In the read mode, 8 bits are read but the 4 LSBs are repeated as the 4 MSBs.

DS03	DS02	DS01	DS00
0	0	0	1

Register 6 – The Digital Configuration Register

The default value of DS07 – DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

Register 7 – The Frame-Sync Delay Register

The default value of DS07 – DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

Register 8 – The Frame-Sync Number Register

The default value of DS07 – DS00 is 1 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	1

2.3 Master-Slave Terminal Function

Table 2–1 describes the function of the master/slave (M/\overline{S}) input. The only difference between master and slave operations in the TLC320AC01 is that SCLK and \overline{FS} are outputs when M/\overline{S} is high and inputs when M/\overline{S} is low.

Table 2–1. Master-Slave Selection

MODE	M/\overline{S}^\dagger	\overline{FS}	SCLK
Master and Stand Alone	H	Output	Output
Slave and Codec Emulation	L	Input	Input

[†] When the stand-alone mode is desired or when the device is permanently in the master mode, M/\overline{S} must be high.

2.4 ADC Signal Channel

To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data. The signal is amplified by the input amplifier at one of three software-selectable gains (typically 0 dB, 6 dB, or 12 dB). A squelch mode can also be programmed for the input amplifier.

The amplifier output is filtered and applied to the ADC input. The ADC converts the signal into discrete digital words in 2s-complement format corresponding to the analog-signal value at the sampling time. These 16-bit digital words, representing sampled values of the analog input signal, are clocked out of the serial port (DOUT), one word for each primary communication interval. During secondary communications, the data previously programmed into the registers can be read out with the appropriate register address and with the read bit set to 1. When a register read is not requested, all 16 bits are 0.

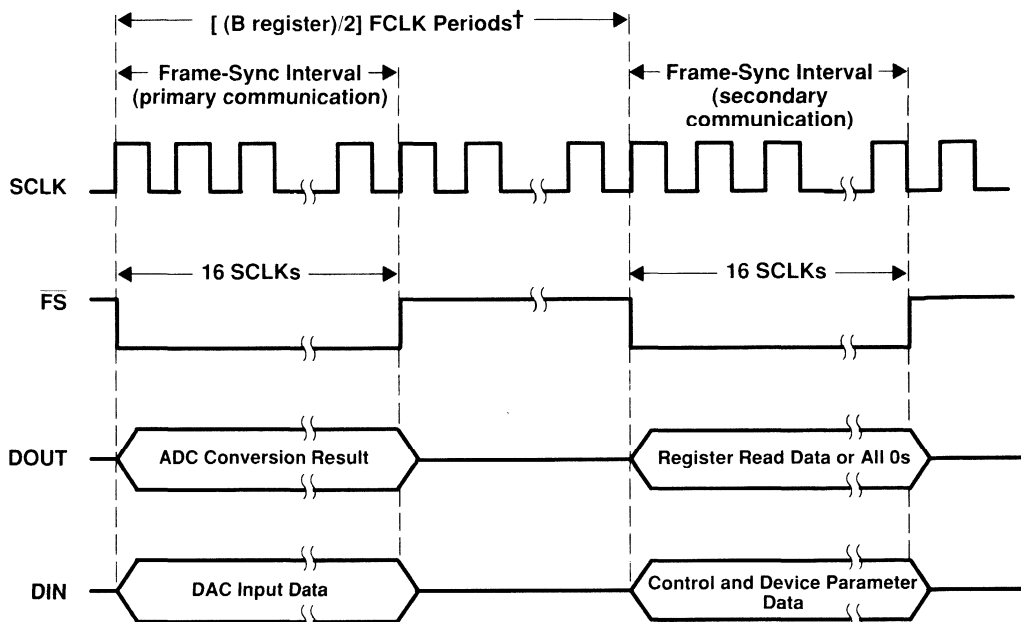
2.5 DAC Signal Channel

DIN receives the 16-bit serial data word (2s complement) from the host during the primary communications interval and latches the data on the seventeenth rising edge of SCLK. The data are converted to an analog voltage by the DAC with a sample and hold and then through a $(\sin x)/x$ correction circuit and a smoothing filter. An output buffer with three software-programmable gains (0 dB, –6 dB, and –12 dB), as shown in register 4, drives the differential outputs OUT+ and OUT–. A squelch mode can also be programmed for the output buffer. During secondary communications, the configuration program data are read into the device control registers.

2.6 Serial Interface

The digital serial interface consists of the shift clock, the frame-synchronization signal, the ADC-channel data output, and the DAC-channel data input. During the primary 16-bit frame-synchronization interval, the SCLK transfers the ADC channel results from DOUT and transfers 16-bit DAC data into DIN.

During the secondary frame-synchronization interval, the SCLK transfers the register read data from DOUT when the read bit is set to a 1. In addition, the SCLK transfers control and device parameter information into DIN. The functional sequence is shown in Figure 2–1.



† The time between the primary and secondary frame sync is the time equal to filter clock (FCLK) period multiplied by the B-register contents divided by two. The time interval is rounded to the nearest shift clock. The secondary frame-sync signal goes from high to low on the next shift clock low-to-high transition after (B register/2) filter clock periods.

Figure 2–1. Functional Sequence for Primary and Secondary Communication

2.7 Number of Slaves

The maximum number of slaves is determined by the sum of the individual device delays from the frame-sync (\overline{FS}) input low to the frame-sync delayed (FSD) low for all slaves according to equation 1:

$$(n) / tp(FS-FSD) < 1/2 \text{ shift-clock period} \quad (1)$$

Where:

n is the number of slave devices.

Example:

From equation 1 above, the number of slaves is given by equation 2:

$$(n) \leq \frac{1}{2} \times (\text{SCLK period}) \times \frac{1}{tp(FS - FSD)} \quad (2)$$

assuming the master clock is 10.368 MHz and the shift clock is 2.5965 MHz and $tp(FS - FSD)$ is 40 ns, then according to equation 3, the number of slaves is:

$$n \leq \frac{1}{2.5965 \text{ MHz}} \times \frac{1}{2} \times \frac{1}{40 \text{ ns}} = \frac{1000}{192} = 4.8 \quad (3)$$

The maximum number of slaves under these conditions is four.

2.8 Required Minimum Number of MCLK Periods

Master with slave operation is summarized in the following sections.

2.8.1 TLC320AC01 AIC Master-Slave Summary

After initial setup and the master and slave frame syncs are separated, when secondary communication is needed for a slave device, a 11 must be placed in the 2 LSBs of each primary data word for all devices in the system, master and slave, by the host processor. In other words, all AICs must receive secondary frame requests.

The host processor must issue the command by setting D01 and D00 to a 1 in the primary frame sync data word of all devices. Then the master generates the master primary frame sync and, after the number of shift clocks set by the FSD register value, the slave primary frame sync intervals. Then, after (B register value/2) FCLK periods, the master secondary frame sync occurs first, and then the slave secondary frame sync occurs. These are also rippled through the slave devices.

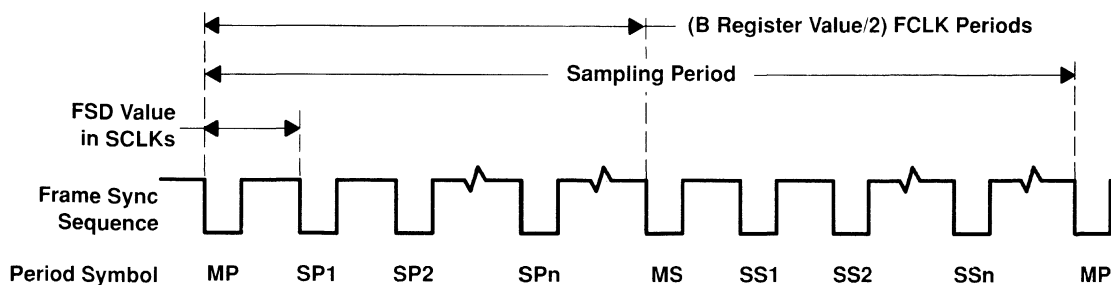
In other words, when a secondary communications interval is requested by the host processor as described above:

1. The master outputs the master primary frame sync interval, and then the slave primary frame sync intervals after the FSD register value number of shift clocks.
2. After (B register value/2) FCLK periods, the master then outputs the master secondary frame sync interval, and after the FSD register value number of shift clocks, the slave secondary frame sync intervals.

This sequence is shown in Figure 2–2.

The host must keep track of whether the master or a slave is then being addressed and also the number of slave devices. The master always outputs a 00 in the last 2 bits of the DOUT word, and a slave always outputs a 1 in the LSB of the DOUT word. This information allows the system to recognize a starting point by interrogating the least significant bit of the DOUT word. If the LSB is 0, then that device is the master, and the system is at the starting point.

Note: This identification always happens except in 16-bit mode when the 2 LSBs are not available for identification purposes.



Periods shown: Each period must be a minimum of 16 SCLKs plus 2 additional SCLKs

MP	= Master Primary Period	MS	= Master Secondary Period
SP1	= 1st Slave Primary Period	SS1	= 1st Slave Secondary Period
SP2	= 2nd Slave Primary Period	SS2	= 2nd Slave Secondary Period
SPn	= nth Slave Primary Period	SSn	= nth Slave Secondary Period

Figure 2–2. Timing Sequence

2.8.2 Notes on TLC320AC01/02 AIC Master-Slave Operation

Master/slave operational detail is summarized in the following notes:

1. The slave devices can be programmed independently of the master as long as the clock divide register numbers are not changed. The gain settings, for example, can be changed independently.
2. The method that is used to program a slave independently is to request a secondary communication of the master and all slaves and ripple the delayed frame sync to the desired slave device to be programmed.
3. Secondary frame syncs must be requested for all devices in the system or none. This is required so that the master generates secondary frames for the slaves and allows the slaves to know that the second frame syncs they receive are secondary frame syncs. Each device in the system must receive a secondary frame request in its corresponding primary frame sync period (11 in the last 2 LSBs).
4. Calculation of the sampling frequency in terms of the master clock and the shift clock and the respective register ratios is (see equations 4–6):

$$\begin{aligned} \text{Sampling frequency} = f_s &= \frac{FCLK}{B \text{ register value}} \\ &= \frac{f(\text{MCLK})}{2 (A \text{ register value}) \times (B \text{ register value})} \end{aligned} \quad (4)$$

Therefore,

$$\frac{f(\text{MCLK})}{f_s} = 2 \times (A \text{ register value}) \times (B \text{ register value}) \quad (5)$$

and in terms of the shift clock frequency, since

$$f(\text{MCLK}) = 4 \times f(\text{SCLK})$$

then

$$\begin{aligned} \frac{f(\text{SCLK})}{f_s} &= \frac{(A \text{ register value}) \times (B \text{ register value})}{2} \\ &= \frac{\text{Number of SCLK periods}}{\text{Sampling period}} \end{aligned} \quad (6)$$

5. The minimum number of shift clocks between falling edges of any two frame syncs is 18 because the frame sync delay register minimum number is 18.

When a secondary communication is requested by the host, the master secondary frame sync begins at the middle of the sampling period (followed by the slave secondary frame syncs), so all primary frame sync intervals (master and slave) must occur within one-half the sampling time.

The first secondary frame-sync falling edge, therefore, occurs at the following time (see equation 7):

$$\begin{aligned} \text{Time to first secondary frame sync} &= \frac{\text{B register value}}{2} \text{ (FCLK periods)} = \\ &\text{A register value} \times \text{B register value (number of MCLK periods)} = \\ &\frac{\text{A register value} \times \text{B register value}}{4} \text{ (number of SCLK periods)} \end{aligned} \quad (7)$$

6. Number of frame sync intervals using equation 8.

All master and slave primary frame sync intervals must occur within the time of equation 7.

Since 18 shift clocks are required for each frame sync interval, then the number of frame sync intervals from equation 8 is:

$$\begin{aligned} \text{Number of frame sync intervals} &= \frac{\text{A register value} \times \text{B register value}}{4 \times 18 \text{ (SCLKs/frame sync interval)}} \\ &= \frac{\text{A register value} \times \text{B register value}}{72} \end{aligned} \quad (8)$$

7. Number of devices, master and slave, in terms of $f(\text{MCLK})$ and f_s .

Substituting the value from equation 5 for the $A \times B$ register value product gives the total number of devices, including the master and all slaves that can be used, for a given master clock and sampling frequency. Therefore, using equation 9:

$$\text{Number of devices} = \frac{f(\text{MCLK})}{144 \times f_s} \quad (9)$$

8. Number of devices, master and slave, if slave devices are reprogrammed.

Equation 9 does not include reprogramming the slave devices after the frame sync delay occurs. So if programming is required after shifting the slave frame syncs by the FSD register, then the total number of devices is given by equation 10 is:

$$\text{Number of devices} = \frac{f(\text{MCLK})}{288 \times f_s} \quad (10)$$

9. Example of the maximum number of devices if the slave devices are reprogrammed assuming the following values:

$$f(\text{MCLK}) = 10.368 \text{ MHz}, f_s = 8 \text{ kHz}$$

then from equation 10,

$$\text{Maximum number of devices} = \frac{10.368 \text{ MHz}}{288 (8 \text{ kHz})} = 4.5$$

therefore, one master and three slaves can be used.

2.9 Operating Frequencies

2.9.1 Master and Stand-Alone Operating Frequencies

The sampling (conversion) frequency is derived from the master-clock (MCLK) input by equation 11:

$$f_s = \text{Sampling (conversion) frequency} = \frac{\text{MCLK}}{(\text{A register value}) \times (\text{B register value}) \times 2} \quad (11)$$

The inverse is the time between the falling edges of two successive primary frame-synchronization signals. The input and output data clock (SCLK) frequency is given in equation 12:

$$\text{SCLK frequency} = \frac{\text{MCLK frequency}}{4} \quad (12)$$

2.9.2 Slave and Codec Operating Frequencies

The slave operating frequencies are either the default values or programmed by the control data word from the master and codec conversion and the data frequencies are determined by the externally applied SCLK and FS signals.

2.10 Switched-Capacitor Filter Frequency (FCLK)

The filter clock (FCLK) is an internal clock signal that determines the filter band-pass frequency and is the B counter clock. The frequency of the filter clock is derived by equation 13:

$$\text{FCLK} = \frac{\text{MCLK}}{(\text{A register value}) \times 2} \quad (13)$$

2.11 Filter Bandwidths

The low-pass (LP) filter –3 dB corner is derived in equation 14:

$$f(\text{LP}) = \frac{\text{FCLK}}{40} = \frac{\text{MCLK}}{40 \times (\text{A register value}) \times 2} \quad (14)$$

The high-pass (HP) filter –3 dB corner is derived in equation 15:

$$f(\text{HP}) = \frac{\text{Sampling frequency}}{200} = \frac{\text{MCLK}}{200 \times 2 \times (\text{A register value}) \times (\text{B register value})} \quad (15)$$

2.12 Master and Stand-Alone Modes

The difference between the master and stand-alone modes is that in the stand-alone mode there are no slave devices. Functionally these two modes are the same. In both, the AIC internally generates the shift clock and frame-sync signal for the serial communications. These signals and the filter clock (FCLK) are derived from the input master clock. The master clock applied at the MCLK input determines the internal device timing. The shift clock frequency is a divide-by-four of the master clock frequency and shifts both the input and output data at DIN and DOUT, respectively, during the frame-sync interval (16 shift clocks long). To begin the communication sequence, the device is reset (see Section 2.2.1), and the first frame sync occurs approximately 648 master clocks after the reset condition disappears.

2.12.1 Register Programming

All register programming occurs during secondary communications, and data is latched and valid on the sixteenth falling edge of SCLK. After a reset condition, eight primary and secondary communications cycles are required to set up the eight programmable registers. Registers 1 through 8 are programmed in secondary communications intervals 1 through 8, respectively. If the default value for a particular register is desired, that register does not need to be addressed during the secondary communications. The no-op command addresses the pseudo-register (register 0), and no register programming takes place during this communications. The no-op command allows phase shifts of the sampling period without reprogramming any register.

During the eight register programming cycles, DOUT is in the high-impedance state. DOUT is released on the rising edge of the eighth primary internal frame-sync interval. In addition, each register can be read back

during DOUT secondary communications by setting the read bit to 1 in the appropriate register. Since the register is in the read mode, no data can be written to the register during this cycle. To return this register to the write mode requires a subsequent secondary communication (see Section 2.19 for detailed register description).

2.12.2 Master and Stand-Alone Functional Sequence

The A counter counts according to the contents of the A register, and the A counter frequency is divided by two to produce the filter clock (FCLK). The B counter is clocked by FCLK with the following functional sequence:

1. The B counter starts counting down from the B register value minus one. Each count remains in the counter for one FCLK period including the zero count. This total counter time is referred to as the B cycle. The end of the zero count is called the end of B cycle.
2. When the B counter gets to a count of nine, the analog-to-digital (A-to-D) conversion starts.
3. The A-to-D conversion is complete ten FCLK periods later.
4. \overline{FS} goes low on a rising edge of SCLK after the A-to-D conversion is complete. That rising edge of SCLK must be preceded by a falling edge of SCLK, which is the first falling edge to occur after the end of B cycle.
5. The D-to-A conversion cycle begins on the rising edge of the internal frame-sync interval and is complete ten FCLK periods later.

2.13 Slave and Codec Modes

The only difference between the slave and codec modes is that the codec mode is controlled directly by the host and does not use a delayed frame-sync signal. In both modes, the shift clock and the frame sync are both externally generated and must be synchronous with MCLK. The conversion frequency is set by the time interval of externally applied frame-sync falling edges except when the free-run function is selected by bit 5 of register 6 (see Section 2.15.4). The slave device or devices share the shift clock generated by the master device but receive the frame sync from the previous slave in the chain. The Nth slave \overline{FS} receives the (N-1)st slave \overline{FSD} output and so on. The first slave device in the chain receives \overline{FSD} from the master.

2.13.1 Slave and Codec Functional Sequence

The A counter counts according to the contents of the A register, and the A counter frequency is divided by two to produce the FCLK. The device function in the slave or codec mode is the same as steps 1 through 3 of the B cycle description in the master mode but differs as follows:

1. Same as master
2. Same as master
3. Same as master
4. All internal clocks stop 1/2 FCLK before the end of count 0 in the B counter cycle.
5. All internal clocks are restarted on the first rising edge of MCLK after the external \overline{FS} input goes low. This operation provides the synchronization necessary when using an external \overline{FS} signal.
6. The D-to-A conversion starts on the rising edge of the internally generated frame-sync interval at the end of the 16-shift clock data transfer.

In the slave mode, the master controls the phase adjustments for itself and all slaves since all devices are programmed in the same frame-sync interval. In the codec mode, the shift clock and frame sync are externally generated and provide the timing for the ADC and DAC if the free-run function has not been selected (see Subsection 2.15.4). In the codec mode, there is usually no need for phase adjustments; however, any required phase adjustments must be made by adjusting the external frame-sync timing (sampling time).

2.13.2 Slave Register Programming

When slave devices are used on power-up or reset, all slave frame-sync signals occur at the same time as the master frame-sync signal and all slave devices are programmed during the master secondary frame-sync interval with the same data as the master. The last register programmed must be the frame-sync delay (FSD) register because the delay starts immediately on the rising edge of the seventeenth shift clock of that frame-sync interval. After the FSD register programming is completed for the master and slave, the slave primary frame interval is shifted in time (time slot allocated) according to the data contained in the slave FSD registers. The master then generates frame-sync intervals for itself and each slave to synchronize the host serial port for data transfers for itself and all slave devices.

The number of slaves is specified in the FSN register (register 8); therefore, the number of frame-sync intervals generated by the master is equal to the number of slaves plus one (see Section 2.7). These master frame-sync intervals are separated in time by the delay time specified by the FSD register (register 7). These master-generated intervals are the only frame-sync interval signals applied to the host serial port to provide the data-transfer time slot for the slave devices.

2.14 Terminal Functions

2.14.1 Frame-Sync Function

The frame-sync signal indicates that the device is ready to send and receive data for both master and slave modes. The data transfer begins on the falling edge of the frame-sync signal.

2.14.1.1 Frame Sync (\overline{FS}), Master Mode

The frame sync is generated internally. \overline{FS} goes low on the rising edge of SCLK and remains low for the 16-bit data transfer. In addition to generating its own frame-sync interval, the master also outputs a frame sync for each slave that is being used.

2.14.1.2 Frame-Sync Delayed ($\overline{\text{FSD}}$), Master Mode

For the master, the frame-sync delayed output occurs 1/2 shift-clock period ahead of $\overline{\text{FS}}$ to compensate for the time delay through the master and slave devices. The timing relationships are as follows:

1. When the FSD register data is 0, then $\overline{\text{FSD}}$ goes low on the falling edge of SCLK prior to the rising edge of SCLK when $\overline{\text{FS}}$ goes low (see Figure 4–4).
2. When the FSD register data is greater than 17, then $\overline{\text{FSD}}$ goes low on a rising edge of SCLK that is the FSD register number of SCLKs after the falling edge of $\overline{\text{FS}}$.

Register data values from 1 to 17 should not be used.

2.14.1.3 Frame Sync ($\overline{\text{FS}}$), Slave Mode

The frame-sync timing is generated externally, applied to $\overline{\text{FS}}$, and controls the ADC and DAC timing (see Subsection 2.15.4). The external frame-sync width must be a minimum of one shift clock to be recognized and can remain low until the next data frame is required.

2.14.1.4 Frame-Sync Delayed ($\overline{\text{FSD}}$), Slave Mode

This output is fed from the master to the first slave and the first slave $\overline{\text{FSD}}$ output to the second and so on down the chain. The FSD timing sequence in the slave mode is as follows:

1. When the FSD register data is 0, then $\overline{\text{FSD}}$ goes low after $\overline{\text{FS}}$ goes low (see Figure 4–5).
2. When the FSD register data is greater than 17, $\overline{\text{FSD}}$ goes low on a rising edge of SCLK that is the FSD register number of SCLKs after the falling edge of $\overline{\text{FS}}$.

Data values from 1 to 17 should not be used.

2.14.2 Data Out (DOUT)

DOUT is placed in the high-impedance state on the seventeenth rising edge of SCLK (internal or external) after the falling edge of frame sync. In the primary communication, the data word is the ADC conversion result. In the secondary communication, the data is the register read results when requested by the read/write (R/W) bit with the eight MSBs set to 0 (see Section 2.16). If no register read is requested, the secondary word is all zeroes.

2.14.2.1 Data Out, Master Mode

In the master mode, DOUT is taken from the high-impedance state by the falling edge of frame sync. The most significant data bit then appears on DOUT.

2.14.2.2 Data Out, Slave Mode

In the slave mode, DOUT is taken from the high-impedance state by the falling edge of the external frame sync or the rising edge of the external SCLK, whichever occurs first (see Figure 4–7). The falling edge of frame sync can occur $\pm 1/4$ SCLK period around the SCLK rising edge (see Figure 4–3). The most significant data bit then appears on DOUT.

2.14.3 Data In (DIN)

In the primary communication, the data word is the digital input signal to the DAC channel. In the secondary communication, the data is the control and configuration data to set up the device for a particular function (see Section 2.16).

2.14.4 Hardware Program Terminals (FC1 and FC0)

These inputs provide for hardware programming requests for secondary communication or phase adjustment. These inputs work in conjunction with the control bits D01 and D00 of the primary data word or control bits DS15 and DS14 of the secondary data word. The data on FC1 and FC0 are latched on the rising edge of the next internally generated primary or secondary frame-sync interval. These inputs should be tied low if not used (see Section 2.17 and Table 2–3).

2.14.5 Midpoint Voltages (ADC V_{MID} and DAC V_{MID})

Since the device operates at a single-supply voltage, two midpoint voltages are generated for internal signal processing. ADC V_{MID} is used for the ADC channel reference, and DAC V_{MID} is used for the DAC channel reference. Two references minimize channel-to-channel noise and crosstalk. ADC V_{MID} and DAC V_{MID} must be buffered when used as a reference for external signal processing.

2.15 Device Functions

2.15.1 Phase Adjustment

In some applications, such as modems, the device sampling period may require an adjustment to synchronize with the incoming bit stream to improve the signal-to-noise ratio. The TLC320AC01 can adjust the sampling period through the use of the A' register and the control bits.

2.15.1.1 Phase-Adjustment Control

A phase adjustment is a programmed variation in the sampling period. A sampling period is adjusted according to the data value in the A' register, and the phase adjustment is that number of master clocks (MCLK). An adjustment is made during device operation with data bits D01 and D00 in the primary communication, with data bits DS15 and DS14 in the secondary word or in combination with the hardware terminals FC1 and FC0 (see Table 2–3). This adjustment request is latched on the rising edge of the next internal frame-sync interval and is only valid for the next sampling period. To repeat the phase adjustment, another phase request must be initiated.

2.15.1.2 Use of the A' Register for Phase Adjustment

The A' register value makes slight timing adjustments to the sampling period. The sampling period increases or decreases according to the sign of the programmed A' register value and the state of data bits D01 and D00 in the primary data word.

The general equation for the conversion frequency is given in equation 16:

$$f_s = \text{conversion frequency} = \frac{\text{MCLK}}{(2 \times \text{A register value} \times \text{B register value}) \pm (\text{A' register value})} \quad (16)$$

Therefore, if A' = 0, the device conversion (sampling) frequency and period is constant.

If a nonzero A' value is programmed, the sampling frequency and period responds as shown in Table 2–2.

Table 2–2. Sampling Variation With A'

D01	D00	SIGN OF THE A' REGISTER VALUE	
		PLUS VALUE (+)	NEGATIVE VALUE (-)
0	1 (increase command)	Frequency decreases, period increases	Frequency increases, period decreases
1	0 (decrease command)	Frequency increases, period decreases	Frequency decreases, period increases

An adjustment to the sampling period, which must be requested through D01 and D00 of the primary data word to DIN, is valid for the following sampling period only. When the adjustment is required for the subsequent sampling period, it must be requested again through D01 and D00 of the primary data word. For each request, only the sampling period occurring immediately after the primary data word request is affected.

The amount of time shift in the entire sampling period ($1/f_s$) is as follows:

When the sampling period is set to 125 μ s (8 kHz), the A' register is loaded with decimal 10 and the TLC320AC01 master clock frequency is 10.386 MHz. The amount of time each sampling period is increased or decreased, when requested, is given in equation 17:

$$\text{Time shift} = (\text{A' register value}) \times (\text{MCLK period}) \quad (17)$$

The device changes the entire sampling period by only the MCLK period times the A' register value as given in equation 18:

$$\begin{aligned} \text{Change in sampling period} &= \text{contents of A' register} \times \text{master clock period} \\ &= 10 \times 96.45 \text{ ns} = 964 \text{ ns (less than 1\% of the sampling period)} \end{aligned} \quad (18)$$

The sampling period changes by 964.5 ns each time the phase adjustment is requested by the primary data word (i.e., once per sampling period).

It is evident then that the change in sampling period is very small compared to the sampling period. To observe this effect over a long period of time ($>$ sampling period), this change must be continuously requested by the primary data word. If the adjustment is not requested again, the sampling period changes only once and it may appear that there was no execution of the command. This is especially true when bench testing the device. Automatic test equipment can test for results within a single sampling period.

Internally, the A' register value only affects one cycle (period) of the A counter. The A and A' values are additive, but only for one A-counter period. The A counter begins the first count at the default or programmed A-register value and counts down to the A'-register value. As the A' value increases or decreases, the first clock cycle from the A counter is lengthened or shortened. The initial A-counter period is the only counter period affected by the A' register such that only this single period is increased or decreased.

2.15.2 Analog Loopback

This function allows the circuit to be tested remotely. In loopback, OUT+ and OUT- are internally connected to IN+ and IN-. The DAC data bits D15 to D02 that are applied to DIN can be compared with the ADC output data bits D15 to D02 at DOUT. There are some differences due to the ADC and DAC channel offset. The loopback function is implemented by setting DS01 and DS00 to zero in control register 5 (see Section 2.19). When analog loopback is enabled, the external inputs to IN+ and IN- are disconnected, but the signals at OUT+ and OUT- may still be read.

2.15.3 16-Bit Mode

In the 16-bit mode, the device ignores the last two control bits (D01 and D00) of the primary word and requests continual secondary communications to occur. By ignoring the last two primary communication bits, compatibility with existing 16-bit software can be maintained. This function is implemented by setting bit DS03 to 1 in register 6. To return to normal operation, DS03 must be reprogrammed to 0.

2.15.4 Free-Run Mode

With the free-run bit set in register 6, the external shift clock and frame sync control only the data transfer. The ADC and DAC timing are controlled by the A and B register values, and the phase-shift adjustment must be done as if the device is in stand-alone mode (by the software or the state of FC1 and FC0).

Phase adjustment cannot be made by adjustment of the frame-sync timing. The external frame sync must occur within $1/2$ FCLK period of the internal frame sync (FCLK as determined by the values of the A and B registers).

When the external frame sync occurs simultaneously with the internal load, the data-transfer request by the external frame sync takes precedence over an internal load command. The latching of the ADC conversion data in the output register is inhibited until the current 16 bits are shifted out of the register by the shift clock.

2.15.5 Force Secondary Communication

With bit 2 in register 6 set to 1, secondary communication is requested continuously. It overrides all software and hardware requests concerning secondary communication. Phase shifting, however, can still be performed with the software and hardware.

2.15.6 Enable Analog Input Summing

By setting bits DS01 and DS00 to 11 in register 5, the normal analog input voltage is summed with the auxiliary input voltage. The gain for the analog input amplifier is set by data bits DS03 and DS02 in register 4.

2.15.7 DAC Channel (sin x)/x Error Correction

The (sin x)/x compensation filter is designed for zero (sin x)/x error using a B-register value of 15. Since the filter cannot be removed from the signal path, operation using another B-register value results in an error in the reconstructed analog output. The error is given by equation 19. Any error compensation needed by a given application can be performed in the software.

$$\text{DAC channel frequency response error} = 20 \times \log_{10} \left[\frac{\sin \left(\frac{2\pi \times A \times B}{f_{\text{MCLK}}} \times f \right)}{\sin \left(\frac{30\pi \times A}{f_{\text{MCLK}}} \times f \right)} \times \frac{15}{B} \right] \quad (19)$$

where:

- f = the frequency of interest
- f_{MCLK} = the TLC320AC01 master-clock frequency
- A = the A-register value
- B = the B-register value

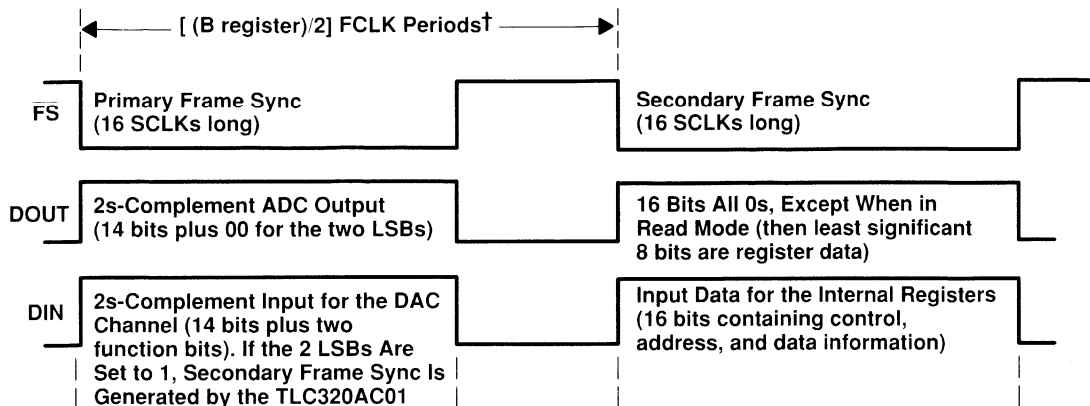
and the arguments of the sin functions are in radians.

2.16 Serial Communications

2.16.1 Stand-Alone and Master-Mode Word Sequence and Information Content During Primary and Secondary Communications

For the stand-alone and master modes, the sequence in Figure 2–2 shows the relationship between the primary and secondary communications interval, the data content into DIN, and the data content from DOUT.

The TLC320AC01 can provide a phase-shift command or the next secondary communications interval by decoding 1) the programmed state of the FC1 and FC0 inputs and the D01 and D00 data bits in the primary data word, or 2) the state of the FC1 and FC0 inputs and the DS15 and DS14 data bits in the secondary data word (see Table 2–3). When DS13 (the R/W bit) is the default value of 0, all 16 bits from DOUT are 0 during secondary communication. However, when the R/W bit is set to 1 in the secondary communication control word, the secondary transmission from DOUT still contains 0s in the eight MSBs. The lower order 8 bits contain the data of the register currently being addressed. This function provides register status information for the host.

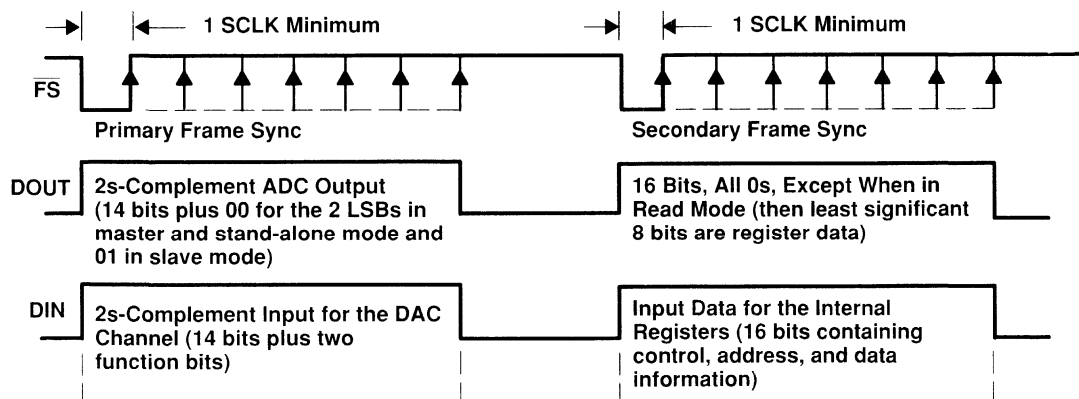


† The time between the primary and secondary frame sync is the time equal to filter clock (FCLK) period multiplied by the B-register contents divided by two. The time interval is rounded to the nearest shift clock. The secondary frame-sync signal goes from high to low on the next shift clock low-to-high transition after (B register/2) filter clock periods.

Figure 2–3. Master and Stand-Alone Functional Sequence

2.16.2 Slave and Codec-Mode Word Sequence and Information Content During Primary and Secondary Communications

For the slave and codec modes, the sequence is basically the same as the stand-alone and master modes with the exception that the frame sync and the shift clock are generated and controlled externally as shown in Figure 2–3. For the codec mode, the frame-sync pulse width needs to be a minimum of one shift clock long. The timing relationship between the frame sync and shift clock is shown in the timing diagrams. Phase shifting is usually not required in the slave or codec mode because the frame-sync timing can be adjusted externally if required.



NOTE A: The time between the primary and secondary frame syncs is determined by the application; however, enough time must be provided so that the host can execute the required number of software instructions in the time between the end of the primary data transfer (rising edge of the primary frame-sync interval) and the falling edge of the secondary frame sync (start of secondary communications).

Figure 2–4. Slave and Codec Functional Sequence

2.17 Request for Secondary Serial Communication and Phase Shift

The following paragraphs describe a request for secondary serial communication and phase shift using hardware control inputs FC1 and FC0, primary data bits D01 and D00, and secondary data bits DS15 and DS14.

2.17.1 Initiating a Request

Combinations of FC1 and FC0 input conditions, bits D01 and D00 in the primary serial data word, FC1 and FC0, and bits DS15 and DS14 in the secondary serial data word can initiate a secondary serial communication or request a phase shift according to the following rules (see Table 2–3).

1. Primary word phase shifts can be requested by either the hardware or software when the other set of signals are 11 or 00. If both hardware and software request phase shifts, the software request is performed.
2. Secondary words can be requested by either the software or hardware at the same time that the other set of signals is requesting a phase shift.
3. Hardware inputs FC1 and FC0 are ignored during the secondary word unless DS15 and DS14 are 11. When DS15 and DS14 are 01 or 10, the corresponding phase shift is performed. When DS15 and DS14 are 00, no phase shift is performed even when the hardware requests a phase shift.

2.17.2 Normal Combinations of Control

The normal combinations of control are as follows:

1. Use D01 and D00 and DS15 and DS14 to request phase shifts and secondary words by holding FC1 and FC0 to 00.
2. Use FC1 and FC0 exclusively to request phase shifts and secondary words by holding D01 and D00 to 00 and DS15 and DS14 to 11.
3. Use D01 and D00 only to request secondary words and FC1 and FC0 to perform phase shifts once per period by holding DS15 and DS14 to 00.

2.17.3 Additional Control Options

Additional control options are unusual and are rarely needed or used; however, they are as follows:

1. Use D01 and D00 only to request secondary words and FC1 and FC0 to perform phase shifts twice per period by holding DS15 and DS14 to 11.
2. Use FC1 and FC0 exclusively to request secondary words and D01 and D00 and DS15 and DS14 to perform phase shifts twice per period.
3. Use FC1 and FC0 to perform the phase shift after the primary word and DS15 and DS14 to perform a phase shift after the secondary word by holding D01 and D00 to 11.

**Table 2–3. Software and Hardware Requests for
Secondary Serial-Communication and Phase-Shift Truth Table**

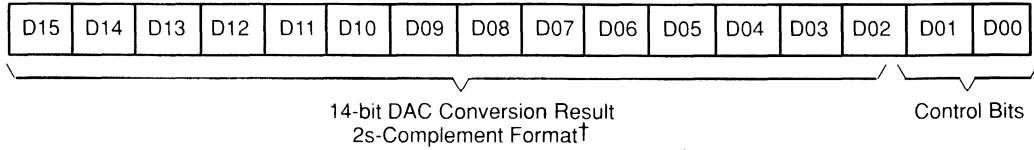
WITHIN PRIMARY OR SECONDARY DATA WORD	CONTROL BITS		HARDWARE TERMINALS		PHASE-SHIFT ADJUSTMENT (see Section 2.15.1)		SECONDARY REQUEST (see Note 1)
	D01	D00	FC1	FC0	EARLIER	LATER	
Primary	0	0	0	0	0	0	0
	0	0	0	1	0	1	0
	0	0	1	0	1	0	0
	0	0	1	1	0	0	1
	0	1	0	0	0	1	0
	0	1	0	1	0	1	0
	0	1	1	0	0	1	0
	0	1	1	1	0	1	1
	1	0	0	0	1	0	0
	1	0	0	1	1	0	0
	1	0	1	0	1	0	0
	1	0	1	1	1	0	1
	1	1	0	0	0	0	1
	1	1	0	1	0	1	1
	1	1	1	0	1	0	1
	1	1	1	1	0	0	1
Secondary	DS15	DS14	FC1	FC0	EARLIER	LATER	No request can be made for secondary communication within the secondary word.
	0	0	0	0	0	0	
	0	0	0	1	0	0	
	0	0	1	0	0	0	
	0	0	1	1	0	0	
	0	1	0	0	0	1	
	0	1	0	1	0	1	
	0	1	1	0	0	1	
	0	1	1	1	0	1	
	1	0	0	0	1	0	
	1	0	0	1	1	0	
	1	0	1	0	1	0	
	1	0	1	1	1	0	
	1	1	0	0	0	0	
	1	1	0	1	0	1	
	1	1	1	0	1	0	
1	1	1	1	0	0		

NOTE 1: The 0 state indicates that a secondary communication is not being requested. The 1 state indicates that a secondary communication is being requested.

2.18 Primary Serial Communications

Primary serial communications transfer the 14-bit DAC input plus two control bits (D01 and D00) to DIN of the TLC320AC01. They simultaneously transfer the 14-bit ADC conversion result from DOUT to the processor. The 2 LSBs are set to 0 in the ADC result.

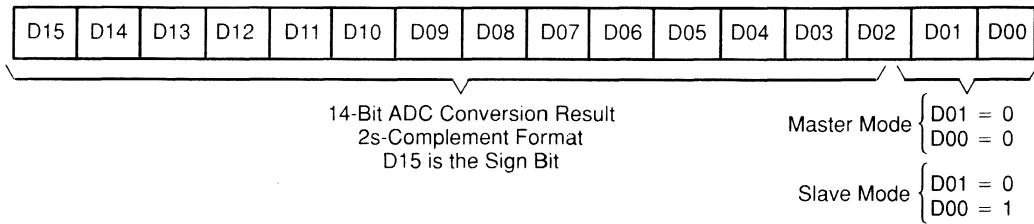
2.18.1 Primary Serial Communications Data Format



† Since the supply voltage is single ended, the reference for 2s-complement format is ADC V_{MID} . Voltages above this reference have a 0 as the MSB, and voltages below this reference have a 1 as the MSB.

During primary serial communications, when D01 and D00 are both high in the DAC data word to DIN, a subsequent 16 bits of control information is received by the device at DIN during a secondary serial-communication interval. This secondary serial-communication interval begins at 1/2 the programmed conversion time when the B register data value is even or 1/2 the programmed value minus one FCLK when the B register data value is odd. The time between primary and secondary serial communication is measured from the falling edge of the primary frame sync to the falling edge of the secondary frame sync (see Section 2.19 for function and format of control words).

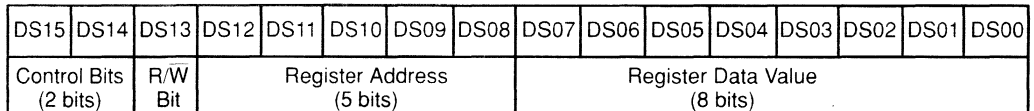
2.18.2 Data Format From DOUT During Primary Serial Communications



2.19 Secondary Serial Communications

2.19.1 Data Format to DIN During Secondary Serial Communications

There are nine 16-bit configuration and control registers numbered from zero to eight. All register data contents are represented in 2s-complement format. The general format of the commands during secondary serial communications is as follows.

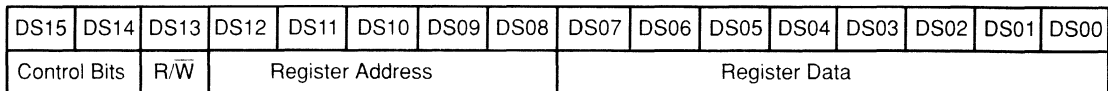


All control register words are latched in the register and valid on the sixteenth falling edge of SCLK.

2.19.2 Control Data-Bit Function in Secondary Serial Communication

2.19.2.1 DS15 and DS14

In the secondary data word, bits DS15 and DS14 perform the same control function as the primary control bits D01 and D00 do in the primary data word.



Hardware terminals FC1 and FC0 are valid inputs when DS15 and DS14 are both high, and they are ignored for all other conditions.

2.19.2.2 DS13 (R/W Bit)

Reset and power-up procedures set this bit to a 0, placing the device in the write mode. When this bit is set to 1, however, the previous data content of the register being addressed is read out to the host from DOUT as the least significant 8 bits of the 16-bit secondary word. The first 8 bits remain set to 0. Reading the data out is nondestructive, and the contents of the register remain unchanged.

A. Write Mode (DS13 = 0)

Data In. The data word to DIN has the following general format in the write mode.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00	
Control Bits		0	Register Address					Register Data								

Data Out. The shift clock shifts out all 0s as the pattern to the host from DOUT.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

B. Read Mode (DS13 = 1)

Data In. The data word to DIN has the following format to allow a register read. Phase shifts can also be done in the read mode.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00	
Control Bits		1	Register Address					Ignored								

Data Out. The shift clock clocks out the data of the register addressed from DOUT in the read mode in the 8 LSBs.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0	Register Data							

2.20 Internal Register Format

2.20.1 Pseudo-Register 0 (No-Op Address)

This address represents a no-operation command. No register I/O operation takes place, so the device can receive secondary commands for phase adjustment without reprogramming any register. A read of the no-op is 0. The format of the command word is as follows:

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		X	0	0	0	0	0	X	X	X	X	X	X	X	X

2.20.2 Register 1 (A Register)

The following command loads DS07 (MSB) – DS00 into the A register.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/W	0	0	0	0	1	Register Data							

The data in DS07 – DS00 determines the division of the master clock to produce the internal FCLK.

$$\text{FCLK frequency} = \text{MCLK}/(\text{A register contents} \times 2)$$

The default value of the A-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

2.20.3 Register 2 (B Register)

The following command loads DS07 (MSB) – DS00 into the B register.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits	R/W	0	0	0	1	0	Register Data								

The data in DS07 – DS00 controls the division of FCLK to generate the conversion clock as given in equation 20:

$$\begin{aligned} \text{Conversion frequency} &= \text{FCLK}/(\text{B register contents}) \\ &= \frac{\text{MCLK}}{2 \times \text{A register contents} \times \text{B register contents}} \end{aligned} \quad (20)$$

The default value of the B-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

2.20.4 Register 3 (A' Register)

The following command contains the A'-register address and loads DS07(MSB) – DS00 into the A' register.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits	R/W	0	0	0	1	1	Register Data								

The data in DS07 – DS00 is in 2s-complement format and controls the number of master-clock periods that the sampling time is shifted.

The default value of the A'-register data is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

2.20.5 Register 4 (Amplifier Gain-Select Register)

The following command contains the amplifier gain-select register address with selection code for the monitor output (DS05–DS04), analog input (DS03–DS02), and analog output (DS01–DS00) programmable gains.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/W	0	0	1	0	0	X	X	*	*	*	*	*	*
Monitor output gain = squelch										0	0				
Monitor output gain = 0 dB										0	1				
Monitor output gain = –8 dB										1	0				
Monitor output gain = –18 dB										1	1				
Analog input gain = squelch												0	0		
Analog input gain = 0 dB												0	1		
Analog input gain = 6 dB												1	0		
Analog input gain = 12 dB												1	1		
Analog output gain = squelch													0	0	
Analog output gain = 0 dB													0	1	
Analog output gain = –6 dB													1	0	
Analog output gain = –12 dB													1	1	

The default value of the monitor output gain is squelch, which corresponds to data bits DS05 and DS04 equal to 00 (binary).

The default value of the analog input gain is 0 dB, which corresponds to data bits DS03 and DS02 equal to 01 (binary).

The default value of the analog output gain is 0 dB, which corresponds to data bits DS01 and DS00 equal to 01 (binary).

The default data value is shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	1	0	1

2.20.6 Register 5 (Analog Configuration Register)

The following command loads the analog configuration register with the individual bit functions described below.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/W	0	0	1	0	1	X	X	X	X	*	*	*	*
Must be set to 0											0				
High-pass filter disabled												1			
High-pass filter enabled												0			
Analog loopback enabled													0	0	
Enables IN+ and IN– (disables AUXIN+ and AUXIN–)													0	1	
Enables AUXIN+ and AUXIN– (disables IN+ and IN–)													1	0	
Enable analog input summing													1	1	

The default value of the high-pass-filter enable bit is 0, which places the high-pass filter in the signal path. The default values of DS01 and DS00 are 0 and 1 which enables IN+ and IN–.

The power-up and reset conditions are as shown below.

DS03	DS02	DS01	DS00
0	0	0	1

In the read mode, eight bits are read but the 4 LSBs are repeated as the 4 MSBs.

2.20.7 Register 6 (Digital Configuration Register)

The following command loads the digital configuration register with the individual bit functions described below.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits	R/W	0	0	1	1	0	X	X	*	*	*	*	*	*	*
ADC and DAC conversion free run										1					
Inactive										0					
FSD output disable										1					
Enable										0					
16-Bit mode, ignore primary LSBs											1				
Normal operation											0				
Force secondary communications													1		
Normal operation													0		
Software reset														1	
(upon reset, this bit is automatically reset to 0)															
Inactive reset														0	
Software power-down active (automatically reset to 0															1
after PWR DWN is cycled high to low and back to high)															
Power-down function external															0
(uses PWR DWN)															

The default value of DS07–DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

2.20.8 Register 7 (Frame-Sync Delay Register)

The following command contains the frame-sync delay (FSD) register address and loads DS07 (MSB)–DS00 into the FSD register. The data byte (DS01–DS00) determines the number of SCLKs between FS and the delayed frame-sync signal, FSD. The minimum data value for this register is decimal 18.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits	R/W	0	0	1	1	1	Register Data								

The default value of DS07 – DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

When using a slave device, register 7 must be the last register programmed.

2.20.9 Register 8 (Frame-Sync Number Register)

The following command contains the frame-sync number (FSN) register address and loads DS07 (MSB)–DS00 into the FSN register. The data byte determines the number of frame-sync signals generated by the TLC320AC01. This number is equal to the number of slaves plus one.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/ \overline{W}	0	1	0	0	0	Register Data							

The default value of DS07–DS00 is 1 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	1

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, DGTL V_{DD} (see Notes 1 and 2)	–0.3 V to 6.5 V
Supply voltage range, DAC V_{DD} (see Notes 1 and 2)	–0.3 V to 6.5 V
Supply voltage range, ADC V_{DD} (see Notes 1 and 2)	–0.3 V to 6.5 V
Differential supply voltage range, DGTL V_{DD} to DAC V_{DD}	–0.3 V to 6.5 V
Differential supply voltage range, all positive supply voltages to ADC GND, DAC GND, DGTL GND, SUBS	–0.3 V to 6.5 V
Output voltage range, DOOUT	–0.3 V to DGTL V_{DD} + 0.3 V
Input voltage range, DIN	–0.3 V to DGTL V_{DD} + 0.3 V
Ground voltage range, ADC GND, DAC GND, DGTL GND, SUBS	–0.3 V to DGTL V_{DD} + 0.3 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive supply voltage	4.5	5	5.5	V
	Steady-state differential voltage between any two supplies			0.1	V
V_{IH}	High-level digital input voltage	2.2			V
V_{IL}	Low-level digital input voltage			0.8	V
I_O	Load output current from ADC V_{MID} and DAC			100	μ A
	Conversion time for the ADC and DAC channels		10 FCLK periods		
f_{MCLK}	Master-clock frequency		10.368	15	MHz
$V_{ID(PP)}$	Analog input voltage (differential, peak to peak)		6		V
R_L	Differential output load resistance	600			Ω
	Single-ended to buffered DAC V_{MID} voltage load resistance	300			
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. Voltage values for DGTL V_{DD} are with respect to DGTL GND, voltage values for DAC V_{DD} are with respect to DAC GND, and voltage values for ADC V_{DD} are with respect to ADC GND. For the subsequent electrical, operating, and timing specifications, the symbol V_{DD} denotes all positive supplies. DAC GND, ADC GND, DGTL GND, and SUBS are at 0 V unless otherwise specified.

2. To avoid possible damage to these CMOS devices and associated operating parameters, the sequence below should be followed when applying power:

- (1) Connect SUBS, DGTL GND, ADC GND, and DAC GND to ground.
- (2) Connect voltages ADC V_{DD} , and DAC V_{DD} .
- (3) Connect voltage DGTL V_{DD} .
- (4) Connect the input signals.

When removing power, follow the steps above in reverse order.

3.3 Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, MCLK = 5.184 MHz, V_{DD} = 5 V, Outputs Unloaded, Total Device

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I _{DD}	Supply current	PWR $\overline{\text{DWN}}$ = 1 and clock signals present		20	25	mA
		PWR $\overline{\text{DWN}}$ = 0 after 500 μ s and clock signals present		1	2	mA
P _D	Power dissipation	PWR $\overline{\text{DWN}}$ = 1 and clock signals present		100		mW
		PWR $\overline{\text{DWN}}$ = 0 after 500 μ s and clock signals present		5		mW
		Software power down, (bit D00, register 6 set to 1)		15	20	mW
ADC V _{MID}	Midpoint voltage	No load	ADC V _{DD} /2 -0.1		ADC V _{DD} /2 +0.1	V
DAC V _{MID}	Midpoint voltage	No load	DAC V _{DD} /2 -0.1		DAC V _{DD} /2 +0.1	V

3.4 Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, V_{DD} = 5 V, Digital I/O Terminals (DIN, DOUT, EOC, FC0, FC1, $\overline{\text{FS}}$, $\overline{\text{FSD}}$, MCLK, M/ $\overline{\text{S}}$, SCLK)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1.6 mA		2.4		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
I _{IH}	High-level input current, any digital input	V _I = 2.2 V to DGTL V _{DD}			10	μ A
I _{IL}	Low-level input current, any digital input	V _I = 0 V to 0.8 V			10	μ A
C _i	Input capacitance			5		pF
C _o	Output capacitance			5		pF

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

3.5 Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, V_{DD} = 5 V, ADC and DAC Channels

3.5.1 ADC Channel Filter Transfer Function, FCLK = 144 kHz, f_s = 8 kHz

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
Gain relative to gain at f _i = 1020 Hz (see Note 3)		f _i = 50 Hz		-2	dB
		f _i = 200 Hz	-1.8	-0.15	
		f _i = 300 Hz to 3 kHz	-0.15	0.15	
		f _i = 3.3 kHz	-0.35	0.03	
		f _i = 3.4 kHz	-1	-0.1	
		f _i = 4 kHz		-14	
		f _i \geq 4.6 kHz		-32	

NOTE 3: The differential analog input signals are sine waves at 6 V peak to peak. The reference gain is at 1020 Hz.

3.5.2 ADC Channel Input, $V_{DD} = 5\text{ V}$, Input Amplifier Gain = 0 dB (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{I(PP)}$	Peak-to-peak input voltage (see Note 4)	Single-ended	3			V
		Differential	6			V
	ADC converter offset error	Band-pass filter selected	10	30		mV
CMRR	Common-mode rejection ratio at IN+, IN-, AUX IN+, AUX IN- (see Note 5)		55			dB
r_i	Input resistance at IN+, IN-, AUX IN+, AUX IN-		100			k Ω
	Squelch	DS03, DS02 = 0 in register 4	60			dB

† All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTES: 4. The differential range corresponds to the full-scale digital output.

5. Common-mode rejection ratio is the ratio of the ADC converter offset error with no signal and the ADC converter offset error with a common-mode nonzero signal applied to either IN+ and IN- together or AUX IN+ and AUX IN- together.

3.5.3 ADC Channel Signal-to-Distortion Ratio, $V_{DD} = 5\text{ V}$, $f_s = 8\text{ kHz}$ (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	$A_V = 0\text{ dB}$		$A_V = 6\text{ dB}$		$A_V = 12\text{ dB}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
ADC channel signal-to-distortion ratio (see Note 6)	$V_I = -6\text{ dB to } -1\text{ dB}$	68	—	—	—	—	—	dB
	$V_I = -12\text{ dB to } -6\text{ dB}$	63	—	68	—	—	—	
	$V_I = -18\text{ dB to } -12\text{ dB}$	56	—	63	—	68	—	
	$V_I = -24\text{ dB to } -18\text{ dB}$	51	—	57	—	63	—	
	$V_I = -30\text{ dB to } -24\text{ dB}$	43	—	51	—	57	—	
	$V_I = -36\text{ dB to } -30\text{ dB}$	39	—	45	—	51	—	
	$V_I = -42\text{ dB to } -36\text{ dB}$	33	—	39	—	45	—	
	$V_I = -48\text{ dB to } -42\text{ dB}$	27	—	32	—	39	—	

NOTE 6: The analog-input test signal is a 1020-Hz sine wave with 0 dB = 6 V peak to peak as the reference level for the analog-input signal.

3.5.4 DAC Channel Filter Transfer Function, $FCLK = 144\text{ kHz}$, $f_s = 9.6\text{ kHz}$, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Gain relative to gain at $f_i = 1020\text{ Hz}$ (see Note 7)	$f_i < 200\text{ Hz}$	0.15		dB
	$f_i = 200\text{ Hz}$	-0.5	0.15	
	$f_i = 300\text{ Hz to } 3\text{ kHz}$	-0.15	0.15	
	$f_i = 3.3\text{ kHz}$	-0.35	0.03	
	$f_i = 3.4\text{ kHz}$	-1	-0.1	
	$f_i = 4\text{ kHz}$	-14		
	$f_i \geq 4.6\text{ kHz}$	-32		

NOTE 7: The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak.

3.5.5 DAC Channel Signal-to-Distortion Ratio, $V_{DD} = 5\text{ V}$, $f_s = 8\text{ kHz}$ (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	$A_V = 0\text{ dB}$		$A_V = -6\text{ dB}$		$A_V = -12\text{ dB}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
DAC channel signal-to-distortion ratio (see Note 8)	$V_O = -6\text{ dB to }0\text{ dB}$	68	—	—	—	—	—	dB
	$V_O = -12\text{ dB to }-6\text{ dB}$	63	68	—	—	—	—	
	$V_O = -18\text{ dB to }-12\text{ dB}$	57	63	68	—	—	—	
	$V_O = -24\text{ dB to }-18\text{ dB}$	51	57	63	68	—	—	
	$V_O = -30\text{ dB to }-24\text{ dB}$	45	51	57	63	68	—	
	$V_O = -36\text{ dB to }-30\text{ dB}$	39	45	51	57	63	68	
	$V_O = -42\text{ dB to }-36\text{ dB}$	33	39	45	51	57	63	
	$V_O = -48\text{ dB to }-42\text{ dB}$	27	33	39	45	51	57	

NOTE 8: The input signal, V_I , is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at full-scale digital input = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT-.

3.5.6 System Distortion, $V_{DD} = 5\text{ V}$, $f_s = 8\text{ kHz}$, $F_{CLK} = 144\text{ kHz}$ (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC channel attenuation	Second harmonic	Single-ended input (see Note 9)	—	82	—	dB
		Differential input (see Note 9)	70	82	—	
	Third harmonic and higher harmonics	Single-ended input (see Note 9)	—	77	—	
		Differential input (see Note 9)	70	77	—	
DAC channel attenuation	Second harmonic	Single-ended output (buffered DAC V_{MID}) (see Note 10)	—	82	—	
		Differential output (see Note 10)	70	82	—	
	Third harmonic and higher harmonics	Single-ended output (see Note 10)	—	77	—	
		Differential output (see Note 10)	70	77	—	

† All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTES: 9. The input signal is a 1020-Hz sine wave for the ADC channel. Harmonic distortion is defined for an input level of -1 dB.

10. The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT-. Harmonic distortion is specified for a signal input level of 0 dB.

3.5.7 Noise, Low-Pass and Band-Pass Switched-Capacitor Filters Included, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC idle-channel noise		Inputs tied to ADC V_{MID} , $f_S = 8\text{ kHz}$, $F_{CLK} = 144\text{ kHz}$, (see Note 11)		180	300	μV_{rms}
DAC idle-channel noise	Broad-band noise	DIN INPUT = 00000000000000, $f_S = 8\text{ kHz}$, $F_{CLK} = 144\text{ kHz}$, (see Note 12)		180	300	
	Noise (0 to 7.2 kHz)			180	300	
	Noise (0 to 3.6 kHz)			180	300	

† All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTES: 11. The ADC channel noise is calculated by taking the RMS value of the digital output codes of the ADC channel and converting to microvolts.

12. The DAC channel noise is measured differentially from $OUT+$ to $OUT-$ across $600\ \Omega$.

3.5.8 Absolute Gain Error, $V_{DD} = 5\text{ V}$, $f_S = 8\text{ kHz}$ (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
ADC channel absolute gain error (see Note 13)	-1-dB input signal	$T_A = 25^\circ\text{C}$	± 0.5	dB
		$T_A = 0 - 70^\circ\text{C}$	± 1	
DAC channel absolute gain error (see Note 14)	0-dB input signal, $R_L = 600\ \Omega$	$T_A = 25^\circ\text{C}$	± 0.5	
		$T_A = 0 - 70^\circ\text{C}$	± 1	

NOTES: 13. ADC absolute gain error is the variation in gain from the ideal gain over the specified input signal levels. The gain is measured with a -1-dB, 1020-Hz sine wave. The -1-dB input signal allows for any positive gain or offset error that may affect gain measurements at or close to 0-dB input signal levels.

14. The DAC input signal is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at digital full-scale input = 0 dB). The nominal differential DAC channel output voltage with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is $600\ \Omega$ from $OUT+$ to $OUT-$.

3.5.9 Relative Gain and Dynamic Range, $V_{DD} = 5\text{ V}$, $f_S = 8\text{ kHz}$ (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
ADC channel relative gain tracking error (see Note 15)	-48-dB to -1-dB input signal range		± 0.15	dB
DAC channel relative gain tracking error (see Note 16)	-48-dB to 0-dB input signal range $R_{L(diff)} = 600\ \Omega$		± 0.15	

NOTES: 15. ADC gain tracking is the ratio of the measured gain at one ADC channel input level to the gain measured at any other input level. The ADC channel input is a -1-dB 1020-Hz sine wave input signal. A -1-dB input signal allows for any positive gain or offset error that may affect gain measurements at or close to 0-dB ADC input signal levels.

16. DAC gain tracking is the ratio of the measured gain at one DAC channel digital input level to the gain measured at any other input level. The DAC-channel input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output voltage with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is $600\ \Omega$ from $OUT+$ to $OUT-$.

3.5.10 Power-Supply Rejection, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted) (see Note 17)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC V_{DD}	Supply-voltage rejection ratio, ADC channel	$f_i = 0$ to 30 kHz		50		dB
		$f_i = 30$ to 50 kHz		55		
DAC V_{DD}	Supply-voltage rejection ratio, DAC channel	$f_i = 0$ to 30 kHz		40		
		$f_i = 30$ to 50 kHz		45		
DGTL V_{DD}	Supply-voltage rejection ratio, ADC channel	$f_i = 0$ to 30 kHz		50		
		$f_i = 30$ to 50 kHz		55		
DGTL V_{DD}	Supply-voltage rejection ratio, DAC channel	Single ended, $f_i = 0$ to 30 kHz		40		
		$f_i = 30$ to 50 kHz		45		
		Differential, $f_i = 0$ to 30 kHz		40		
		$f_i = 30$ to 50 kHz		45		

† All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTE 17: Power supply rejection measurements are made with both the ADC and the DAC channels idle and a 200-mV peak-to-peak signal applied to the appropriate supply.

3.5.11 Crosstalk Attenuation, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC channel crosstalk attenuation	DAC channel idle with DIN = 00000000000000, ADC input – 0 dB, 1020-Hz sine wave, Gain = 0 dB (see Note 18)		80		dB
DAC channel crosstalk attenuation	ADC channel idle with INP, INM, AUX IN+, and AUX IN– at ADC V_{MID}		80		dB
	DAC channel input = digital equivalent of a 1020-Hz sine wave (see Note 19)		80		

† All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTES: 18. The test signal is a 1020-Hz sine wave with a 0 dB = 6-V peak-to-peak reference level for the analog input signal.

19. The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT–.

3.5.12 Monitor Output Characteristics, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted) (see Note 20)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{O(PP)}$	Peak-to-peak ac output voltage	Quiescent level = ADC V_{MID} $Z_L = 10\text{ k}\Omega$ and 60 pF	1.3	1.5		V
V_{OO}	Output offset voltage	No load, single ended relative to ADC V_{MID}		5	10	mV
V_{OC}	Output common-mode voltage	No load	0.4 ADC V_{DD}	0.5 ADC V_{DD}	0.6 ADC V_{DD}	V
r_o	DC output resistance			50		Ω
A_V	Voltage gain (see Note 21)	Gain = 0 dB	-0.2	0	0.2	dB
		Gain 2 = -8 dB	-8.2	-8	-7.8	
		Gain 3 = -18 dB	-18.4	-18	-17.6	
		Squelch (see Note 22)			-60	

† All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTES: 20. All monitor output tests are performed with a $10\text{-k}\Omega$ load resistance.

21. Monitor gains are measured with a 1020-Hz , 6-V peak-to-peak sine wave applied differentially between $IN+$ and $IN-$. The monitor output gains are nominally 0 dB , -8 dB , and -18 dB relative to its input; however, the output gains are -6 dB relative to $IN+$ and $IN-$ or $AUX\ IN+$ and $AUX\ IN-$.

22. Squelch is measured differentially with respect to ADC V_{MID} .

3.6 Timing Requirements and Specifications in Master Mode

3.6.1 Recommended Input Timing Requirements for Master Mode, $V_{DD} = 5\text{ V}$

		MIN	NOM	MAX	UNIT
$t_r(\text{MCLK})$	Master clock rise time		5		ns
$t_f(\text{MCLK})$	Master clock fall time		5		ns
	Master clock duty cycle	40%		60%	
$t_w(\text{RESET})$	$\overline{\text{RESET}}$ pulse duration	1 MCLK			
$t_{su}(\text{DIN})$	DIN setup time before SCLK low (see Figure 4–2)	25			ns
$t_h(\text{DIN})$	DIN hold time after SCLK low (see Figure 4–2)			20	ns

3.6.2 Operating Characteristics Over Recommended Range of Operating Free-Air Temperature, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted) (see Note 23)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_f(\text{SCLK})$	Shift clock fall time (see Figure 4–2)		13	18	ns
$t_r(\text{SCLK})$	Shift clock rise time (see Figure 4–2)		13	18	ns
	Shift clock duty cycle	45%		55%	
$t_d(\text{CH-FL})$	Delay time from SCLK high to $\overline{\text{FSD}}$ low (see Figures 4–2 and 4–4 and Note 24)		5	15	ns
$t_d(\text{CH-FH})$	Delay time from SCLK high to $\overline{\text{FS}}$ high (see Figure 4–2)		5	20	ns
$t_d(\text{CH-DOUT})$	Delay time from SCLK high to DOUT valid (see Figures 4–2 and 4–7)			20	ns
$t_d(\text{CH-DOUTZ})$	Delay time from SCLK \uparrow to DOUT in high-impedance state (see Figure 4–8)		20		ns
$t_d(\text{ML-EL})$	Delay time from MCLK low to EOC low (see Figure 4–9)		40		ns
$t_d(\text{ML-EH})$	Delay time from MCLK low to EOC high (see Figure 4–9)		40		ns
$t_f(\text{EL})$	EOC fall time (see Figure 4–9)		13		ns
$t_r(\text{EH})$	EOC rise time (see Figure 4–9)		13		ns
$t_d(\text{MH-CH})$	Delay time from MCLK high to SCLK high			50	ns
$t_d(\text{MH-CL})$	Delay time from MCLK high to SCLK low			50	ns

† All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTES: 23. All timing specifications are valid with $C_L = 20\text{ pF}$.

24. $\overline{\text{FSD}}$ occurs 1/2 shift-clock cycle ahead of $\overline{\text{FS}}$ when the device is operating in the master mode.

3.7 Timing Requirements and Specifications in Slave Mode and Codec Emulation Mode

3.7.1 Recommended Input Timing Requirements for Slave Mode, $V_{DD} = 5\text{ V}$

		MIN	NOM	MAX	UNIT
$t_r(\text{MCLK})$	Master clock rise time		5		ns
$t_f(\text{MCLK})$	Master clock fall time		5		ns
	Master clock duty cycle	40%		60%	
$t_w(\text{RESET})$	$\overline{\text{RESET}}$ pulse duration	1 MCLK			
$t_{su}(\text{DIN})$	DIN setup time before SCLK low (see Figure 4-3)	20			ns
$t_h(\text{DIN})$	DIN hold time after SCLK high (see Figure 4-3)			20	ns
$t_{su}(\text{FL-CH})$	Setup time from $\overline{\text{FS}}$ low to SCLK high			$\pm \text{SCLK}/4$	ns

3.7.2 Operating Characteristics Over Recommended Range of Operating Free-Air Temperature, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted) (see Note 23)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_c(\text{SCLK})$	Shift clock cycle time (see Figure 4-3)	125			ns
$t_f(\text{SCLK})$	Shift clock fall time (see Figure 4-3)			18	ns
$t_r(\text{SCLK})$	Shift clock rise time (see Figure 4-3)			18	ns
	Shift clock duty cycle	45%		55%	
$t_d(\text{CH-FDL})$	Delay time from SCLK high to $\overline{\text{FSD}}$ low (see Figure 4-6)			50	ns
$t_d(\text{CH-FDH})$	Delay time from SCLK high to $\overline{\text{FSD}}$ high			40	ns
$t_d(\text{FL-FDL})$	Delay time from $\overline{\text{FS}}$ low to $\overline{\text{FSD}}$ low (slave to slave) (see Figure 4-5)			40	ns
$t_d(\text{CH-DOOUT})$	Delay time from SCLK high to DOUT valid (see Figures 4-3 and 4-7)			40	ns
$t_d(\text{CH-DOOUTZ})$	Delay time from SCLK \uparrow to DOUT in high-impedance state (see Figure 4-8)		20		ns
$t_d(\text{ML-EL})$	Delay time from MCLK low to EOC low (see Figure 4-9)		40		ns
$t_d(\text{ML-EH})$	Delay time from MCLK low to EOC high (see Figure 4-9)		40		ns
$t_f(\text{EL})$	EOC fall time (see Figure 4-9)		13		ns
$t_r(\text{EH})$	EOC rise time (see Figure 4-9)		13		ns
$t_d(\text{MH-CH})$	Delay time from MCLK high to SCLK high			50	ns
$t_d(\text{MH-CL})$	Delay time from MCLK high to SCLK low			50	ns

† All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTE 23: All timing specifications are valid with $C_L = 20\text{ pF}$.

4 Parameter Measurement Information

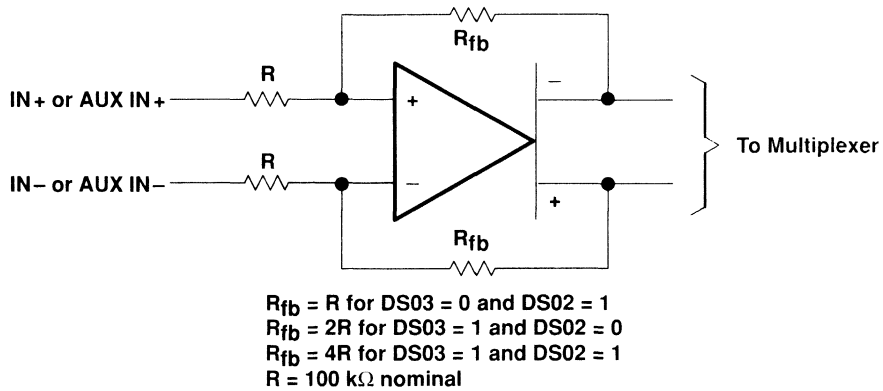


Figure 4-1. IN+ and IN- Gain-Control Circuitry

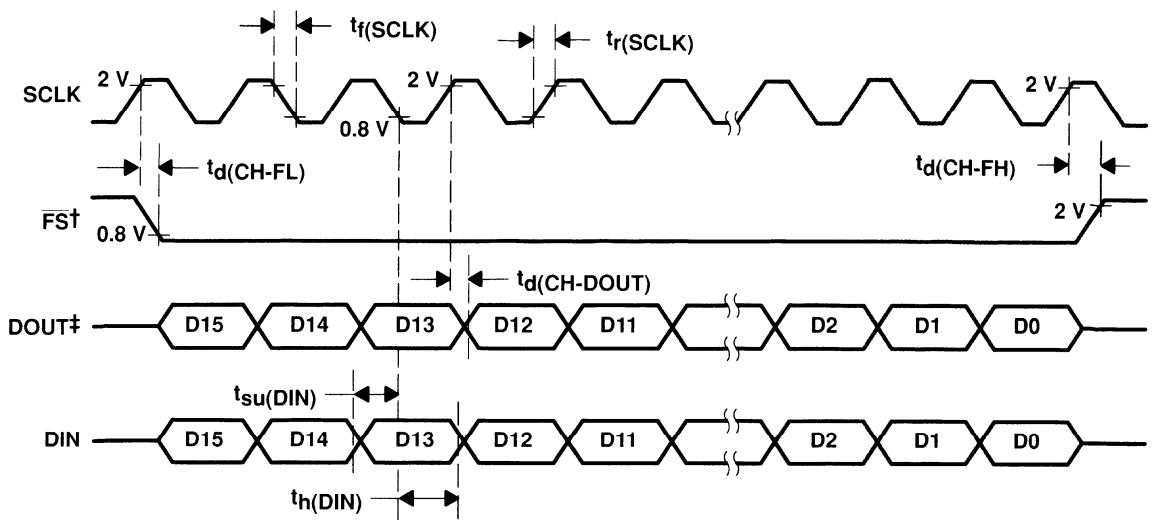
Table 4-1. Gain Control (Analog Input Signal Required for Full-Scale Bipolar A/D-Conversion 2s Complement)[†]

INPUT CONFIGURATION	CONTROL REGISTER 4		ANALOG INPUT [‡]	A/D CONVERSION RESULT
	DS03	DS02		
Differential configuration Analog input = IN+ - IN- = AUX IN+ - AUX IN-	0	0	All	Squelch
	0	1	$V_{ID} = \pm 3\text{ V}$	\pm Full scale
	1	0	$V_{ID} = \pm 1.5\text{ V}$	\pm Full scale
	1	1	$V_{ID} = \pm 0.75\text{ V}$	\pm Full scale
Single-ended configuration [§] Analog input = IN+ - V_{MID} = AUX IN+ - V_{MID}	0	0	All	Squelch
	0	1	$V_I = \pm 1.5\text{ V}$	\pm Half scale
	1	0	$V_I = \pm 1.5\text{ V}$	\pm Full scale
	1	1	$V_I = \pm 0.75\text{ V}$	\pm Full scale

[†] $V_{DD} = 5\text{ V}$

[‡] V_{ID} = differential input voltage, V_I = input voltage referenced to ADC V_{MID} with IN- or AUX IN- connected to ADC V_{MID} . In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.

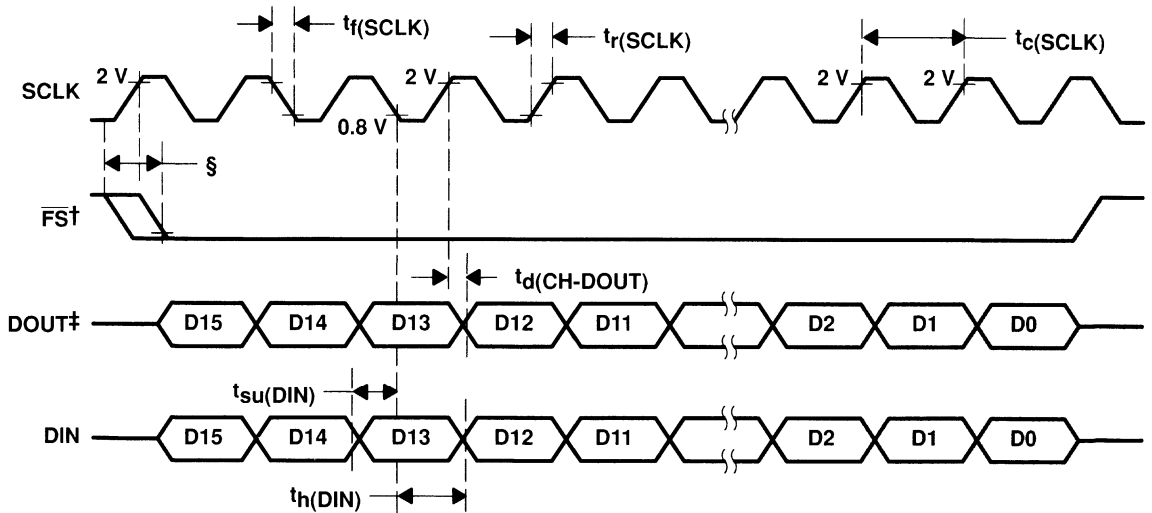
[§] For single-ended inputs, the analog input voltage should not exceed the supply rails. All single-ended inputs should be referenced to the internal reference voltage, ADC V_{MID} , for best common-mode performance.



† The time between falling edges of two primary \overline{FS} signals is the conversion period.

‡ The data on DOUT are shifted out on the rising edge of the shift clock, and the data on DIN are shifted in on the falling edge of the shift clock.

Figure 4–2. AIC Stand-Alone and Master-Mode Timing

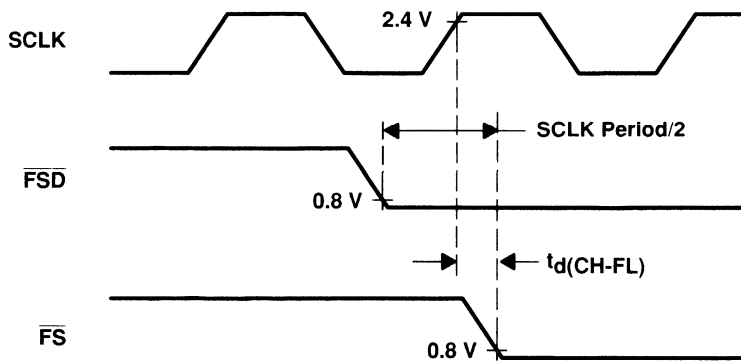


† The time between falling edges of two primary \overline{FS} signals is the conversion period.

‡ The data on DOUT are shifted out on the rising edge of the shift clock, and the data on DIN are shifted in on the falling edge of the shift clock.

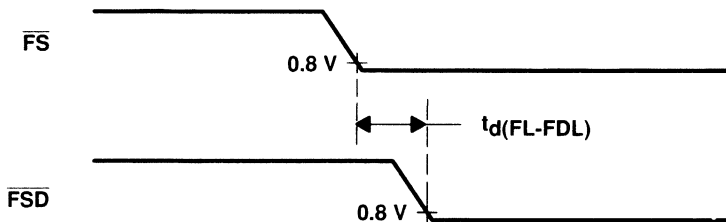
§ The high-to-low transition of \overline{FS} must occur within $\pm 1/4$ of a shift-clock period around the 2-V level of the shift clock for the codec mode.

Figure 4–3. AIC Slave and Codec Emulation Mode



NOTE A: Timing shown is for the TLC320AC01 operating as the master or as a stand-alone device.

Figure 4–4. Master or Stand-Alone \overline{FS} and \overline{FSD} Timing



NOTE A: Timing shown is for the TLC320AC01 operating in the slave mode (\overline{FS} and SCLK signals are generated externally). The programmed data value in the FSD register is 0.

Figure 4–5. Slave \overline{FS} to \overline{FSD} Timing



NOTE A: Timing shown is for the TLC320AC01 operating in the slave mode (\overline{FS} and SCLK signals are generated externally). There is a data value in the FSD register greater than 18 (decimal).

Figure 4 – 6. Slave SCLK to \overline{FSD} Timing

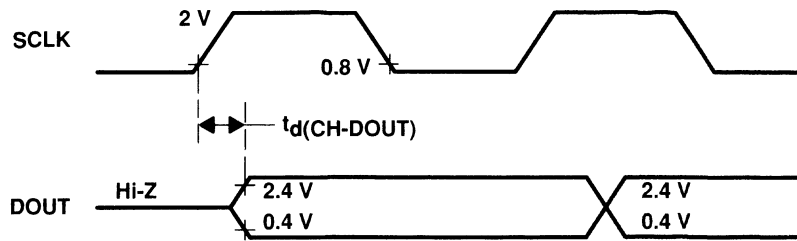


Figure 4-7. DOUT Enable Timing From Hi-Z

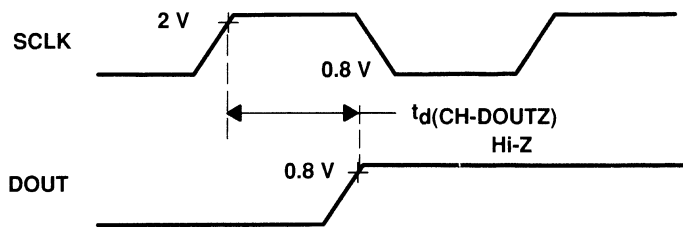


Figure 4-8. DOUT Delay Timing to Hi-Z

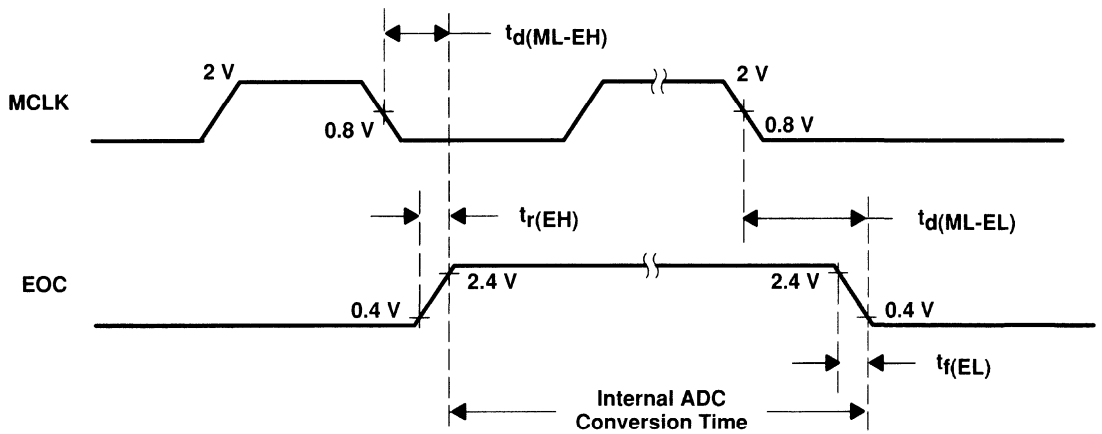
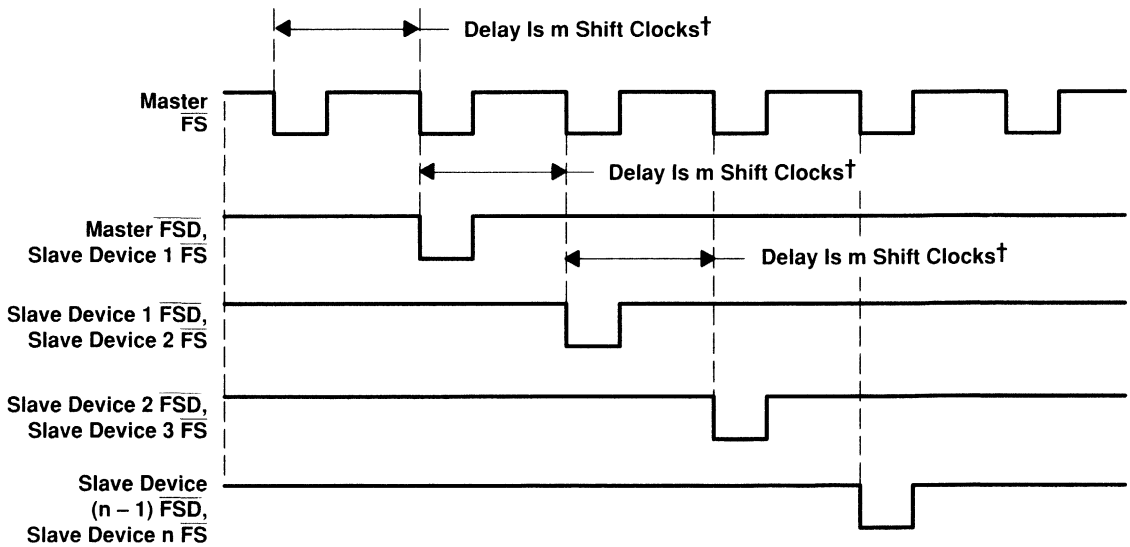


Figure 4-9. EOC Frame Timing



† The delay time from any \overline{FS} signals to the corresponding \overline{FSD} signals is m shift clocks with the value of m being the numerical value of the data programmed into the FSD register. In the master mode with slaves, the same data word programs the master and all slave devices; therefore, master to slave 1, slave 1 to slave 2, slave 2 to slave 3, etc., have the same delay time.

Figure 4–10. Master-Slave Frame-Sync Timing After a Delay Has Been Programmed Into the FSD Registers

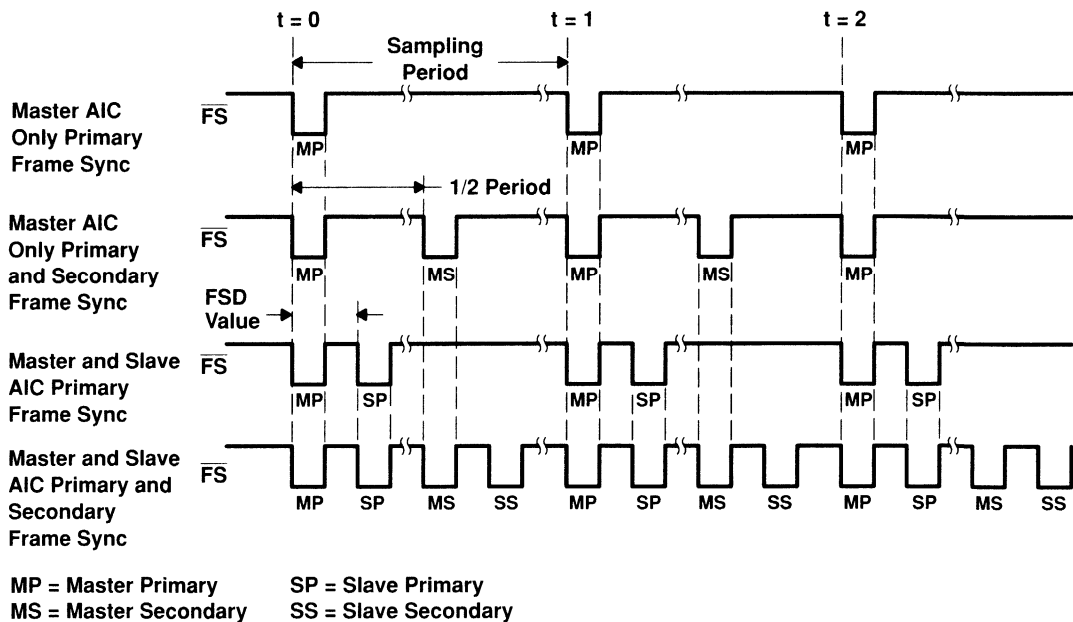
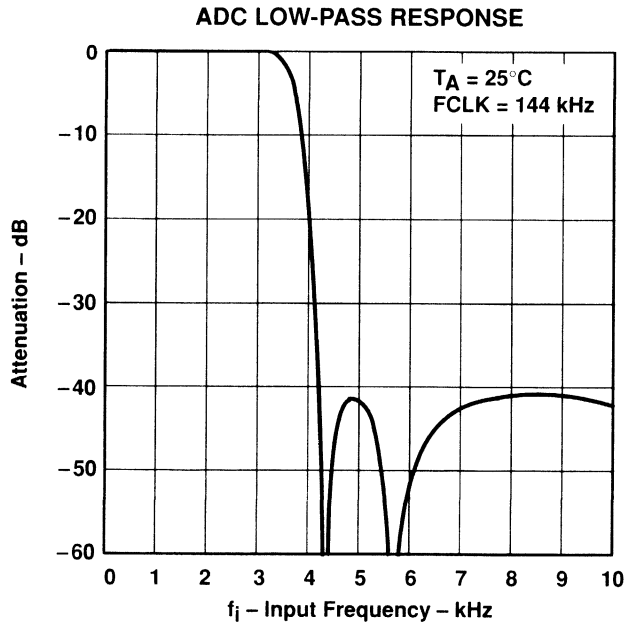


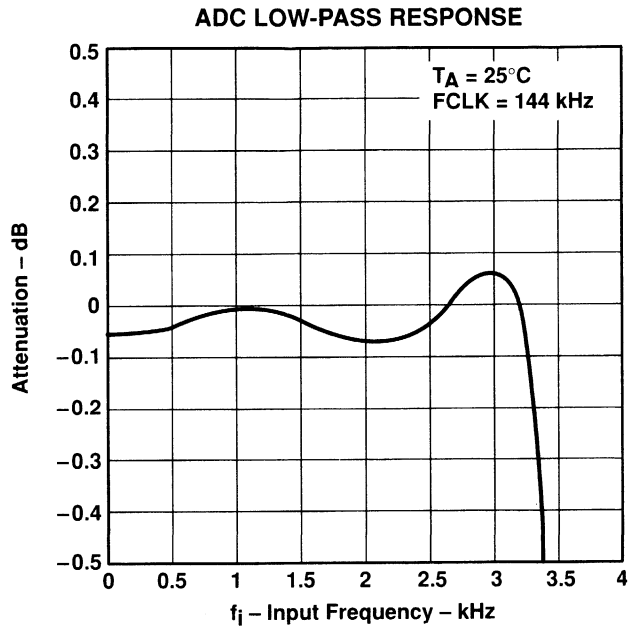
Figure 4–11. Master and Slave Frame-Sync Sequence with One Slave

5 Typical Characteristics



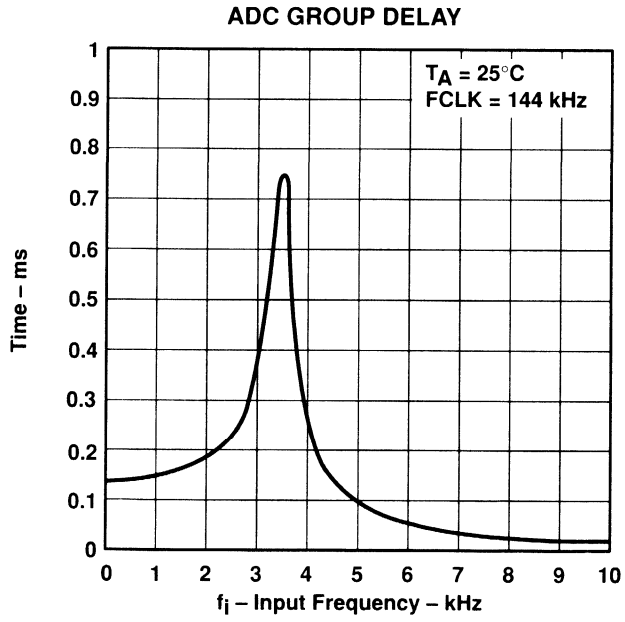
NOTE A: Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

Figure 5-1



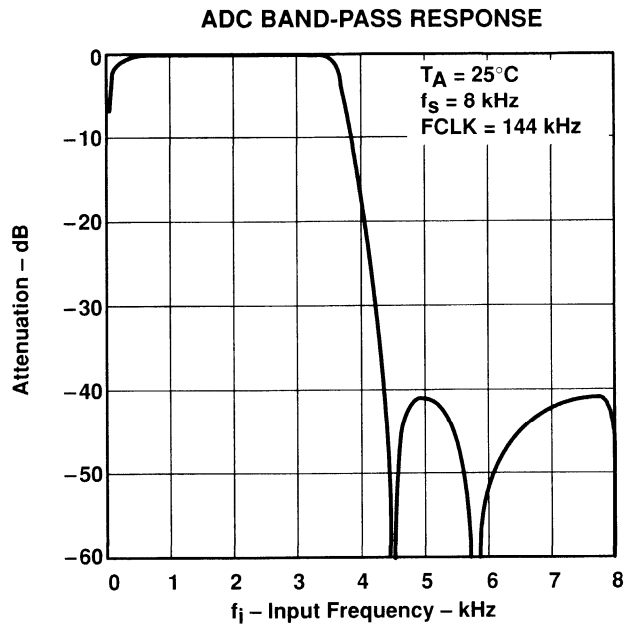
NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times FCLK \text{ (kHz)}}{144}$

Figure 5-2



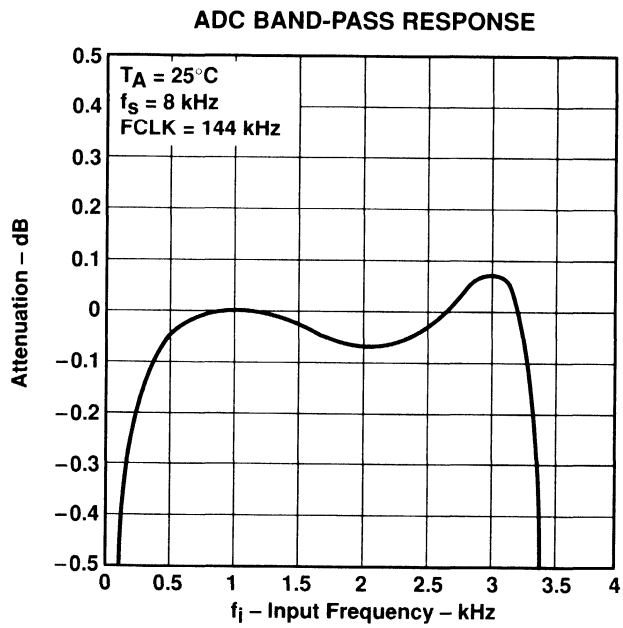
NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

Figure 5-3



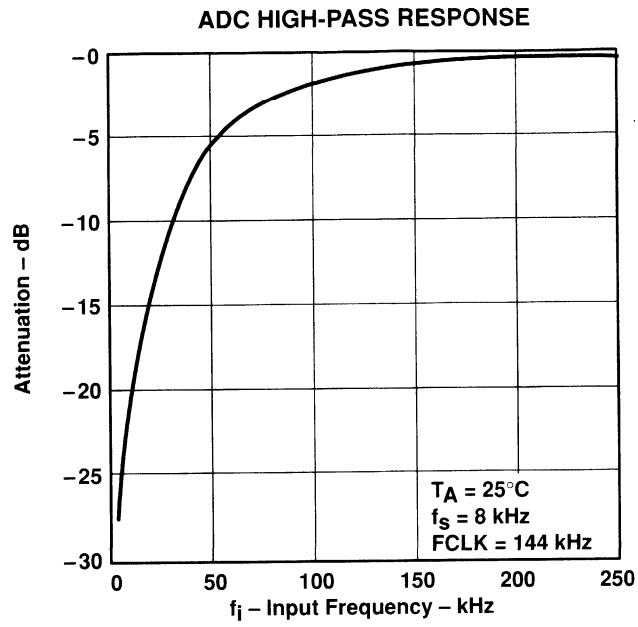
NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times FCLK\text{ (kHz)}}{144}$

Figure 5-4



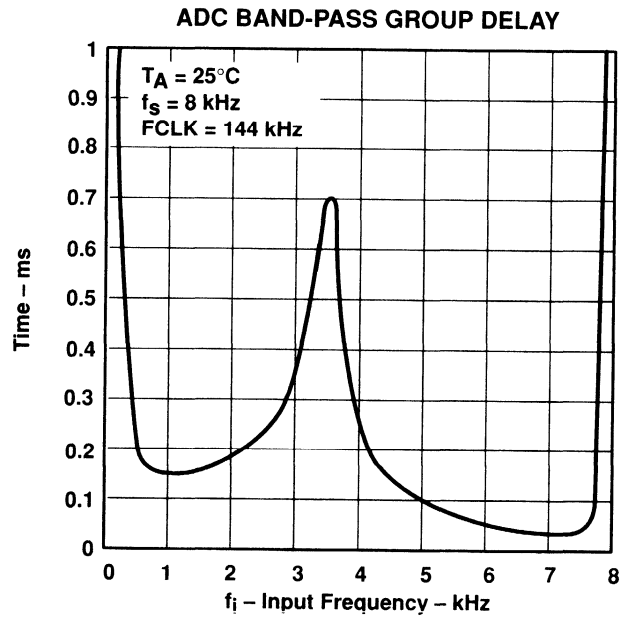
NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times FCLK\text{ (kHz)}}{144}$

Figure 5-5



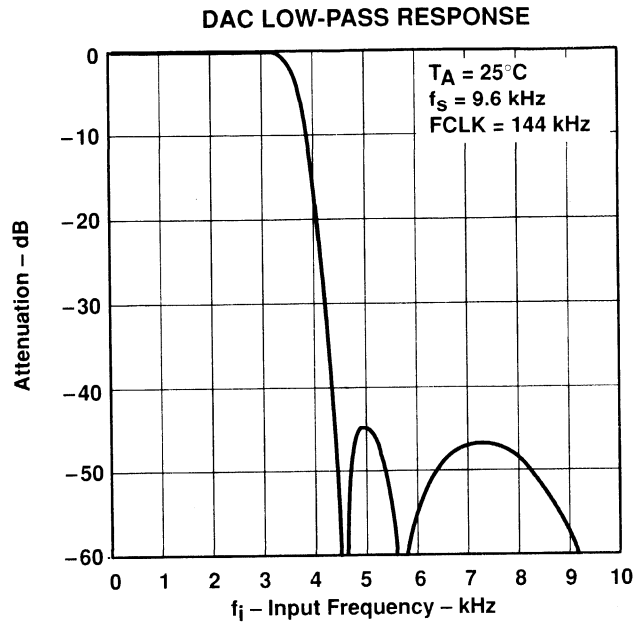
NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times FCLK \text{ (kHz)}}{144}$

Figure 5-6



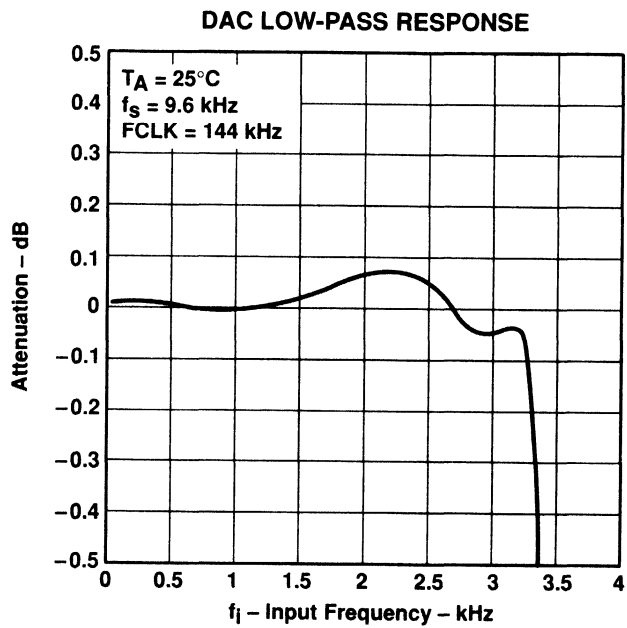
NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times FCLK \text{ (kHz)}}{144}$

Figure 5-7



NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

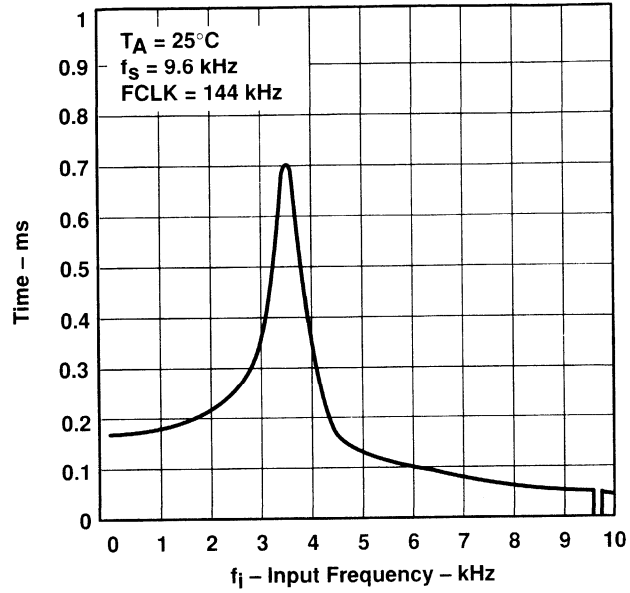
Figure 5-8



NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

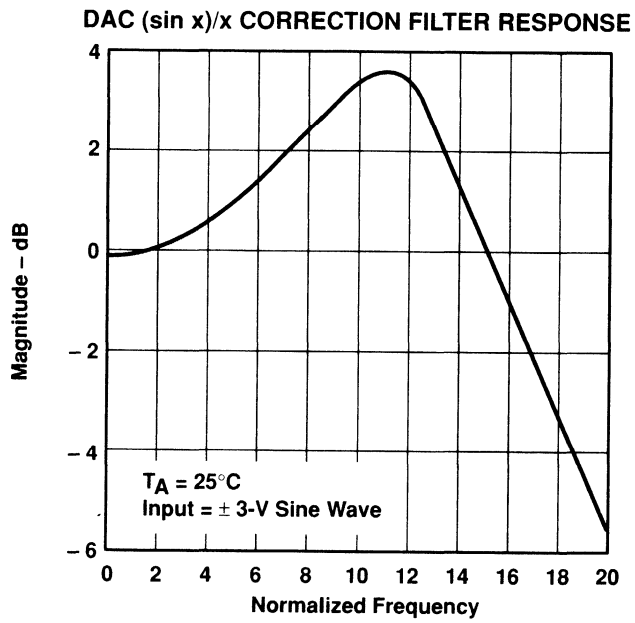
Figure 5-9

DAC LOW-PASS GROUP DELAY



NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times FCLK\text{ (kHz)}}{144}$

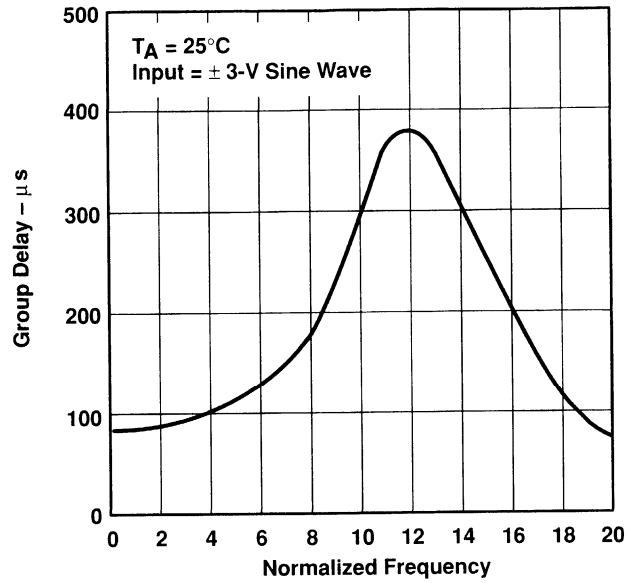
Figure 5-10



NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{288}$

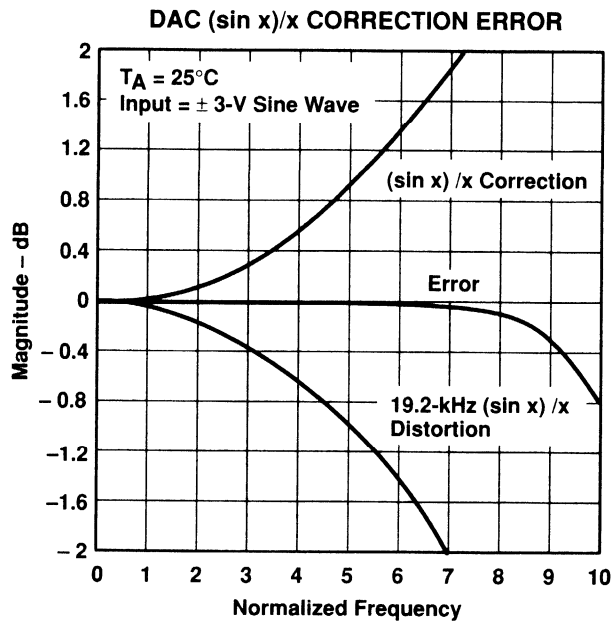
Figure 5-11

DAC (sin x)/x CORRECTION FILTER RESPONSE



NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{288}$

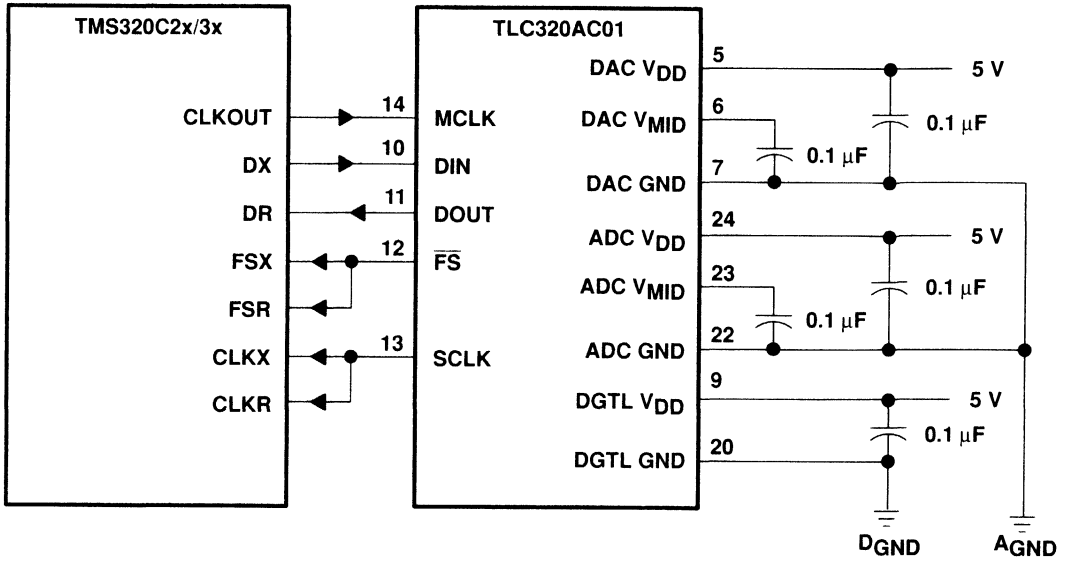
Figure 5-12



NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{288}$

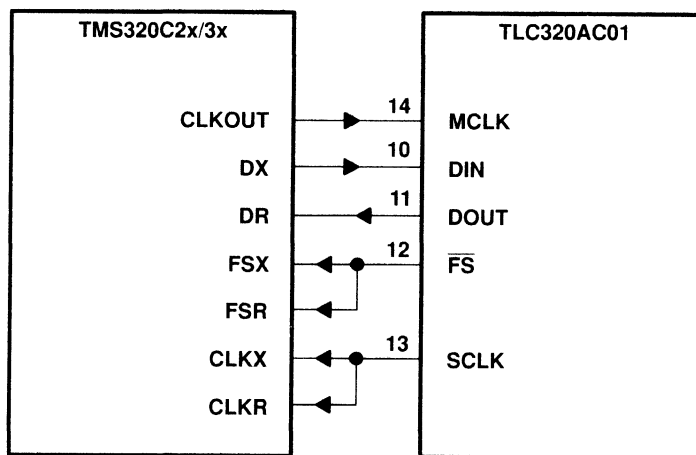
Figure 5-13

6 Application Information



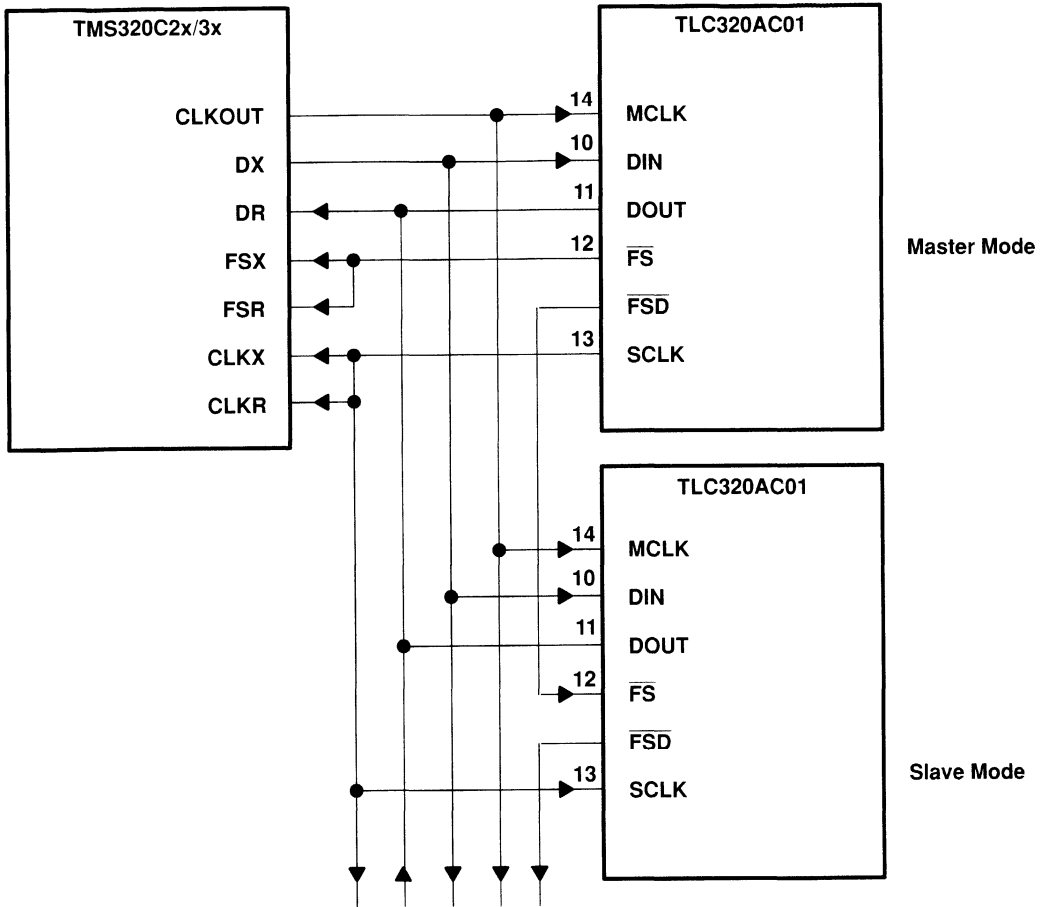
NOTE A: Terminal numbers shown are for the FN package.

Figure 6–1. Stand-Alone Mode (to DSP Interface)



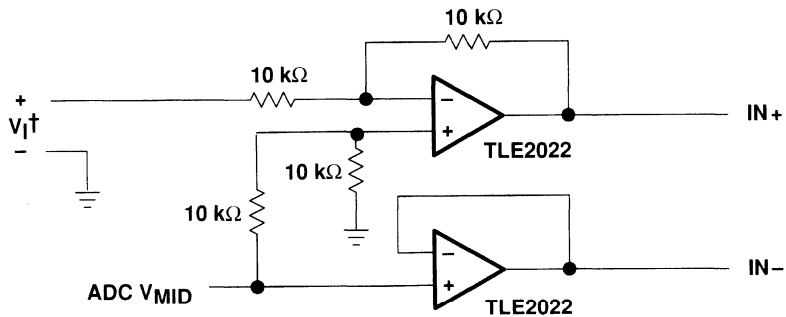
NOTE A: Terminal numbers shown are for the FN package.

Figure 6–2. Codec Mode (to DSP Interface)



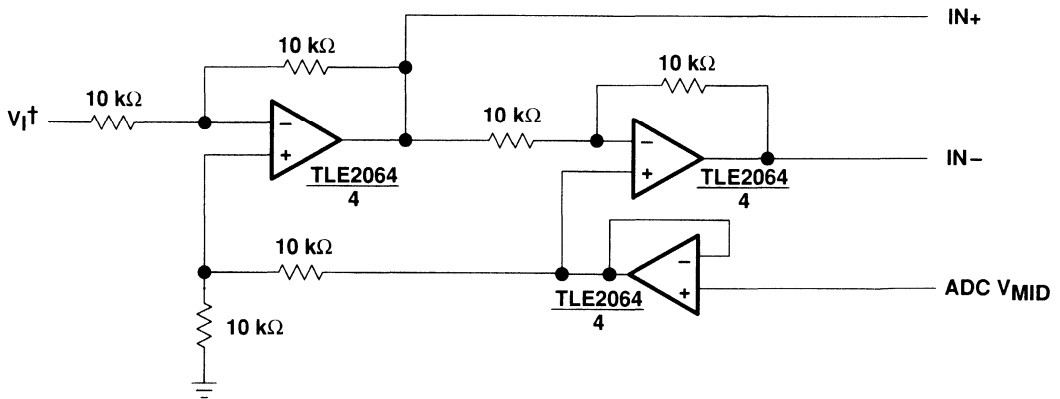
NOTE A: Terminal numbers shown are for the FN package.

Figure 6-3. Master With Slave (to DSP Interface)



† The V_j source must be capable of sinking a current equal to $[ADC V_{MID} + |V_j|(\max)]/10 \text{ k}\Omega$.

Figure 6-4. Single-Ended Input (Ground Referenced)



† The V_I source must be capable of sinking a current equal to $[(ADC V_{MID}/2) + |V_I|(\max)]/10 \text{ k}\Omega$.

Figure 6-5. Single-Ended to Differential Input (Ground Referenced)

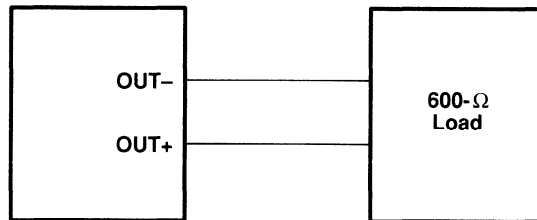
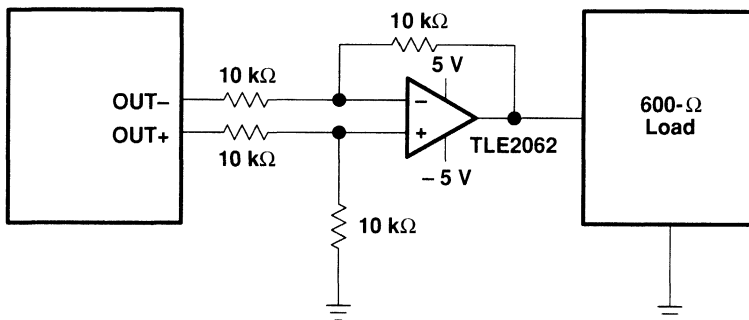


Figure 6-6. Differential Load



NOTE A: When a signal changes from a single supply with a nonzero reference system to a grounded load, the operational amplifier must be powered from plus and minus supplies or the load must be capacitively coupled.

Figure 6-7. Differential Output Drive (Ground Referenced)

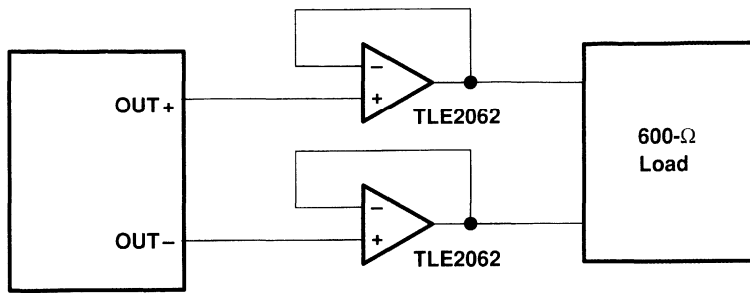
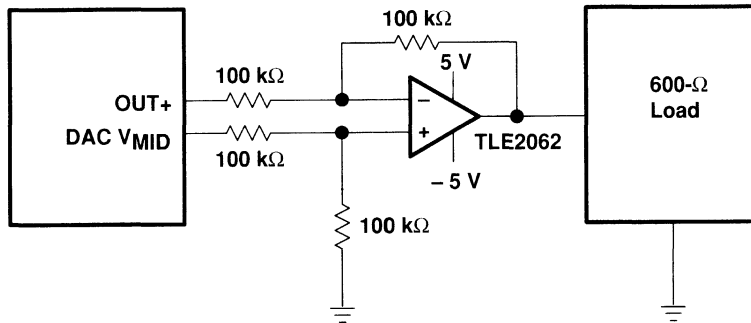


Figure 6-8. Low-Impedance Output Drive



NOTE A: When a signal changes from a single supply with a nonzero reference system to a grounded load, the operational amplifier must be powered from plus and minus supplies or the load must be capacitively coupled.

Figure 6-9. Single-Ended Output Drive (Ground Referenced)

Appendix A

Primary Control Bits

The function of the primary-word control bits D01 and D00 and the hardware terminals FC0 and FC1 are shown below. Any combinational state of D01, D00, FC1, and FC0 not shown is ignored.

CONTROL FUNCTION OF CONTROL BITS

BITS		TERMINALS		
D01	D00	FC1	FC0	
0	0	0	0	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT.
0	0	0	1	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of the next internal \overline{FS} , the next ADC/DAC sampling time occurs later by the number of MCLK periods equal to the value contained in the A' register. When the A' register value is negative, the internal falling edge of \overline{FS} occurs earlier.
0	0	1	0	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the rising edge of the next internal \overline{FS} , the next ADC/DAC sample time occurs earlier by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, the internal falling edge of \overline{FS} occurs later.
0	0	1	1	On the next falling edge of the primary \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. When FC0 and FC1 are both taken high, the AIC initiates a secondary \overline{FS} to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary \overline{FS} .
0	1	0	0	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00 such that on the next rising edge of \overline{FS} , the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, the falling edge of \overline{FS} occurs earlier.
1	0	0	0	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00. On the next rising edge of \overline{FS} , the next ADC/DAC sampling time occurs earlier by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, the internal falling edge of \overline{FS} occurs later.
1	1	0	0	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. When D00 and D01 are both high, the AIC initiates a secondary \overline{FS} to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary \overline{FS} .

CONTROL FUNCTION OF CONTROL BITS (Continued)

BITS		TERMINALS		
D01	D00	FC1	FC0	
0	1	1	1	<p>On the next falling edge of \overline{FS}, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT.</p> <p>The phase adjustment is determined by the state of D01 and D00 such that on the next rising edge of \overline{FS}, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, \overline{FS} occurs earlier.</p> <p>When FC0 and FC1 are both taken high, the AIC initiates a secondary \overline{FS} to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary \overline{FS}.</p>
1	0	1	1	<p>On the next falling edge of \overline{FS}, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.</p> <p>The phase adjustment is determined by the state of D01 and D00. On the next rising edge of \overline{FS}, the next ADC/DAC sample time occurs earlier by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, \overline{FS} occurs later.</p> <p>When FC0 and FC1 are both taken high, the AIC initiates a secondary \overline{FS} to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary \overline{FS}.</p>
1	1	1	1	<p>On the next falling edge of the primary \overline{FS}, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.</p> <p>When FC1 and FC0 are both high or D01 and D00 are both high, the AIC initiates a secondary \overline{FS} to receive a secondary control word at DIN. The secondary \overline{FS} occurs at 1/2 the sampling time measured from the falling edge of the primary \overline{FS}.</p>
1	1	0	1	<p>On the next falling edge of \overline{FS}, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT.</p> <p>When D00 and D01 are high, the AIC initiates a secondary \overline{FS} to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary \overline{FS}.</p> <p>The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of \overline{FS}, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, \overline{FS} occurs earlier.</p>
1	1	1	0	<p>On the next falling edge of \overline{FS}, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT.</p> <p>When D00 and D01 are high, the AIC initiates a secondary \overline{FS} to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary \overline{FS}.</p> <p>The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of \overline{FS}, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, \overline{FS} occurs earlier.</p>
1	1	1	1	<p>On the next falling edge of \overline{FS}, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.</p> <p>When FC1 and FC0 are both high or D01 and D00 are both high, the AIC initiates a secondary \overline{FS} to receive a secondary control word at DIN. The secondary \overline{FS} occurs at 1/2 the sampling time measured from the falling edge of the primary \overline{FS}.</p>

Appendix B

Secondary Communications

The function of the control bits DS15 and DS14 and the hardware terminals FC0 and FC1 are shown below. Any combinational state of DS15, DS14, FC1, and FC0 not shown is ignored.

CONTROL FUNCTION OF SECONDARY COMMUNICATION

BITS		TERMINALS		
DS15	DS14	FC1	FC0	
0	0	Ignored		On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.
0	1	Ignored		On the next falling edge of the \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of DS15 and DS14 such that on the next rising edge of \overline{FS} , the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, \overline{FS} occurs earlier.
1	0	Ignored		On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00. On the next rising edge of \overline{FS} , the next ADC/DAC sampling time occurs earlier by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, \overline{FS} occurs later.
1	1	0	0	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.
1	1	0	1	On the next falling edge of the \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of \overline{FS} , the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, \overline{FS} occurs earlier.
1	1	1	0	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of \overline{FS} , the next ADC/DAC sampling time occurs earlier by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, \overline{FS} occurs later.
1	1	1	1	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.

Appendix C

TLC320AC01C/TLC320AC02C Specification Comparisons

Texas Instruments manufactures the TLC320AC01C and the TLC320AC02C specified for the 0°C to 70°C commercial temperature range and the TLC320AC02I specified for the -40°C to 85°C temperature range. The TLC320AC02C and TLC320AC02I operate at a relaxed TLC320AC01C specification. The differences are listed in the following tables.

ADC Channel Signal-to-Distortion Ratio, $V_{DD} = 5\text{ V}$, $f_s = 8\text{ kHz}$ (Unless Otherwise Noted) (see Note 1)

PARAMETER	TEST CONDITIONS	$A_V = 0\text{ dB}$		$A_V = 6\text{ dB}$		$A_V = 12\text{ dB}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
TLC320AC01	$V_I = -6\text{ dB to } -1\text{ dB}$	68		—		—		dB
TLC320AC02		64		—		—		
TLC320AC01	$V_I = -12\text{ dB to } -6\text{ dB}$	63		68		—		
TLC320AC02		59		64		—		
TLC320AC01	$V_I = -18\text{ dB to } -12\text{ dB}$	57		63		68		
TLC320AC02		56		59		64		
TLC320AC01	$V_I = -24\text{ dB to } -18\text{ dB}$	51		57		63		
TLC320AC02		50		56		59		
TLC320AC01	$V_I = -30\text{ dB to } -24\text{ dB}$	45		51		57		
TLC320AC02		44		50		56		
TLC320AC01	$V_I = -36\text{ dB to } -30\text{ dB}$	39		45		51		
TLC320AC02		38		44		50		
TLC320AC01	$V_I = -42\text{ dB to } -36\text{ dB}$	33		39		45		
TLC320AC02		32		38		44		
TLC320AC01	$V_I = -48\text{ dB to } -42\text{ dB}$	27		33		39		
TLC320AC02		26		32		38		

NOTE 1: The analog-input test signal is a 1020-Hz sine wave with 0 dB = 6 V peak to peak as the reference level for the analog input signal.

DAC Channel Signal-to-Distortion Ratio, $V_{DD} = 5\text{ V}$, $f_s = 8\text{ kHz}$ (Unless Otherwise Noted) (see Note 2)

PARAMETER	TEST CONDITIONS	$A_V = 0\text{ dB}$		$A_V = -6\text{ dB}$		$A_V = -12\text{ dB}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
TLC320AC01	$V_O = -6\text{ dB to } 0\text{ dB}$	68		—		—		dB
TLC320AC02		64		—		—		
TLC320AC01	$V_O = -12\text{ dB to } -6\text{ dB}$	63		68		—		
TLC320AC02		59		64		—		
TLC320AC01	$V_O = -18\text{ dB to } -12\text{ dB}$	57		63		68		
TLC320AC02		56		59		64		
TLC320AC01	$V_O = -24\text{ dB to } -18\text{ dB}$	51		57		63		
TLC320AC02		50		56		59		
TLC320AC01	$V_O = -30\text{ dB to } -24\text{ dB}$	45		51		57		
TLC320AC02		44		50		56		
TLC320AC01	$V_O = -36\text{ dB to } -30\text{ dB}$	39		45		51		
TLC320AC02		38		44		50		
TLC320AC01	$V_O = -42\text{ dB to } -36\text{ dB}$	33		39		45		
TLC320AC02		32		38		44		
TLC320AC01	$V_O = -48\text{ dB to } -42\text{ dB}$	27		33		39		
TLC320AC02		26		32		38		

NOTE 2: The input signal, V_I , is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at full-scale digital input = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT-.

**System Distortion, ADC Channel Attenuation, $V_{DD} = 5\text{ V}$, $f_S = 8\text{ kHz}$,
FCLK = 144 kHz (Unless Otherwise Noted)**

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
TLC320AC01	Second harmonic	Differential input (see Note 3)	70		dB
TLC320AC02			64		dB
TLC320AC01	Third harmonic and higher harmonics		70		dB
TLC320AC02			64		dB

NOTE 3: The input signal is a 1020 Hz-sine wave for the ADC channel. Harmonic distortion is defined for an input level of -1 dB .

**System Distortion, DAC Channel Attenuation, $V_{DD} = 5\text{ V}$, $f_S = 8\text{ kHz}$,
FCLK = 144 kHz (Unless Otherwise Noted)**

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
TLC320AC01	Second harmonic	Differential output (see Note 4)	70		dB
TLC320AC02			64		dB
TLC320AC01	Third harmonic and higher harmonics		70		dB
TLC320AC02			64		dB

NOTE 4: The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is $600\ \Omega$ from OUT+ to OUT-. Harmonic distortion is specified for a signal input level of 0 dB.

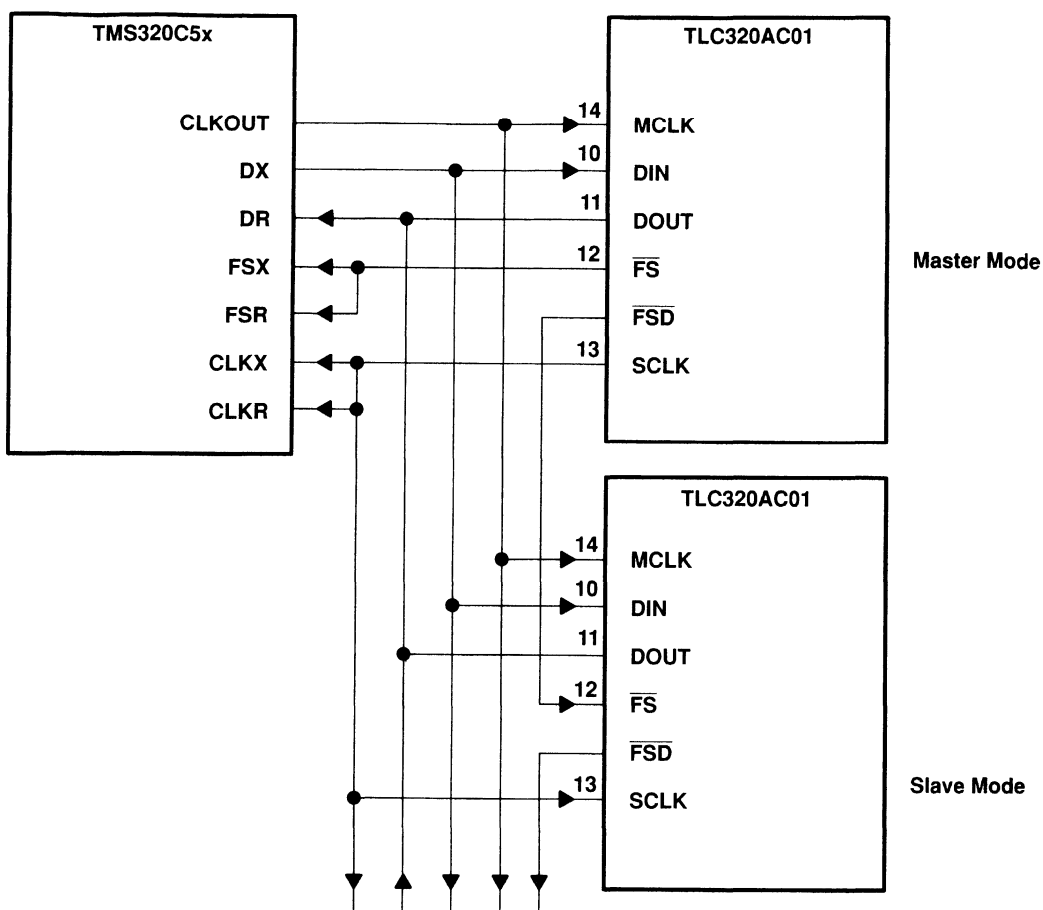
Appendix D

Multiple TLC320AC01/02 Analog Interface Circuits on One TMS320C5X DSP Serial Port

In many applications, digital signal processors (DSP) must obtain information from multiple analog-to-digital (A/D) channels and transmit digital data to multiple digital-to-analog (D/A) conversion channels. The problem is how to do it easily and efficiently.

This application report addresses the issue of connecting two channels of an analog interface circuit (AIC) to one TMS320C5X DSP serial port. In this application report, the AIC is the TLC320AC01.

The TLC320AC01 (and TLC320AC02) analog interface circuit contains both A/D and D/A converters and using the master/slave mode, it is possible to connect two of them to one TMS320C5X DSP serial port with no additional logic. The hardware schematic is shown in Figure D-1.



NOTE A: Terminal numbers shown are for the FN package.

Figure D-1. Master With Slave (to DSP Interface)

HARDWARE AND SOFTWARE SOLUTION

Once the hardware connections are completed, the issue becomes distinguishing one channel from another. Fortunately, this is very easy to do in software and adds very little overhead. The mode that the AC01s run in is called master/slave mode. One AC01 is the master and all of the rest of the AC01s are slaves. The master can be distinguished from all of the slaves by examining the least significant bit (LSB) in the receive word coming from the AC01. The master has a 0 in the LSB and all of the slaves have a 1 in the LSB.

The AC01s in master/slave mode take turns communicating with the DSP serial port. They do this in a round robin or circular fashion. Synchronizing the system involves looking for the master AC01 and then starting the software associated with the first AC01. All other AC01s follow in order. It is possible to have different software for each AC01.

A reference design was constructed using a TMS320C5X DSP starter kit (DSK). The AC01s were connected to the TDM serial port which is available at the headers on the edge of the DSK.

A listing of the DSK assembly code for a simple stereo input/output program is included in the following section.

SOFTWARE MODULE

```
*****
*
* MODULE NAME: INOUTB.ASM
*
* In-out routine for C5X DSK with two TLC320AC01s on the
* TDM serial port of the C5X in master/slave mode.
*
* This version performs the in/out task for both the master
* and slave TLC320AC01 in the receive interrupt service
* routine.
*
*
*****
```

```
*          .mmregs
*
*          .ds          01000h
*
PR1        .word       0104h          ;A register
PR2        .word       0219h          ;B register
PR3        .word       0300h          ;A prime register
PR4        .word       0405h          ;amplifier gain register
PR5        .word       0501h          ;analog configuration register
PR6        .word       0600h          ;digital configuration register
PR7        .word       0730h          ;frame synch delay register
PR8        .word       0802h          ;frame synch number register
value     .word       0800h
value2    .word       0800h
val_add   .word       0200h
val_add2  .word       0400h
```

```
*****
*
* Set up the ISR vector
*
*****
```

```
          .ps          080ah
rint:     B           RECEIVE          ; 0A; Serial port receive interrupt RINT.
xint:     B           TRANSMIT         ; 0C; Serial port transmit interrupt XINT.
trint:    B           TDMREC
txint:    B           TDMTX
;-----
```

```
*
*****
*
* TMS320C5X INITIALIZATION
*
*****
```

```
          .ps 0a00h
          .entry
START:    SETC         INTM            ; Disable interrupts
          LDP          #0              ; Set data page pointer
          OPL          #0834h, PMST
          LACC         #0
          SAMP         CWSR
          SAMP         PDWSR
```

```

    splk      #00c8h
    SPLK      082h,IMR
    call      AC01INIT

    CLRC      OVM          ; OVM = 0
    SPM       0            ; PM = 0
    SPLK      #042h,IMR    ; TDMA ser port rec interrupt
    SPLK      #0C8h,TSPC   ;
    CLRC      INTM         ; enable interrupts

loop                                ; main program here does nothing.
    nop                                             ; a user program can be inserted.
    b        loop                                  ;

;----- end of main program ----- ;
;
; TDM serial port receiver interrupt service routine
;
TDMREC:
                                ; This loop insures that the master AC01
    ldp      #trcv              ; is the first one that is written to in the
    bit     trcv,15            ; loop. the slave AC01(s) will follow in
    bcnd    xxx,tc             ; sequential order. The master AC01 has a
                                ; 0 in the 1sb. the slave AC01(s) have a 1
                                ; in the 1sb of the receive word.

    ldp      #trcv
    lacc    trcv
    and     #0fffch

                                ;
                                ; user code would go here for master AC01
                                ;

    sacl    tdxr
    b       YYY

xxx

    ldp      #trcv
    lacc    trcv
    and     #0fffch

                                ;
                                ; user code would go here for slave AC01
                                ;

    sacl    tdxr

YYY

    rete

```

```
;
; TDM serial port transmit interrupt service routine
;
TDMTX:
    rete

;
; RECEIVER INTERRUPT SERVICE ROUTINE
;
RECEIVE:
    rete

TRANSMIT:
    RETE
```

AC01INIT

```
SPLK      #020h,TCR
SPLK      #01h,PRD
MAR        *,AR0
LACC      #0008h
SACL      TSPC
LACC      #00c8h
SACL      TSPC
SETC      SXM
```

;-----

```
LDP       #PR1
LACC      PR1
CALL     AC01_2ND
```

;-----

```
LDP       #PR2
LACC      PR2
CALL     AC01_2ND
```

;-----

```
LDP       #PR8
LACC      PR8
CALL     AC01_2ND
```

;-----

```
LDP       #PR7
LACC      PR7
CALL     AC01_2ND
```

ret

AC01_2ND:

```
LDP       #0
SACH      TDXR      ;
CLRC      INTM
IDLE
ADD       #6h, 15      ; 0000 0000 0000 0011 XXXX XXXX XXXX XXXX b
SACH      TDXR      ;
IDLE
SACL      TDXR      ;
IDLE
LACL      #0          ;
SACL      TDXR      ; make sure the word got sent
IDLE
SETC      INTM      ;
RET
```

TLC320AC02C, TLC320AC02I ***Data Manual***

Single-Supply Analog Interface Circuit

SLAS084C
October 1997



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Contents

<i>Section</i>	<i>Title</i>	<i>Page</i>
1	Introduction	4–281
1.1	Features	4–282
1.2	Functional Block Diagram	4–283
1.3	Terminal Assignments	4–283
1.4	Terminal Functions	4–285
1.5	Register Functional Summary	4–288
2	Detailed Description	4–289
2.1	Definitions and Terminology	4–289
2.2	Reset and Power-Down Functions	4–290
2.2.1	Reset	4–290
2.2.2	Conditions of Reset	4–290
2.2.3	Software and Hardware Power-Down	4–290
2.2.4	Register Default Values After POR, Software Reset or RESET Is Applied	4–290
2.3	Master-Slave Terminal Function	4–292
2.4	ADC Signal Channel	4–292
2.5	DAC Signal Channel	4–292
2.6	Serial Interface	4–292
2.7	Number of Slaves	4–293
2.8	Required Minimum Number of MCLK Periods	4–294
2.8.1	TLC320AC02 AIC Master-Slave Summary	4–294
2.8.2	Notes on TLC320AC01/02 AIC Master-Slave Operation	4–295
2.9	Operating Frequencies	4–297
2.9.1	Master and Stand-Alone Operating Frequencies	4–297
2.9.2	Slave and Codec Operating Frequencies	4–297
2.10	Switched-Capacitor Filter Frequency (FCLK)	4–297
2.11	Filter Bandwidths	4–297
2.12	Master and Stand-Alone Modes	4–297
2.12.1	Register Programming	4–297
2.12.2	Master and Stand-Alone Functional Sequence	4–298
2.13	Slave and Codec Modes	4–298
2.13.1	Slave and Codec Functional Sequence	4–299
2.13.2	Slave Register Programming	4–299
2.14	Terminal Functions	4–299
2.14.1	Frame-Sync Function	4–299
2.14.2	Data Out (DOUT)	4–300
2.14.3	Data In (DIN)	4–300
2.14.4	Hardware Program Terminals (FC1 and FC0)	4–300
2.14.5	Midpoint Voltages (ADC V_{MID} and DAC V_{MID})	4–301

2.15	Device Functions	4-301
2.15.1	Phase Adjustment	4-301
2.15.2	Analog Loopback	4-302
2.15.3	16-Bit Mode	4-302
2.15.4	Free-Run Mode	4-302
2.15.5	Force Secondary Communication	4-302
2.15.6	Enable Analog Input Summing	4-303
2.15.7	DAC Channel (sin x)/x Error Correction	4-303
2.16	Serial Communications	4-303
2.16.1	Stand-Alone and Master-Mode Word Sequence and Information Content During Primary and Secondary Communications	4-303
2.16.2	Slave and Codec-Mode Word Sequence and Information Content During Primary and Secondary Communications	4-304
2.17	Request for Secondary Serial Communication and Phase Shift	4-305
2.17.1	Initiating a Request	4-305
2.17.2	Normal Combinations of Control	4-305
2.17.3	Additional Control Options	4-305
2.18	Primary Serial Communications	4-306
2.18.1	Primary Serial Communications Data Format	4-307
2.18.2	Data Format From DOUT During Primary Serial Communications	4-307
2.19	Secondary Serial Communications	4-307
2.19.1	Data Format to DIN During Secondary Serial Communications	4-307
2.19.2	Control Data-Bit Function in Secondary Serial Communication	4-307
2.20	Internal Register Format	4-308
2.20.1	Pseudo-Register 0 (No-Op Address)	4-308
2.20.2	Register 1 (A Register)	4-308
2.20.3	Register 2 (B Register)	4-309
2.20.4	Register 3 (A' Register)	4-309
2.20.5	Register 4 (Amplifier Gain-Select Register)	4-310
2.20.6	Register 5 (Analog Configuration Register)	4-310
2.20.7	Register 6 (Digital Configuration Register)	4-311
2.20.8	Register 7 (Frame-Sync Delay Register)	4-311
2.20.9	Register 8 (Frame-Sync Number Register)	4-312
3	Specifications	4-313
3.1	Absolute Maximum Ratings Over Operating Free-Air Temperature Range	4-313
3.2	Recommended Operating Conditions	4-313
3.3	Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, MCLK = 5.184 MHz, V _{DD} = 5 V, Outputs Unloaded, Total Device	4-314
3.4	Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, V _{DD} = 5 V, Digital I/O Terminals (DIN, DOUT, EOC, FC0, FC1, FS, FSD, MCLK, M/S, SCLK)	4-314
3.5	Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, V _{DD} = 5 V, ADC and DAC Channels	4-314
3.5.1	ADC Channel Filter Transfer Function, FCLK = 144 kHz, f _s = 8 kHz	4-314
3.5.2	ADC Channel Input, V _{DD} = 5 V, Input Amplifier Gain = 0 dB	4-315
3.5.3	ADC Channel Signal-to-Distortion Ratio, V _{DD} = 5 V, f _s = 8 kHz	4-315

3.5.4	DAC Channel Filter Transfer Function, FCLK = 144 kHz, $f_s = 9.6$ kHz, $V_{DD} = 5$ V	4-315
3.5.5	DAC Channel Signal-to-Distortion Ratio, $V_{DD} = 5$ V, $f_s = 8$ kHz	4-316
3.5.6	System Distortion, $V_{DD} = 5$ V, $f_s = 8$ kHz, FCLK = 144 kHz	4-316
3.5.7	Noise, Low-Pass and Band-Pass Switched-Capacitor Filters Included, $V_{DD} = 5$ V	4-317
3.5.8	Absolute Gain Error, $V_{DD} = 5$ V, $f_s = 8$ kHz	4-317
3.5.9	Relative Gain and Dynamic Range, $V_{DD} = 5$ V, $f_s = 8$ kHz	4-317
3.5.10	Power-Supply Rejection, $V_{DD} = 5$ V	4-318
3.5.11	Crosstalk Attenuation, $V_{DD} = 5$ V	4-318
3.5.12	Monitor Output Characteristics, $V_{DD} = 5$ V	4-319
3.6	Timing Requirements and Specifications in Master Mode	4-320
3.6.1	Recommended Input Timing Requirements for Master Mode, $V_{DD} = 5$ V	4-320
3.6.2	Operating Characteristics Over Recommended Range of Operating Free-Air Temperature, $V_{DD} = 5$ V	4-320
3.7	Timing Requirements and Specifications in Slave Mode and Codec Emulation Mode	4-321
3.7.1	Recommended Input Timing Requirements for Slave Mode, $V_{DD} = 5$ V	4-321
3.7.2	Operating Characteristics Over Recommended Range of Operating Free-Air Temperature, $V_{DD} = 5$ V	4-321
4	Parameter Measurement Information	4-323
5	Typical Characteristics	4-329
6	Application Information	4-343
A	Primary Control Bits	4-347
B	Secondary Communications	4-349
C	TLC320AC01C/TLC320AC02C Specification Comparisons	4-351
D	Multiple TLC320AC01/02 Analog Interface Circuits on One TMS320C5X DSP Serial Port	4-355

List of Illustrations

<i>Figure</i>	<i>Title</i>	<i>Page</i>
1–1	Control Flow Diagram	4–287
2–1	Functional Sequence for Primary and Secondary Communication	4–293
2–2	Timing Sequence	4–294
2–3	Master and Stand-Alone Functional Sequence	4–304
2–4	Slave and Codec Functional Sequence	4–304
4–1	IN+ and IN– Gain-Control Circuitry	4–323
4–2	AIC Stand-Alone and Master-Mode Timing	4–324
4–3	AIC Slave and Codec Emulation Mode	4–324
4–4	Master or Stand-Alone FS and FSD Timing	4–325
4–5	Slave FS to FSD Timing	4–325
4–6	Slave SCLK to FSD Timing	4–325
4–7	DOUT Enable Timing From Hi-Z	4–326
4–8	DOUT Delay Timing to Hi-Z	4–326
4–9	EOC Frame Timing	4–326
4–10	Master-Slave Frame-Sync Timing After a Delay Has Been Programmed Into the FSD Registers	4–327
4–11	Master and Slave Frame-Sync Sequence with One Slave	4–327
5–1	ADC Low-Pass Response	4–329
5–2	ADC Low-Pass Response	4–330
5–3	ADC Group Delay	4–331
5–4	ADC Band-Pass Response	4–332
5–5	ADC Band-Pass Response	4–333
5–6	ADC High-Pass Response	4–334
5–7	ADC Band-Pass Group Delay	4–335
5–8	DAC Low-Pass Response	4–336
5–9	DAC Low-Pass Response	4–337
5–10	DAC Low-PASS Group Delay	4–338
5–11	DAC (sin x)/x Correction Filter Response	4–339
5–12	DAC (sin x)/x Correction Filter Response	4–340
5–13	DAC (sin x)/x Correction Error	4–341

List of Tables

<i>Table</i>	<i>Title</i>	<i>Page</i>
1-1	Operating Frequencies	4-287
2-1	Master-Slave Selection	4-292
2-2	Sampling Variation With A'	4-301
2-3	Software and Hardware Requests for Secondary Serial-Communication and Phase-Shift Truth Table	4-306
4-1	Gain Control	4-323

1 Introduction

The TLC320AC02† analog interface circuit (AIC) is an audio-band processor that provides an analog-to-digital and digital-to-analog input/output interface system on a single monolithic CMOS chip. This device integrates a band-pass switched-capacitor antialiasing input filter, a 14-bit-resolution analog-to-digital converter (ADC), a 14-bit-resolution digital-to-analog converter (DAC), a low-pass switched-capacitor output-reconstruction filter, $(\sin x)/x$ compensation, and a serial port for data and control transfers.

The internal circuit configuration and performance parameters are determined by reading control information into the eight available data registers. The register data sets up the device for a given mode of operation and application.

The major functions of the TLC320AC02 are:

1. To convert audio-signal data to digital format by the ADC channel
2. To provide the interface and control logic to transfer data between its serial input and output terminals and a digital signal processor (DSP) or microprocessor
3. To convert received digital data back to an audio signal through the DAC channel

The antialiasing input low-pass filter is a switched-capacitor filter with a sixth-order elliptic characteristic. The high-pass filter is a single-pole filter to preserve low-frequency response as the low-pass filter cutoff is adjusted. There is a three-pole continuous-time filter that precedes this filter to eliminate any aliasing caused by the filter clock signal.

The output-reconstruction switched-capacitor filter is a sixth-order elliptic transitional low-pass filter followed by a second-order $(\sin x)/x$ correction filter. This filter is followed by a three-pole continuous-time filter to eliminate images of the filter clock signal.

The TLC320AC02 consists of two signal-processing channels, an ADC channel and a DAC channel, and the associated digital control. The two channels operate synchronously; data reception at the DAC channel and data transmission from the ADC channel occur during the same time interval. The data transfer is in 2s-complement format.

There are three basic modes of operation available: the stand-alone analog-interface mode, the master-slave mode, and the linear-codec mode. In the stand-alone mode, the TLC320AC02 generates the shift clock and frame synchronization for the data transfers and is the only AIC used. The master-slave mode has one TLC320AC02 as the master that generates the master-shift clock and frame synchronization; the remaining AICs are slaves to these signals. In the linear-codec mode, the shift clock and the frame-synchronization signals are externally generated and the timing can be any of the standard codec-timing patterns.

Typical applications for this device include modems, speech processing, analog interface for DSPs, industrial-process control, acoustical-signal processing, spectral analysis, data acquisition, and instrumentation recorders.

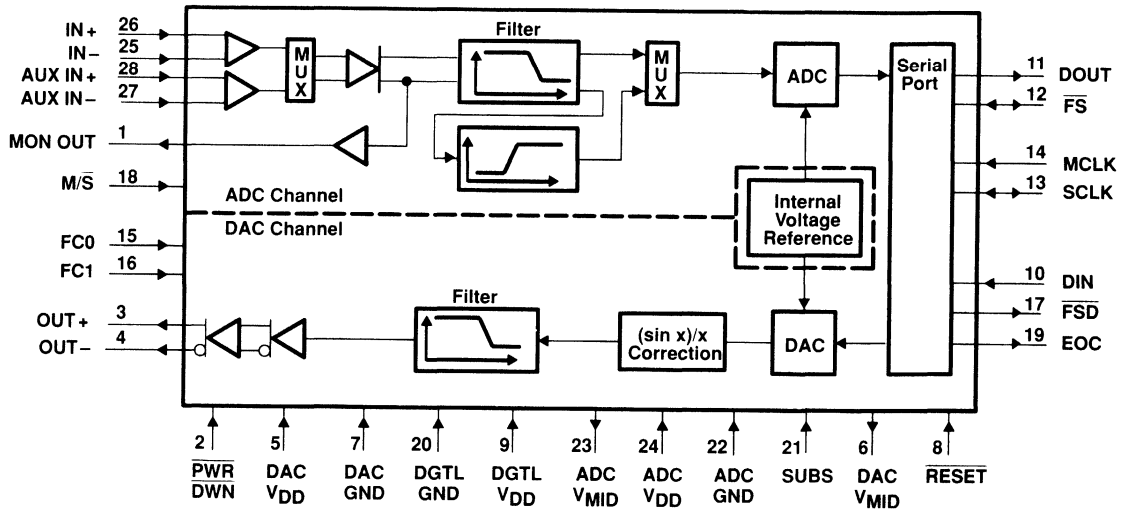
The TLC320AC02C is characterized for operation from 0°C to 70°C and the TLC320AC02I is characterized for operation from -40°C to 85°C.

† The TLC320AC02 is functionally equivalent to the TLC320AC01 and differs in the electrical specifications as shown in Appendix C.

1.1 Features

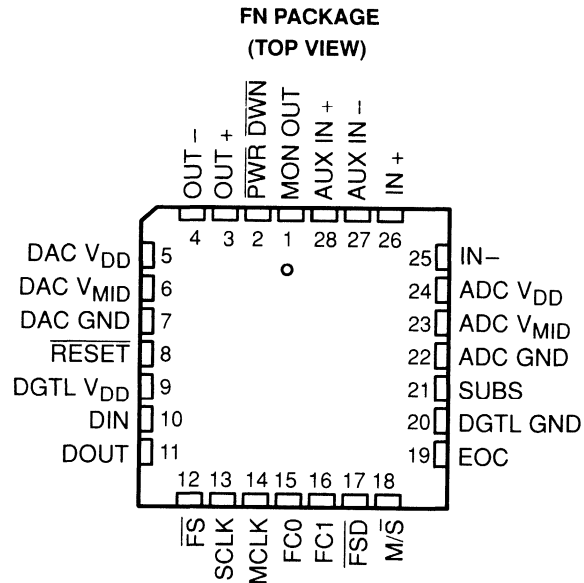
- General-Purpose Signal-Processing Analog Front End (AFE)
- Single 5-V Power Supply
- Power Dissipation . . . 100 mW Typ
- Signal-to-Distortion Ratio . . . 70 dB Typ
- Programmable Filter Bandwidths (Up to 10.8 kHz) and Synchronous ADC and DAC Sampling
- Serial-Port Interface
- Monitor Output With Programmable Gains of 0 dB, –8 dB, –18 dB, and Squelch
- Two Sets of Differential Inputs With Programmable Gains of 0 dB, 6 dB, 12 dB, and Squelch
- Differential or Single-Ended Analog Output With Programmable Gains of 0 dB, –6 dB, –12 dB, and Squelch
- Differential Outputs Drive 3-V Peak Into a 600- Ω Differential Load
- Differential Architecture Throughout
- 1- μ m Advanced LinEPIC™ Process
- 14-Bit Dynamic-Range ADC and DAC
- 2s-Complement Data Format

1.2 Functional Block Diagram

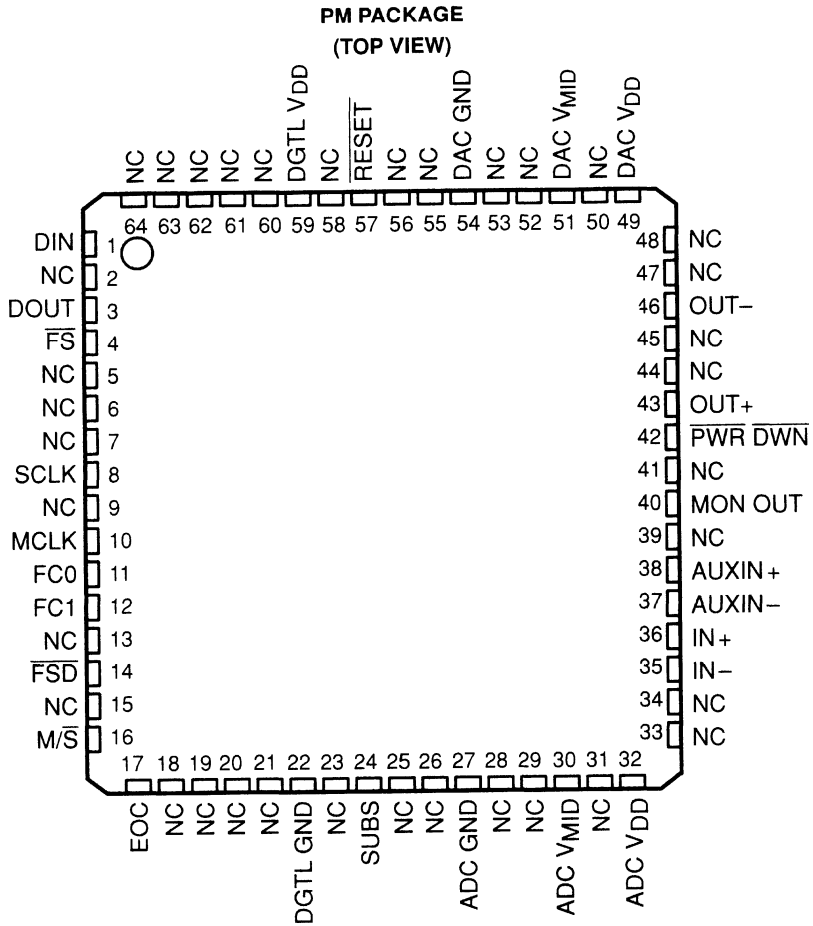


Terminal numbers shown are for the FN package.

1.3 Terminal Assignments



1.3 Terminal Assignments (Continued)



NC – No internal connection

1.4 Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.†	NO.‡		
ADC V _{DD}	24	32	I	Analog supply voltage for the ADC channel
ADC V _{MID}	23	30	O	Midsupply for the ADC channel (requires a bypass capacitor). ADC V _{MID} must be buffered when used as an external reference.
ADC GND	22	27	I	Analog ground for the ADC channel
AUX IN+	28	38	I	Noninverting input to auxiliary analog input amplifier
AUX IN–	27	37	I	Inverting input to auxiliary analog input amplifier
DAC V _{DD}	5	49	I	Digital supply voltage for the DAC channel
DAC V _{MID}	6	51	O	Midsupply for the DAC channel (requires a bypass capacitor). DAC V _{MID} must be buffered when used as an external reference.
DAC GND	7	54	I	Analog ground for the DAC channel
DIN	10	1	I	Data input. DIN receives the DAC input data and command information and is synchronized with SCLK.
DOUT	11	3	O	Data output. DOUT outputs the ADC data results and register read contents. DOUT is synchronized with SCLK.
DGTL V _{DD}	9	59	I	Digital supply voltage for control logic
DGTL GND	20	22	I	Digital ground for control logic
EOC	19	17	O	End-of-conversion output. EOC goes high at the start of the ADC conversion period and low when conversion is complete. EOC remains low until the next ADC conversion period begins and indicates the internal device conversion period.
FC0	15	11	I	Hardware control input. FC0 is used in conjunction with FC1 to request secondary communication and phase adjustments. FC0 should be tied low if it is not used.
FC1	16	12	I	Hardware control input. FC1 is used in conjunction with FC0 to request secondary communication and phase adjustments. FC1 should be tied low if it is not used.
FS	12	4	I/O	Frame synchronization. When FS goes low, DIN begins receiving data bits and DOUT begins transmitting data bits. In master mode, FS is low during the simultaneous 16-bit transmission to DIN and from DOUT. In slave mode, FS is externally generated and must be low for one shift-clock period minimum to initiate the data transfer.
FSD	17	14	O	Frame-synchronization delayed output. This active-low output synchronizes a slave device to the frame synchronization timing of the master device. FSD is applied to the slave FS input and is the same duration as the master FS signal but delayed in time by the number of shift clocks programmed in the FSD register.
IN+	26	36	I	Noninverting input to analog input amplifier
IN–	25	35	I	Inverting input to analog input amplifier
MCLK	14	10	I	The master-clock input drives all the key logic signals of the AIC.
MON OUT	1	40	O	The monitor output allows monitoring of analog input and is a high-impedance output.
M/S	18	16	I	Master/slave select input. When M/S is high, the device is the master and when low, it is a slave.

† Terminal numbers shown are for the FN package.

‡ Terminal numbers shown are for the PM package.

1.4 Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.†	NO.‡		
OUT+	3	43	O	Noninverting output of analog output power amplifier. OUT+ can drive transformer hybrids or high-impedance loads directly in a differential connection or a single-ended configuration with a buffered V _{MID} .
OUT-	4	46	O	Inverting output of analog output power amplifier. OUT- is functionally identical with and complementary to OUT+.
PWR DWN	2	42	I	Power-down input. When PWR DWN is taken low, the device is powered down such that the existing internally programmed state is maintained. When PWR DWN is brought high, full operation resumes.
RESET	8	57	I	Reset input that initializes the internal counters and control registers. RESET initiates the serial data communications, initializes all of the registers to their default values, and puts the device in a preprogrammed state. After a low-going pulse on RESET, the device registers are initialized to provide a 16-kHz data-conversion rate and 7.2-kHz filter bandwidth for a 10.368-MHz master clock input signal.
SCLK	13	8	I/O	Shift clock. SCLK clocks the digital data into DIN and out of DOUT during the frame-synchronization interval. When configured as an output (M/S high), SCLK is generated internally by dividing the master clock signal frequency by four. When configured as an input (M/S low), SCLK is generated externally and synchronously to the master clock. This signal clocks the serial data into and out of the device.
SUBS	21	24	I	Substrate connection. SUBS should be tied to ADC GND.

† Terminal numbers shown are for the FN package.

‡ Terminal numbers shown are for the PM package.

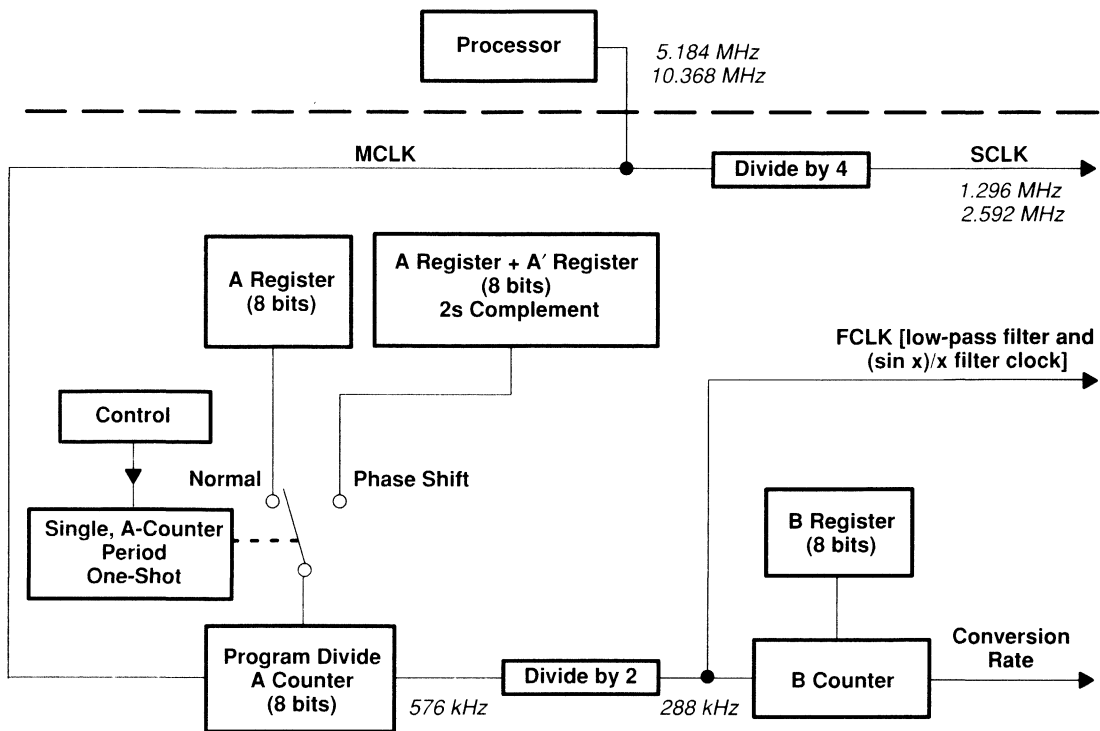


Figure 1–1. Control Flow Diagram

Table 1–1. Operating Frequencies

FCLK (kHz)	LOW-PASS FILTER BANDWIDTH (kHz)	B REGISTER CONTENTS (Program No. of Filter Clocks) (Decimal)	CONVERSION RATE (kHz)	HIGH-PASS POLE FREQUENCY (Hz)
144	3.6	20 (see Note 1)	7.2	36
		18	8	40
		15	9.6	48
		10 (see Note 2)	14.4	72
288	7.2	20 (see Note 1)	14.4	72
		18	16	80
		15	19.2	96
		10 (see Notes 2 and 3)	28.8	144
432	10.8	20 (see Note 1)	21.6	108
		18	24	120
		15 (see Note 3)	28.8	144
		10 (see Notes 2 and 3)	43.2	216

- NOTES: 1. The B register can be programmed for values greater than 20; however, since the sample rate is lower than 7.2 kHz and the internal filter remains at 3.6 kHz, an external antialiasing filter is required.
2. When the B register is programmed for a value less than 10, the ADC and the DAC conversions are not completed before the next frame-sync signal and the results are in error.
3. The maximum sampling rate for the ADC channel is 43.2 kHz. The maximum rate for the DAC channel is 25 kHz.

1.5 Register Functional Summary

There are nine data registers that are used as follows:

- Register 0 The No-op register. The 0 address allows phase adjustments to be made without reprogramming a data register.
- Register 1 The A register controls the count of the A counter.
- Register 2 The B register controls the count of the B counter.
- Register 3 The A' register controls the phase adjustment of the sampling period. The adjustment is equal to the register value multiplied by the input master period.
- Register 4 The amplifier gain register controls the gains of the input, output, and monitor amplifiers.
- Register 5 The analog configuration register controls:
- The addition/deletion of the high-pass filter to the ADC signal path
 - The enable/disable of the analog loopback
 - The selection of the regular inputs or auxiliary inputs
 - The function that allows processing of signals that are the sum of the regular inputs and the auxiliary inputs ($V_{IN} + V_{AUX IN}$)
- Register 6 The digital configuration register controls:
- Selection of the free-run function
 - \overline{FSD} [frame-synchronization (sync) delay] output enable/disable
 - Selection of 16-bit function
 - Forcing secondary communications
 - Software reset
 - Software power down
- Register 7 The frame-sync delay register controls the time delay between the master-device frame sync and slave-device frame sync. Register 7 must be the last register programmed when using slave devices since all register data is latched and valid on the sixteenth falling edge of SCLK. On the sixteenth falling edge of SCLK, all delayed frame-sync intervals are shifted by this programmed amount.
- Register 8 The frame-sync number register informs the master device of the number of slaves that are connected in the chain. The frame-sync number is equal to the number of slaves plus one.

2 Detailed Description

2.1 Definitions and Terminology

ADC Channel	All signal processing circuits between the analog input and the digital conversion results at DOUT
Codec Mode	The operating mode under which the device receives shift clock and frame-sync signals from a host processor. The device has no slaves.
d	The d represents valid programmed or default data in the control register format (see Section 2.19) when discussing other data-bit portions of the register.
Dxx	Bit position in the primary data word (xx is the bit number)
DAC Channel	All signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUT+ and OUT-
Data Transfer Interval	The time during which data is transferred from DOUT and to DIN. This interval is 16 shift clocks regardless of whether the shift clock is internally or externally generated. The data transfer is initiated by the falling edge of the frame-sync signal.
DSxx	Bit position in the secondary data word (xx is the bit number)
FCLK	An internal clock frequency that is a division of MCLK that controls the low-pass filter and (sinx)/x filter clock (see Figure 1-1 and Table 1-1).
f _i	The analog input frequency of interest
Frame Sync	The falling edge of the signal that initiates the data-transfer interval. The primary frame sync starts the primary communications, and the secondary frame sync starts the secondary communications.
Frame Sync and Sampling Period	The time between falling edges of successive primary frame-sync signals
Frame-Sync Interval	The time period occupied by 16 shift clocks. Regardless of the mode of operation, there is always an internal frame-sync interval signal that goes low on the rising edge of SCLK and remains low for 16 shift clocks. It is used for synchronization of the serial-port internal signals. It goes high on the seventeenth rising edge of SCLK.
f _s	The sampling frequency that is the reciprocal of the sampling period.
Host	Any processing system that interfaces to DIN, DOUT, SCLK, or FS.
Master Mode	The operating mode under which the device generates and uses its own shift clock and frame-sync signal and generates all delayed frame-sync signals necessary to support slave devices.
Phase Adjustment	The programmed time variation from the falling edge of one frame-sync signal to the falling edge of the next frame sync signal. The time variation is determined by the contents of the A' register. Since the time between falling edges of successive frame-sync signals is the the sampling period, the sampling period is adjusted.
Primary (Serial) Communications	The digital data-transfer interval. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.
Secondary (Serial) Communications	The digital control and configuration data-transfer interval into DIN and the register read-data cycle from DOUT. The data-transfer interval occurs when requested by hardware or software.
Signal Data	The input signal and all of the converted representations through the ADC channel and return through the DAC channel to the analog output. This is contrasted with the purely digital software-control data.
Slave Mode	The operating mode under which the device receives shift clock and frame-sync signals from a master device.

- Stand-Alone Mode The operating mode under which the device generates and uses its own shift clock and frame-sync signal. The device has no slave devices.
- X The X represents a don't-care bit position within the control register format.

2.2 Reset and Power-Down Functions

2.2.1 Reset

The TLC320AC02 resets both the internal counters and registers, including the programmed registers, by any of the following:

- Applying power to the device, causing a power-on reset (POR)
- Applying a low reset pulse to $\overline{\text{RESET}}$
- Reading in the programmable software reset bit (DS01 in register 6)

$\overline{\text{PWR DWN}}$ resets the counters only and preserves the programmed register contents.

2.2.2 Conditions of Reset

The two internal reset signals used for the reset and synchronization functions are as follows:

1. Counter reset: This signal resets all flip-flops and latches that are not externally programmed with the exception of those generating the reset pulse itself. In addition, this signal resets the software power-down bit.

$$\text{Counter reset} = \text{power-on reset} + \overline{\text{RESET}} + \text{RESET bit} + \overline{\text{PWR DWN}}$$

2. Register reset: This signal resets all flip-flops and latches that are not reset by the counter reset except those generating the reset pulse itself.

$$\text{Register reset} = \text{power-on reset} + \overline{\text{RESET}} + \text{RESET bit}$$

Both reset signals are at least one master-clock period long and release on the falling edge of the master clock.

2.2.3 Software and Hardware Power-Down

Given the definitions and conditions of $\overline{\text{RESET}}$, the software-programmed power-down condition is cleared by resetting the software bit (DS00 in register 6) to zero. It is also cleared by either cycling the power to the device, bringing $\overline{\text{PWR DWN}}$ low, or bringing $\overline{\text{RESET}}$ low.

$\overline{\text{PWR DWN}}$ powers down the entire chip (< 1 mA). The software-programmable power-down bit only powers down the analog section of the chip (< 3 mA), which allows a software power-up function. Cycling $\overline{\text{PWR DWN}}$ high to low and back to high resets all flip-flops and latches that are not externally programmed, thereby preserving the register contents.

When $\overline{\text{PWR DWN}}$ is not used, it should be tied high.

2.2.4 Register Default Values After POR, Software Reset, or $\overline{\text{RESET}}$ Is Applied

Register 1 – The A Register

The default value of the A-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

Register 2 – The B Register

The default value of the B-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

Register 3 – The A' Register

The default value of the A'-register data is decimal 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

Register 4 – The Amplifier Gain-Select Register

The default value of the amplifier gain-select register data is shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	1	0	1

Register 5 – The Analog Control-Configuration Register

The power-up and reset conditions are as shown below. In the read mode, 8 bits are read but the 4 LSBs are repeated as the 4 MSBs.

DS03	DS02	DS01	DS00
0	0	0	1

Register 6 – The Digital Configuration Register

The default value of DS07 – DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

Register 7 – The Frame-Sync Delay Register

The default value of DS07 – DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

Register 8 – The Frame-Sync Number Register

The default value of DS07 – DS00 is 1 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	1

2.3 Master-Slave Terminal Function

Table 2–1 describes the function of the master/slave (M/\bar{S}) input. The only difference between master and slave operations in the TLC320AC02 is that SCLK and \bar{FS} are outputs when M/\bar{S} is high and inputs when M/\bar{S} is low.

Table 2–1. Master-Slave Selection

MODE	M/\bar{S}^\dagger	\bar{FS}	SCLK
Master and Stand Alone	H	Output	Output
Slave and Codec Emulation	L	Input	Input

[†] When the stand-alone mode is desired or when the device is permanently in the master mode, M/\bar{S} must be high.

2.4 ADC Signal Channel

To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data. The signal is amplified by the input amplifier at one of three software-selectable gains (typically 0 dB, 6 dB, or 12 dB). A squelch mode can also be programmed for the input amplifier.

The amplifier output is filtered and applied to the ADC input. The ADC converts the signal into discrete digital words in 2s-complement format corresponding to the analog-signal value at the sampling time. These 16-bit digital words, representing sampled values of the analog input signal, are clocked out of the serial port (DOUT), one word for each primary communication interval. During secondary communications, the data previously programmed into the registers can be read out with the appropriate register address and with the read bit set to 1. When a register read is not requested, all 16 bits are 0.

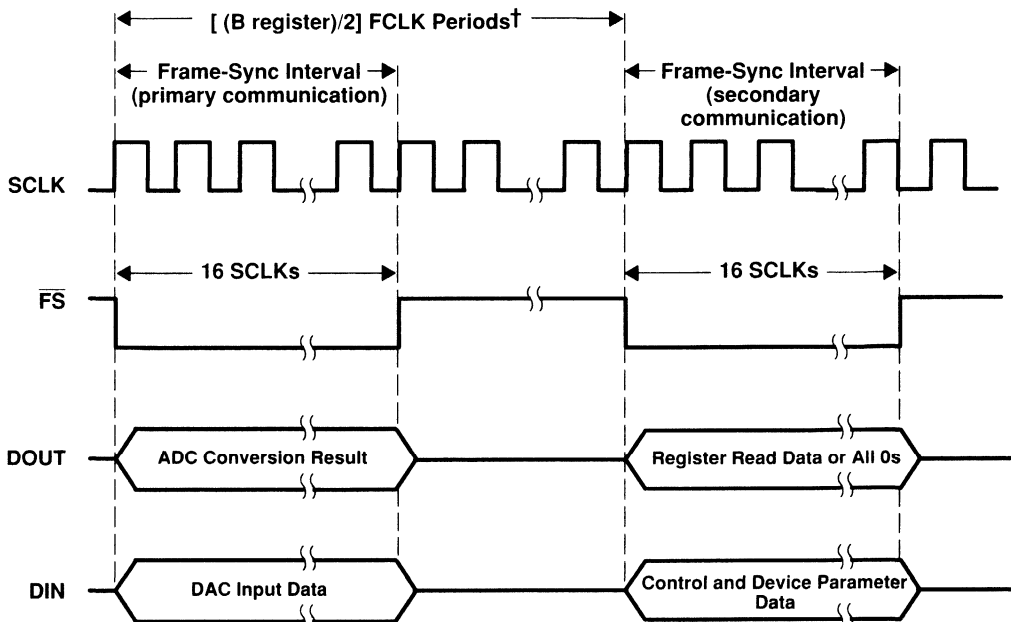
2.5 DAC Signal Channel

DIN receives the 16-bit serial data word (2s complement) from the host during the primary communications interval and latches the data on the seventeenth rising edge of SCLK. The data are converted to an analog voltage by the DAC with a sample and hold and then through a $(\sin x)/x$ correction circuit and a smoothing filter. An output buffer with three software-programmable gains (0 dB, –6 dB, and –12 dB), as shown in register 4, drives the differential outputs OUT+ and OUT–. A squelch mode can also be programmed for the output buffer. During secondary communications, the configuration program data are read into the device control registers.

2.6 Serial Interface

The digital serial interface consists of the shift clock, the frame-synchronization signal, the ADC-channel data output, and the DAC-channel data input. During the primary 16-bit frame-synchronization interval, the SCLK transfers the ADC channel results from DOUT and transfers 16-bit DAC data into DIN.

During the secondary frame-synchronization interval, the SCLK transfers the register read data from DOUT when the read bit is set to a 1. In addition, the SCLK transfers control and device parameter information into DIN. The functional sequence is shown in Figure 2–1.



† The time between the primary and secondary frame sync is the time equal to filter clock (FCLK) period multiplied by the B-register contents divided by two. The time interval is rounded to the nearest shift clock. The secondary frame-sync signal goes from high to low on the next shift clock low-to-high transition after (B register/2) filter clock periods.

Figure 2–1. Functional Sequence for Primary and Secondary Communication

2.7 Number of Slaves

The maximum number of slaves is determined by the sum of the individual device delays from the frame-sync (FS) input low to the frame-sync delayed (FSD) low for all slaves according to equation 1:

$$(n) / tp(FS-FSD) < 1/2 \text{ shift-clock period} \tag{1}$$

Where:

n is the number of slave devices.

Example:

From equation 1 above, the number of slaves is given by equation 2:

$$(n) \leq \frac{1}{2} \times (\text{SCLK period}) \times \frac{1}{tp(FS - FSD)} \tag{2}$$

assuming the master clock is 10.368 MHz and the shift clock is 2.5965 MHz and tp(FS – FSD) is 40 ns, then according to equation 3, the number of slaves is:

$$n \leq \frac{1}{2.5965 \text{ MHz}} \times \frac{1}{2} \times \frac{1}{40 \text{ ns}} = \frac{1000}{192} = 4.8 \tag{3}$$

The maximum number of slaves under these conditions is four.

2.8 Required Minimum Number of MCLK Periods

Master with slave operation is summarized in the following sections.

2.8.1 TLC320AC02 AIC Master-Slave Summary

After initial setup and the master and slave frame syncs are separated, when secondary communication is needed for a slave device, a 11 must be placed in the 2 LSBs of each primary data word for all devices in the system, master and slave, by the host processor. In other words, all AICs must receive secondary frame requests.

The host processor must issue the command by setting D01 and D00 to a 1 in the primary frame sync data word of all devices. Then the master generates the master primary frame sync and, after the number of shift clocks set by the FSD register value, the slave primary frame sync intervals. Then, after (B register value/2) FCLK periods, the master secondary frame sync occurs first, and then the slave secondary frame sync occurs. These are also rippled through the slave devices.

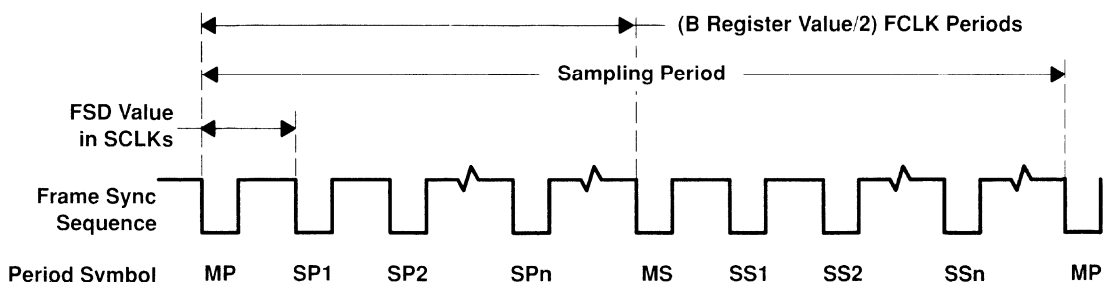
In other words, when a secondary communications interval is requested by the host processor as described above:

1. The master outputs the master primary frame sync interval, and then the slave primary frame sync intervals after the FSD register value number of shift clocks.
2. After (B register value/2) FCLK periods, the master then outputs the master secondary frame sync interval, and after the FSD register value number of shift clocks, the slave secondary frame sync intervals.

This sequence is shown in Figure 2–2.

The host must keep track of whether the master or a slave is then being addressed and also the number of slave devices. The master always outputs a 00 in the last 2 bits of the DOUT word, and a slave always outputs a 1 in the LSB of the DOUT word. This information allows the system to recognize a starting point by interrogating the least significant bit of the DOUT word. If the LSB is 0, then that device is the master, and the system is at the starting point.

Note: This identification always happens except in 16-bit mode when the 2 LSBs are not available for identification purposes.



Periods shown: Each period must be a minimum of 16 SCLKs plus 2 additional SCLKs

MP	= Master Primary Period	MS	= Master Secondary Period
SP1	= 1st Slave Primary Period	SS1	= 1st Slave Secondary Period
SP2	= 2nd Slave Primary Period	SS2	= 2nd Slave Secondary Period
SPn	= nth Slave Primary Period	SSn	= nth Slave Secondary Period

Figure 2–2. Timing Sequence

2.8.2 Notes on TLC320AC01/02 AIC Master-Slave Operation

Master/slave operational detail is summarized in the following notes:

1. The slave devices can be programmed independently of the master as long as the clock divide register numbers are not changed. The gain settings, for example, can be changed independently.
2. The method that is used to program a slave independently is to request a secondary communication of the master and all slaves and ripple the delayed frame sync to the desired slave device to be programmed.
3. Secondary frame syncs must be requested for all devices in the system or none. This is required so that the master generates secondary frames for the slaves and allows the slaves to know that the second frame syncs they receive are secondary frame syncs. Each device in the system must receive a secondary frame request in its corresponding primary frame sync period (11 in the last 2 LSBs).
4. Calculation of the sampling frequency in terms of the master clock and the shift clock and the respective register ratios is (see equations 4–6):

$$\begin{aligned} \text{Sampling frequency} = f_s &= \frac{\text{FCLK}}{\text{B register value}} \\ &= \frac{f(\text{MCLK})}{2 (\text{A register value}) \times (\text{B register value})} \end{aligned} \quad (4)$$

Therefore,

$$\frac{f(\text{MCLK})}{f_s} = 2 \times (\text{A register value}) \times (\text{B register value}) \quad (5)$$

and in terms of the shift clock frequency, since

$$f(\text{MCLK}) = 4 \times f(\text{SCLK})$$

then

$$\begin{aligned} \frac{f(\text{SCLK})}{f_s} &= \frac{(\text{A register value}) \times (\text{B register value})}{2} \\ &= \frac{\text{Number of SCLK periods}}{\text{Sampling period}} \end{aligned} \quad (6)$$

5. The minimum number of shift clocks between falling edges of any two frame syncs is 18 because the frame sync delay register minimum number is 18.

When a secondary communication is requested by the host, the master secondary frame sync begins at the middle of the sampling period (followed by the slave secondary frame syncs), so all primary frame sync intervals (master and slave) must occur within one-half the sampling time.

The first secondary frame-sync falling edge, therefore, occurs at the following time (see equation 7):

$$\begin{aligned} \text{Time to first secondary frame sync} &= \frac{\text{B register value}}{2} \text{ (FCLK periods)} = \\ &\text{A register value} \times \text{B register value (number of MCLK periods)} = \\ &\frac{\text{A register value} \times \text{B register value}}{4} \text{ (number of SCLK periods)} \end{aligned} \quad (7)$$

6. Number of frame sync intervals using equation 8.

All master and slave primary frame sync intervals must occur within the time of equation 7.

Since 18 shift clocks are required for each frame sync interval, then the number of frame sync intervals from equation 8 is:

$$\begin{aligned} \text{Number of frame sync intervals} &= \frac{\text{A register value} \times \text{B register value}}{4 \times 18 \text{ (SCLKs/frame sync interval)}} \\ &= \frac{\text{A register value} \times \text{B register value}}{72} \end{aligned} \quad (8)$$

7. Number of devices, master and slave, in terms of $f(\text{MCLK})$ and f_s .

Substituting the value from equation 5 for the $A \times B$ register value product gives the total number of devices, including the master and all slaves that can be used, for a given master clock and sampling frequency. Therefore, using equation 9:

$$\text{Number of devices} = \frac{f(\text{MCLK})}{144 \times f_s} \quad (9)$$

8. Number of devices, master and slave, if slave devices are reprogrammed.

Equation 9 does not include reprogramming the slave devices after the frame sync delay occurs. So if programming is required after shifting the slave frame syncs by the FSD register, then the total number of devices is given by equation 10 is:

$$\text{Number of devices} = \frac{f(\text{MCLK})}{288 \times f_s} \quad (10)$$

9. Example of the maximum number of devices if the slave devices are reprogrammed assuming the following values:

$$f(\text{MCLK}) = 10.368 \text{ MHz}, f_s = 8 \text{ kHz}$$

then from equation 10,

$$\text{Maximum number of devices} = \frac{10.368 \text{ MHz}}{288 (8 \text{ kHz})} = 4.5$$

therefore, one master and three slaves can be used.

2.9 Operating Frequencies

2.9.1 Master and Stand-Alone Operating Frequencies

The sampling (conversion) frequency is derived from the master-clock (MCLK) input by equation 11:

$$f_s = \text{Sampling (conversion) frequency} = \frac{\text{MCLK}}{(\text{A register value}) \times (\text{B register value}) \times 2} \quad (11)$$

The inverse is the time between the falling edges of two successive primary frame-synchronization signals. The input and output data clock (SCLK) frequency is given in equation 12:

$$\text{SCLK frequency} = \frac{\text{MCLK frequency}}{4} \quad (12)$$

2.9.2 Slave and Codec Operating Frequencies

The slave operating frequencies are either the default values or programmed by the control data word from the master and codec conversion and the data frequencies are determined by the externally applied SCLK and $\overline{\text{FS}}$ signals.

2.10 Switched-Capacitor Filter Frequency (FCLK)

The filter clock (FCLK) is an internal clock signal that determines the filter band-pass frequency and is the B counter clock. The frequency of the filter clock is derived by equation 13:

$$\text{FCLK} = \frac{\text{MCLK}}{(\text{A register value}) \times 2} \quad (13)$$

2.11 Filter Bandwidths

The low-pass (LP) filter –3 dB corner is derived in equation 14:

$$f(\text{LP}) = \frac{\text{FCLK}}{40} = \frac{\text{MCLK}}{40 \times (\text{A register value}) \times 2} \quad (14)$$

The high-pass (HP) filter –3 dB corner is derived in equation 15:

$$f(\text{HP}) = \frac{\text{Sampling frequency}}{200} = \frac{\text{MCLK}}{200 \times 2 \times (\text{A register value}) \times (\text{B register value})} \quad (15)$$

2.12 Master and Stand-Alone Modes

The difference between the master and stand-alone modes is that in the stand-alone mode there are no slave devices. Functionally these two modes are the same. In both, the AIC internally generates the shift clock and frame-sync signal for the serial communications. These signals and the filter clock (FCLK) are derived from the input master clock. The master clock applied at the MCLK input determines the internal device timing. The shift clock frequency is a divide-by-four of the master clock frequency and shifts both the input and output data at DIN and DOUT, respectively, during the frame-sync interval (16 shift clocks long). To begin the communication sequence, the device is reset (see Section 2.2.1), and the first frame sync occurs approximately 648 master clocks after the reset condition disappears.

2.12.1 Register Programming

All register programming occurs during secondary communications, and data is latched and valid on the sixteenth falling edge of SCLK. After a reset condition, eight primary and secondary communications cycles are required to set up the eight programmable registers. Registers 1 through 8 are programmed in secondary communications intervals 1 through 8, respectively. If the default value for a particular register is desired, that register does not need to be addressed during the secondary communications. The no-op command addresses the pseudo-register (register 0), and no register programming takes place during this communications. The no-op command allows phase shifts of the sampling period without reprogramming any register.

During the eight register programming cycles, DOUT is in the high-impedance state. DOUT is released on the rising edge of the eighth primary internal frame-sync interval. In addition, each register can be read back

during DOUT secondary communications by setting the read bit to 1 in the appropriate register. Since the register is in the read mode, no data can be written to the register during this cycle. To return this register to the write mode requires a subsequent secondary communication (see Section 2.19 for detailed register description).

2.12.2 Master and Stand-Alone Functional Sequence

The A counter counts according to the contents of the A register, and the A counter frequency is divided by two to produce the filter clock (FCLK). The B counter is clocked by FCLK with the following functional sequence:

1. The B counter starts counting down from the B register value minus one. Each count remains in the counter for one FCLK period including the zero count. This total counter time is referred to as the B cycle. The end of the zero count is called the end of B cycle.
2. When the B counter gets to a count of nine, the analog-to-digital (A-to-D) conversion starts.
3. The A-to-D conversion is complete ten FCLK periods later.
4. \overline{FS} goes low on a rising edge of SCLK after the A-to-D conversion is complete. That rising edge of SCLK must be preceded by a falling edge of SCLK, which is the first falling edge to occur after the end of B cycle.
5. The D-to-A conversion cycle begins on the rising edge of the internal frame-sync interval and is complete ten FCLK periods later.

2.13 Slave and Codec Modes

The only difference between the slave and codec modes is that the codec mode is controlled directly by the host and does not use a delayed frame-sync signal. In both modes, the shift clock and the frame sync are both externally generated and must be synchronous with MCLK. The conversion frequency is set by the time interval of externally applied frame-sync falling edges except when the free-run function is selected by bit 5 of register 6 (see Section 2.15.4). The slave device or devices share the shift clock generated by the master device but receive the frame sync from the previous slave in the chain. The Nth slave \overline{FS} receives the (N-1)st slave \overline{FSD} output and so on. The first slave device in the chain receives \overline{FSD} from the master.

2.13.1 Slave and Codec Functional Sequence

The A counter counts according to the contents of the A register, and the A counter frequency is divided by two to produce the FCLK. The device function in the slave or codec mode is the same as steps 1 through 3 of the B cycle description in the master mode but differs as follows:

1. Same as master
2. Same as master
3. Same as master
4. All internal clocks stop 1/2 FCLK before the end of count 0 in the B counter cycle.
5. All internal clocks are restarted on the first rising edge of MCLK after the external \overline{FS} input goes low. This operation provides the synchronization necessary when using an external \overline{FS} signal.
6. The D-to-A conversion starts on the rising edge of the internally generated frame-sync interval at the end of the 16-shift clock data transfer.

In the slave mode, the master controls the phase adjustments for itself and all slaves since all devices are programmed in the same frame-sync interval. In the codec mode, the shift clock and frame sync are externally generated and provide the timing for the ADC and DAC if the free-run function has not been selected (see Subsection 2.15.4). In the codec mode, there is usually no need for phase adjustments; however, any required phase adjustments must be made by adjusting the external frame-sync timing (sampling time).

2.13.2 Slave Register Programming

When slave devices are used on power-up or reset, all slave frame-sync signals occur at the same time as the master frame-sync signal and all slave devices are programmed during the master secondary frame-sync interval with the same data as the master. The last register programmed must be the frame-sync delay (FSD) register because the delay starts immediately on the rising edge of the seventeenth shift clock of that frame-sync interval. After the FSD register programming is completed for the master and slave, the slave primary frame interval is shifted in time (time slot allocated) according to the data contained in the slave FSD registers. The master then generates frame-sync intervals for itself and each slave to synchronize the host serial port for data transfers for itself and all slave devices.

The number of slaves is specified in the FSN register (register 8); therefore, the number of frame-sync intervals generated by the master is equal to the number of slaves plus one (see Section 2.7). These master frame-sync intervals are separated in time by the delay time specified by the FSD register (register 7). These master-generated intervals are the only frame-sync interval signals applied to the host serial port to provide the data-transfer time slot for the slave devices.

2.14 Terminal Functions

2.14.1 Frame-Sync Function

The frame-sync signal indicates that the device is ready to send and receive data for both master and slave modes. The data transfer begins on the falling edge of the frame-sync signal.

2.14.1.1 Frame Sync (\overline{FS}), Master Mode

The frame sync is generated internally. \overline{FS} goes low on the rising edge of SCLK and remains low for the 16-bit data transfer. In addition to generating its own frame-sync interval, the master also outputs a frame sync for each slave that is being used.

2.14.1.2 Frame-Sync Delayed ($\overline{\text{FSD}}$), Master Mode

For the master, the frame-sync delayed output occurs 1/2 shift-clock period ahead of $\overline{\text{FS}}$ to compensate for the time delay through the master and slave devices. The timing relationships are as follows:

1. When the FSD register data is 0, then $\overline{\text{FSD}}$ goes low on the falling edge of SCLK prior to the rising edge of SCLK when $\overline{\text{FS}}$ goes low (see Figure 4–4).
2. When the FSD register data is greater than 17, then $\overline{\text{FSD}}$ goes low on a rising edge of SCLK that is the FSD register number of SCLKs after the falling edge of $\overline{\text{FS}}$.

Register data values from 1 to 17 should not be used.

2.14.1.3 Frame Sync ($\overline{\text{FS}}$), Slave Mode

The frame-sync timing is generated externally, applied to $\overline{\text{FS}}$, and controls the ADC and DAC timing (see Subsection 2.15.4). The external frame-sync width must be a minimum of one shift clock to be recognized and can remain low until the next data frame is required.

2.14.1.4 Frame-Sync Delayed ($\overline{\text{FSD}}$), Slave Mode

This output is fed from the master to the first slave and the first slave $\overline{\text{FSD}}$ output to the second and so on down the chain. The FSD timing sequence in the slave mode is as follows:

1. When the FSD register data is 0, then $\overline{\text{FSD}}$ goes low after $\overline{\text{FS}}$ goes low (see Figure 4–5).
2. When the FSD register data is greater than 17, $\overline{\text{FSD}}$ goes low on a rising edge of SCLK that is the FSD register number of SCLKs after the falling edge of $\overline{\text{FS}}$.

Data values from 1 to 17 should not be used.

2.14.2 Data Out (DOUT)

DOUT is placed in the high-impedance state on the seventeenth rising edge of SCLK (internal or external) after the falling edge of frame sync. In the primary communication, the data word is the ADC conversion result. In the secondary communication, the data is the register read results when requested by the read/write (R/\overline{W}) bit with the eight MSBs set to 0 (see Section 2.16). If no register read is requested, the secondary word is all zeroes.

2.14.2.1 Data Out, Master Mode

In the master mode, DOUT is taken from the high-impedance state by the falling edge of frame sync. The most significant data bit then appears on DOUT.

2.14.2.2 Data Out, Slave Mode

In the slave mode, DOUT is taken from the high-impedance state by the falling edge of the external frame sync or the rising edge of the external SCLK, whichever occurs first (see Figure 4–7). The falling edge of frame sync can occur $\pm 1/4$ SCLK period around the SCLK rising edge (see Figure 4–3). The most significant data bit then appears on DOUT.

2.14.3 Data In (DIN)

In the primary communication, the data word is the digital input signal to the DAC channel. In the secondary communication, the data is the control and configuration data to set up the device for a particular function (see Section 2.16).

2.14.4 Hardware Program Terminals (FC1 and FC0)

These inputs provide for hardware programming requests for secondary communication or phase adjustment. These inputs work in conjunction with the control bits D01 and D00 of the primary data word or control bits DS15 and DS14 of the secondary data word. The data on FC1 and FC0 are latched on the rising edge of the next internally generated primary or secondary frame-sync interval. These inputs should be tied low if not used (see Section 2.17 and Table 2–3).

2.14.5 Midpoint Voltages (ADC V_{MID} and DAC V_{MID})

Since the device operates at a single-supply voltage, two midpoint voltages are generated for internal signal processing. ADC V_{MID} is used for the ADC channel reference, and DAC V_{MID} is used for the DAC channel reference. Two references minimize channel-to-channel noise and crosstalk. ADC V_{MID} and DAC V_{MID} must be buffered when used as a reference for external signal processing.

2.15 Device Functions

2.15.1 Phase Adjustment

In some applications, such as modems, the device sampling period may require an adjustment to synchronize with the incoming bit stream to improve the signal-to-noise ratio. The TLC320AC02 can adjust the sampling period through the use of the A' register and the control bits.

2.15.1.1 Phase-Adjustment Control

A phase adjustment is a programmed variation in the sampling period. A sampling period is adjusted according to the data value in the A' register, and the phase adjustment is that number of master clocks (MCLK). An adjustment is made during device operation with data bits D01 and D00 in the primary communication, with data bits DS15 and DS14 in the secondary word or in combination with the hardware terminals FC1 and FC0 (see Table 2–3). This adjustment request is latched on the rising edge of the next internal frame-sync interval and is only valid for the next sampling period. To repeat the phase adjustment, another phase request must be initiated.

2.15.1.2 Use of the A' Register for Phase Adjustment

The A' register value makes slight timing adjustments to the sampling period. The sampling period increases or decreases according to the sign of the programmed A' register value and the state of data bits D01 and D00 in the primary data word.

The general equation for the conversion frequency is given in equation 16:

$$f_s = \text{conversion frequency} = \frac{\text{MCLK}}{(2 \times \text{A register value} \times \text{B register value}) \pm (\text{A' register value})} \quad (16)$$

Therefore, if A' = 0, the device conversion (sampling) frequency and period is constant.

If a nonzero A' value is programmed, the sampling frequency and period responds as shown in Table 2–2.

Table 2–2. Sampling Variation With A'

D01	D00	SIGN OF THE A' REGISTER VALUE	
		PLUS VALUE (+)	NEGATIVE VALUE (-)
0	1 (increase command)	Frequency decreases, period increases	Frequency increases, period decreases
1	0 (decrease command)	Frequency increases, period decreases	Frequency decreases, period increases

An adjustment to the sampling period, which must be requested through D01 and D00 of the primary data word to DIN, is valid for the following sampling period only. When the adjustment is required for the subsequent sampling period, it must be requested again through D01 and D00 of the primary data word. For each request, only the sampling period occurring immediately after the primary data word request is affected.

The amount of time shift in the entire sampling period ($1/f_s$) is as follows:

When the sampling period is set to 125 μ s (8 kHz), the A' register is loaded with decimal 10 and the TLC320AC02 master clock frequency is 10.386 MHz. The amount of time each sampling period is increased or decreased, when requested, is given in equation 17:

$$\text{Time shift} = (\text{A' register value}) \times (\text{MCLK period}) \quad (17)$$

The device changes the entire sampling period by only the MCLK period times the A' register value as given in equation 18:

$$\begin{aligned} \text{Change in sampling period} &= \text{contents of A' register} \times \text{master clock period} \\ &= 10 \times 96.45 \text{ ns} = 964 \text{ ns (less than 1\% of the sampling period)} \end{aligned} \quad (18)$$

The sampling period changes by 964.5 ns each time the phase adjustment is requested by the primary data word (i.e., once per sampling period).

It is evident then that the change in sampling period is very small compared to the sampling period. To observe this effect over a long period of time ($>$ sampling period), this change must be continuously requested by the primary data word. If the adjustment is not requested again, the sampling period changes only once and it may appear that there was no execution of the command. This is especially true when bench testing the device. Automatic test equipment can test for results within a single sampling period.

Internally, the A' register value only affects one cycle (period) of the A counter. The A and A' values are additive, but only for one A-counter period. The A counter begins the first count at the default or programmed A-register value and counts down to the A'-register value. As the A' value increases or decreases, the first clock cycle from the A counter is lengthened or shortened. The initial A-counter period is the only counter period affected by the A' register such that only this single period is increased or decreased.

2.15.2 Analog Loopback

This function allows the circuit to be tested remotely. In loopback, OUT+ and OUT- are internally connected to IN+ and IN-. The DAC data bits D15 to D02 that are applied to DIN can be compared with the ADC output data bits D15 to D02 at DOUT. There are some differences due to the ADC and DAC channel offset. The loopback function is implemented by setting DS01 and DS00 to zero in control register 5 (see Section 2.19). When analog loopback is enabled, the external inputs to IN+ and IN- are disconnected, but the signals at OUT+ and OUT- may still be read.

2.15.3 16-Bit Mode

In the 16-bit mode, the device ignores the last two control bits (D01 and D00) of the primary word and requests continual secondary communications to occur. By ignoring the last two primary communication bits, compatibility with existing 16-bit software can be maintained. This function is implemented by setting bit DS03 to 1 in register 6. To return to normal operation, DS03 must be reprogrammed to 0.

2.15.4 Free-Run Mode

With the free-run bit set in register 6, the external shift clock and frame sync control only the data transfer. The ADC and DAC timing are controlled by the A and B register values, and the phase-shift adjustment must be done as if the device is in stand-alone mode (by the software or the state of FC1 and FC0).

Phase adjustment cannot be made by adjustment of the frame-sync timing. The external frame sync must occur within 1/2 FCLK period of the internal frame sync (FCLK as determined by the values of the A and B registers).

When the external frame sync occurs simultaneously with the internal load, the data-transfer request by the external frame sync takes precedence over an internal load command. The latching of the ADC conversion data in the output register is inhibited until the current 16 bits are shifted out of the register by the shift clock.

2.15.5 Force Secondary Communication

With bit 2 in register 6 set to 1, secondary communication is requested continuously. It overrides all software and hardware requests concerning secondary communication. Phase shifting, however, can still be performed with the software and hardware.

2.15.6 Enable Analog Input Summing

By setting bits DS01 and DS00 to 11 in register 5, the normal analog input voltage is summed with the auxiliary input voltage. The gain for the analog input amplifier is set by data bits DS03 and DS02 in register 4.

2.15.7 DAC Channel (sin x)/x Error Correction

The (sin x)/x compensation filter is designed for zero (sin x)/x error using a B-register value of 15. Since the filter cannot be removed from the signal path, operation using another B-register value results in an error in the reconstructed analog output. The error is given by equation 19. Any error compensation needed by a given application can be performed in the software.

$$\text{DAC channel frequency response error} = 20 \times \log_{10} \left[\frac{\sin \left(\frac{2\pi \times A \times B}{f_{\text{MCLK}}} \times f \right)}{\sin \left(\frac{30\pi \times A}{f_{\text{MCLK}}} \times f \right)} \times \frac{15}{B} \right] \quad (19)$$

where:

- f = the frequency of interest
- f_{MCLK} = the TLC320AC02 master-clock frequency
- A = the A-register value
- B = the B-register value

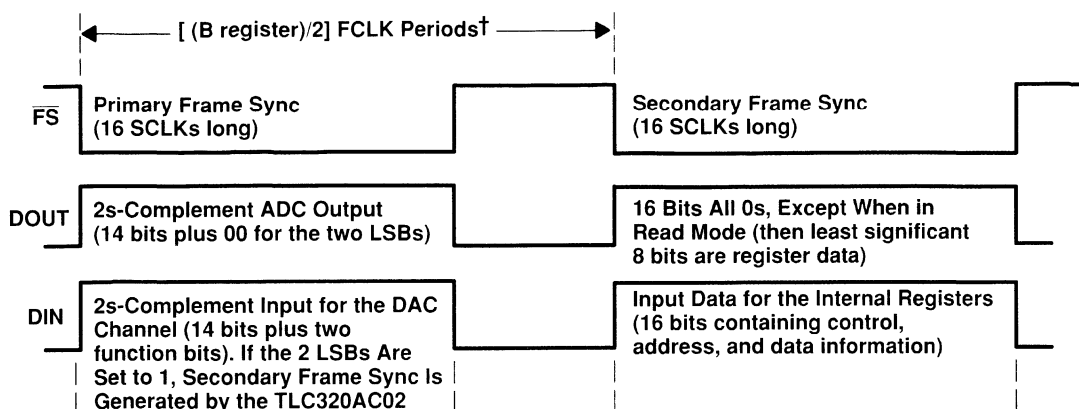
and the arguments of the sin functions are in radians.

2.16 Serial Communications

2.16.1 Stand-Alone and Master-Mode Word Sequence and Information Content During Primary and Secondary Communications

For the stand-alone and master modes, the sequence in Figure 2–2 shows the relationship between the primary and secondary communications interval, the data content into DIN, and the data content from DOUT.

The TLC320AC02 can provide a phase-shift command or the next secondary communications interval by decoding 1) the programmed state of the FC1 and FC0 inputs and the D01 and D00 data bits in the primary data word, or 2) the state of the FC1 and FC0 inputs and the DS15 and DS14 data bits in the secondary data word (see Table 2–3). When DS13 (the R/W bit) is the default value of 0, all 16 bits from DOUT are 0 during secondary communication. However, when the R/W bit is set to 1 in the secondary communication control word, the secondary transmission from DOUT still contains 0s in the eight MSBs. The lower order 8 bits contain the data of the register currently being addressed. This function provides register status information for the host.

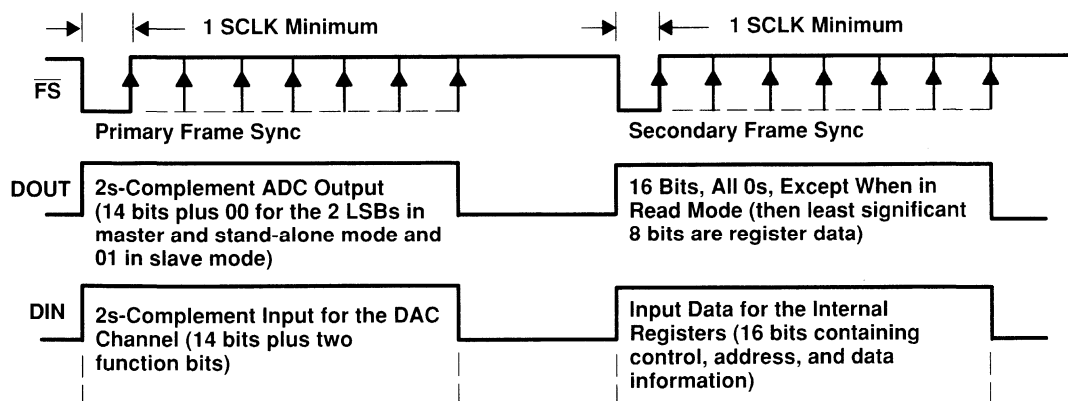


† The time between the primary and secondary frame sync is the time equal to filter clock (FCLK) period multiplied by the B-register contents divided by two. The time interval is rounded to the nearest shift clock. The secondary frame-sync signal goes from high to low on the next shift clock low-to-high transition after (B register/2) filter clock periods.

Figure 2–3. Master and Stand-Alone Functional Sequence

2.16.2 Slave and Codec-Mode Word Sequence and Information Content During Primary and Secondary Communications

For the slave and codec modes, the sequence is basically the same as the stand-alone and master modes with the exception that the frame sync and the shift clock are generated and controlled externally as shown in Figure 2–3. For the codec mode, the frame-sync pulse width needs to be a minimum of one shift clock long. The timing relationship between the frame sync and shift clock is shown in the timing diagrams. Phase shifting is usually not required in the slave or codec mode because the frame-sync timing can be adjusted externally if required.



NOTE A: The time between the primary and secondary frame syncs is determined by the application; however, enough time must be provided so that the host can execute the required number of software instructions in the time between the end of the primary data transfer (rising edge of the primary frame-sync interval) and the falling edge of the secondary frame sync (start of secondary communications).

Figure 2–4. Slave and Codec Functional Sequence

2.17 Request for Secondary Serial Communication and Phase Shift

The following paragraphs describe a request for secondary serial communication and phase shift using hardware control inputs FC1 and FC0, primary data bits D01 and D00, and secondary data bits DS15 and DS14.

2.17.1 Initiating a Request

Combinations of FC1 and FC0 input conditions, bits D01 and D00 in the primary serial data word, FC1 and FC0, and bits DS15 and DS14 in the secondary serial data word can initiate a secondary serial communication or request a phase shift according to the following rules (see Table 2–3).

1. Primary word phase shifts can be requested by either the hardware or software when the other set of signals are 11 or 00. If both hardware and software request phase shifts, the software request is performed.
2. Secondary words can be requested by either the software or hardware at the same time that the other set of signals is requesting a phase shift.
3. Hardware inputs FC1 and FC0 are ignored during the secondary word unless DS15 and DS14 are 11. When DS15 and DS14 are 01 or 10, the corresponding phase shift is performed. When DS15 and DS14 are 00, no phase shift is performed even when the hardware requests a phase shift.

2.17.2 Normal Combinations of Control

The normal combinations of control are as follows:

1. Use D01 and D00 and DS15 and DS14 to request phase shifts and secondary words by holding FC1 and FC0 to 00.
2. Use FC1 and FC0 exclusively to request phase shifts and secondary words by holding D01 and D00 to 00 and DS15 and DS14 to 11.
3. Use D01 and D00 only to request secondary words and FC1 and FC0 to perform phase shifts once per period by holding DS15 and DS14 to 00.

2.17.3 Additional Control Options

Additional control options are unusual and are rarely needed or used; however, they are as follows:

1. Use D01 and D00 only to request secondary words and FC1 and FC0 to perform phase shifts twice per period by holding DS15 and DS14 to 11.
2. Use FC1 and FC0 exclusively to request secondary words and D01 and D00 and DS15 and DS14 to perform phase shifts twice per period.
3. Use FC1 and FC0 to perform the phase shift after the primary word and DS15 and DS14 to perform a phase shift after the secondary word by holding D01 and D00 to 11.

Table 2–3. Software and Hardware Requests for Secondary Serial-Communication and Phase-Shift Truth Table

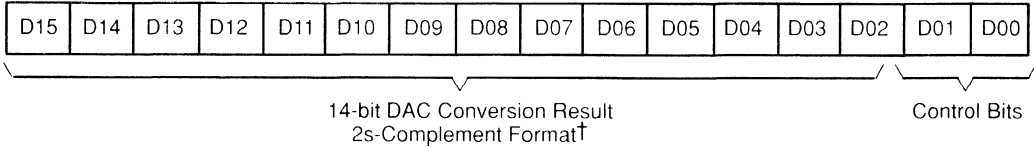
WITHIN PRIMARY OR SECONDARY DATA WORD	CONTROL BITS		HARDWARE TERMINALS		PHASE-SHIFT ADJUSTMENT (see Section 2.15.1)		SECONDARY REQUEST (see Note 1)
	D01	D00	FC1	FC0	EARLIER	LATER	
Primary	0	0	0	0	0	0	0
	0	0	0	1	0	1	0
	0	0	1	0	1	0	0
	0	0	1	1	0	0	1
	0	1	0	0	0	1	0
	0	1	0	1	0	1	0
	0	1	1	0	0	1	0
	0	1	1	1	0	1	1
	1	0	0	0	1	0	0
	1	0	0	1	1	0	0
	1	0	1	0	1	0	0
	1	0	1	1	1	0	1
	1	1	0	0	0	0	1
	1	1	0	1	0	1	1
	1	1	1	0	1	0	1
	1	1	1	1	0	0	1
Secondary	DS15	DS14	FC1	FC0	EARLIER	LATER	No request can be made for secondary communication within the secondary word.
	0	0	0	0	0	0	
	0	0	0	1	0	0	
	0	0	1	0	0	0	
	0	0	1	1	0	0	
	0	1	0	0	0	1	
	0	1	0	1	0	1	
	0	1	1	0	0	1	
	0	1	1	1	0	1	
	1	0	0	0	1	0	
	1	0	0	1	1	0	
	1	0	1	0	1	0	
	1	0	1	1	1	0	
	1	1	0	0	0	0	
	1	1	0	1	0	1	
	1	1	1	0	1	0	
1	1	1	1	0	0		

NOTE 1: The 0 state indicates that a secondary communication is not being requested. The 1 state indicates that a secondary communication is being requested.

2.18 Primary Serial Communications

Primary serial communications transfer the 14-bit DAC input plus two control bits (D01 and D00) to DIN of the TLC320AC02. They simultaneously transfer the 14-bit ADC conversion result from DOUT to the processor. The 2 LSBs are set to 0 in the ADC result.

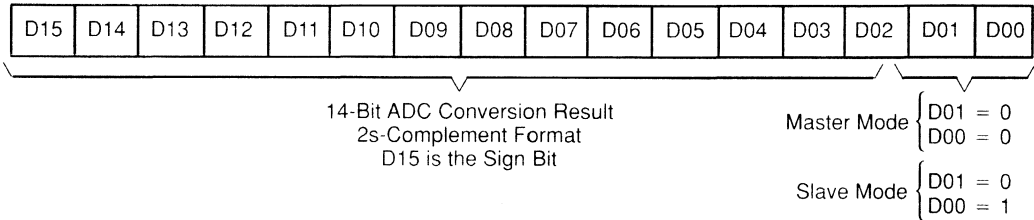
2.18.1 Primary Serial Communications Data Format



† Since the supply voltage is single ended, the reference for 2s-complement format is ADC V_{MID} . Voltages above this reference have a 0 as the MSB, and voltages below this reference have a 1 as the MSB.

During primary serial communications, when D01 and D00 are both high in the DAC data word to DIN, a subsequent 16 bits of control information is received by the device at DIN during a secondary serial-communication interval. This secondary serial-communication interval begins at 1/2 the programmed conversion time when the B register data value is even or 1/2 the programmed value minus one FCLK when the B register data value is odd. The time between primary and secondary serial communication is measured from the falling edge of the primary frame sync to the falling edge of the secondary frame sync (see Section 2.19 for function and format of control words).

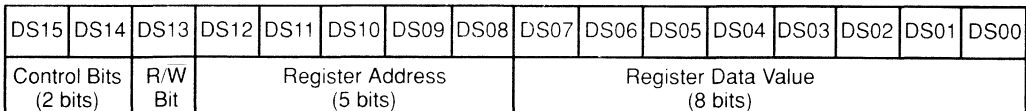
2.18.2 Data Format From DOUT During Primary Serial Communications



2.19 Secondary Serial Communications

2.19.1 Data Format to DIN During Secondary Serial Communications

There are nine 16-bit configuration and control registers numbered from zero to eight. All register data contents are represented in 2s-complement format. The general format of the commands during secondary serial communications is as follows.

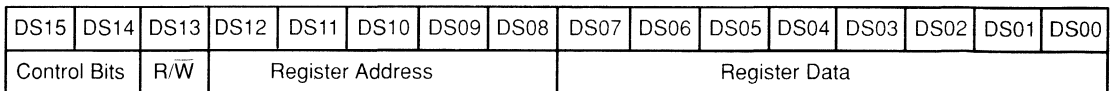


All control register words are latched in the register and valid on the sixteenth falling edge of SCLK.

2.19.2 Control Data-Bit Function in Secondary Serial Communication

2.19.2.1 DS15 and DS14

In the secondary data word, bits DS15 and DS14 perform the same control function as the primary control bits D01 and D00 do in the primary data word.



Hardware terminals FC1 and FC0 are valid inputs when DS15 and DS14 are both high, and they are ignored for all other conditions.

2.19.2.2 DS13 (R/W Bit)

Reset and power-up procedures set this bit to a 0, placing the device in the write mode. When this bit is set to 1, however, the previous data content of the register being addressed is read out to the host from DOUT as the least significant 8 bits of the 16-bit secondary word. The first 8 bits remain set to 0. Reading the data out is nondestructive, and the contents of the register remain unchanged.

A. Write Mode (DS13 = 0)

Data In. The data word to DIN has the following general format in the write mode.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits	0	Register Address						Register Data							

Data Out. The shift clock shifts out all 0s as the pattern to the host from DOUT.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

B. Read Mode (DS13 = 1)

Data In. The data word to DIN has the following format to allow a register read. Phase shifts can also be done in the read mode.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits	1	Register Address						Ignored							

Data Out. The shift clock clocks out the data of the register addressed from DOUT in the read mode in the 8 LSBs.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0	Register Data							

2.20 Internal Register Format

2.20.1 Pseudo-Register 0 (No-Op Address)

This address represents a no-operation command. No register I/O operation takes place, so the device can receive secondary commands for phase adjustment without reprogramming any register. A read of the no-op is 0. The format of the command word is as follows:

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits	X	0	0	0	0	0	0	X	X	X	X	X	X	X	X

2.20.2 Register 1 (A Register)

The following command loads DS07 (MSB) – DS00 into the A register.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits	R/W	0	0	0	0	1	Register Data								

The data in DS07 – DS00 determines the division of the master clock to produce the internal FCLK.

$$\text{FCLK frequency} = \text{MCLK}/(\text{A register contents} \times 2)$$

The default value of the A-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

2.20.3 Register 2 (B Register)

The following command loads DS07 (MSB) – DS00 into the B register.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/W	0	0	0	1	0	Register Data							

The data in DS07 – DS00 controls the division of FCLK to generate the conversion clock as given in equation 20:

$$\begin{aligned} \text{Conversion frequency} &= \text{FCLK}/(\text{B register contents}) \\ &= \frac{\text{MCLK}}{2 \times \text{A register contents} \times \text{B register contents}} \end{aligned} \quad (20)$$

The default value of the B-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

2.20.4 Register 3 (A' Register)

The following command contains the A'-register address and loads DS07(MSB) – DS00 into the A' register.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/W	0	0	0	1	1	Register Data							

The data in DS07 – DS00 is in 2s-complement format and controls the number of master-clock periods that the sampling time is shifted.

The default value of the A'-register data is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

2.20.5 Register 4 (Amplifier Gain-Select Register)

The following command contains the amplifier gain-select register address with selection code for the monitor output (DS05–DS04), analog input (DS03–DS02), and analog output (DS01–DS00) programmable gains.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits	R/W	0	0	1	0	0	X	X	X	*	*	*	*	*	*
Monitor output gain = squelch										0	0				
Monitor output gain = 0 dB										0	1				
Monitor output gain = -8 dB										1	0				
Monitor output gain = -18 dB										1	1				
Analog input gain = squelch												0	0		
Analog input gain = 0 dB												0	1		
Analog input gain = 6 dB												1	0		
Analog input gain = 12 dB												1	1		
Analog output gain = squelch													0	0	
Analog output gain = 0 dB													0	1	
Analog output gain = -6 dB													1	0	
Analog output gain = -12 dB													1	1	

The default value of the monitor output gain is squelch, which corresponds to data bits DS05 and DS04 equal to 00 (binary).

The default value of the analog input gain is 0 dB, which corresponds to data bits DS03 and DS02 equal to 01 (binary).

The default value of the analog output gain is 0 dB, which corresponds to data bits DS01 and DS00 equal to 01 (binary).

The default data value is shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	1	0	1

2.20.6 Register 5 (Analog Configuration Register)

The following command loads the analog configuration register with the individual bit functions described below.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits	R/W	0	0	1	0	1	X	X	X	X	*	*	*	*	
Must be set to 0												0			
High-pass filter disabled												1			
High-pass filter enabled												0			
Analog loopback enabled													0	0	
Enables IN+ and IN- (disables AUXIN+ and AUXIN-)													0	1	
Enables AUXIN+ and AUXIN- (disables IN+ and IN-)													1	0	
Enable analog input summing													1	1	

The default value of the high-pass-filter enable bit is 0, which places the high-pass filter in the signal path. The default values of DS01 and DS00 are 0 and 1 which enables IN+ and IN-.

The power-up and reset conditions are as shown below.

DS03	DS02	DS01	DS00
0	0	0	1

In the read mode, eight bits are read but the 4 LSBs are repeated as the 4 MSBs.

2.20.7 Register 6 (Digital Configuration Register)

The following command loads the digital configuration register with the individual bit functions described below.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits	R/W	0	0	1	1	0	X	X	*	*	*	*	*	*	*
ADC and DAC conversion free run										1					
Inactive										0					
FSD output disable											1				
Enable											0				
16-Bit mode, ignore primary LSBs											1				
Normal operation											0				
Force secondary communications													1		
Normal operation													0		
Software reset														1	
(upon reset, this bit is automatically reset to 0)															
Inactive reset														0	
Software power-down active (automatically reset to 0 after PWR DWN is cycled high to low and back to high)															1
Power-down function external (uses PWR DWN)															0

The default value of DS07–DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

2.20.8 Register 7 (Frame-Sync Delay Register)

The following command contains the frame-sync delay (FSD) register address and loads DS07 (MSB)–DS00 into the FSD register. The data byte (DS01–DS00) determines the number of SCLKs between \overline{FS} and the delayed frame-sync signal, \overline{FSD} . The minimum data value for this register is decimal 18.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits	R/W	0	0	1	1	1	Register Data								

The default value of DS07 – DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

When using a slave device, register 7 must be the last register programmed.

2.20.9 Register 8 (Frame-Sync Number Register)

The following command contains the frame-sync number (FSN) register address and loads DS07 (MSB)–DS00 into the FSN register. The data byte determines the number of frame-sync signals generated by the TLC320AC02. This number is equal to the number of slaves plus one.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/ \overline{W}	0	1	0	0	0	Register Data							

The default value of DS07–DS00 is 1 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	1

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)[†]

Supply voltage range, DGTL V_{DD} (see Notes 1 and 2)	−0.3 V to 6.5 V
Supply voltage range, DAC V_{DD} (see Notes 1 and 2)	−0.3 V to 6.5 V
Supply voltage range, ADC V_{DD} (see Notes 1 and 2)	−0.3 V to 6.5 V
Differential supply voltage range, DGTL V_{DD} to DAC V_{DD}	−0.3 V to 6.5 V
Differential supply voltage range, all positive supply voltages to ADC GND, DAC GND, DGTL GND, SUBS	−0.3 V to 6.5 V
Output voltage range, DOOUT	−0.3 V to DGTL V_{DD} + 0.3 V
Input voltage range, DIN	−0.3 V to DGTL V_{DD} + 0.3 V
Ground voltage range, ADC GND, DAC GND, DGTL GND, SUBS	−0.3 V to DGTL V_{DD} + 0.3 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	−40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive supply voltage	4.5	5	5.5	V
	Steady-state differential voltage between any two supplies			0.1	V
V_{IH}	High-level digital input voltage	2.2			V
V_{IL}	Low-level digital input voltage			0.8	V
I_O	Load output current from ADC V_{MID} and DAC			100	μA
	Conversion time for the ADC and DAC channels		10 FCLK periods		
f_{MCLK}	Master-clock frequency		10.368	15	MHz
$V_{ID(PP)}$	Analog input voltage (differential, peak to peak)		6		V
R_L	Differential output load resistance	600			Ω
	Single-ended to buffered DAC V_{MID} voltage load resistance	300			
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. Voltage values for DGTL V_{DD} are with respect to DGTL GND, voltage values for DAC V_{DD} are with respect to DAC GND, and voltage values for ADC V_{DD} are with respect to ADC GND. For the subsequent electrical, operating, and timing specifications, the symbol V_{DD} denotes all positive supplies. DAC GND, ADC GND, DGTL GND, and SUBS are at 0 V unless otherwise specified.

2. To avoid possible damage to these CMOS devices and associated operating parameters, the sequence below should be followed when applying power:

- (1) Connect SUBS, DGTL GND, ADC GND, and DAC GND to ground.
- (2) Connect voltages ADC V_{DD} and DAC V_{DD} .
- (3) Connect voltage DGTL V_{DD} .
- (4) Connect the input signals.

When removing power, follow the steps above in reverse order.

3.3 Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, MCLK = 5.184 MHz, V_{DD} = 5 V, Outputs Unloaded, Total Device

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I _{DD} Supply current	PWR $\overline{\text{DWN}}$ = 1 and clock signals present		20	22	mA
	PWR $\overline{\text{DWN}}$ = 0 after 500 μs and clock signals present		1	2	mA
P _D Power dissipation	PWR $\overline{\text{DWN}}$ = 1 and clock signals present		100		mW
	PWR $\overline{\text{DWN}}$ = 0 after 500 μs and clock signals present		5		mW
	Software power down, (bit D00, register 6 set to 1)		15	20	mW
ADC V _{MID} Midpoint voltage	No load	ADC V _{DD} /2 - 0.1		ADC V _{DD} /2 + 0.1	V
DAC V _{MID} Midpoint voltage	No load	DAC V _{DD} /2 - 0.1		DAC V _{DD} /2 + 0.1	V

3.4 Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, V_{DD} = 5 V, Digital I/O Terminals (DIN, DOUT, EOC, FC0, FC1, $\overline{\text{FS}}$, $\overline{\text{FSD}}$, MCLK, M/ $\overline{\text{S}}$, SCLK)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH} High-level output voltage	I _{OH} = -1.6 mA	2.4			V
V _{OL} Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
I _{IH} High-level input current, any digital input	V _I = 2.2 V to DGTL V _{DD}			10	μA
I _{IL} Low-level input current, any digital input	V _I = 0 V to 0.8 V			10	μA
C _i Input capacitance			5		pF
C _o Output capacitance			5		pF

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

3.5 Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, V_{DD} = 5 V, ADC and DAC Channels

3.5.1 ADC Channel Filter Transfer Function, FCLK = 144 kHz, f_s = 8 kHz

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Gain relative to gain at f _i = 1020 Hz (see Note 3)	f _i = 50 Hz		-2	dB
	f _i = 200 Hz	-1.8	-0.2	
	f _i = 300 Hz to 3 kHz	-0.15	0.2	
	f _i = 3.3 kHz	-0.35	0.03	
	f _i = 3.4 kHz	-1	-0.1	
	f _i = 4 kHz		-14	
	f _i ≥ 4.6 kHz		-32	

NOTE 3: The differential analog input signals are sine waves at 6 V peak to peak. The reference gain is at 1020 Hz.

3.5.2 ADC Channel Input, $V_{DD} = 5\text{ V}$, Input Amplifier Gain = 0 dB (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{I(PP)}$	Peak-to-peak input voltage (see Note 4)	Single-ended	3			V
		Differential	6			V
	ADC converter offset error	Band-pass filter selected	10	30		mV
CMRR	Common-mode rejection ratio at IN+, IN-, AUX IN+, AUX IN- (see Note 5)		55			dB
r_i	Input resistance at IN+, IN-, AUX IN+, AUX IN-		100			k Ω
	Squelch	DS03, DS02 = 0 in register 4	60			dB

† All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTES: 4. The differential range corresponds to the full-scale digital output.

5. Common-mode rejection ratio is the ratio of the ADC converter offset error with no signal and the ADC converter offset error with a common-mode nonzero signal applied to either IN+ and IN- together or AUX IN+ and AUX IN- together.

3.5.3 ADC Channel Signal-to-Distortion Ratio, $V_{DD} = 5\text{ V}$, $f_s = 8\text{ kHz}$ (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	$A_V = 0\text{ dB}$		$A_V = 6\text{ dB}$		$A_V = 12\text{ dB}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
ADC channel signal-to-distortion ratio (see Note 6)	$V_I = -6\text{ dB to } -1\text{ dB}$	64		—		—		dB
	$V_I = -12\text{ dB to } -6\text{ dB}$	59		64		—		
	$V_I = -18\text{ dB to } -12\text{ dB}$	56		59		64		
	$V_I = -24\text{ dB to } -18\text{ dB}$	50		56		59		
	$V_I = -30\text{ dB to } -24\text{ dB}$	44		50		56		
	$V_I = -36\text{ dB to } -30\text{ dB}$	38		44		50		
	$V_I = -42\text{ dB to } -36\text{ dB}$	32		38		44		
	$V_I = -48\text{ dB to } -42\text{ dB}$	26		32		38		

NOTE 6: The analog-input test signal is a 1020-Hz sine wave with 0 dB = 6 V peak to peak as the reference level for the analog-input signal.

3.5.4 DAC Channel Filter Transfer Function, $F_{CLK} = 144\text{ kHz}$, $f_s = 9.6\text{ kHz}$, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Gain relative to gain at $f_i = 1020\text{ Hz}$ (see Note 7)	$f_i < 200\text{ Hz}$	0.15		dB
	$f_i = 200\text{ Hz}$	-0.5	0.2	
	$f_i = 300\text{ Hz to } 3\text{ kHz}$	-0.15	0.2	
	$f_i = 3.3\text{ kHz}$	-0.35	0.03	
	$f_i = 3.4\text{ kHz}$	-1	-0.1	
	$f_i = 4\text{ kHz}$	-14		
	$f_i \geq 4.6\text{ kHz}$	-32		

NOTE 7: The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak.

3.5.5 DAC Channel Signal-to-Distortion Ratio, $V_{DD} = 5\text{ V}$, $f_s = 8\text{ kHz}$ (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	$A_V = 0\text{ dB}$		$A_V = -6\text{ dB}$		$A_V = -12\text{ dB}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
DAC channel signal-to-distortion ratio (see Note 8)	$V_O = -6\text{ dB to } 0\text{ dB}$	64	—	—	—	—	—	dB
	$V_O = -12\text{ dB to } -6\text{ dB}$	59	—	64	—	—	—	
	$V_O = -18\text{ dB to } -12\text{ dB}$	56	—	59	—	64	—	
	$V_O = -24\text{ dB to } -18\text{ dB}$	50	—	56	—	59	—	
	$V_O = -30\text{ dB to } -24\text{ dB}$	44	—	50	—	56	—	
	$V_O = -36\text{ dB to } -30\text{ dB}$	38	—	44	—	50	—	
	$V_O = -42\text{ dB to } -36\text{ dB}$	32	—	38	—	44	—	
	$V_O = -48\text{ dB to } -42\text{ dB}$	26	—	32	—	38	—	

NOTE 8: The input signal, V_I , is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at full-scale digital input = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT-.

3.5.6 System Distortion, $V_{DD} = 5\text{ V}$, $f_s = 8\text{ kHz}$, $F_{CLK} = 144\text{ kHz}$ (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC channel attenuation	Second harmonic	Single-ended input (see Note 9)	—	82	—	dB
		Differential input (see Note 9)	64	82	—	
	Third harmonic and higher harmonics	Single-ended input (see Note 9)	—	77	—	
		Differential input (see Note 9)	64	77	—	
DAC channel attenuation	Second harmonic	Single-ended output (buffered DAC V_{MID}) (see Note 10)	—	82	—	
		Differential output (see Note 10)	64	82	—	
	Third harmonic and higher harmonics	Single-ended output (see Note 10)	—	77	—	
		Differential output (see Note 10)	64	77	—	

† All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTES: 9. The input signal is a 1020-Hz sine wave for the ADC channel. Harmonic distortion is defined for an input level of -1 dB.

10. The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT-. Harmonic distortion is specified for a signal input level of 0 dB.

3.5.7 Noise, Low-Pass and Band-Pass Switched-Capacitor Filters Included, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC idle-channel noise		Inputs tied to ADC V_{MID} , $f_S = 8\text{ kHz}$, $F_{CLK} = 144\text{ kHz}$, (see Note 11)		180	300	μV_{rms}
DAC idle-channel noise	Broad-band noise	DIN INPUT = 00000000000000,		180	300	
	Noise (0 to 7.2 kHz)	$f_S = 8\text{ kHz}$, $F_{CLK} = 144\text{ kHz}$, (see Note 12)		180	300	
	Noise (0 to 3.6 kHz)			180	300	

† All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTES: 11. The ADC channel noise is calculated by taking the RMS value of the digital output codes of the ADC channel and converting to microvolts.

12. The DAC channel noise is measured differentially from OUT+ to OUT– across $600\ \Omega$.

3.5.8 Absolute Gain Error, $V_{DD} = 5\text{ V}$, $f_S = 8\text{ kHz}$ (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
ADC channel absolute gain error (see Note 13)	–1-dB input signal	$T_A = -40 - 85^\circ\text{C}$		± 1	dB
DAC channel absolute gain error (see Note 14)	0-dB input signal, $R_L = 600\ \Omega$	$T_A = -40 - 85^\circ\text{C}$		± 1	

NOTES: 13. ADC absolute gain error is the variation in gain from the ideal gain over the specified input signal levels. The gain is measured with a –1-dB, 1020-Hz sine wave. The –1-dB input signal allows for any positive gain or offset error that may affect gain measurements at or close to 0-dB input signal levels.

14. The DAC input signal is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at digital full-scale input = 0 dB). The nominal differential DAC channel output voltage with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is $600\ \Omega$ from OUT+ to OUT–.

3.5.9 Relative Gain and Dynamic Range, $V_{DD} = 5\text{ V}$, $f_S = 8\text{ kHz}$ (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
ADC channel relative gain tracking error (see Note 15)	–48-dB to –1-dB input signal range		± 0.2	dB
DAC channel relative gain tracking error (see Note 16)	–48-dB to 0-dB input signal range $R_{L(diff)} = 600\ \Omega$		± 0.2	

NOTES: 15. ADC gain tracking is the ratio of the measured gain at one ADC channel input level to the gain measured at any other input level. The ADC channel input is a –1-dB 1020-Hz sine wave input signal. A –1-dB input signal allows for any positive gain or offset error that may affect gain measurements at or close to 0-dB ADC input signal levels.

16. DAC gain tracking is the ratio of the measured gain at one DAC channel digital input level to the gain measured at any other input level. The DAC-channel input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output voltage with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is $600\ \Omega$ from OUT+ to OUT–.

3.5.10 Power-Supply Rejection, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted) (see Note 17)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC V_{DD} Supply-voltage rejection ratio, ADC channel	$f_i = 0$ to 30 kHz		50		dB
	$f_i = 30$ to 50 kHz		55		
DAC V_{DD} Supply-voltage rejection ratio, DAC channel	$f_i = 0$ to 30 kHz		40		
	$f_i = 30$ to 50 kHz		45		
DGTL V_{DD} Supply-voltage rejection ratio, ADC channel	$f_i = 0$ to 30 kHz		50		
	$f_i = 30$ to 50 kHz		55		
DGTL V_{DD} Supply-voltage rejection ratio, DAC channel	Single ended, $f_i = 0$ to 30 kHz		40		
	$f_i = 30$ to 50 kHz		45		
	Differential, $f_i = 0$ to 30 kHz		40		
	$f_i = 30$ to 50 kHz		45		

† All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTE 17: Power supply rejection measurements are made with both the ADC and the DAC channels idle and a 200-mV peak-to-peak signal applied to the appropriate supply.

3.5.11 Crosstalk Attenuation, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC channel crosstalk attenuation	DAC channel idle with DIN = 0000000000000000, ADC input = 0 dB, 1020-Hz sine wave, Gain = 0 dB (see Note 18)		80		dB
DAC channel crosstalk attenuation	ADC channel idle with INP, INM, AUX IN+, and AUX IN– at ADC V_{MID}		80		dB
	DAC channel input = digital equivalent of a 1020-Hz sine wave (see Note 19)		80		

† All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTES: 18. The test signal is a 1020-Hz sine wave with a 0 dB = 6-V peak-to-peak reference level for the analog input signal.

19. The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT–.

3.5.12 Monitor Output Characteristics, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted) (see Note 20)

PARAMETER	TEST CONDITIONS	MIN	TYPT	MAX	UNIT
$V_{O(PP)}$ Peak-to-peak ac output voltage	Quiescent level = ADC V_{MID} $Z_L = 10\text{ k}\Omega$ and 60 pF	1.3	1.5		V
V_{OO} Output offset voltage	No load, single ended relative to ADC V_{MID}		5	10	mV
V_{OC} Output common-mode voltage	No load	0.4 ADC V_{DD}	0.5 ADC V_{DD}	0.6 ADC V_{DD}	V
r_o DC output resistance			50		Ω
A_V Voltage gain (see Note 21)	Gain = 0 dB	-0.2	0	0.2	dB
	Gain 2 = -8 dB	-8.2	-8	-7.8	
	Gain 3 = -18 dB	-18.4	-18	-17.6	
	Squelch (see Note 22)			-60	

† All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTES: 20. All monitor output tests are performed with a $10\text{-k}\Omega$ load resistance.

21. Monitor gains are measured with a 1020-Hz , 6-V peak-to-peak sine wave applied differentially between $IN+$ and $IN-$. The monitor output gains are nominally 0 dB , -8 dB , and -18 dB relative to its input; however, the output gains are -6 dB relative to $IN+$ and $IN-$ or $AUX\ IN+$ and $AUX\ IN-$.

22. Squelch is measured differentially with respect to ADC V_{MID} .

3.6 Timing Requirements and Specifications in Master Mode

3.6.1 Recommended Input Timing Requirements for Master Mode, $V_{DD} = 5\text{ V}$

		MIN	NOM	MAX	UNIT
$t_{r}(\text{MCLK})$	Master clock rise time		5		ns
$t_{f}(\text{MCLK})$	Master clock fall time		5		ns
	Master clock duty cycle	40%		60%	
$t_{w}(\text{RESET})$	RESET pulse duration	1 MCLK			
$t_{su}(\text{DIN})$	DIN setup time before SCLK low (see Figure 4–2)	25			ns
$t_{h}(\text{DIN})$	DIN hold time after SCLK low (see Figure 4–2)			20	ns

3.6.2 Operating Characteristics Over Recommended Range of Operating Free-Air Temperature, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted) (see Note 23)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{f}(\text{SCLK})$	Shift clock fall time (see Figure 4–2)		13	18	ns
$t_{r}(\text{SCLK})$	Shift clock rise time (see Figure 4–2)		13	18	ns
	Shift clock duty cycle	45%		55%	
$t_{d}(\text{CH-FL})$	Delay time from SCLK high to $\overline{\text{FSD}}$ low (see Figures 4–2 and 4–4 and Note 24)		5	20	ns
$t_{d}(\text{CH-FH})$	Delay time from SCLK high to $\overline{\text{FS}}$ high (see Figure 4–2)		5	20	ns
$t_{d}(\text{CH-DOUT})$	Delay time from SCLK high to DOUT valid (see Figures 4–2 and 4–7)			20	ns
$t_{d}(\text{CH-DOUTZ})$	Delay time from SCLK↑ to DOUT in high-impedance state (see Figure 4–8)		20		ns
$t_{d}(\text{ML-EL})$	Delay time from MCLK low to EOC low (see Figure 4–9)		40		ns
$t_{d}(\text{ML-EH})$	Delay time from MCLK low to EOC high (see Figure 4–9)		40		ns
$t_{f}(\text{EL})$	EOC fall time (see Figure 4–9)		13		ns
$t_{r}(\text{EH})$	EOC rise time (see Figure 4–9)		13		ns
$t_{d}(\text{MH-CH})$	Delay time from MCLK high to SCLK high			50	ns
$t_{d}(\text{MH-CL})$	Delay time from MCLK high to SCLK low			50	ns

† All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTES: 23. All timing specifications are valid with $C_L = 20\text{ pF}$.

24. FSD occurs 1/2 shift-clock cycle ahead of $\overline{\text{FS}}$ when the device is operating in the master mode.

3.7 Timing Requirements and Specifications in Slave Mode and Codec Emulation Mode

3.7.1 Recommended Input Timing Requirements for Slave Mode, $V_{DD} = 5\text{ V}$

		MIN	NOM	MAX	UNIT
$t_r(\text{MCLK})$	Master clock rise time		5		ns
$t_f(\text{MCLK})$	Master clock fall time		5		ns
	Master clock duty cycle	40%		60%	
$t_w(\text{RESET})$	RESET pulse duration	1 MCLK			
$t_{su}(\text{DIN})$	DIN setup time before SCLK low (see Figure 4-3)	20			ns
$t_h(\text{DIN})$	DIN hold time after SCLK high (see Figure 4-3)			20	ns
$t_{su}(\text{FL-CH})$	Setup time from $\overline{\text{FS}}$ low to SCLK high			$\pm \text{SCLK}/4$	ns

3.7.2 Operating Characteristics Over Recommended Range of Operating Free-Air Temperature, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted) (see Note 23)

	PARAMETER	MIN	TYP†	MAX	UNIT
$t_c(\text{SCLK})$	Shift clock cycle time (see Figure 4-3)	125			ns
$t_f(\text{SCLK})$	Shift clock fall time (see Figure 4-3)			18	ns
$t_r(\text{SCLK})$	Shift clock rise time (see Figure 4-3)			18	ns
	Shift clock duty cycle	45%		55%	
$t_d(\text{CH-FDL})$	Delay time from SCLK high to $\overline{\text{FSD}}$ low (see Figure 4-6)			50	ns
$t_d(\text{CH-FDH})$	Delay time from SCLK high to $\overline{\text{FSD}}$ high			40	ns
$t_d(\text{FL-FDL})$	Delay time from $\overline{\text{FS}}$ low to $\overline{\text{FSD}}$ low (slave to slave) (see Figure 4-5)			40	ns
$t_d(\text{CH-DOU})$	Delay time from SCLK high to DOUT valid (see Figures 4-3 and 4-7)			40	ns
$t_d(\text{CH-DOU}Z)$	Delay time from SCLK \uparrow to DOUT in high-impedance state (see Figure 4-8)		20		ns
$t_d(\text{ML-EL})$	Delay time from MCLK low to EOC low (see Figure 4-9)		40		ns
$t_d(\text{ML-EH})$	Delay time from MCLK low to EOC high (see Figure 4-9)		40		ns
$t_f(\text{EL})$	EOC fall time (see Figure 4-9)		13		ns
$t_r(\text{EH})$	EOC rise time (see Figure 4-9)		13		ns
$t_d(\text{MH-CH})$	Delay time from MCLK high to SCLK high			50	ns
$t_d(\text{MH-CL})$	Delay time from MCLK high to SCLK low			50	ns

† All typical values are at $V_{DD} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTE 23: All timing specifications are valid with $C_L = 20\text{ pF}$.

4 Parameter Measurement Information

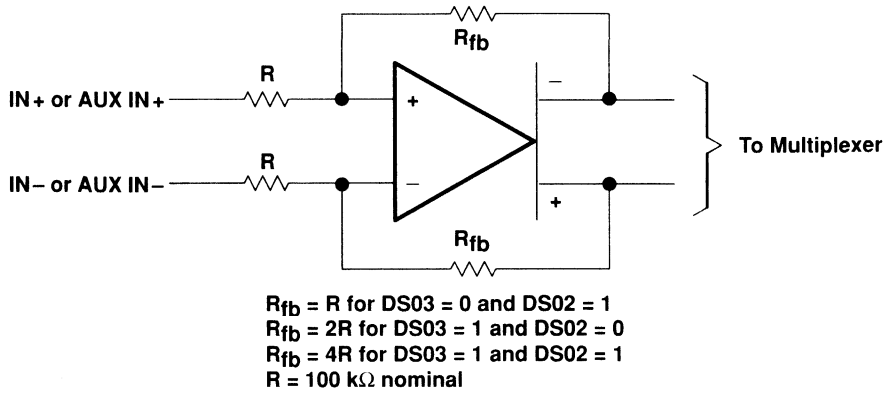


Figure 4–1. IN+ and IN– Gain-Control Circuitry

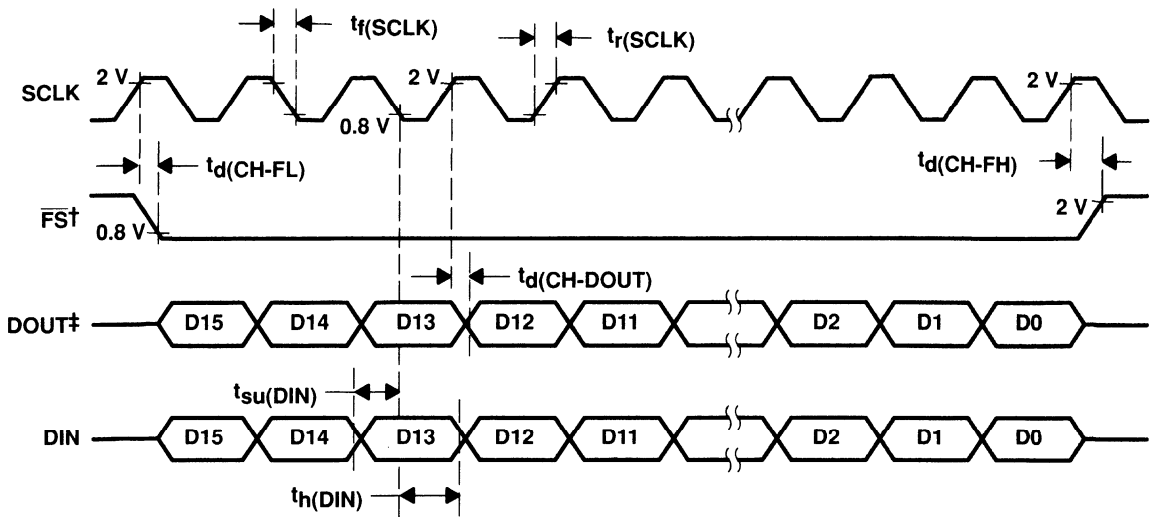
Table 4–1. Gain Control (Analog Input Signal Required for Full-Scale Bipolar A/D-Conversion 2s Complement)[†]

INPUT CONFIGURATION	CONTROL REGISTER 4		ANALOG INPUT [‡]	A/D CONVERSION RESULT
	DS03	DS02		
Differential configuration Analog input = IN+ – IN– = AUX IN+ – AUX IN–	0	0	All	Squelch
	0	1	$V_{ID} = \pm 3\text{ V}$	\pm Full scale
	1	0	$V_{ID} = \pm 1.5\text{ V}$	\pm Full scale
	1	1	$V_{ID} = \pm 0.75\text{ V}$	\pm Full scale
Single-ended configuration [§] Analog input = IN+ – V_{MID} = AUX IN+ – V_{MID}	0	0	All	Squelch
	0	1	$V_I = \pm 1.5\text{ V}$	\pm Half scale
	1	0	$V_I = \pm 1.5\text{ V}$	\pm Full scale
	1	1	$V_I = \pm 0.75\text{ V}$	\pm Full scale

[†] $V_{DD} = 5\text{ V}$

[‡] V_{ID} = differential input voltage, V_I = input voltage referenced to ADC V_{MID} with IN– or AUX IN– connected to ADC V_{MID} . In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.

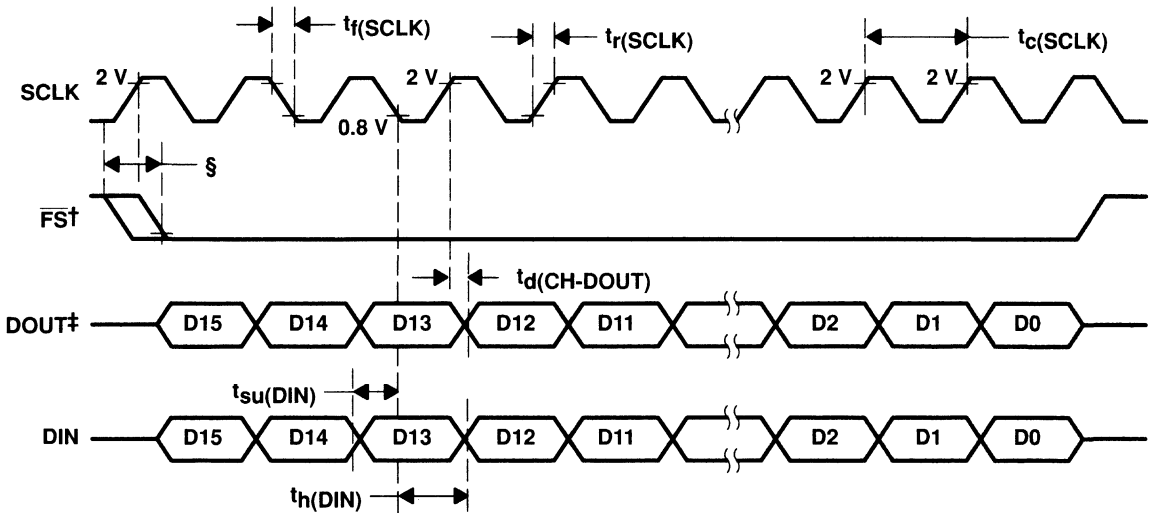
[§] For single-ended inputs, the analog input voltage should not exceed the supply rails. All single-ended inputs should be referenced to the internal reference voltage, ADC V_{MID} , for best common-mode performance.



† The time between falling edges of two primary \overline{FS} signals is the conversion period.

‡ The data on DOUT are shifted out on the rising edge of the shift clock, and the data on DIN are shifted in on the falling edge of the shift clock.

Figure 4–2. AIC Stand-Alone and Master-Mode Timing

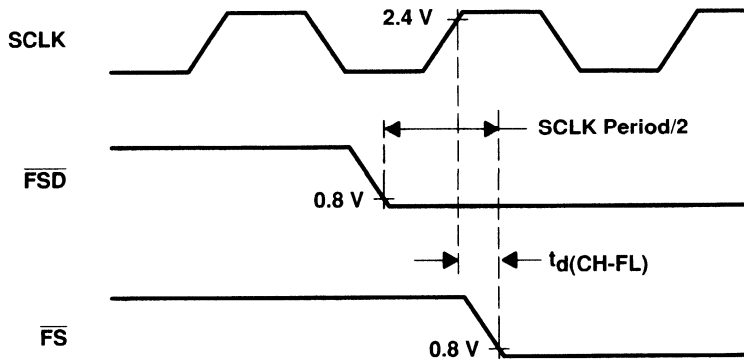


† The time between falling edges of two primary \overline{FS} signals is the conversion period.

‡ The data on DOUT are shifted out on the rising edge of the shift clock, and the data on DIN are shifted in on the falling edge of the shift clock.

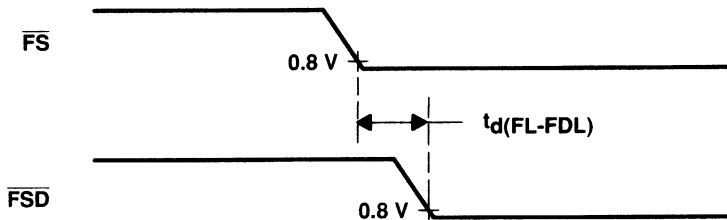
§ The high-to-low transition of \overline{FS} must occur within $\pm 1/4$ of a shift-clock period around the 2-V level of the shift clock for the codec mode.

Figure 4–3. AIC Slave and Codec Emulation Mode



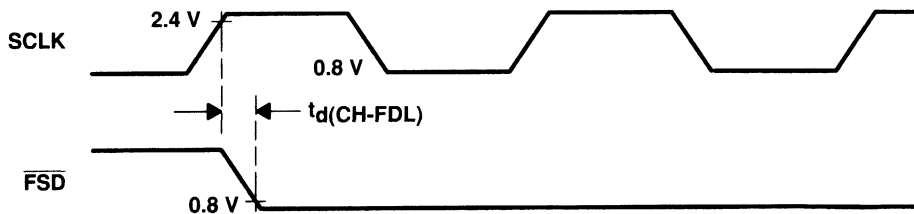
NOTE A: Timing shown is for the TLC320AC02 operating as the master or as a stand-alone device.

Figure 4–4. Master or Stand-Alone $\overline{\text{FS}}$ and $\overline{\text{FSD}}$ Timing



NOTE A: Timing shown is for the TLC320AC02 operating in the slave mode ($\overline{\text{FS}}$ and SCLK signals are generated externally). The programmed data value in the FSD register is 0.

Figure 4–5. Slave $\overline{\text{FS}}$ to $\overline{\text{FSD}}$ Timing



NOTE A: Timing shown is for the TLC320AC02 operating in the slave mode ($\overline{\text{FS}}$ and SCLK signals are generated externally). There is a data value in the FSD register greater than 18 (decimal).

Figure 4 – 6. Slave SCLK to $\overline{\text{FSD}}$ Timing

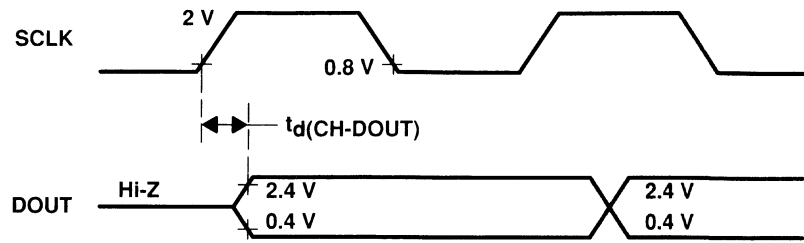


Figure 4–7. DOUT Enable Timing From Hi-Z

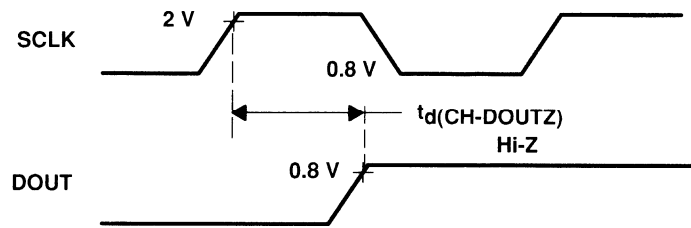


Figure 4–8. DOUT Delay Timing to Hi-Z

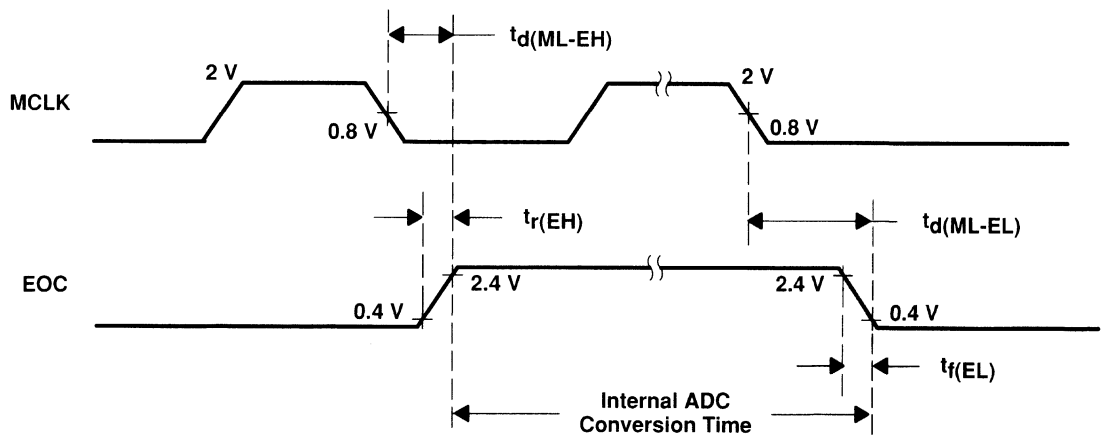
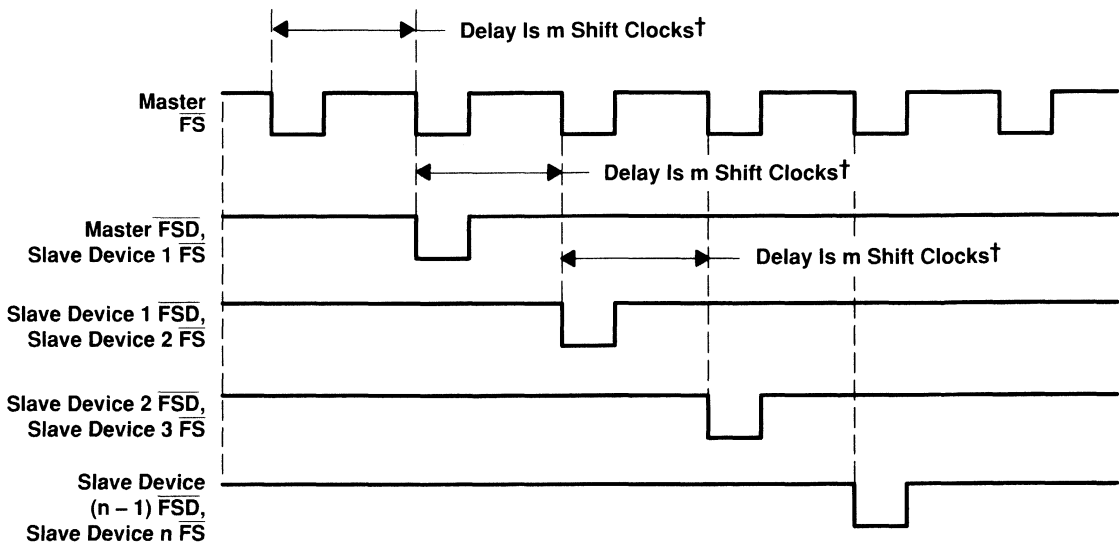


Figure 4–9. EOC Frame Timing



† The delay time from any $\overline{\text{FS}}$ signals to the corresponding $\overline{\text{FSD}}$ signals is m shift clocks with the value of m being the numerical value of the data programmed into the FSD register. In the master mode with slaves, the same data word programs the master and all slave devices; therefore, master to slave 1, slave 1 to slave 2, slave 2 to slave 3, etc., have the same delay time.

Figure 4–10. Master-Slave Frame-Sync Timing After a Delay Has Been Programmed Into the FSD Registers

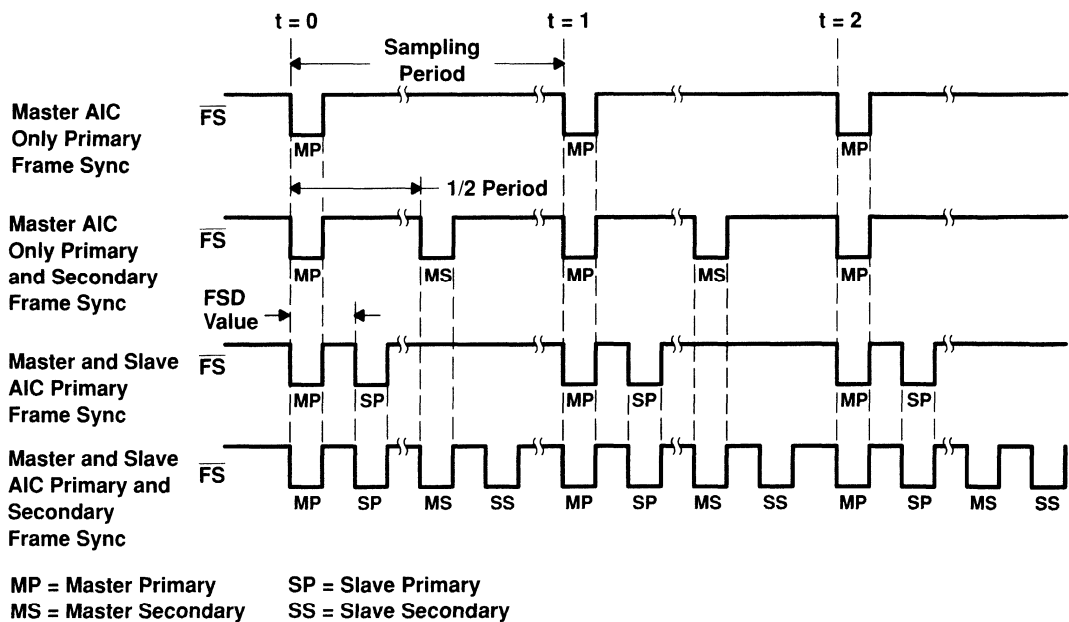
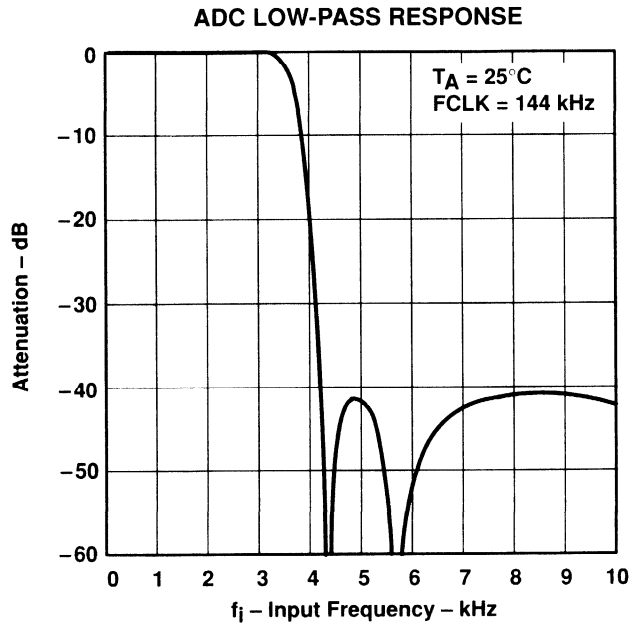


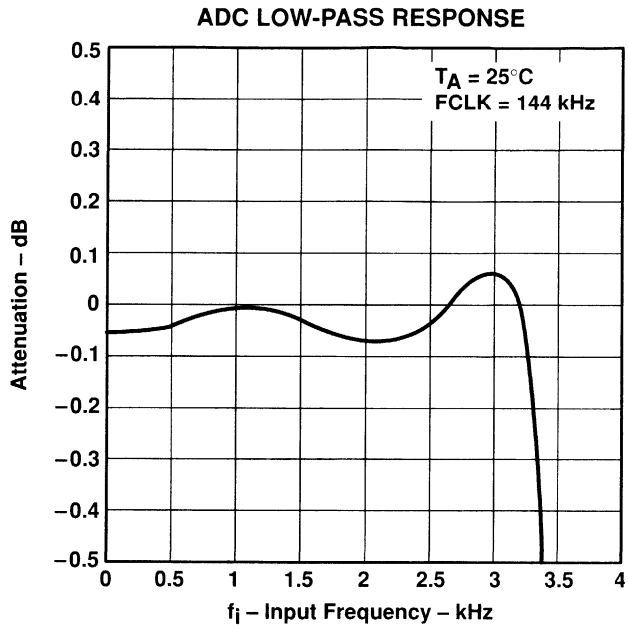
Figure 4–11. Master and Slave Frame-Sync Sequence with One Slave

5 Typical Characteristics



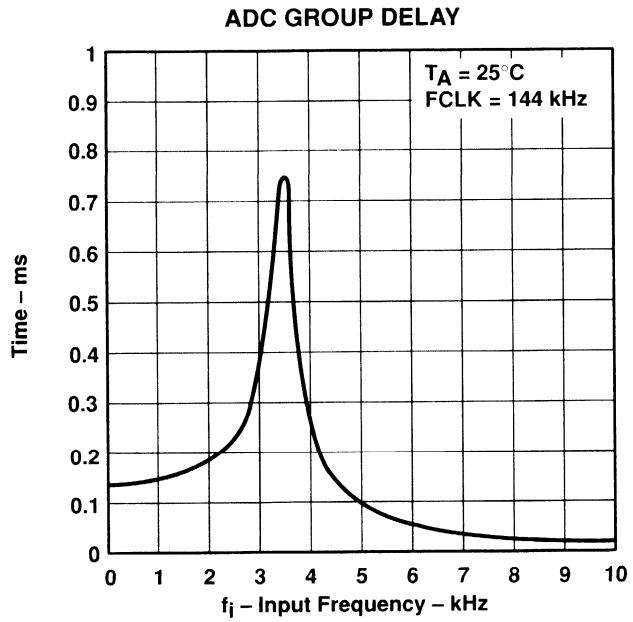
NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

Figure 5-1



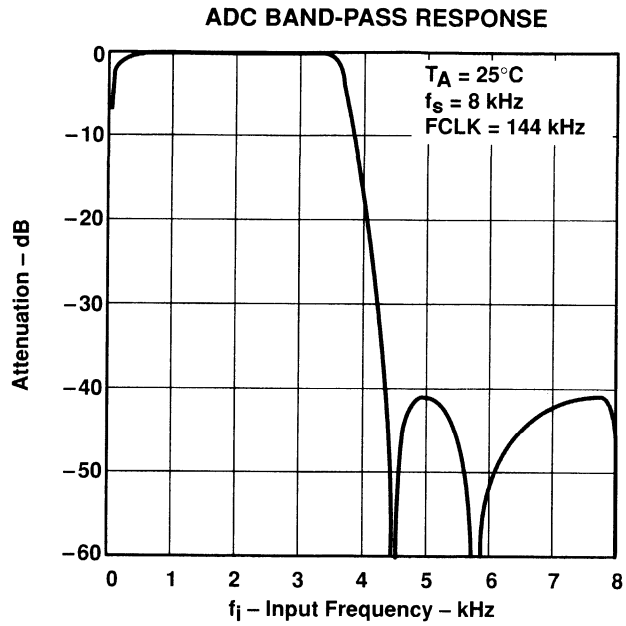
NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

Figure 5-2



NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

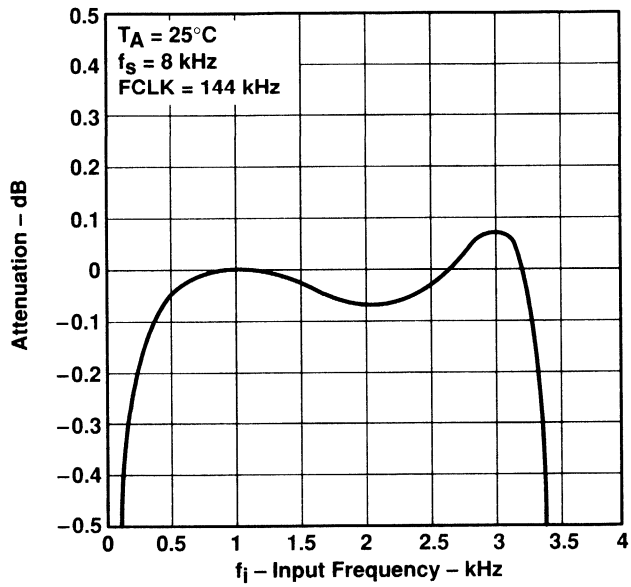
Figure 5-3



NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times FCLK\text{ (kHz)}}{144}$

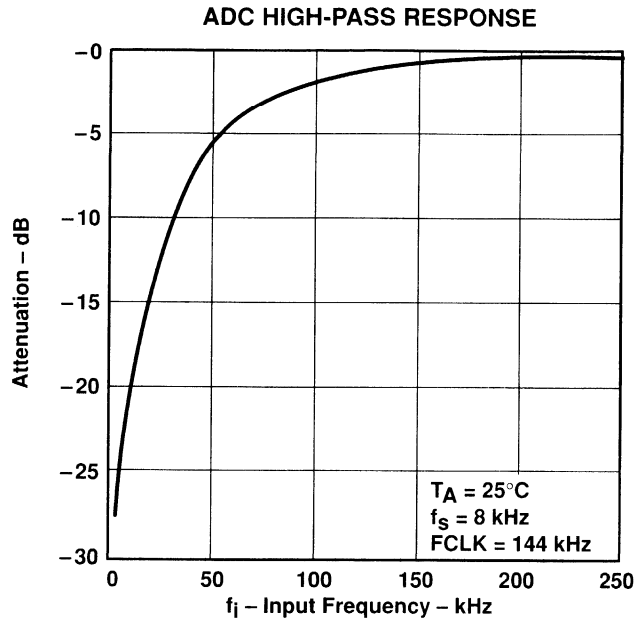
Figure 5-4

ADC BAND-PASS RESPONSE



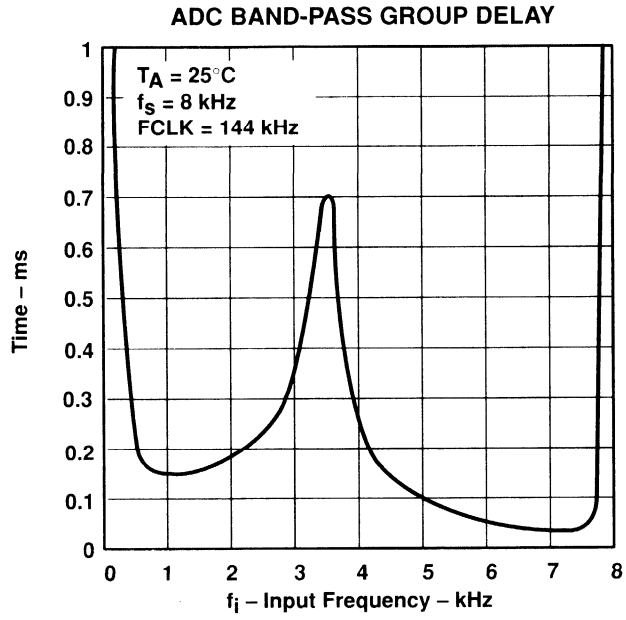
NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

Figure 5-5



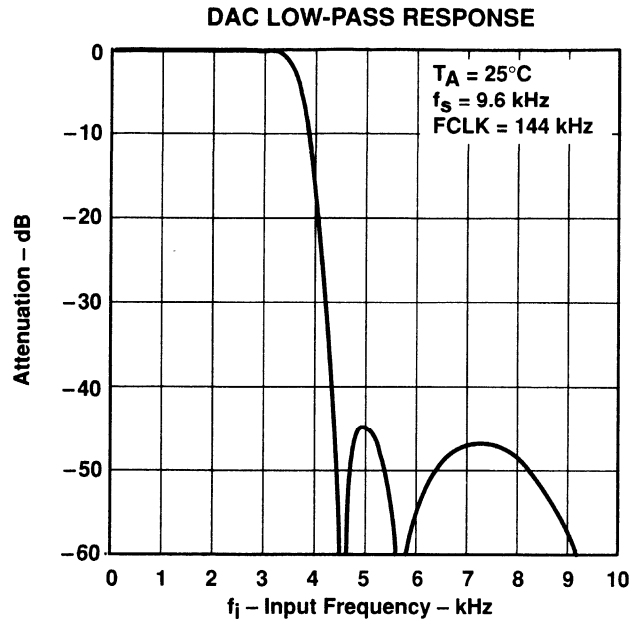
NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times FCLK \text{ (kHz)}}{144}$

Figure 5-6



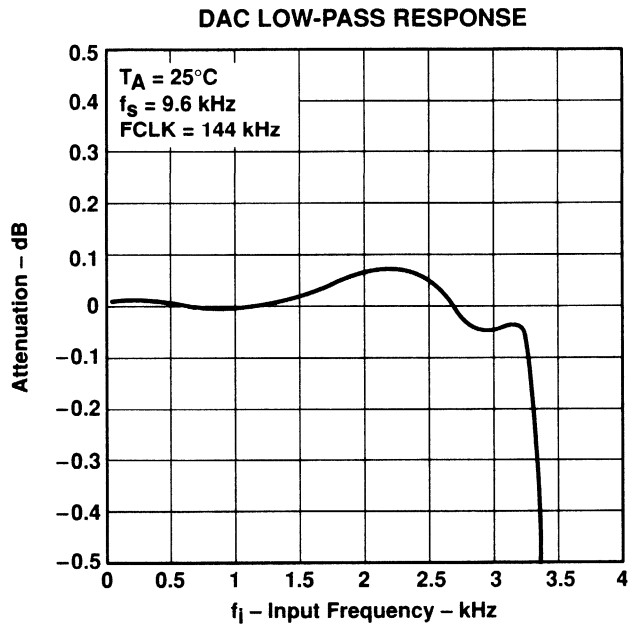
NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times FCLK\text{ (kHz)}}{144}$

Figure 5-7



NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

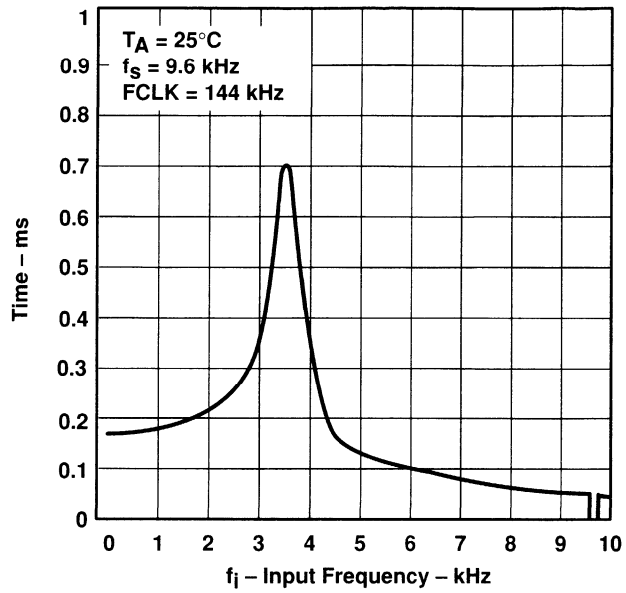
Figure 5-8



NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times FCLK \text{ (kHz)}}{144}$

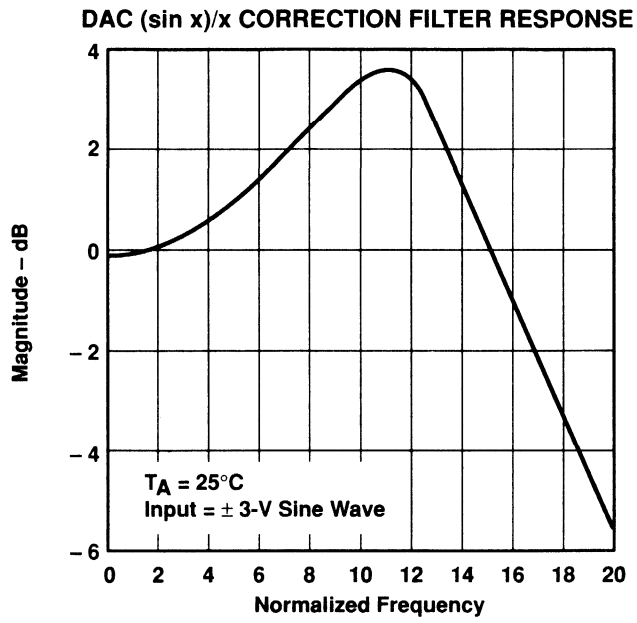
Figure 5-9

DAC LOW-PASS GROUP DELAY



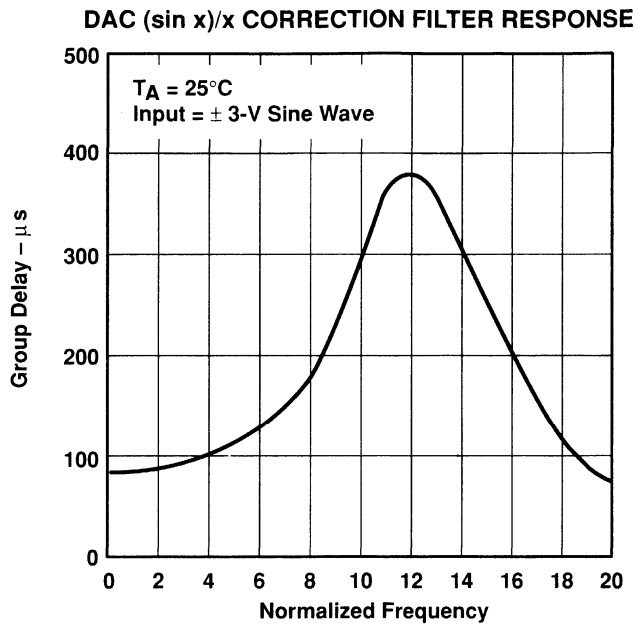
NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

Figure 5-10



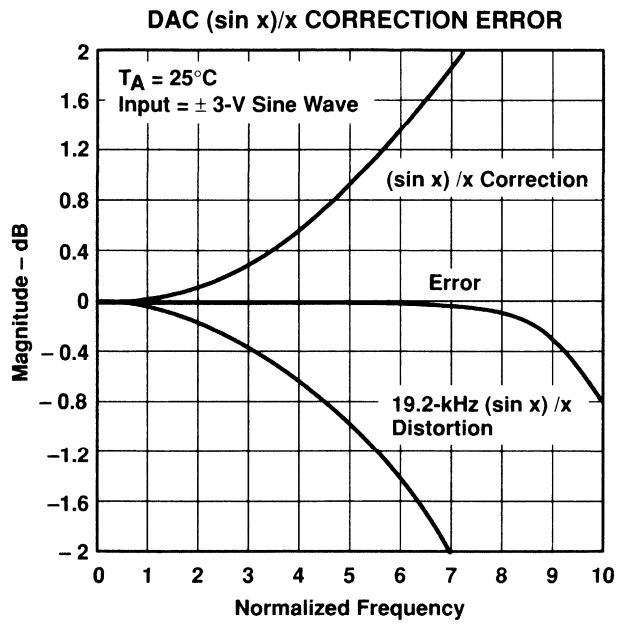
NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{288}$

Figure 5-11



NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{288}$

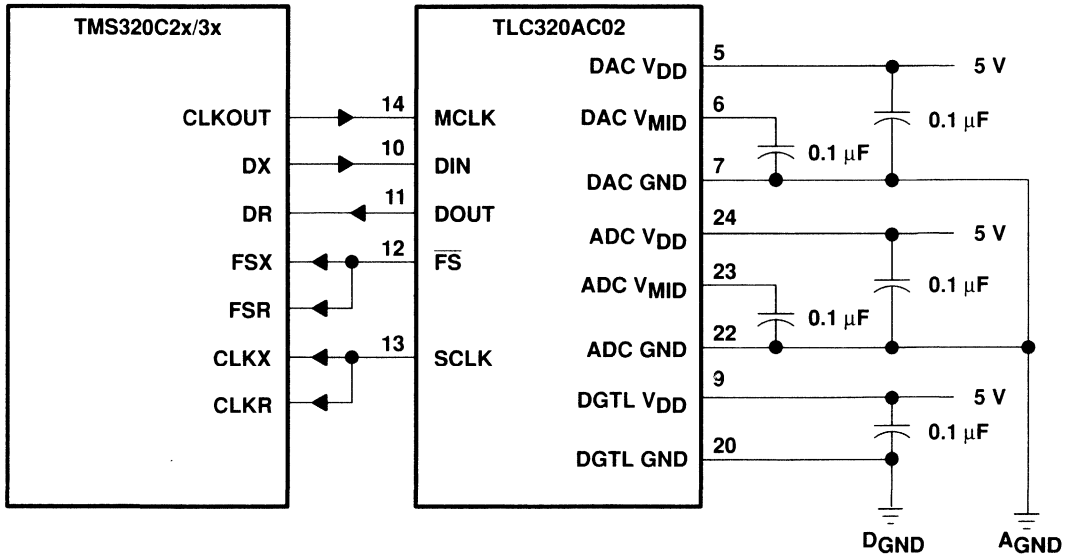
Figure 5-12



NOTE A : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{288}$

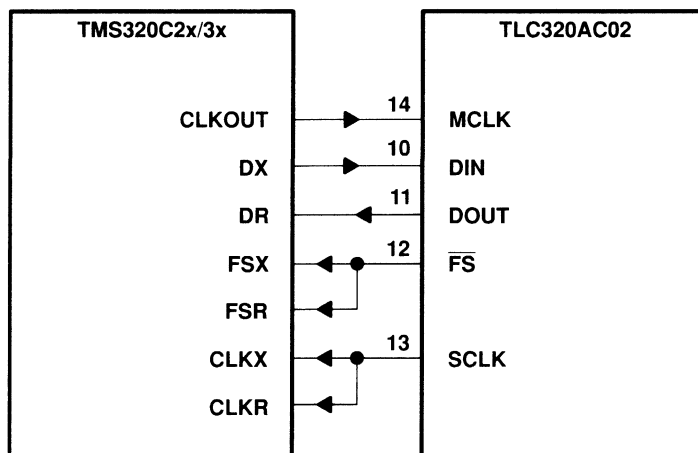
Figure 5-13

6 Application Information



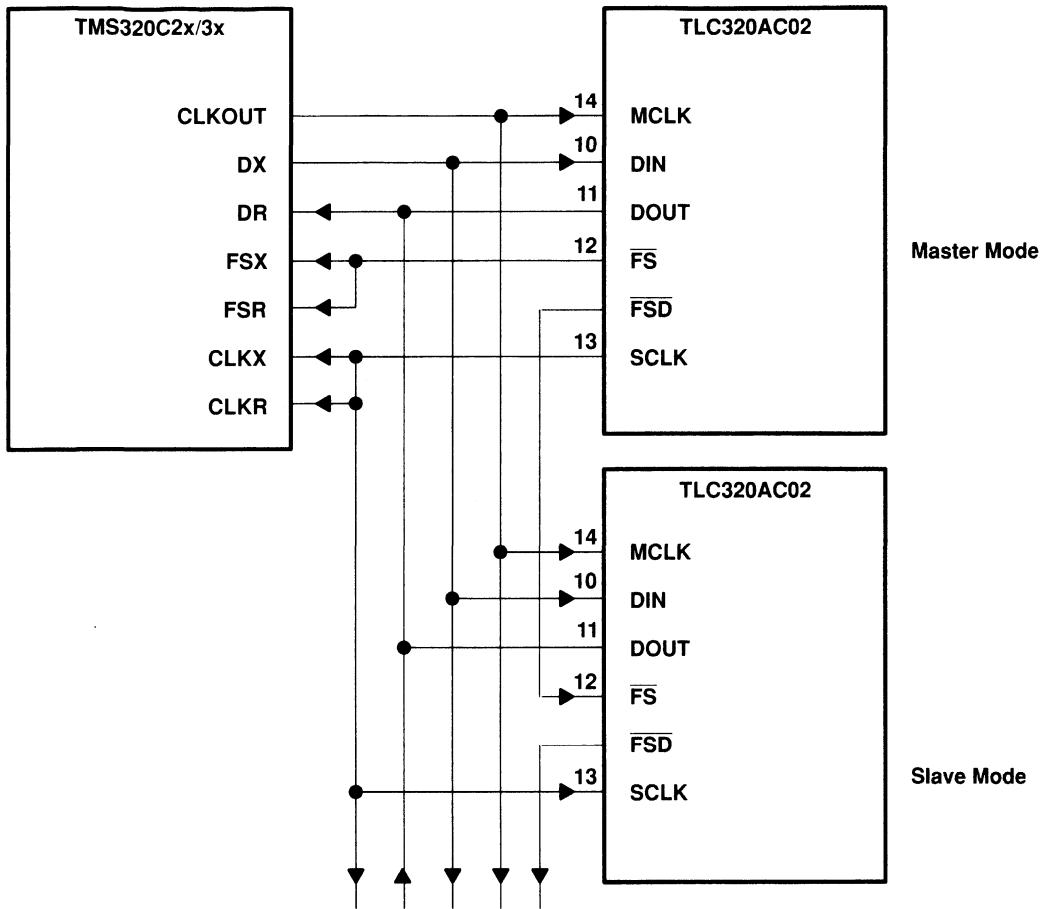
NOTE A: Terminal numbers shown are for the FN package.

Figure 6–1. Stand-Alone Mode (to DSP Interface)



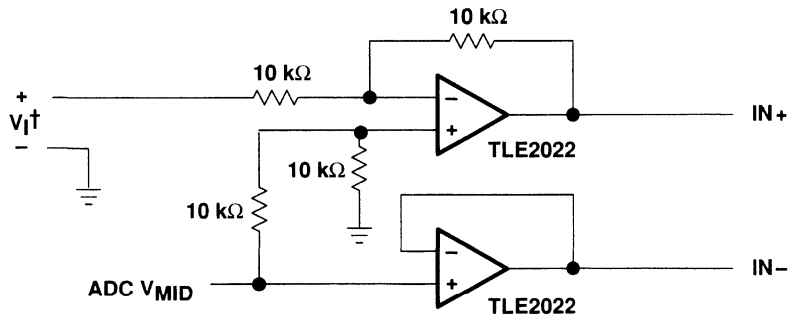
NOTE A: Terminal numbers shown are for the FN package.

Figure 6–2. Codec Mode (to DSP Interface)



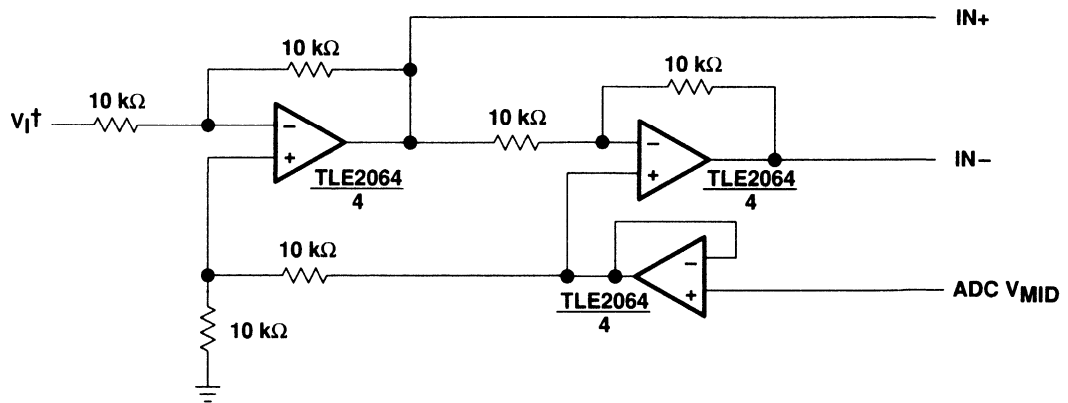
NOTE A: Terminal numbers shown are for the FN package.

Figure 6-3. Master With Slave (to DSP Interface)



† The V_1 source must be capable of sinking a current equal to $[ADC V_{MID} + |V_1|(\max)]/10 \text{ k}\Omega$.

Figure 6-4. Single-Ended Input (Ground Referenced)



† The V_1 source must be capable of sinking a current equal to $[(ADC V_{MID}/2) + |V_1|(\max)]/10 \text{ k}\Omega$.

Figure 6–5. Single-Ended to Differential Input (Ground Referenced)

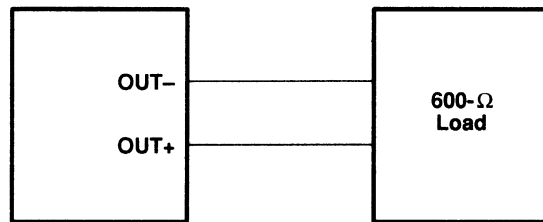
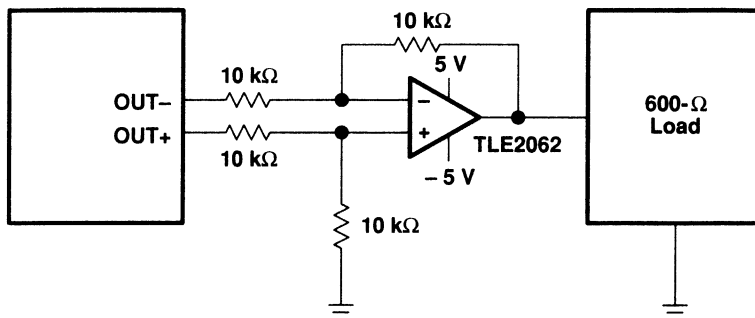


Figure 6–6. Differential Load



NOTE A: When a signal changes from a single supply with a nonzero reference system to a grounded load, the operational amplifier must be powered from plus and minus supplies or the load must be capacitively coupled.

Figure 6–7. Differential Output Drive (Ground Referenced)

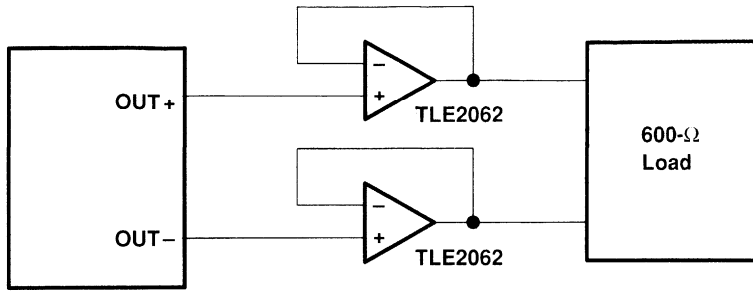
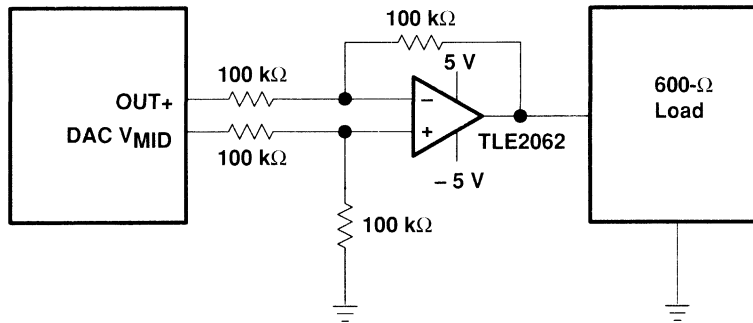


Figure 6-8. Low-Impedance Output Drive



NOTE A: When a signal changes from a single supply with a nonzero reference system to a grounded load, the operational amplifier must be powered from plus and minus supplies or the load must be capacitively coupled.

Figure 6-9. Single-Ended Output Drive (Ground Referenced)

Appendix A

Primary Control Bits

The function of the primary-word control bits D01 and D00 and the hardware terminals FC0 and FC1 are shown below. Any combinational state of D01, D00, FC1, and FC0 not shown is ignored.

CONTROL FUNCTION OF CONTROL BITS

BITS		TERMINALS		
D01	D00	FC1	FC0	
0	0	0	0	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT.
0	0	0	1	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of the next internal FS, the next ADC/DAC sampling time occurs later by the number of MCLK periods equal to the value contained in the A' register. When the A' register value is negative, the internal falling edge of FS occurs earlier.
0	0	1	0	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the rising edge of the next internal \overline{FS} , the next ADC/DAC sample time occurs earlier by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, the internal falling edge of FS occurs later.
0	0	1	1	On the next falling edge of the primary FS, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. When FC0 and FC1 are both taken high, the AIC initiates a secondary \overline{FS} to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary FS.
0	1	0	0	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00 such that on the next rising edge of \overline{FS} , the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, the falling edge of \overline{FS} occurs earlier.
1	0	0	0	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00. On the next rising edge of \overline{FS} , the next ADC/DAC sampling time occurs earlier by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, the internal falling edge of \overline{FS} occurs later.
1	1	0	0	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. When D00 and D01 are both high, the AIC initiates a secondary \overline{FS} to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary FS.

CONTROL FUNCTION OF CONTROL BITS (Continued)

BITS		TERMINALS		
D01	D00	FC1	FC0	
0	1	1	1	<p>On the next falling edge of \overline{FS}, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT.</p> <p>The phase adjustment is determined by the state of D01 and D00 such that on the next rising edge of \overline{FS}, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, \overline{FS} occurs earlier.</p> <p>When FC0 and FC1 are both taken high, the AIC initiates a secondary \overline{FS} to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary \overline{FS}.</p>
1	0	1	1	<p>On the next falling edge of \overline{FS}, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.</p> <p>The phase adjustment is determined by the state of D01 and D00. On the next rising edge of \overline{FS}, the next ADC/DAC sample time occurs earlier by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, \overline{FS} occurs later.</p> <p>When FC0 and FC1 are both taken high, the AIC initiates a secondary \overline{FS} to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary \overline{FS}.</p>
1	1	1	1	<p>On the next falling edge of the primary \overline{FS}, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.</p> <p>When FC1 and FC0 are both high or D01 and D00 are both high, the AIC initiates a secondary \overline{FS} to receive a secondary control word at DIN. The secondary \overline{FS} occurs at 1/2 the sampling time measured from the falling edge of the primary \overline{FS}.</p>
1	1	0	1	<p>On the next falling edge of \overline{FS}, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT.</p> <p>When D00 and D01 are high, the AIC initiates a secondary \overline{FS} to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary \overline{FS}.</p> <p>The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of \overline{FS}, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, \overline{FS} occurs earlier.</p>
1	1	1	0	<p>On the next falling edge of \overline{FS}, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT.</p> <p>When D00 and D01 are high, the AIC initiates a secondary \overline{FS} to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary \overline{FS}.</p> <p>The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of \overline{FS}, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, \overline{FS} occurs earlier.</p>
1	1	1	1	<p>On the next falling edge of \overline{FS}, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.</p> <p>When FC1 and FC0 are both high or D01 and D00 are both high, the AIC initiates a secondary \overline{FS} to receive a secondary control word at DIN. The secondary \overline{FS} occurs at 1/2 the sampling time measured from the falling edge of the primary \overline{FS}.</p>

Appendix B

Secondary Communications

The function of the control bits DS15 and DS14 and the hardware terminals FC0 and FC1 are shown below. Any combinational state of DS15, DS14, FC1, and FC0 not shown is ignored.

CONTROL FUNCTION OF SECONDARY COMMUNICATION

BITS		TERMINALS		
DS15	DS14	FC1	FC0	
0	0	Ignored		On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.
0	1	Ignored		On the next falling edge of the \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of DS15 and DS14 such that on the next rising edge of \overline{FS} , the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, \overline{FS} occurs earlier.
1	0	Ignored		On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00. On the next rising edge of \overline{FS} , the next ADC/DAC sampling time occurs earlier by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, \overline{FS} occurs later.
1	1	0	0	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.
1	1	0	1	On the next falling edge of the \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of \overline{FS} , the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, \overline{FS} occurs earlier.
1	1	1	0	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of \overline{FS} , the next ADC/DAC sampling time occurs earlier by the number of MCLK periods determined by the value contained in the A' register. When the A' register value is negative, \overline{FS} occurs later.
1	1	1	1	On the next falling edge of \overline{FS} , the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.

Appendix C

TLC320AC01C/TLC320AC02C Specification Comparisons

Texas Instruments manufactures the TLC320AC01C and the TLC320AC02C specified for the 0°C to 70°C commercial temperature range and the TLC320AC02I specified for the -40°C to 85°C temperature range. The TLC320AC02C and TLC320AC02I operate at a relaxed TLC320AC01C specification. The differences are listed in the following tables.

ADC Channel Signal-to-Distortion Ratio, $V_{DD} = 5\text{ V}$, $f_s = 8\text{ kHz}$ (Unless Otherwise Noted) (see Note 1)

PARAMETER	TEST CONDITIONS	$A_V = 0\text{ dB}$		$A_V = 6\text{ dB}$		$A_V = 12\text{ dB}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
TLC320AC01	$V_I = -6\text{ dB to } -1\text{ dB}$	68		—		—		dB
TLC320AC02		64		—		—		
TLC320AC01	$V_I = -12\text{ dB to } -6\text{ dB}$	63		68		—		
TLC320AC02		59		64		—		
TLC320AC01	$V_I = -18\text{ dB to } -12\text{ dB}$	57		63		68		
TLC320AC02		56		59		64		
TLC320AC01	$V_I = -24\text{ dB to } -18\text{ dB}$	51		57		63		
TLC320AC02		50		56		59		
TLC320AC01	$V_I = -30\text{ dB to } -24\text{ dB}$	45		51		57		
TLC320AC02		44		50		56		
TLC320AC01	$V_I = -36\text{ dB to } -30\text{ dB}$	39		45		51		
TLC320AC02		38		44		50		
TLC320AC01	$V_I = -42\text{ dB to } -36\text{ dB}$	33		39		45		
TLC320AC02		32		38		44		
TLC320AC01	$V_I = -48\text{ dB to } -42\text{ dB}$	27		33		39		
TLC320AC02		26		32		38		

NOTE 1: The analog-input test signal is a 1020-Hz sine wave with 0 dB = 6 V peak to peak as the reference level for the analog input signal.

DAC Channel Signal-to-Distortion Ratio, $V_{DD} = 5\text{ V}$, $f_s = 8\text{ kHz}$ (Unless Otherwise Noted) (see Note 2)

PARAMETER	TEST CONDITIONS	$A_V = 0\text{ dB}$		$A_V = -6\text{ dB}$		$A_V = -12\text{ dB}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
TLC320AC01	$V_O = -6\text{ dB to } 0\text{ dB}$	68		—		—		dB
TLC320AC02		64		—		—		
TLC320AC01	$V_O = -12\text{ dB to } -6\text{ dB}$	63		68		—		
TLC320AC02		59		64		—		
TLC320AC01	$V_O = -18\text{ dB to } -12\text{ dB}$	57		63		68		
TLC320AC02		56		59		64		
TLC320AC01	$V_O = -24\text{ dB to } -18\text{ dB}$	51		57		63		
TLC320AC02		50		56		59		
TLC320AC01	$V_O = -30\text{ dB to } -24\text{ dB}$	45		51		57		
TLC320AC02		44		50		56		
TLC320AC01	$V_O = -36\text{ dB to } -30\text{ dB}$	39		45		51		
TLC320AC02		38		44		50		
TLC320AC01	$V_O = -42\text{ dB to } -36\text{ dB}$	33		39		45		
TLC320AC02		32		38		44		
TLC320AC01	$V_O = -48\text{ dB to } -42\text{ dB}$	27		33		39		
TLC320AC02		26		32		38		

NOTE 2: The input signal, V_I , is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at full-scale digital input = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT-.

**System Distortion, ADC Channel Attenuation, $V_{DD} = 5\text{ V}$, $f_S = 8\text{ kHz}$,
FCLK = 144 kHz (Unless Otherwise Noted)**

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
TLC320AC01	Second harmonic	Differential input (see Note 3)	70		dB
TLC320AC02			64		dB
TLC320AC01	Third harmonic and higher harmonics		70		dB
TLC320AC02			64		dB

NOTE 3: The input signal is a 1020 Hz-sine wave for the ADC channel. Harmonic distortion is defined for an input level of -1 dB .

**System Distortion, DAC Channel Attenuation, $V_{DD} = 5\text{ V}$, $f_S = 8\text{ kHz}$,
FCLK = 144 kHz (Unless Otherwise Noted)**

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
TLC320AC01	Second harmonic	Differential output (see Note 4)	70		dB
TLC320AC02			64		dB
TLC320AC01	Third harmonic and higher harmonics		70		dB
TLC320AC02			64		dB

NOTE 4: The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is $600\ \Omega$ from OUT+ to OUT-. Harmonic distortion is specified for a signal input level of 0 dB.

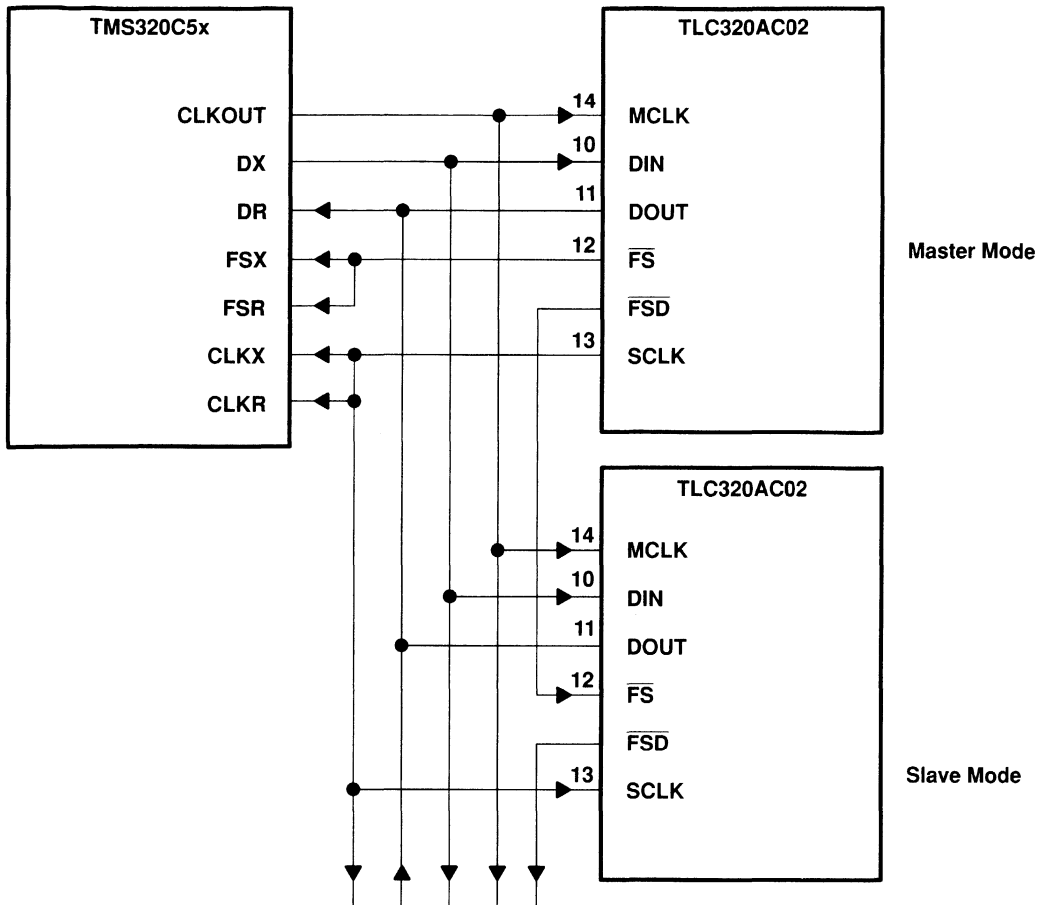
Appendix D

Multiple TLC320AC01/02 Analog Interface Circuits on One TMS320C5X DSP Serial Port

In many applications, digital signal processors (DSP) must obtain information from multiple analog-to-digital (A/D) channels and transmit digital data to multiple digital-to-analog (D/A) conversion channels. The problem is how to do it easily and efficiently.

This application report addresses the issue of connecting two channels of an analog interface circuit (AIC) to one TMS320C5X DSP serial port. In this application report, the AIC is the TLC320AC02.

The TLC320AC02 (and TLC320AC01) analog interface circuit contains both A/D and D/A converters and using the master/slave mode, it is possible to connect two of them to one TMS320C5X DSP serial port with no additional logic. The hardware schematic is shown in Figure D-1.



NOTE A: Terminal numbers shown are for the FN package.

Figure D-1. Master With Slave (to DSP Interface)

HARDWARE AND SOFTWARE SOLUTION

Once the hardware connections are completed, the issue becomes distinguishing one channel from another. Fortunately, this is very easy to do in software and adds very little overhead. The mode that the AC02s run in is called master/slave mode. One AC02 is the master and all of the rest of the AC02s are slaves. The master can be distinguished from all of the slaves by examining the least significant bit (LSB) in the receive word coming from the AC02. The master has a 0 in the LSB and all of the slaves have a 1 in the LSB.

The AC02s in master/slave mode take turns communicating with the DSP serial port. They do this in a round robin or circular fashion. Synchronizing the system involves looking for the master AC02 and then starting the software associated with the first AC02. All other AC02s follow in order. It is possible to have different software for each AC02.

A reference design was constructed using a TMS320C5X DSP starter kit (DSK). The AC02s were connected to the TDM serial port which is available at the headers on the edge of the DSK.

A listing of the DSK assembly code for a simple stereo input/output program is included in the following section.

SOFTWARE MODULE

```
*****
*
* MODULE NAME: INOUTB.ASM
*
* In-out routine for C5X DSK with two TLC320AC02s on the
* TDM serial port of the C5X in master/slave mode.
*
* This version performs the in/out task for both the master
* and slave TLC320AC02 in the receive interrupt service
* routine.
*
*****
```

```
*
* .mmregs
*
* .ds      01000h
*
PR1      .word    0104h      ;A register
PR2      .word    0219h      ;B register
PR3      .word    0300h      ;A prime register
PR4      .word    0405h      ;amplifier gain register
PR5      .word    0501h      ;analog configuration register
PR6      .word    0600h      ;digital configuration register
PR7      .word    0730h      ;frame synch delay register
PR8      .word    0802h      ;frame synch number register
value    .word    0800h
value2   .word    0800h
val_add  .word    0200h
val_add2 .word    0400h
```

```
*****
*
* Set up the ISR vector
*
*****
```

```

* .ps      080ah
*
rint:    B      RECEIVE      ; 0A; Serial port receive interrupt RINT.
xint:    B      TRANSMIT     ; 0C; Serial port transmit interrupt XINT.
trint:   B      TDMREC
txint:   B      TDMTX
; -----
```

```
*
* *****
*
* TMS320C5X INITIALIZATION
*
*****
```

```

* .ps 0a00h
*
* .entry
*
START:   SETC      INTM      ; Disable interrupts
         LDP       #0        ; Set data page pointer
         OPL      #0834h,PMST
         LACC     #0
         SAMP     CWSR
         SAMP     PDWSR
```

```

splk          #00c8h
SPLK          082h,IMR
call          AC02INIT

CLRC          OVM          ; OVM = 0
SPM           0           ; PM = 0
SPLK          #042h,IMR   ; TDMA ser port rec interrupt
SPLK          #0C8h,TSPC  ;
CLRC          INTM        ; enable interrupts

loop          ; main program here does nothing.
nop          ; a user program can be inserted.
b            loop        ;

;----- end of main program ----- ;
;
; TDM serial port receiver interrupt service routine
;
TDMREC:
; This loop insures that the master AC02
ldp          #trcv        ; is the first one that is written to in the
bit          trcv,15      ; loop. the slave AC02(s) will follow in
bcnd         xxx,tc       ; sequential order. The master AC02 has a
; 0 in the 1sb. the slave AC02(s) have a 1
; in the 1sb of the receive word.

ldp          #trcv
lacc         trcv
and          #0fffch

;
; user code would go here for master AC02
;

sacl         tdxr
b            yyy

xxx

ldp          #trcv
lacc         trcv
and          #0fffch

;
; user code would go here for slave AC02
;

sacl         tdxr

yyy

rete

```

```
;
; TDM serial port transmit interrupt service routine
;
TDMTX:
    rete

;
; RECEIVER INTERRUPT SERVICE ROUTINE
;
RECEIVE:
    rete

TRANSMIT:
    RETE
```

AC02INIT

```
SPLK      #020h,TCR
SPLK      #01h,PRD
MAR        *,AR0
LACC      #0008h
SACL      TSPC
LACC      #00c8h
SACL      TSPC
SETC      SXM
```

; -----

```
LDP        #PR1
LACC      PR1
CALL      AC02_2ND
```

; -----

```
LDP        #PR2
LACC      PR2
CALL      AC02_2ND
```

; -----

```
LDP        #PR8
LACC      PR8
CALL      AC02_2ND
```

; -----

```
LDP        #PR7
LACC      PR7
CALL      AC02_2ND
```

ret

AC02_2ND:

```
LDP        #0
SACH      TDXR      ;
CLRC      INTM
IDLE
ADD        #6h, 15      ; 0000 0000 0000 0011 XXXX XXXX XXXX XXXX b
SACH      TDXR      ;
IDLE
SACL      TDXR      ;
IDLE
LACL      #0      ;
SACL      TDXR      ; make sure the word got sent
IDLE
SETC      INTM      ;
RET
```

TLC320AD50C, TLC320AD52C Data Manual

***Sigma-Delta Analog Interface Circuits
With Master-Slave Function***

***SLAS131A
November 1997***



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Contents

<i>Section</i>	<i>Title</i>	<i>Page</i>
1	Introduction	4–367
1.1	Features	4–367
1.2	Functional Block Diagram	4–368
1.3	Terminal Assignments	4–369
1.4	Ordering Information	4–370
1.5	Terminal Functions	4–370
1.6	Definitions and Terminology	4–372
1.7	Register Functional Summary	4–373
2	Detailed Description	4–375
2.1	Device Functions	4–375
2.1.1	Operating Frequencies	4–375
2.1.2	ADC Signal Channel	4–375
2.1.3	DAC Signal Channel	4–376
2.1.4	Serial Interface	4–378
2.1.5	Register Programming	4–378
2.1.6	Sigma–Delta ADC	4–380
2.1.7	Decimation Filter	4–380
2.1.8	Sigma–Delta DAC	4–380
2.1.9	Interpolation Filter	4–380
2.1.10	Analog and Digital Loopback	4–380
2.1.11	FIR Overflow Flag	4–380
2.2	Reset and Power-Down Functions	4–381
2.2.1	Software and Hardware Reset	4–381
2.2.2	Software and Hardware Power Down	4–381
2.3	Master Clock Circuit	4–382
2.4	Data Out (DOUT)	4–382
2.4.1	Data Out, Master Mode	4–382
2.4.2	Data Out, Slave Mode	4–382
2.5	Data In (DIN)	4–382
2.6	FC (Hardware Secondary Communication Request)	4–382
2.7	Frame-Sync Function for TLC320AD50C	4–382
2.7.1	Frame Sync (FS) Function, Master Mode	4–383
2.7.2	Frame Sync (FS) Function, Slave Mode	4–384
2.7.3	Frame-Sync Delayed (FSD) Function, Master Mode	4–384
2.7.4	Frame-Sync Delayed (FSD), Slave Mode	4–386
2.8	Frame-Sync Function For TLC320AD52C	4–387
2.9	Multiplexed Analog Input and Output	4–388
2.9.1	Multiplexed Analog Input	4–388
2.9.2	Analog Output	4–389
3	Serial Communications	4–391
3.1	Primary Serial Communication	4–391

3.2	Secondary Serial Communication	4-392
3.2.1	Hardware Secondary Serial Communication Request	4-393
3.2.2	Software Secondary Serial Communication Request	4-393
3.3	Conversion Rate Versus Serial Port	4-394
3.5	DIN and DOUT Data Format	4-395
3.5.1	Primary Serial Communication DIN and DOUT Data Format	4-395
3.5.2	Secondary Serial Communication DIN and DOUT Data Format	4-395
4	Specifications	4-397
4.1	Absolute Maximum Ratings Over Operating Free-Air Temperature Range	4-397
4.2	Recommended Operating Conditions	4-397
4.2.1	Recommended Operating Conditions, DVDD = 5 V	4-397
4.2.2	Recommended Operating Conditions, DVDD = 3 V	4-397
4.3	Electrical Characteristics Over Recommended Operating Free-Air Temperature Range	4-398
4.3.1	Digital Inputs and Outputs	4-398
4.3.2	Digital Inputs and Outputs, DVDD = 3 V	4-398
4.3.3	ADC Path Filter	4-398
4.3.4	ADC Dynamic Performance	4-398
4.3.5	ADC Channel Characteristics	4-399
4.3.6	DAC Path Filter	4-399
4.3.7	DAC Dynamic Performance	4-400
4.3.8	DAC Channel Characteristics	4-401
4.3.9	Power Supply	4-401
4.3.10	Power-Supply Rejection	4-401
4.4	Timing Characteristics	4-402
4.4.1	Master Mode Timing Requirements	4-402
4.4.2	Slave Mode Timing Requirements	4-402
4.4.3	Master Mode Switching Characteristics	4-402
4.4.4	Slave Mode Switching Characteristics	4-402
5	Parameter Measurement Information	4-409
6	Register Set	4-411
6.1	Control 1 Register	4-412
6.2	Control 2 Register	4-412
6.3	Control 3 Register	4-413
6.4	Control 4 Register	4-413
7	Application Information	4-415

List of Illustrations

<i>Figure</i>	<i>Title</i>	<i>Page</i>
2-1	Timing Sequence of ADC Channel (Primary Communication Only)	4-376
2-2	Timing Sequence of ADC Channel (Primary and Secondary Communication) . . .	4-376
2-3	Timing Sequence of DAC Channel (Primary Communication Only)	4-377
2-4	Timing Sequence of DAC Channel (Primary and Secondary Communication) . . .	4-377
2-5	Register 1 Read Operation Timing Diagram	4-378
2-6	Register 1 Write Operation Timing Diagram	4-379
2-7	Internal Power-Down Logic	4-381
2-8	Master Device Frame-Sync Signal With Primary and Secondary Communications (No Slaves)	4-383
2-9	Master Device Frame-Sync Signal With Primary and Secondary Communications (With 1 Slave Device)	4-383
2-10	Master Device FS and FSD Output When FSD Register (D0-D5, Control Register 3) is 0	4-384
2-11	Master Device FS and FSD Output After Control Register 3 Is Programmed (One Slave Device)	4-385
2-12	Master With Slaves (To DSP Interface)	4-386
2-13	Master-Slave Frame-Sync Timing After A Delay Has Been Programmed Into The FSD Register (D0-D5 of Control Register 3)	4-386
2-14	Master Device FS and FSD Output After Control Register 3 Is Programmed with 49H	4-387
2-15	RC Antialias Filter	4-388
2-16	INP and INM Internal Self-Biased (2.5 V) Circuit	4-388
2-17	Differential Output Drive (Ground Referenced)	4-389
3-1	Primary Serial Communication Timing	4-391
3-2	Hardware and Software Methods to Make a Secondary Request	4-392
3-3	FS Output When Hardware Secondary Serial Communication Is Requested Only Once (No Slave)	4-393
3-4	FS Output When Hardware Secondary Serial Communication Is Requested Only Once (Three Slaves)	4-393
3-5	FS Output During Software Secondary Serial Communication Request (No Slave)	4-394
3-6	Phone Mode Timing When Phone Mode is Enabled	4-394
3-7	Primary Communication DIN and DOUT Data Format	4-395
3-8	Secondary Communication DIN and DOUT Data Format	4-395
4-1	ADC Decimation Filter Response	4-403
4-2	ADC Decimation Filter Passband Ripple	4-403
4-3	DAC Interpolation Filter Response	4-404
4-4	DAC Interpolation Filter Passband Ripple	4-404

List of Illustrations (continued)

<i>Figure</i>	<i>Title</i>	<i>Page</i>
5-1	Master FS and FSD Timing	4-409
5-2	Slave FS to FSD Timing	4-409
5-3	Slave SCLK to FSD Timing	4-409
5-4	Serial Communication Timing (Master Mode)	4-410
5-5	Serial Communication Timing (Slave Mode)	4-410
7-1	Master Device and Slave Device Connections (to DSP Interface)	4-415
7-2	Power Supply Decoupling	4-416

List of Tables

<i>Table</i>	<i>Title</i>	<i>Page</i>
3-1	Least Significant Bit Control Function	4-392
6-1	Register Map	4-411
6-2	Control 1 Register	4-412
6-3	Control 2 Register	4-412
6-4	Control 3 Register	4-413
6-5	Control 4 Register	4-413

1 Introduction

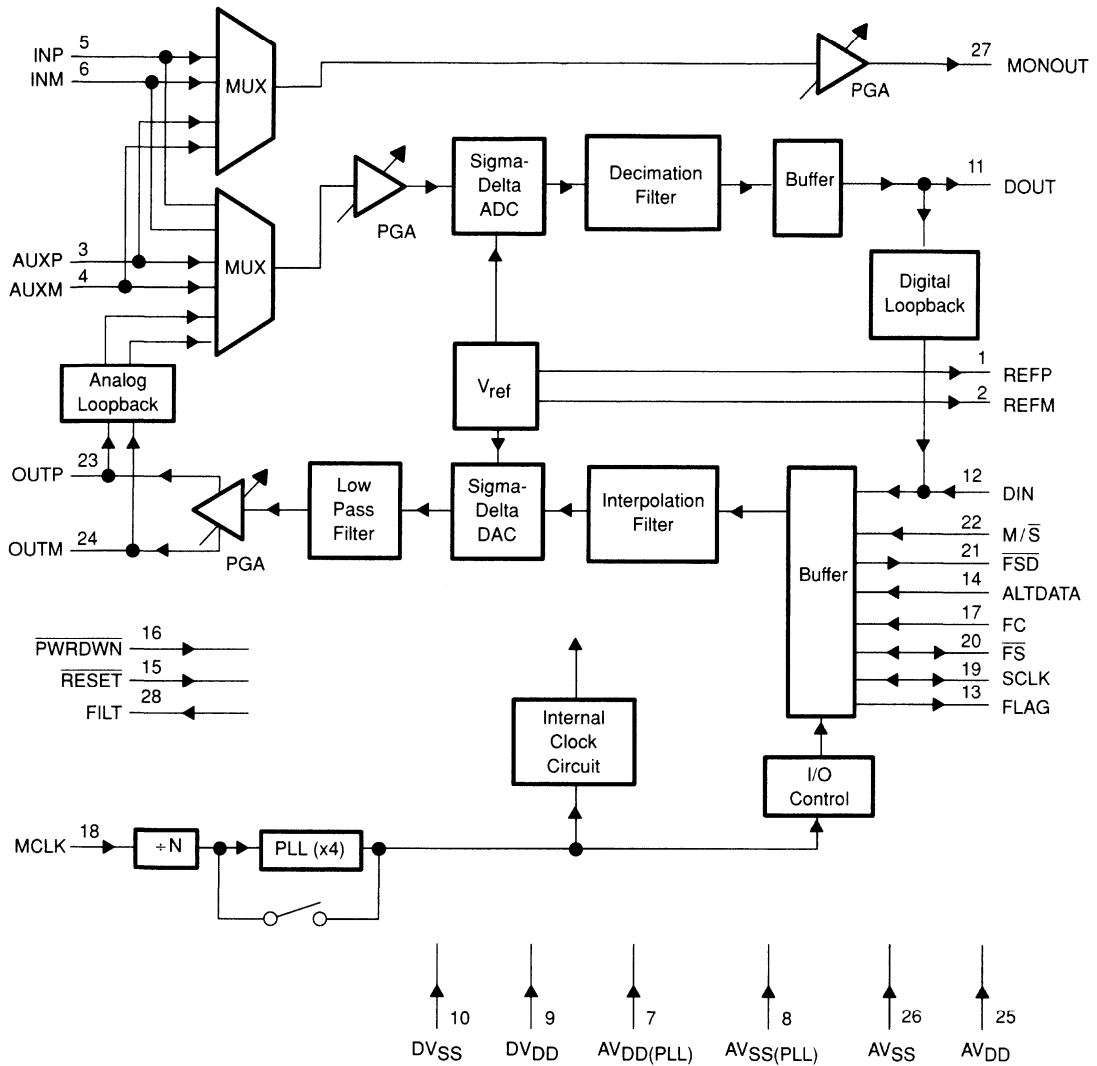
The TLC320AD50C and TLC320AD52 provide high-resolution signal conversion from digital-to-analog (D/A) and from analog-to-digital (A/D) using oversampling sigma–delta technology. This device consists of a pair of 16-bit synchronous serial conversion paths (one for each direction) and includes an interpolation filter before the DAC and a decimation filter after the ADC. Other overhead functions on the chip include timing (sample rate, \overline{FSD} delay) and control (programmable gain amplifier, PLL, communication protocol, etc.). The sigma–delta architecture produces high resolution A/D and D/A conversion at a low system cost.

Programmable functions of this device can be selected through the serial interface. Options include reset, power down, communications protocol, signal sampling rate, gain control, and system test modes (see section 6). The TLC320AD50C and TLC320AD52 are characterized for operation from 0°C to 70°C.

1.1 Features

- General-purpose analog interface circuit for V.34+ modem and business audio applications
- 16-bit oversampling sigma–delta ADC and DAC
- Serial port interface
- Typical 89-dB SNR (signal-to-noise ratio) for ADC and DAC
- Typical 90-dB THD (signal to total harmonic distortion) for ADC and DAC
- Typical 88-dB dynamic range
- Test mode that includes a digital loopback test and analog loopback test
- Programmable A/D and D/A conversion rate
- Programmable input and output gain control
- Maximum conversion rate: 22.05 kHz
- Single 5-V power supply voltage or 5-V analog and 3-V digital power supply voltage
- Power dissipation (P_D) of 120 mW rms typical in the operating mode
- Hardware power-down mode to 7.5 mW
- Internal reference voltage (V_{ref})
- Differential architecture throughout device
- TLC320AD50C can support up to three slave devices; TLC320AD52C can support one slave
- 2's complement data format
- ALTDATA terminal provides data monitoring
- Monitor amplifier to monitor input signals
- On-chip phase locked loop (PLL)

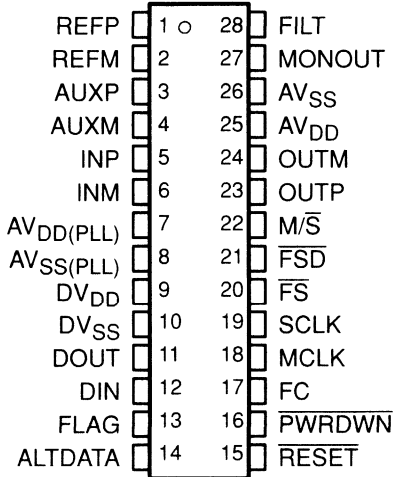
1.2 Functional Block Diagram



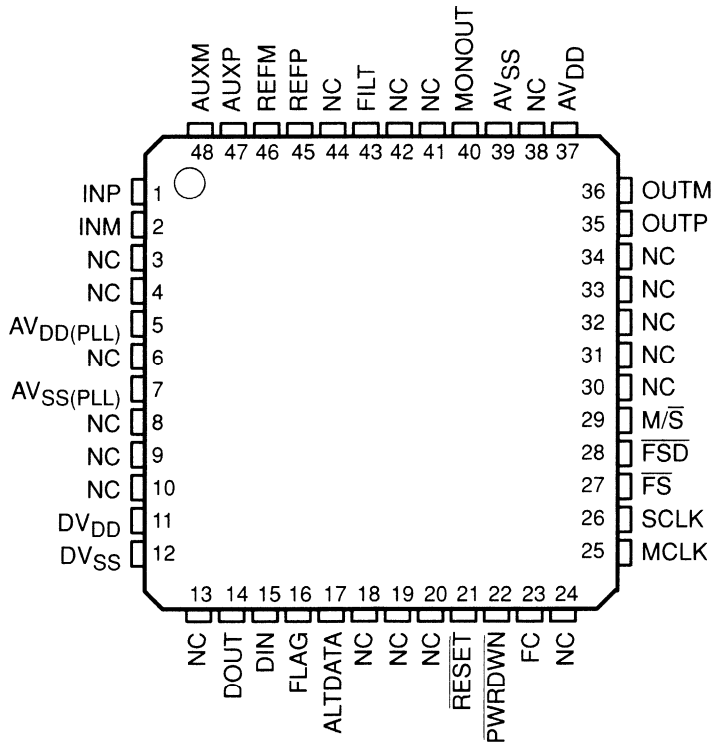
NOTE: Pin numbers shown are for the DW package.

1.3 Terminal Assignments

**DW PACKAGE
(TOP VIEW)**



**PT PACKAGE
(TOP VIEW)**



NC – No internal connection

1.4 Ordering Information

T _A	PACKAGE	
	SMALL OUTLINE PLASTIC DIP (DW)	QUAD FLAT PACK (PT)
0°C to 70°C	TLC320AD50CDW TLC320AD52CDW	TLC320AD50CPT TLC320AD52CPT

1.5 Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PT	DW		
ALTDATA	17	14	I	Alternate data. ALTDATA signals are routed to DOUT during secondary communication if phone mode is enabled using control 2 register.
AUXM	48	4	I	Inverting input to auxiliary analog input. AUXM requires an external single-pole antialias filter with a low output impedance and should be tied to V _{SS} if not used.
AUXP	47	3	I	Noninverting input to auxiliary analog input. AUXP requires an external single-pole antialias filter with a low output impedance and should be tied to V _{SS} if not used.
AV _{DD}	37	25	I	Analog ADC power supply (5 V only)
AV _{DD} (PLL)	5	7	I	Analog power supply for the internal PLL (5 V only)
AV _{SS}	39	26	I	Analog ground
AV _{SS} (PLL)	7	8	I	Analog ground for the internal PLL
DIN	15	12	I	Data input. DIN receives the DAC input data and register data from the external DSP (digital signal processor) and is synchronized to SCLK and \overline{FS} . Data is latched at the falling edge of SCLK when \overline{FS} is low. DIN is at high impedance when \overline{FS} is not active.
DOUT	14	11	O	Data output. DOUT transmits the ADC output bits and register data, and is synchronized to SCLK. Data is sent out at the rising edge of SCLK when \overline{FS} is low. DOUT is at high impedance when \overline{FS} is not activated.
DV _{DD}	11	9	I	Digital power supply (5 V or 3 V)
DV _{SS}	12	10	I	Digital ground
FC	23	17	I	Hardware secondary communication request. When FC is set to high, a secondary communication, followed by the primary communication, will occur to transfer AIC register data between AIC and DSP. FC is sampled and latched on the rising edge of \overline{FS} at the end of the primary serial communication. See section 3 for details.
FILT	43	28	O	Bandgap filter. FILT is provided for decoupling of the bandgap reference, and provides 3.2 V. The optimal capacitor value is 0.1 μ F (ceramic). This voltage node should be loaded only with a high-impedance dc load.
FLAG	16	13	O	Output flag. During phone mode, FLAG contains the value set in control 2 register.
\overline{FS}	27	20	I/O	Frame sync. When \overline{FS} goes low, DIN begins receiving data bits and DOUT begins transmitting data bits. In master mode, \overline{FS} is internally generated and is low during the data transmission into DIN and out from DOUT. In slave mode, \overline{FS} is externally generated.

1.5 Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PT	DW		
FSD	28	21	O	Frame sync delayed output. The $\overline{\text{FSD}}$ (active-low) output synchronizes a slave device to the frame sync of the master device. $\overline{\text{FSD}}$ is applied to the slave $\overline{\text{FS}}$ input and is the same duration as the master $\overline{\text{FS}}$ signal but is delayed in time by the number of shift clocks programmed in the control 3 register.
INM	2	6	I	Inverting input to analog modulator. INM requires an external single-pole antialias filter with a low output impedance.
INP	1	5	I	Noninverting input to analog modulator. INP requires an external single-pole antialias filter with a low output impedance.
M/S	29	22	I	Master/slave select input. When M/S is high, the device is the master, and when it is low, it is a slave.
MCLK	25	18	I	Master clock. MCLK derives the internal clocks of the sigma-delta analog interface circuit.
MONOUT	40	27	O	Monitor output. MONOUT allows for monitoring of the analog input and is a high-impedance output. The gain or mute is selected using control 1 register.
OUTM	36	24	O	Inverting output of the DAC. The OUTM output can be loaded with 600 Ω . OUTM is functionally identical with and complementary to OUTP. OUTM can also be used alone for single-ended operation.
OUTP	35	23	O	Noninverting output of the DAC. The OUTP output can be loaded with 600 Ω . OUTP can also be used alone for single-ended operation.
$\overline{\text{PWRDWN}}$	22	16	I	Power down. When $\overline{\text{PWRDWN}}$ is pulled low, the device goes into a power-down mode, the serial interface is disabled, and most of the high-speed clocks are disabled. However, all the register values are sustained and the device resumes full power operation without reinitialization when $\overline{\text{PWRDWN}}$ is pulled high again. $\overline{\text{PWRDWN}}$ resets the counters only and preserves the programmed register contents (see paragraph 2.2.2 for more information).
REFM	46	2	O	Voltage reference filter input. REFM is provided for low-pass filtering of the internal bandgap reference. The optimal ceramic capacitor value is 0.1 μF and should be connected between REFM and REFP. DC voltage at REFM is 0 V.
REFP	45	1	O	Voltage reference filter positive input. REFP is provided for low-pass filtering of the internal bandgap reference. The optimal ceramic capacitor value is 0.1 μF and should be connected between REFP and REFM. DC voltage at REFP is 3.2 V.
RESET	21	15	I	Reset. RESET initializes all of the internal registers to their default values. The serial port can be configured to the default state accordingly. See section 6 and paragraph 2.2.1 for more information.
SCLK	26	19	I/O	Shift clock. The SCLK signal clocks serial data in through DIN and out through DOUT during the frame-sync interval. When configured as an output (M/S high), SCLK is generated internally by multiplying the frame-sync signal frequency by 256. When configured as an input (M/S low), SCLK is generated externally and must be synchronous with the master clock and frame sync.

NOTE: All digital inputs and outputs are TTL compatible, unless otherwise noted (for $\text{DV}_{\text{DD}} = 5 \text{ V}$).

1.6 Definitions and Terminology

ADC Channel	ADC channel refers to all signal processing circuits between the analog input and the digital conversion results at DOUT.
d	The alpha character d represents valid programmed or default data in the control register format (see Section 3.2) when discussing other data bit portions of the register.
Dxx	Dxx is the bit position in the primary data word (xx is the bit number).
DSxx	DSxx is the bit position in the secondary data word (xx is the bit number).
DAC Channel	DAC channel refers to all signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUTP and OUTM.
Data Transfer Interval	The time during which data is transferred from DOUT and to DIN. The interval is 16 shift clocks and the data transfer is initiated by the falling edge of the frame-sync signal.
FIR	Finite duration impulse response
f_s	The sampling frequency.
Frame Sync and Sampling Period	Frame sync and sampling period is the time between falling edges of successive primary frame-sync signals. It is always equal to 256 SCLK.
Frame Sync	Frame sync refers only to the falling edge of the signal that initiates the data transfer interval. The primary frame sync starts the primary communications, and the secondary frame sync starts the secondary communications.
Frame-Sync Interval	Frame-sync interval is the the time period occupied by 16 shift clocks. The frame-sync signal goes high on the seventeenth rising edge of SCLK.
Host	A host is any processing system that interfaces to DIN, DOUT, SCLK, \overline{FS} , and/or MCLK.
PGA	Programmable gain amplifier
Primary Communications	Primary communications refers to the digital data transfer interval. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.
Secondary Communications	Secondary communications refers to the digital control and configuration data transfer interval into DIN and the register read data cycle from DOUT. The data transfer interval occurs when requested by hardware or software.
Signal Data	This refers to the input signal and all of the converted representations through the ADC channel and the signal through the DAC channel to the analog output. This is contrasted with the purely digital software control data.
X	The alpha character X represents a <i>don't care</i> bit-position within the control register format.

1.7 Register Functional Summary

There are seven control registers that are used as follows:

- Register 0 The No-Op register. Addressing register 0 allows secondary communications requests without altering any other register.
- Register 1 The Control 1 register. The data in this register controls:
- Software reset
 - Software power down
 - Normal or auxiliary analog inputs enabling
 - Normal or auxiliary analog inputs monitoring
 - Selection of monitor amplifier output gain
 - Selection of digital loopback
 - Selection of 16-bit or (15+1)-bit mode of DAC operation
- Register 2 The Control 2 register. The data in this register:
- Contains the output value of FLAG
 - Selects phone mode
 - Contains the output flag indicating a decimator FIR filter overflow
 - Selects either 16-bit mode or (15+1)-bit mode of ADC operation
 - Enables analog loopback
- Register 3 The Control 3 register. The data in this register:
- Sets the number of SCLK delays between \overline{FS} and \overline{FSD}
 - Informs the master device of how many slaves are connected in the chain
- Register 4 The Control 4 register. The data in this register:
- Selects the amplifier gain for the input and output amplifiers
 - Sets the sample rate by choosing the value of N from 1 to 8
where $f_s = MCLK/(128 \times N)$ or $MCLK/(512 \times N)$
 - Selects the PLL. If the PLL is selected, the sampling rate is set to $MCLK/(128 \times N)$. If the PLL is bypassed, the sampling rate can be set to $MCLK/(512 \times N)$.
- Register 5 Reserved for factory test. Do not write to this register.
- Register 6 Reserved for factory test. Do not write to this register.

2 Detailed Description

2.1 Device Functions

2.1.1 Operating Frequencies

If the sampling frequency is higher than 7 kHz, the sampling frequency is derived from the master clock (MCLK) input by either equation 1 or 2.

$$f_s = \text{Sampling (conversion) frequency} = \frac{\text{MCLK}}{128 \times N} \quad (\text{when bit D7 of register 4 is set to 0}) \quad (1)$$

$$f_s = \text{Sampling (conversion) frequency} = \frac{\text{MCLK}}{512 \times N} \quad (\text{when bit D7 of register 4 is set to 1}) \quad (2)$$

If the sampling frequency is lower than 7 kHz, the sampling frequency is derived from the master clock (MCLK) using equation 2 only, which bypasses the PLL. Equation 2 *must* be used in this case because the PLL input clock for sampling frequencies lower than 7 kHz is outside of the working range for the PLL input clock.

The inverse of the sampling frequency is the time between the falling edges of two successive primary frame-sync signals. This time is the conversion period.

For example, to set the conversion rate to 8 kHz,

- when bit D7 of register 4 is set to 0, use equation 1 to determine MCLK (MCLK = 128 × N × 8000)
- when bit D7 of register 4 is set to 1, use equation 2 to determine MCLK (MCLK = 512 × N × 8000)

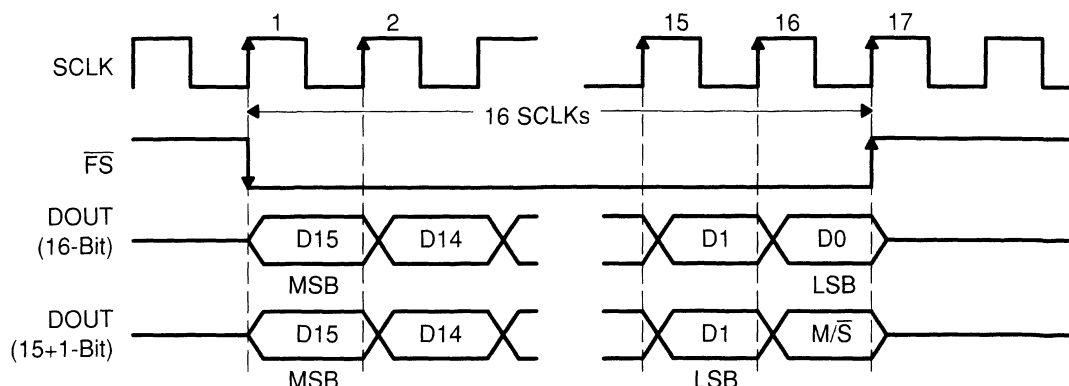
To set the conversion rate to 4 kHz,

- bit D7 of register 4 *must* be set to 1 to bypass the PLL. then use equation 2 to determine MCLK (MCLK = 512 × N × 4000)

2.1.2 ADC Signal Channel

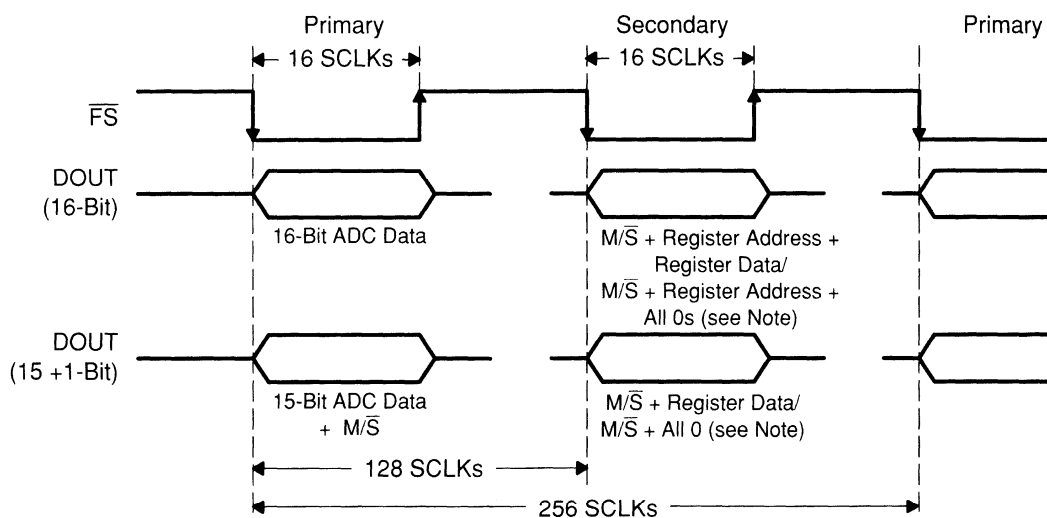
The input signal is amplified and applied to the ADC input. The ADC converts the signal into discrete output digital words in 2's-complement data format, corresponding to the instantaneous analog-signal value at the sampling time. These 16-bit (or 15-bit) digital words, representing sampled values of the analog input signal after the PGA, are clocked out of the serial port (DOUT) at the positive edge of SCLK during the frame-sync interval, one bit for each SCLK and one word for each primary communication interval (256 SCLKs).

During secondary communication, the data previously programmed into the registers can be read out. This read operation is accomplished by sending the appropriate register address (DS12 – DS8) with the read bit (DS13) set to 1 in through DIN during present secondary communication. If a register read is not requested, all 16 bits are cleared to 0 in the secondary communication. The timing sequence is shown in figure 2–1 and figure 2–2.



- NOTES: A. M/\bar{S} is used to indicate whether the 15-bit data comes from master device or slave device. (Master: $M/\bar{S} = 1$, Slave $M/\bar{S} = 0$)
 B. The MSB (D15) is stable (the host can latch the data in at this time) at the falling edging of SCLK #1, the last bit (D0, M/\bar{S}) is stable at the falling edging of SCLK #16.

Figure 2-1. Timing Sequence of ADC Channel (Primary Communication Only)

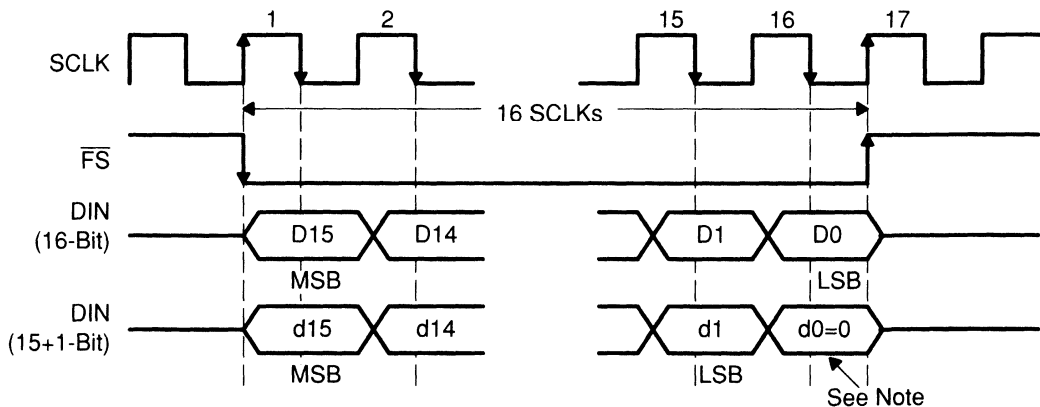


- NOTE: M/\bar{S} bit (DS15) in the secondary communication is used to indicate whether the register data (address and content) comes from the master device or the slave device if the read bit is set. During register read operations, bits DS7 – DS0 are the contents of the specified register. In register write operations, bits DS7 – DS0 are all 0s.

Figure 2-2. Timing Sequence of ADC Channel (Primary and Secondary Communication)

2.1.3 DAC Signal Channel

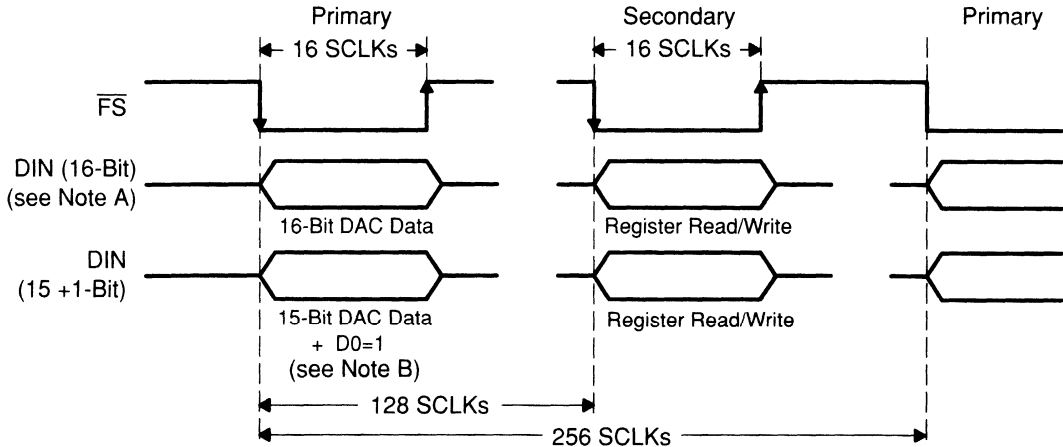
DIN receives the 16-bit serial data word (2's complement) from the host during the primary communications interval. These 16-bit digital words, representing the analog output signal before PGA, are clocked into the serial port (DIN) at the falling edge of SCLK during the frame-sync interval, one bit for each SCLK and one word for each primary communication interval (256 SCLKs). The data are converted to a pulse train by the sigma-delta DAC, which consists of a digital interpolation filter and a digital modulator. The output of the modulator is then passed to an internal low-pass filter to complete the analog signal reconstruction. Finally, the resulting analog signal is applied to the input of a programmable-gain amplifier, which is capable of driving a 600-Ω load differentially at OUTP and OUTM. The timing sequence is shown in figure 2-3.



NOTE: d0 = 0 means no secondary communication request (software secondary communication request control — paragraph 3.2)

Figure 2–3. Timing Sequence of DAC Channel (Primary Communication Only)

During secondary communication, the digital control and configuration data (together with the register address), are clocked in through DIN. These 16-bits of data are used either to initialize the register, or to read the register content through DOUT. If a register initialization is not required, a no-operation word (DS15 – DS8 are all set to 0) can be used. If DS13 is set to 1, the content of the control register, specified by DS12–DS8, will be sent out through DOUT during the same secondary communication (see section 2.1.5). The timing sequence is shown in figure 2–4.



NOTES: A. FS has to be set high for a secondary communication request when 16-bit DAC data format is used (paragraph 3.2).
 B. D0 = 1 means secondary communication request (software secondary communication request control — paragraph 3.2).

Figure 2–4. Timing Sequence of DAC Channel (Primary and Secondary Communication)

2.1.4 Serial Interface

The digital serial interface consists of the shift clock (SCLK), the frame-sync signal (\overline{FS}), the ADC-channel data output (DOUT), and the DAC-channel data input (DIN). During the primary frame synchronization interval, SCLK clocks the ADC channel results out through DOUT and clocks 16-bit/(15+1)-bit DAC data in through DIN.

During the secondary frame-sync interval, SCLK clocks the register read data out through DOUT if the read bit (DS13) is set to 1 and transfers control and device parameter in through DIN. The timing sequence is shown in Figures 2-2 and 2-4.

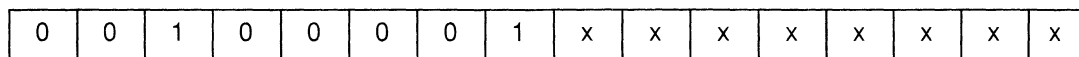
2.1.5 Register Programming

All register programming occurs during secondary communications through DIN, and data are latched and valid on the falling edge of SCLK during the frame-sync signal. If the default value for a particular register is desired, that register does not need to be addressed during the secondary communications interval. The no-op command (DS15 – DS8 all set to 0) addresses the pseudo-register (register 0), and no register programming takes place during the communications.

In addition, each register can be read back through DOUT during secondary communications by setting the read bit (DS13) to 1. When the register is in the read mode, no data can be written to the register during this cycle. DS13 must be cleared to write to the register.

For example, if the contents of control register 1 is desired to be read out from DOUT, the following procedure must be performed through DIN:

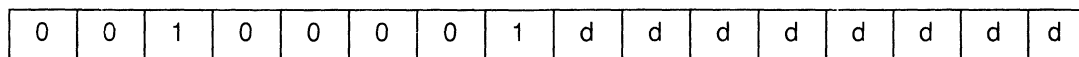
1. Request secondary communication by setting either D0 = 1 (software request) or FC = high (hardware request) during the primary communication interval.
2. At the secondary communication interval (\overline{FS}), send data in the following format in through DIN:



DS15

DS0

3. Then the following data is read from DOUT, with the last 8 bits containing the register 1 data.



DS15

DS0

Figure 2-5 is a timing diagram of this procedure.

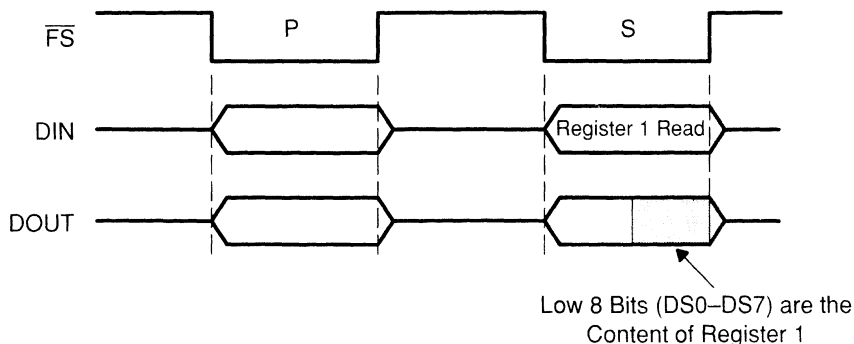
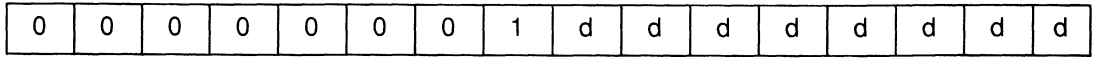


Figure 2-5. Register 1 Read Operation Timing Diagram

If control register 1 needs to be programmed, the following procedure must be performed through DIN:

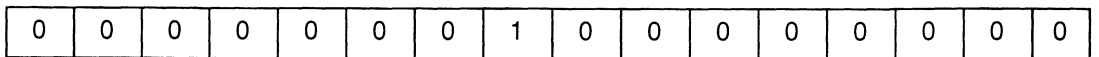
1. Request secondary communication by setting either D0 = 1 (software request) or FC = high (hardware request) during the primary communication interval.
2. At the secondary communication interval (\overline{FS}), send data in the following format in through DIN:



DS15

DS0

3. Then the following data is read from DOUT:



DS15

DS0

Figure 2-6 is a timing diagram of this procedure.

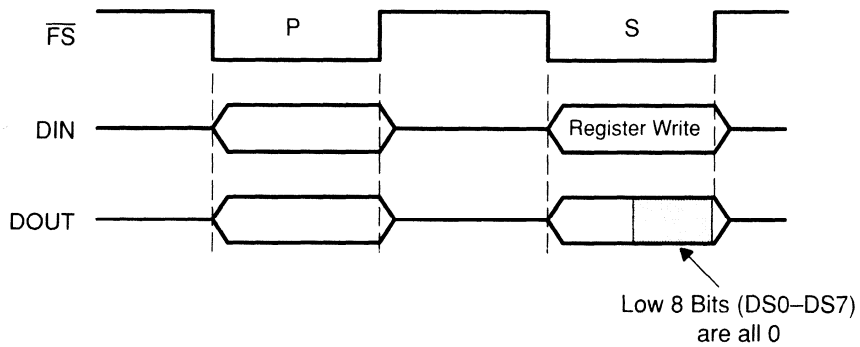


Figure 2-6. Register 1 Write Operation Timing Diagram

2.1.6 Sigma-Delta ADC

The sigma-delta analog-to-digital converter in the device is a sigma-delta modulator with 64- \times oversampling. The ADC provides high-resolution, low-noise performance using oversampling techniques. Due to the oversampling employed, only single-pole antialiasing filters are required on the analog inputs.

2.1.7 Decimation Filter

The decimation filters reduce the digital data rate to the sampling rate. This is accomplished by decimating with a ratio of 1:64. The output of the decimation filter is a 16-bit 2's-complement data word clocking at the sample rate selected for that particular data channel. The bandwidth of the filter is $0.439 \times f_{\text{sample}}$ and scales linearly with the sample rate.

2.1.8 Sigma-Delta DAC

The sigma-delta digital-to-analog converter in the device is a sigma-delta modulator with 256- \times oversampling. The DAC provides high-resolution, low-noise performance using oversampling techniques.

2.1.9 Interpolation Filter

The interpolation filter resamples the digital data at a rate of 256 times the incoming sample rate. The high-speed data output from the interpolation filter is then used in the sigma-delta DAC. The bandwidth of the filter is $0.439 \times f_{\text{sample}}$ and scales linearly with the sample rate.

2.1.10 Analog and Digital Loopback

The analog and digital loopbacks provide a means of testing the modem data ADC/DAC channels and can be used for in-circuit system-level tests. The analog loopback routes the DAC low-pass filter output into the analog input where it is then converted by the ADC into a digital word. The digital loopback routes the ADC output to the DAC input on the device and is enabled by setting bit D1 in control 1 register to 1. Analog loopback is enabled by setting bit D3 in control 2 register to 1 (see section 6).

2.1.11 FIR Overflow Flag

The decimator FIR filter sets an overflow flag (bit D5) of control 2 register to indicate that the input analog signal has exceeded the range of the internal decimation filter calculations. Once the FIR overflow flag has been set in the register, it remains set until the register is read by the user. Reading this value resets the overflow flag.

If FIR overflow occurs, the input signal must be attenuated either by the PGA or some other method.

2.2 Reset and Power-Down Functions

2.2.1 Software and Hardware Reset

The TLC320AD50C and TLC320AD52C reset the internal counters and registers in response to either of two events:

1. A low-going reset pulse is applied to terminal $\overline{\text{RESET}}$
2. A 1 is written to the programmable software reset bit (D7 of control register 1)

Either event resets the control registers and clears all the sequential circuits in the device. Reset signals should be at least 6 master clock periods long.

2.2.2 Software and Hardware Power Down

Most of the device (all except the digital interface) enters the power-down mode when D6 in control register 1 is set to 1. When $\overline{\text{PWRDWN}}$ is taken low, the entire device is powered down. In either case, the register contents are preserved and the output of the monitor amplifier is held at the midpoint voltage to minimize pops and clicks.

The amount of power drawn during software power down is higher than it is during a hardware power down because of the current required to keep the digital interface active. Additional differences between software and hardware power-down modes are detailed in the following paragraphs. Figure 2–7 represents the internal power-down logic.

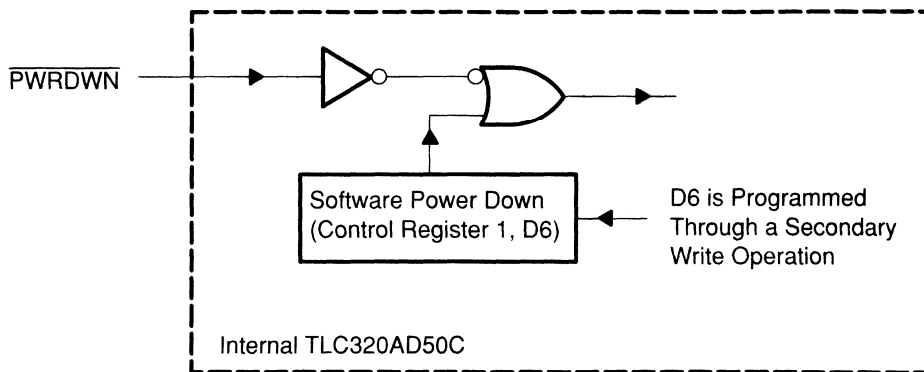


Figure 2–7. Internal Power-Down Logic

2.2.2.1 Software Power Down

When D6 of control register 1 is set to 1, the device enters the software power-down mode. In this state, the digital interface circuit is still active while the internal ADC and DAC channels and differential outputs OUP_T and OUP_M are disabled, and DOUT and $\overline{\text{FSD}}$ are inactive. Register data in the secondary serial communications is still accepted but data in the primary serial communications is ignored. The device returns to normal operation when D6 of control register 1 is reset to 0.

2.2.2.2 Hardware Power Down

When $\overline{\text{PWRDWN}}$ is held low, the device enters the hardware power-down mode. In this state, the internal clock control circuit and the differential outputs OUP_T and OUP_M are disabled. All other digital I/Os either are disabled or remain in the state they were in immediately before power down. DIN cannot accept any data input. The device can only be returned to normal operation by taking and holding $\overline{\text{PWRDWN}}$ high. When not holding the device in the hardware power-down mode, $\overline{\text{PWRDWN}}$ should be tied high.

2.3 Master Clock Circuit

MCLK is the external master clock input. The internal clock circuit generates and distributes necessary clocks throughout the device. An internal PLL circuit is used for upsampling to provide the appropriate clocks for the digital filters and modulators.

When the device is in the master mode, SCLK and \overline{FS} are derived from MCLK in order to provide clocking of the serial communications between the device and a DSP (digital signal processor). When in the slave mode, SCLK and \overline{FS} are both inputs.

2.4 Data Out (DOUT)

DOUT is placed in the high-impedance state on the rising edge of the frame sync. In the primary communication, the data word is the ADC conversion result. In the secondary communication, the data is the register-read results when requested by the read/write (R/W) bit. If a register read is not requested, the low eight bits of the secondary word is all zeroes. The state of the master/slave (M/S) terminal is reflected by the MSB in secondary communication (DOUT, bit DS15) and the LSB in the primary communication (DOUT, bit D0). When the device is in the slave mode, DOUT remains in a high-impedance state until a nonzero value is written as a number of slaves in control register 3 (bits D7 and D6).

2.4.1 Data Out, Master Mode

In the master mode, DOUT is taken from the high-impedance state by the falling edge of the master frame sync (\overline{FS}). The most significant data bit then appears first on DOUT.

2.4.2 Data Out, Slave Mode

In the slave mode, DOUT is taken from the high-impedance state by the falling edge of the frame sync (\overline{FS}). The most significant data bit then appears on DOUT. When in the slave mode, DOUT is not enabled until the control 3 register is programmed with the number of slaves. This must be done even if there is only one slave device.

2.5 Data In (DIN)

In a primary communication, the data word is the input digital signal to the DAC channel. If the (15+1)-bit data format is used, the LSB (D0) is used to request a secondary communication. In a secondary communication, the data is the control and configuration data that sets the device for a particular function (see Section 3, Secondary Serial Communication for details).

2.6 FC (Hardware Secondary Communication Request)

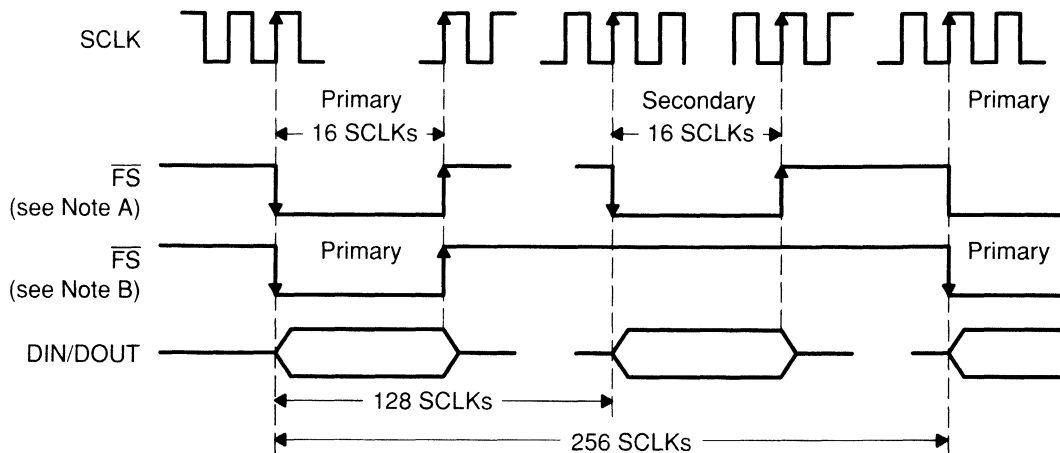
The FC input provides for hardware requests for secondary communications. FC works in conjunction with the LSB of the primary data word. The signal on FC is latched on the rising edge of the primary frame sync (\overline{FS}). FC should be tied low if not used.

2.7 Frame-Sync Function for TLC320AD50C

The frame-sync signal (\overline{FS}) indicates the device is ready to send and receive data. The data transfer out of DOUT and into DIN begins on the falling edge of the frame-sync signal.

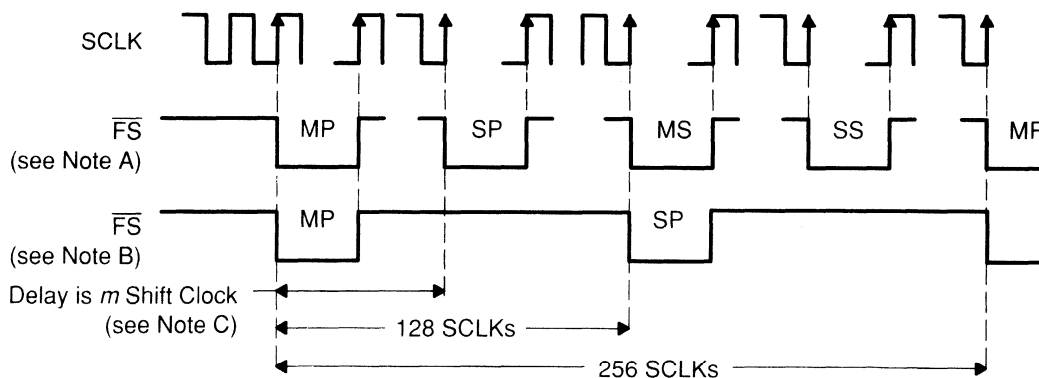
2.7.1 Frame Sync (\overline{FS}) Function, Master Mode

The frame sync is generated internally and goes low on the rising edge of SCLK and remains low during a 16-bit data transfer. In addition to generating its own frame-sync signal, the master also outputs a frame sync for each slave that is being used (see figures 2–8 and 2–9).



NOTES: A. Primary and secondary serial communication.
B. Primary serial communication, only.

Figure 2–8. Master Device Frame-Sync Signal With Primary and Secondary Communications (No Slaves)



NOTE: MP: Master Primary (master device data is transferred in this period, DOUT of the slave device device is in high impedance state).
SP: Slave Primary (slave device data is transferred in this period, DOUT of master device device is in high impedance state).
MS: Master Secondary (master device control register information is transferred in this period, DOUT of the slave device is in high impedance state).
SS: Slave Secondary (slave device control register information is transferred in this period, DOUT of the master device is in high impedance state).

NOTES: A. Primary and secondary serial communications
B. Primary serial communication only
C. m is the value programmed into the FSD register (control register 3: D0–D5)

Figure 2–9. Master Device Frame-Sync Signal With Primary and Secondary Communications (With 1 Slave Device)

2.7.2 Frame Sync (\overline{FS}) Function, Slave Mode

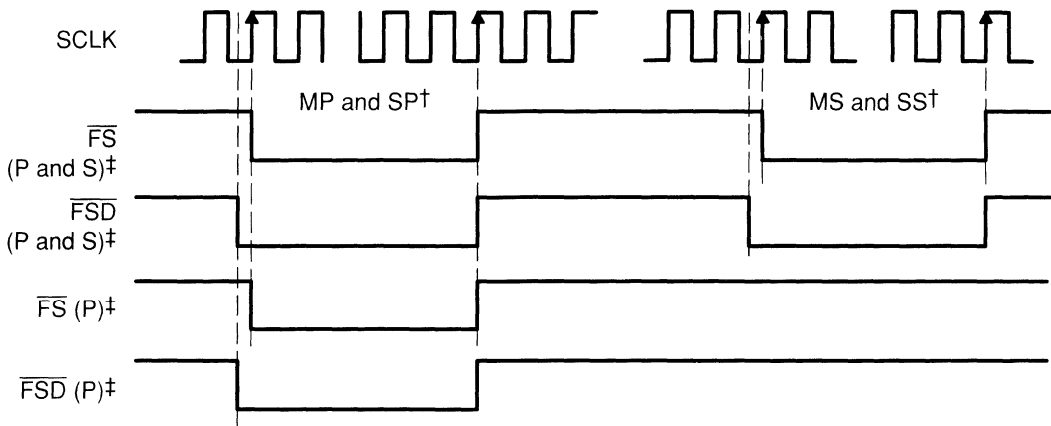
Frame-sync timing is generated externally by the master \overline{FSD} and is applied to \overline{FS} of the slave to control the ADC and DAC timing.

2.7.3 Frame-Sync Delayed (\overline{FSD}) Function, Master Mode

For the master, the \overline{FSD} (frame-sync delayed) output occurs 1/4 shift-clock period ahead of \overline{FS} to compensate for the time delay through the master and slave devices. The timing relationships are as follows:

- When the \overline{FSD} register (control 3 register) data is 0, then \overline{FSD} goes low 1/4 SCLK prior to the rising edge of SCLK when \overline{FS} goes low (figure 2–10).
- When the \overline{FSD} register data is greater than 17, then \overline{FSD} goes low on the rising edge of SCLK that is the \overline{FSD} register number of SCLKs after the falling edge of \overline{FS} (figure 2–11).

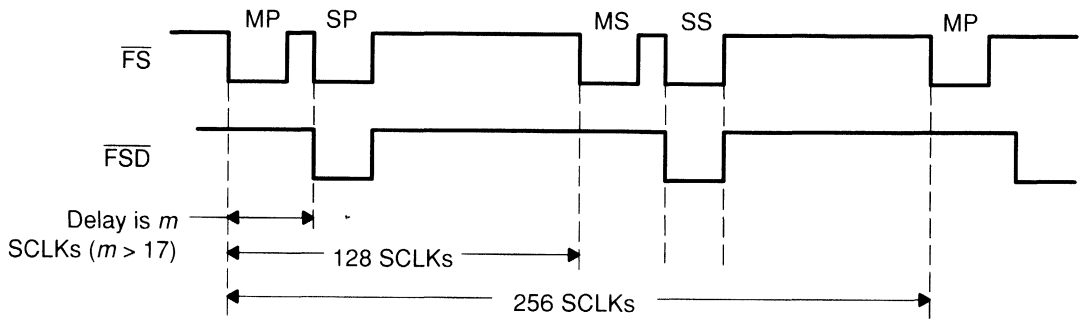
Register data values from 1 to 17 result in a default register value of zero and should not be used.



† The DIN of master and slave devices share the same DIN bus during first initialization. The DOUT is occupied by Master device only until the control register 3 of master and slave device is programmed with slave devices number and number of SCLKs between FS and FSD ($m > 17$).

‡ P&S: Primary and secondary communications P: Primary communication only

Figure 2–10. Master Device \overline{FS} and \overline{FSD} Output When \overline{FSD} Register (D0–D5, Control Register 3) is 0



- NOTES: A. Since Master and slave share the same DIN bus during first initialization, they share the same input data word. Only one write cycle is needed to program control register 3 of master device and slave device(s).
 B. After the control register 3 is programmed, the DIN or DOUT bus of master and slave(s) are separated by time, although they still physically connect to each other.

Figure 2-11. Master Device \overline{FS} and \overline{FSD} Output After Control Register 3 Is Programmed (One Slave Device)

2.7.4 Frame-Sync Delayed ($\overline{\text{FSD}}$), Slave Mode

The master $\overline{\text{FSD}}$ is output to the first slave and the first slave $\overline{\text{FSD}}$ is output to the second slave device and so on (see figure 2–12). The $\overline{\text{FSD}}$ output of each device is input to the $\overline{\text{FS}}$ terminal of the succeeding device. The $\overline{\text{FSD}}$ timing sequence in the slave mode is as follows:

- When the FSD register data is 0, then $\overline{\text{FSD}}$ goes low 1/4 SCLK cycle before $\overline{\text{FS}}$ goes low.
- When the FSD register data is greater than 17, then $\overline{\text{FSD}}$ goes low on the rising edge of SCLK that is the FSD register number of SCLKs after the falling edge of $\overline{\text{FS}}$ (see figure 2–13).

Data values from 1 to 17 should not be used.

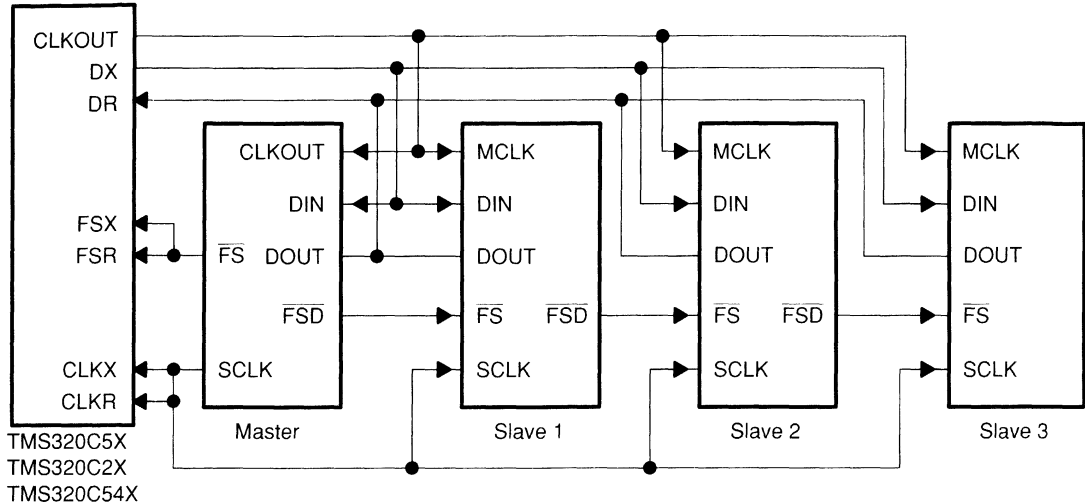
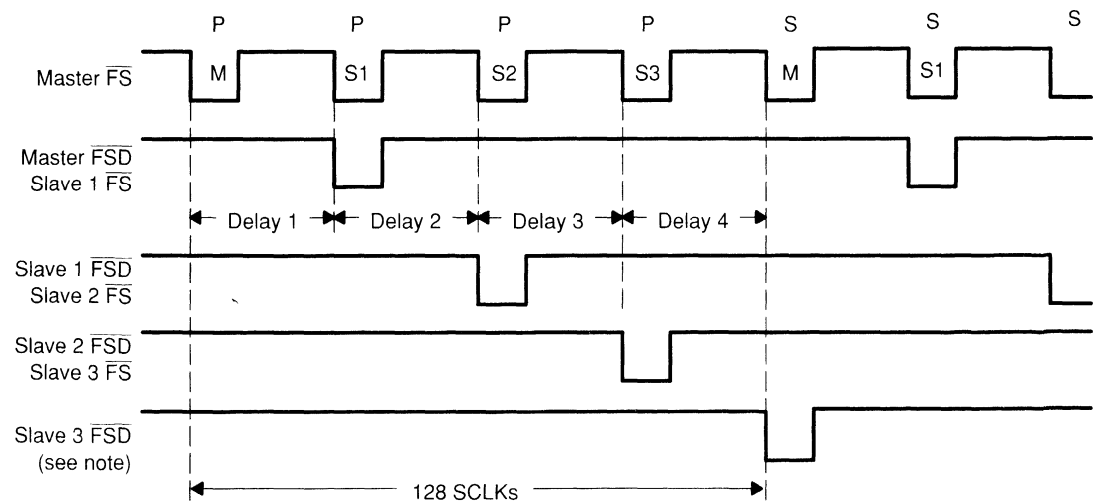


Figure 2–12. Master With Slaves (To DSP Interface)



NOTE: Slave 3 $\overline{\text{FSD}}$ cannot be used.

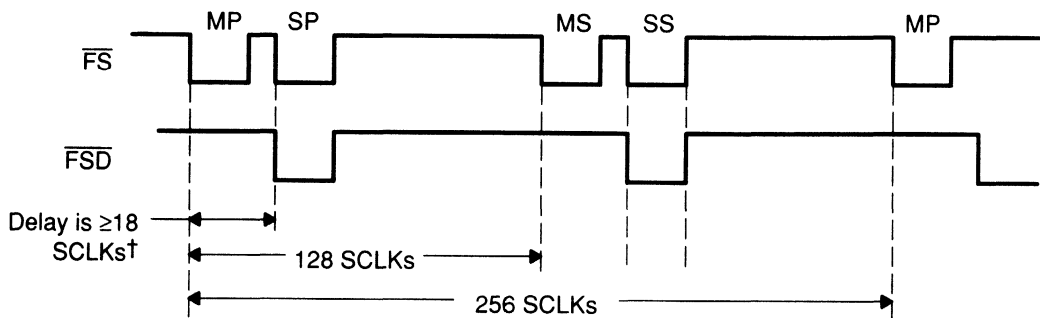
Figure 2–13. Master-Slave Frame-Sync Timing After A Delay Has Been Programmed Into The FSD Register (D0–D5 of Control Register 3)

2.8 Frame-Sync Function for TLC320AD52C

The frame-sync function for TLC320AD52C is very similar to that of the TLC320AD50C except the following:

1. TLC320AD52C can support only one slave.
2. The $\overline{\text{FSD}}$ terminal function can be disabled for TLC320AD52C by programming bit D2 in control 2 register.
3. The $\overline{\text{FSD}}$ value need to be multiplied by 2 for actually number of SCLK delay.

For example, if $\overline{\text{FSD}}$ register (control register 3) is programmed with 49H, it means that the TLC320AD52C has one slave and the $\overline{\text{FSD}}$ terminal has 18 SCLKs delay after master primary $\overline{\text{FS}}$ output. See figure 2–14.

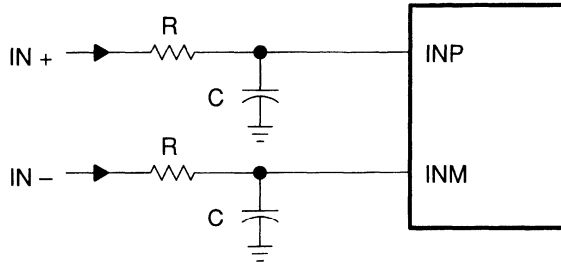


† Minimum SCLK delay number in $\overline{\text{FSD}}$ register is 9. This means that a delay of at least 18 SCLKs is required for proper operation of the TLC320AD52C.

Figure 2–14. Master Device $\overline{\text{FS}}$ and $\overline{\text{FSD}}$ Output After Control Register 3 Is Programmed with 49H

2.9 Multiplexed Analog Input and Output

The two differential analog inputs (INP and INM or AUXP and AUXM) are multiplexed into the sigma-delta modulator. The performance of the AUX channel is similar to the normal input channel. A single-pole antialias filter must be connected to INP and INM (also AUXP and AUXM, if used). If an RC is used for the single-pole filter (Figure 2–15) the value of R should not be greater than 1 kΩ. The gain of the input amplifiers is set by through the control 4 register.



- NOTES: A. The bandwidth of this RC antialias is determined by: $(f_0 = 1/(2\pi RC))$
 B. AUXP and AUXM need to connect to AVSS if not used.
 C. Bandwidth of the anti-alias filter can be $4 \times f_s$.

Figure 2–15. RC Antialias Filter

2.9.1 Multiplexed Analog Input

To produce the best possible common-mode rejection of unwanted signal performance, the analog signal is processed differentially until it is converted to digital data. The signal applied to the terminals INM and INP should be differential to preserve the device specifications. As much as 6 dB of signal level will be lost if the single-ended input is used directly. The signal source driving the analog inputs (INP and INM or AUXP and AUXM) should have a low source impedance for best low-noise performance and accuracy.

To obtain maximum dynamic range, the signal should be AC coupled to the input terminal. The analog input signal is self-biased to the mid-supply voltage if the monitor-amplifier input source is selected as the same source for the ADC input. These input sources are selected by bits D4 and D5 of control 1 register. The default condition self-biases the input since the register default value selects INP and INM as the source for both the ADC and monitor amplifier input (see figure 2–16). A simple single-pole antialias filter with low output impedance must be connected to INP and INM (also AUXP and AUXM, if used).

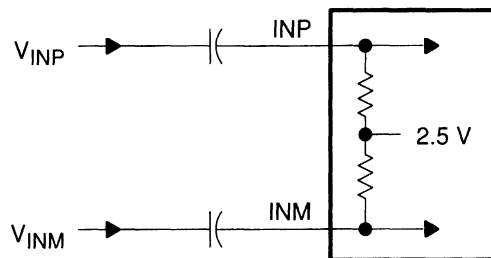


Figure 2–16. INP and INM Internal Self-Biased (2.5 V) Circuit

2.9.2 Analog Output

The OUTP and OUTM are differential outputs and can drive a typical 600- Ω load directly. Figure 2-17 shows the circuit when load is ground referenced.

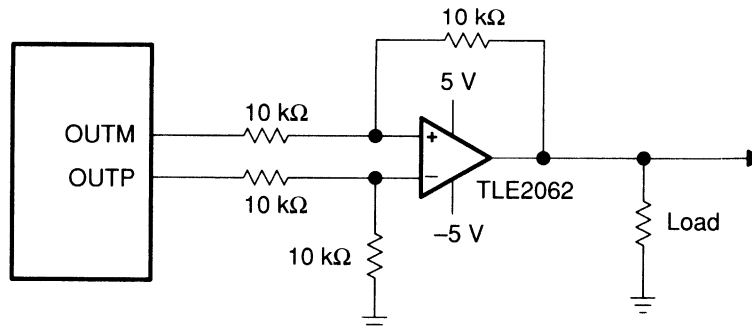


Figure 2-17. Differential Output Drive (Ground Referenced)

3 Serial Communications

DOUT, DIN, SCLK, \overline{FS} , and FC are the serial communication signals. The digital output data from the ADC is taken from DOUT. The digital input data for the DAC is applied to DIN. The synchronizing clock for the serial communication data and the frame sync is taken from SCLK. The frame-sync pulse that encloses the ADC and DAC data transfer interval is taken from \overline{FS} . For signal data transmitted from the ADC or to the DAC, primary serial communication is used. To read or write words that control both the options and the circuit configurations of the device, secondary communication is used.

The purpose of the primary and secondary communications is to allow conversion data and control data to be transferred across the same serial port. A primary transfer is always dedicated to conversion data. A secondary transfer is used to set up and/or read the register values. A primary transfer occurs for every conversion period. A secondary transfer occurs only when requested. Secondary serial communication can be requested either by hardware (FC terminal) or by software (D0 of primary data input to DIN).

3.1 Primary Serial Communication

Primary serial communication is used both to transmit and receive conversion signal data. The DAC word length depends on the state of bit D0 in control 1 register. After power up or reset, the device defaults to the 15-bit mode. When the DAC word length is 15 bits, the last bit of the primary 16-bit serial communication word is a control bit used to request secondary serial communication. In the 16-bit mode, all 16 bits of the primary communication word are used as data for the DAC and the hardware terminal FC must be used to request secondary communication.

Figure 3–1 shows the timing relationship for SCLK, \overline{FS} , DOUT and DIN in a primary communication. The timing sequence for this operation is as follows:

1. \overline{FS} is brought low by the TLC320AD50C or TLC320AD52C.
2. A 16-bit word is transmitted from the ADC (DOUT) and a 16-bit word is received from the DAC (DIN).
3. \overline{FS} is brought high by the TLC320AD50C or TLC320AD52C, signaling the end of the data transfer.

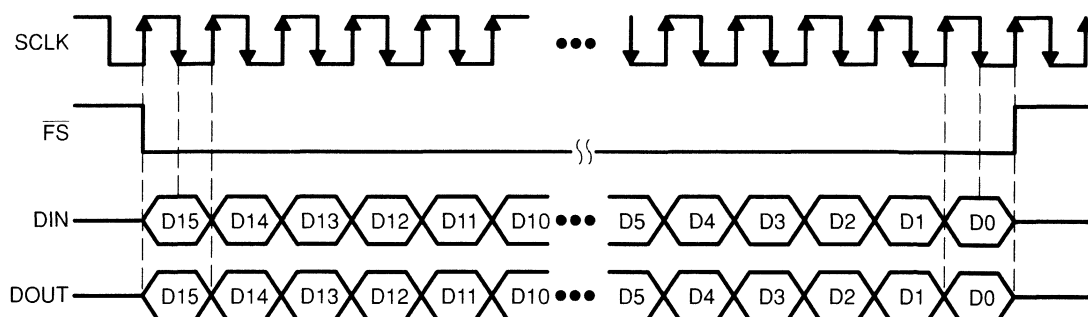


Figure 3–1. Primary Serial Communication Timing

3.2 Secondary Serial Communication

Secondary serial communication is used to read or write 16-bit words that program both the options and the circuit configurations of the device. Register programming always occurs during secondary communication. Four primary and secondary communication cycles are required to program the four registers. If the default value for particular register is desired, then the register addressing can be omitted during secondary communications. The NOOP command addresses a pseudo-register, register 0, and no register programming takes place during this secondary communication. If secondary communication is desired for any device (either master or slave), then a secondary communication must be requested for all devices, starting with the master. This results in a secondary frame sync (\overline{FS}) for all devices. The NOOP command can be used for devices that do not need a secondary operation.

During a secondary communication, a register may be written to or read from. When writing a value to a register, DIN contains the value to be written. When reading the value in a register, the data is stepped out on DOUT.

There are two methods for initiating secondary communications:

1. by asserting a high level on FC
2. by asserting the LSB of the DIN 16-bit serial communication high while in the 15-bit mode

Both methods are illustrated in figure 3–2.

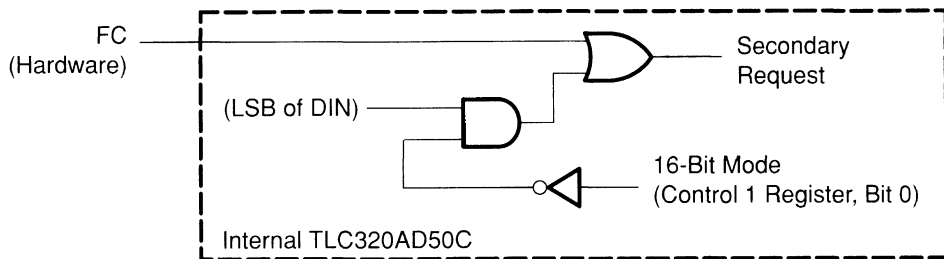


Figure 3–2. Hardware and Software Methods to Make a Secondary Request

FC should be pulled high before the rising edge of the frame sync (\overline{FS}). This causes the start of the secondary communication, 128 SCLKs after the start of the primary communication frame. If slaves are present, FC should remain high until the rising edge of the frame sync for the last slave.

The second method for secondary communication is by asserting the LSB high. A software request is typically used when the request resolution of the DAC channel is less than 16 bits. Then the least significant bit (D0) can be used for the secondary requests as shown in table 3–1. The request is made by placing the device in the 15-bit DAC mode and making the LSB of DIN high. All devices should be in the 15-bit DAC mode and secondary communication should be requested for all devices.

Table 3–1. Least Significant Bit Control Function

CONTROL BIT D0	CONTROL BIT FUNCTION
0	No operation (NOOP)
1	Secondary communication request

If a secondary communication request is made, \overline{FS} goes low after 128 SCLKs after the beginning of the primary frame.

3.2.1 Hardware Secondary Serial Communication Request

The FC requests a secondary communication when it is asserted. The FC terminal is latched at the rising edge of \overline{FS} (primary communication), so FC should be pulled high before the rising edge of the primary frame sync (\overline{FS}). FC needs to have a bounce from high to low and then back to high (1→0→1) if another secondary serial communication is desired. Otherwise (FC kept high or low), there is no additional secondary communication. Figures 3–3 and 3–4 show the \overline{FS} output from a master device.

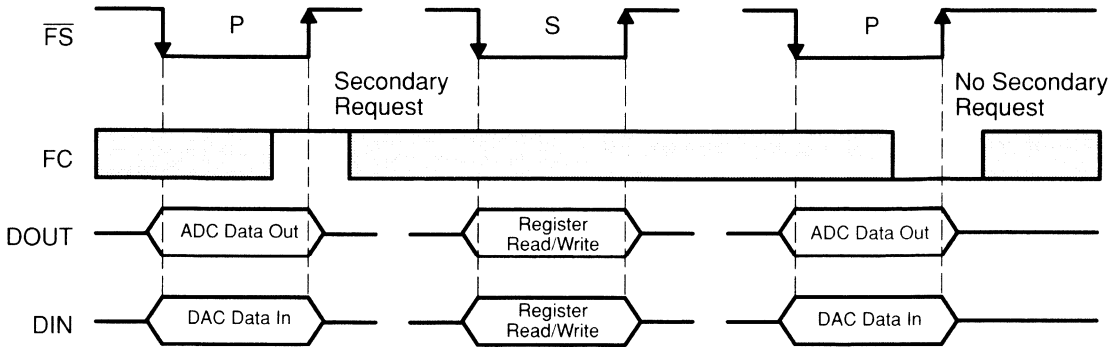
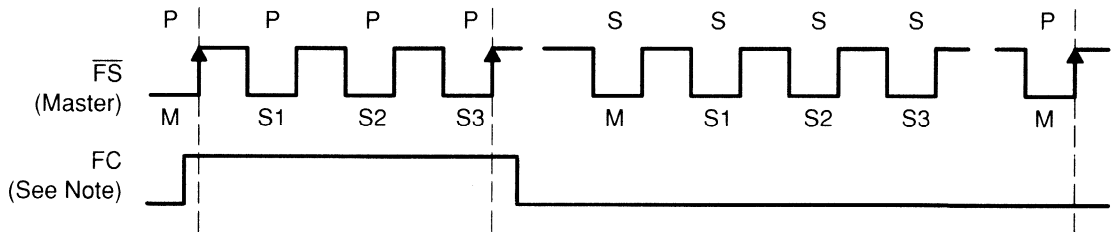


Figure 3–3. \overline{FS} Output When Hardware Secondary Serial Communication Is Requested Only Once (No Slave)



NOTE: FC of master device and slave devices should connect together

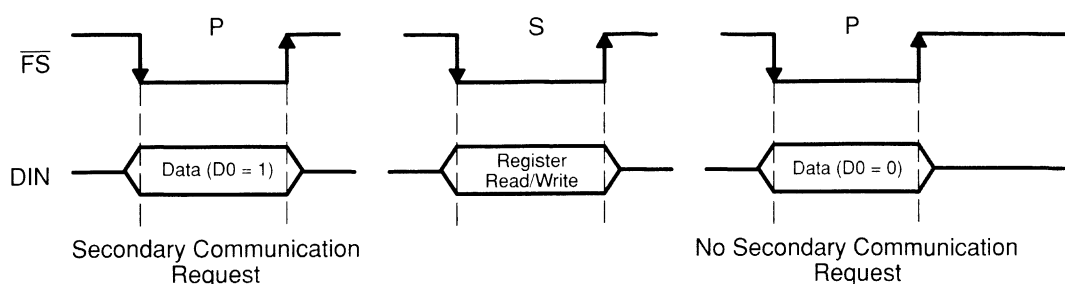
Figure 3–4. \overline{FS} Output When Hardware Secondary Serial Communication Is Requested Only Once (Three Slaves)

3.2.2 Software Secondary Serial Communication Request

The LSB of the DAC data within a primary transfer can request a secondary communication when the device is in the 15-bit mode.

For all serial communications, the most significant bit is transferred first. For a 16-bit ADC word and a 16-bit DAC word, D15 is the most significant bit and D0 is the least significant bit. For a 15-bit DAC data word in a primary communication, D15 is the most significant bit and D1 is the least significant bit. Bit D0 is then used for the secondary communication request control. All digital data values are in 2's complement data format (figure 3–5).

If the data format is set to the 16-bit word mode, all 16 bits are either ADC or DAC data and secondary communication can then be requested only by hardware (FC terminal).



NOTE: See figure 3-8 for secondary communication DIN data format

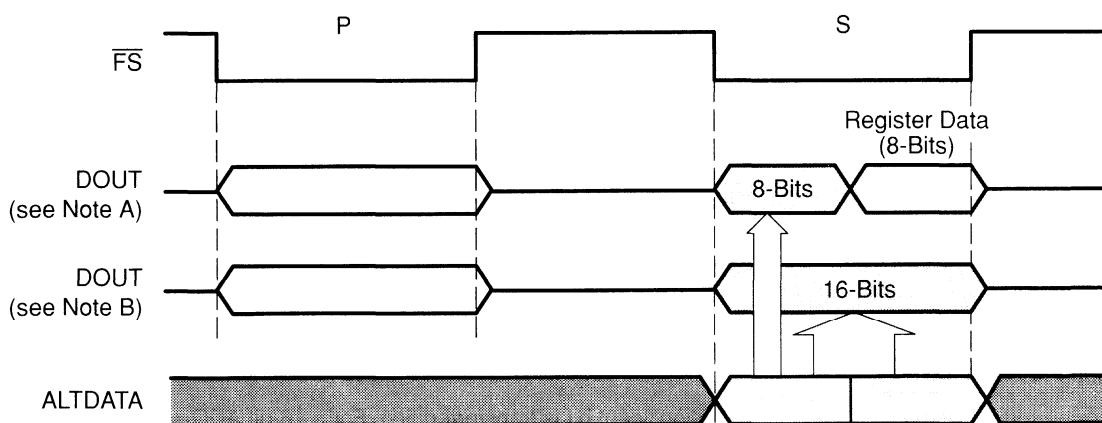
Figure 3-5. \overline{FS} Output During Software Secondary Serial Communication Request (No Slave)

3.3 Conversion Rate Versus Serial Port

The SCLK frequency is set equal to the frequency of the frame-sync signal (\overline{FS}) multiplied by 256. The conversion rate or sample rate is equal to the frequency of \overline{FS} .

3.4 Phone Mode Control

Phone mode control is provided for applications that need hardware control and monitoring of external events. By allowing the device to drive the FLAG terminal (set through control 2 register), the host DSP is capable of system control through the same serial port that connects the device. Along with this control is the capability of monitoring the value of the ALTDATA terminal during a secondary communication cycle. One application for this function is in monitoring RING DETECT or OFFHOOK DETECT from a phone answering system. FLAG allows response to these incoming control signals. Figure 3-6 shows the timing associated with this operating mode.



NOTES: A. When DIN performs a read operation (set D13 to 1) during secondary communication.
 B. When DIN perform a write operation (set D13 to 0) during secondary communication.

Figure 3-6. Phone Mode Timing When Phone Mode is Enabled

3.5 DIN and DOUT Data Format

3.5.1 Primary Serial Communication DIN and DOUT Data Format (Figure 3–7)

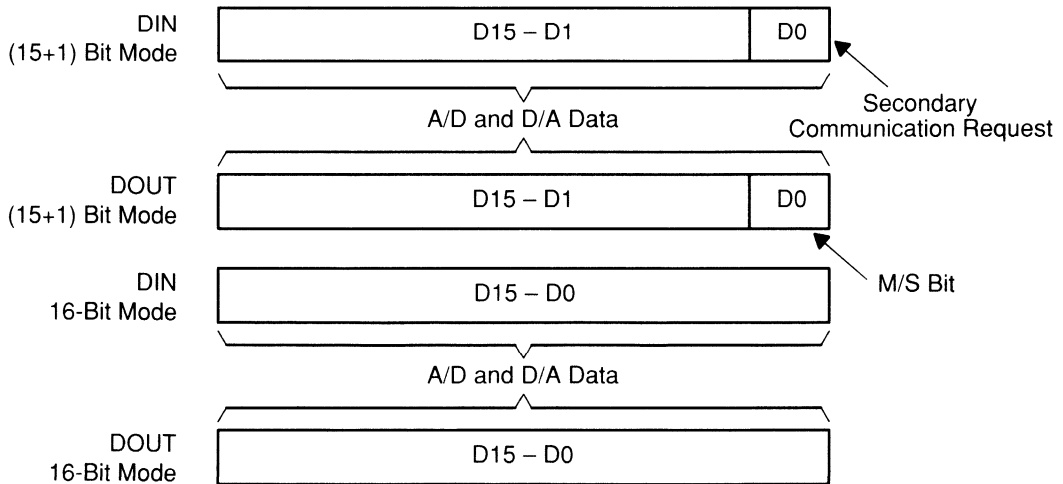


Figure 3–7. Primary Communication DIN and DOUT Data Format

3.5.2 Secondary Serial Communication DIN and DOUT Data Format (Figure 3–8)

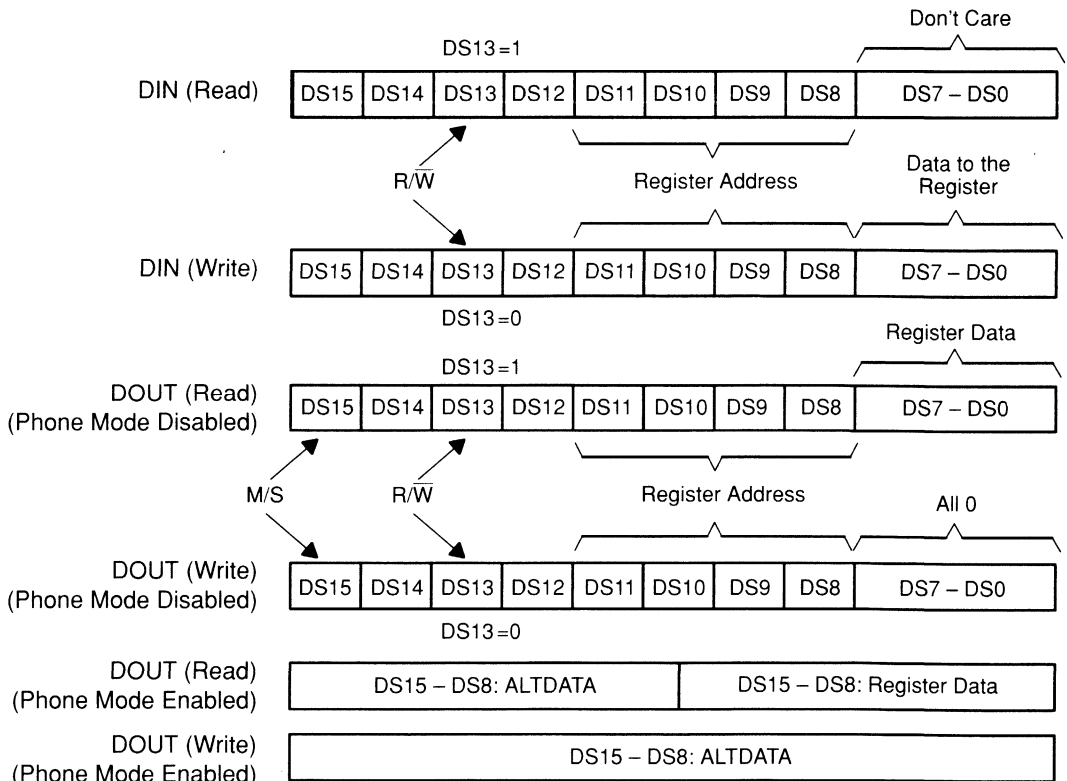


Figure 3–8. Secondary Communication DIN and DOUT Data Format

4 Specifications

4.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, DV_{DD} , AV_{DD} (see Note 1)	−0.3 V to 7 V
Output voltage range, $DOUT$, \overline{FS} , $SCLK$, $FLAG$	−0.3 V to $DV_{DD} + 0.3$ V
Output voltage range, $OUTP$, $OUTM$	−0.3 V to $V_{DD} + 0.3$ V
Input voltage range, DIN , $PWRDWN$, \overline{RESET} , $ALTDATA$, MCLK, FC	−0.3 V to $DV_{DD} + 0.3$ V
Input voltage range, INP , INM , $AUXP$, $AUXM$	−0.3 V to $V_{DD} + 0.3$ V
Case temperature for 10 seconds: DW package	260°C
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

4.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, AV_{DD} (see Note 2)	4.75		5.5	V
Analog signal input voltage, $V_{I(\text{analog})}$	Differential (INP–INM) peak, for full scale operation		6	V
Differential output load resistance, $OUTP$, $OUTM$, R_L	600			Ω
Differential output load capacitance, $OUTP$, $OUTM$, C_L	15			pF
ADC or DAC conversion rate	8		22.05	kHz
Operating free-air temperature, T_A	0		70	°C

NOTE 2: Voltages at analog inputs and outputs and V_{DD} are with respect to the V_{SS} terminal.

4.2.1 Recommended Operating Conditions, $DV_{DD} = 5$ V

	MIN	NOM	MAX	UNIT
Supply voltage, DV_{DD} (see Note 2)	4.5		5.5	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
MCLK frequency		8.192	11.290	MHz

NOTE 2: Voltages at analog inputs and outputs and V_{DD} are with respect to the V_{SS} terminal.

4.2.2 Recommended Operating Conditions, $DV_{DD} = 3$ V

	MIN	NOM	MAX	UNIT
Supply voltage, DV_{DD} (see Note 2)	2.7	3	3.3	V
High-level input voltage, V_{IH}	1.8			V
Low-level input voltage, V_{IL}			0.6	V
MCLK frequency		8.192	11.290	MHz

NOTE 2: Voltages at analog inputs and outputs and V_{DD} are with respect to the V_{SS} terminal.

4.3 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, $DV_{DD} = 5\text{ V}$, $R_L = 600\ \Omega$ (Unless Otherwise Noted)

4.3.1 Digital Inputs and Outputs, $MCLK = 8.192\text{ MHz}$, $f_s = 8\text{ kHz}$, Outputs Not Loaded

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage, DOUT	$I_O = 360\ \mu\text{A}$	2.4	4.6		V
V_{OL} Low-level output voltage, DOUT	$I_O = 2\text{ mA}$		0.2	0.4	V
I_{IH} High-level input current, any digital input	$V_{IH} = 5\text{ V}$			10	μA
I_{IL} Low-level input current, any digital input	$V_{IL} = 0.8\text{ V}$			10	μA
C_j Input capacitance			5		pF
C_o Output capacitance			5		pF

4.3.2 Digital Inputs and Outputs, $MCLK = 8.192\text{ MHz}$, $f_s = 8\text{ kHz}$, Outputs Not Loaded, $DV_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage, DOUT	$I_O = 360\ \mu\text{A}$	2.4	4.6		V
V_{OL} Low-level output voltage, DOUT	$I_O = 2\text{ mA}$		0.2	0.4	V
I_{IH} High-level input current, any digital input	$V_{IH} = 3\text{ V}$			10	μA
I_{IL} Low-level input current, any digital input	$V_{IL} = 0.6\text{ V}$			10	μA
C_j Input capacitance			5		pF
C_o Output capacitance			5		pF

4.3.3 ADC Path Filter, $MCLK = 8.192\text{ MHz}$, $f_s = 8\text{ kHz}$ (see Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	0 to 300 Hz	-0.5		0.2	dB
	300 Hz to 3 kHz	-0.25		0.25	
	3.3 kHz	-0.35		0.3	
	3.6 kHz			-3	
	4 kHz			-40	
	$\geq 4.4\text{ kHz}$			-74	

NOTE 3: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The analog input test signal is a sine wave with 0 dB = 4 V_{pp} as the reference level for the analog input signal. The passband is 0 to 3600 Hz for an 8-kHz sample rate. This passband scales linearly with the sample rate.

4.3.4 ADC Dynamic Performance, $MCLK = 8.192\text{ MHz}$, $f_s = 8\text{ kHz}$

4.3.4.1 ADC Signal-to-Noise (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio (SNR)	$V_I = -1\text{ dB}$ (5.35 V)	85	89		dB
	$V_I = -9\text{ dB}$ (2.13 V)	77	81		
	$V_I = -40\text{ dB}$ (60 mV)	46	50		
	$V_I = -65\text{ dB}$ (3 mV)	21	25		
	$V_{AUX} = -9\text{ dB}$	77	81		

NOTE 4: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output are referenced to $AV_{DD}/2$.

4.3.4.2 ADC Signal-to-Distortion (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	$V_I = -3$ dB (4.25 V)	80	85		dB
	$V_I = -9$ dB (2.13 V)	79	90		
	$V_I = -40$ dB (60 mV)	67	72		
	$V_I = -65$ dB (3 mV)	43	48		
	$V_{AUX} = -9$ dB	79	90		

NOTE 4. The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output are referenced to $V_{DD}/2$.

4.3.4.3 ADC Signal-to-Distortion + Noise (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion + noise (THD + N)	$V_I = -3$ dB (4.25 V)	78	82		dB
	$V_I = -9$ dB (2.13 V)	76	80		
	$V_I = -40$ dB (60 mV)	45	49		
	$V_I = -65$ dB (3 mV)	20	24		
	$V_{AUX} = -9$ dB	76	80		

NOTE 4. The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output are referenced to $V_{DD}/2$.

4.3.5 ADC Channel Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(PP)}$ Peak-to-peak input voltage			6		V
Dynamic range	$V_I = -1$ dB (5.35 V)		88		dB
Interchannel isolation			100		dB
E_G Gain error	$V_I = -1$ dB at 1020 kHz		± 0.3		dB
$E_{O(ADC)}$ ADC converter offset error			5		mV
CMRR Common-mode rejection ratio at INM, INP or AUXM, AUXP	$V_I = -1$ dB at 1020 kHz		74		dB
Idle channel noise (on-chip reference)	$V_{INP, INM} = 2.5$ V			75	μ V rms
R_j Input resistance	$T_A = 25^\circ\text{C}$		35		k Ω
Channel delay			$17/f_s$		s

4.3.6 DAC Path Filter, MCLK = 8.192 MHz, $f_s = 8$ kHz (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	0 to 300 Hz	-0.5		0.2	dB
	300 Hz to 3 kHz	-0.25		0.25	
	3.3 kHz	-0.35		0.3	
	3.6 kHz			-3	
	4 kHz			-40	
	≥ 4.4 kHz			-74	

NOTE 5: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is $6 V_{I(PP)}$. The pass band is 0 to 3600 Hz for an 8-kHz sample rate. This pass band scales linearly with the conversion rate.

4.3.7 DAC Dynamic Performance

4.3.7.1 DAC Signal-to-Noise when load is 600 Ω (see Note 6)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio (SNR)	$V_I = 0$ dB	85	89		dB
	$V_I = -9$ dB	76	80		
	$V_I = -40$ dB	45	49		
	$V_I = -65$ dB	20	24		

NOTE 6: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of application schematic low-pass filter. The test is conducted in 16-bit mode.

4.3.7.2 DAC Signal-to-Noise when load is 10 kΩ (see Note 6)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio (SNR)	$V_I = 0$ dB		89		dB
	$V_I = -9$ dB		80		
	$V_I = -40$ dB		50		
	$V_I = -65$ dB		25		

NOTE 6: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of application schematic low-pass filter. The test is conducted in 16-bit mode.

4.3.7.3 DAC Signal-to-Distortion when load is 600 Ω (see Note 6)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	$V_I = -3$ dB	76	80		dB
	$V_I = -9$ dB	84	90		
	$V_I = -40$ dB	64	72		
	$V_I = -65$ dB	42	48		

NOTE 6: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of application schematic low-pass filter. The test is conducted in 16-bit mode.

4.3.7.4 DAC Signal-to-Distortion when load is 10 kΩ (see Note 6)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	$V_I = -3$ dB		82		dB
	$V_I = -9$ dB		91		
	$V_I = -40$ dB		77		
	$V_I = -65$ dB		49		

NOTE 6: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of application schematic low-pass filter. The test is conducted in 16-bit mode.

4.3.7.5 DAC Signal-to-Distortion+Noise when load is 600 Ω (see Note 6)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion + noise (THD + N)	$V_I = -3$ dB	75	79		dB
	$V_I = -9$ dB	75	79		
	$V_I = -40$ dB	45	49		
	$V_I = -65$ dB	20	24		

NOTE 6: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of application schematic low-pass filter. The test is conducted in 16-bit mode.

4.3.8 DAC Channel Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic range				88		dB
Interchannel isolation				100		dB
E _G	Gain error, 0 dB	V _O = 0 dB at 1020 Hz		±0.3		dB
Idle channel narrow band noise		0 – 4 kHz, See Note 7			125	μV rms
V _{OO}	Output offset voltage at OUT (differential)	DIN = All 0s		30		mV
V _O	Analog output voltage, OUTP–OUTM	R _L = 600 Ω max (see Figure 3–8) with internal reference and full-scale digital input, see Note 8, differential			6	V _{PP}
Total out of band energy (0.55 f _S to 3 MHz)					–45	dB
Channel delay				18/f _S		

- NOTES: 7. The conversion rate is 8 kHz; the-out-of-band measurement is made from 4400 Hz to 3 MHz.
8. The digital input to the DAC channel at DIN is in 2's complement format. The TLC320AD50C/52C DAC is of the current-type and requires a load resistor for current to voltage conversion.

4.3.9 Power Supply, AV_{DD} = DV_{DD} = 5 V, No Load

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{DD} (analog)	Power supply current, ADC	Operating		18	24	mA
		Power down		1		
I _{DD} (PLL)	Power supply current, PLL	Operating		2	4	mA
		Power down		0.5		
I _{DD} (digital 1)	Power supply current, digital	Operating		4	6	mA
		Power down		10		
I _{DD} (digital 2)	Power supply current, digital, DV _{DD} = 3 V	Operating		4		mA
		Power down		10		
P _D	Power dissipation	Operating		120	170	mW
		H/W-power down		7.5	20	

4.3.10 Power-Supply Rejection, AV_{DD} = DV_{DD} = 5 V (see Note 9)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AV _{DD}	Supply voltage rejection ratio, analog supply	f _j = 0 to f _S /2		50		dB
DV _{DD}	Supply voltage rejection ratio, DAC channel	f _j = 0 to 30 kHz		40		
DV _{DD}	Supply voltage rejection ratio, ADC channel	f _j = 0 to 30 kHz		50		

NOTE 9: Power supply rejection measurements are made with both the ADC and the DAC channels idle and a 200-mV peak-to-peak signal applied to the appropriate supply.

4.4 Timing Characteristics (see Parameter Measurement Information)

4.4.1 Master Mode Timing Requirements

		MIN	NOM	MAX	UNIT
t_{d1}	Delay time, SCLK \uparrow to $\overline{FS}\downarrow$			0	ns
t_{su1}	Setup time, DIN, before SCLK low	25			
t_{h1}	Hold time, DIN, after SCLK high			20	
t_{d3}	Delay time, MCLK \downarrow to SCLK \uparrow			50	
$t_{d(CH-FDL)}$	Delay time, SCLK high to \overline{FSD} low (see Figure 5-1)			50	
t_{wH}	Pulse duration, MCLK high	32			
t_{wL}	Pulse duration, MCLK low	20			

4.4.2 Slave Mode Timing Requirements

		MIN	NOM	MAX	UNIT
t_{d4}	Delay time, SCLK \uparrow to $\overline{FS}\downarrow$			0	ns
t_{su2}	Setup time, DIN, before SCLK low	20			
t_{h2}	Hold time, DIN, after SCLK high			20	
t_{d6}	Delay time, MCLK \downarrow to SCLK \uparrow			50	
$t_{d(FL-FDL)}$	Delay time, \overline{FS} low to \overline{FSD} low, (see Figure 5-2)			40	
$t_{d(CH-FDL)}$	Delay time, SCLK high to \overline{FSD} low, slave mode (see Figure 5-1)			50	
t_{wH}	Pulse duration, MCLK high	32			
t_{wL}	Pulse duration, MCLK low	20			

4.4.3 Master Mode Switching Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d2}	Delay time, SCLK \uparrow to DOUT			20	ns
t_{en1}	Enable time, $\overline{FS}\downarrow$ to DOUT			25	
t_{dis1}	Disable time, $\overline{FS}\uparrow$ to DOUT hi-Z		20		

4.4.4 Slave Mode Switching Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d5}	Delay time, SCLK \uparrow to DOUT			20	ns
t_{en2}	Enable time, $\overline{FS}\downarrow$ to DOUT			25	
t_{dis2}	Disable time, $\overline{FS}\uparrow$ to DOUT hi-Z		20		

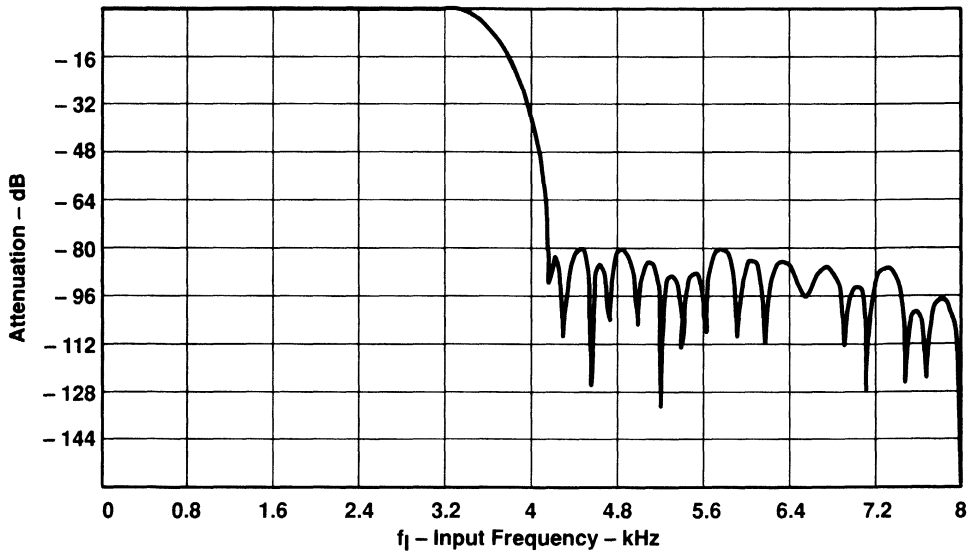


Figure 4 - 1. ADC Decimation Filter Response

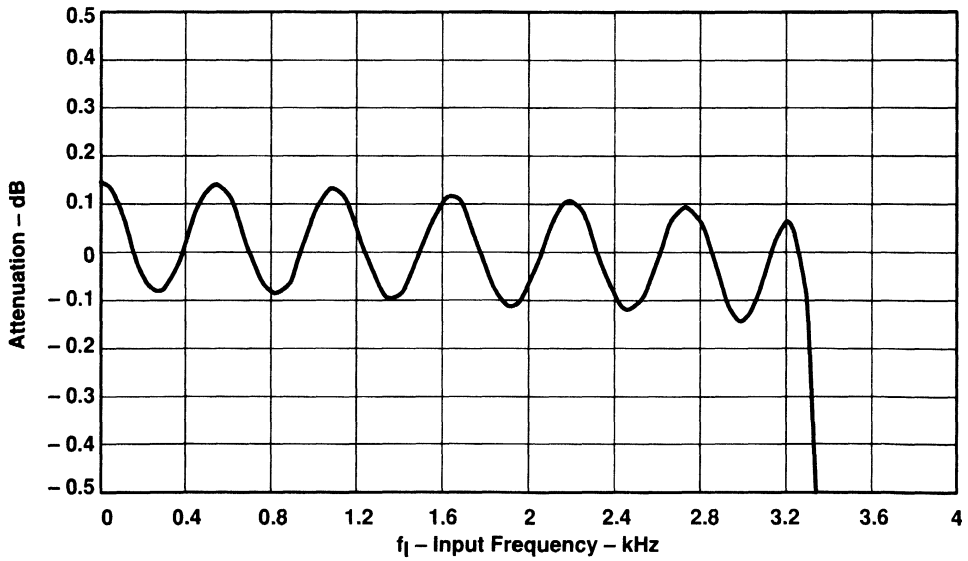


Figure 4 - 2. ADC Decimation Filter Passband Ripple

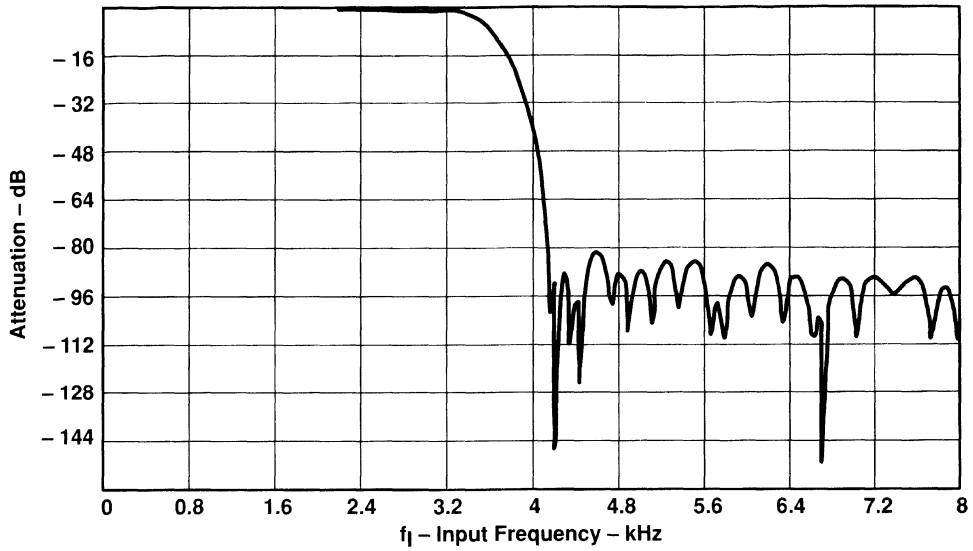


Figure 4-1. DAC Interpolation Filter Response

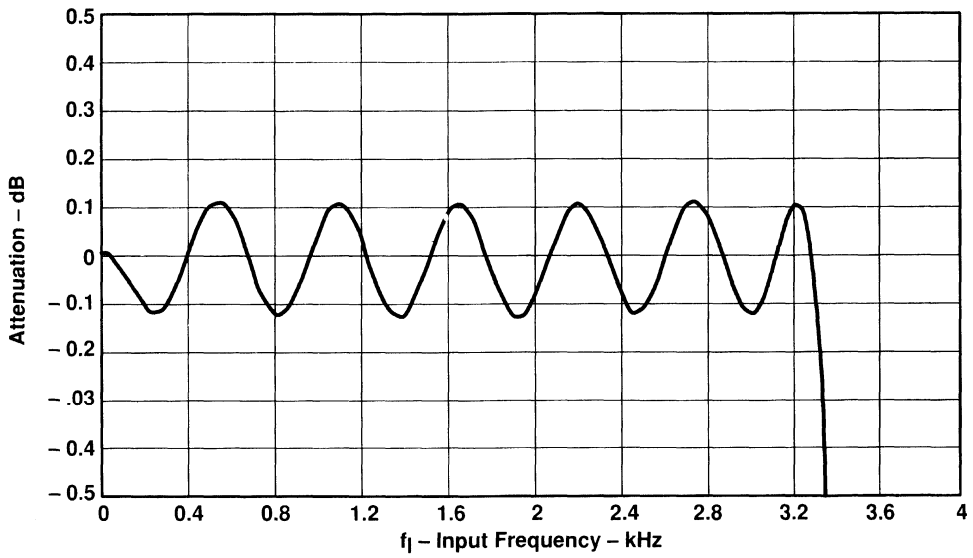


Figure 4-2. DAC Interpolation Filter Passband Ripple

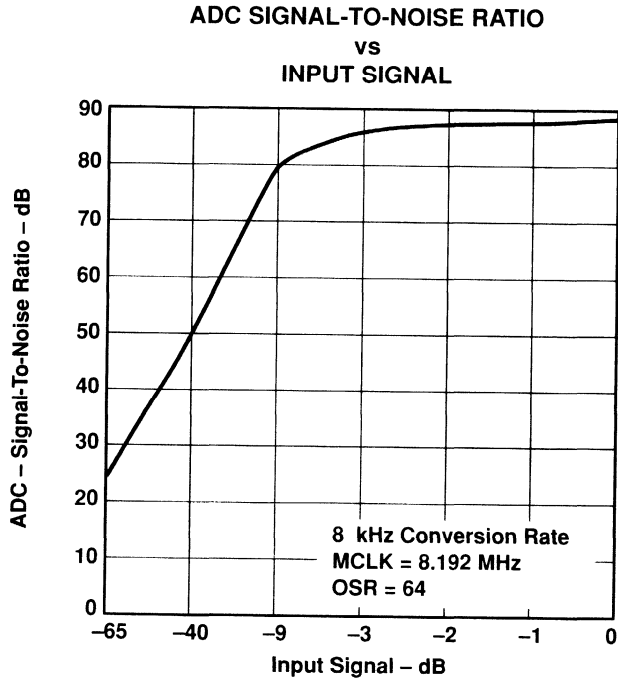


Figure 4-3.

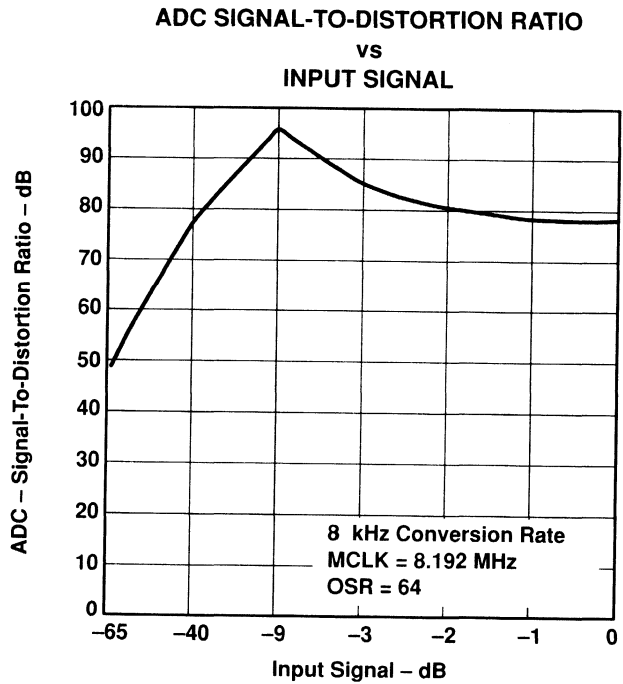


Figure 4-4.

**ADC SIGNAL-TO-(NOISE AND DISTORTION) RATIO
vs
INPUT SIGNAL**

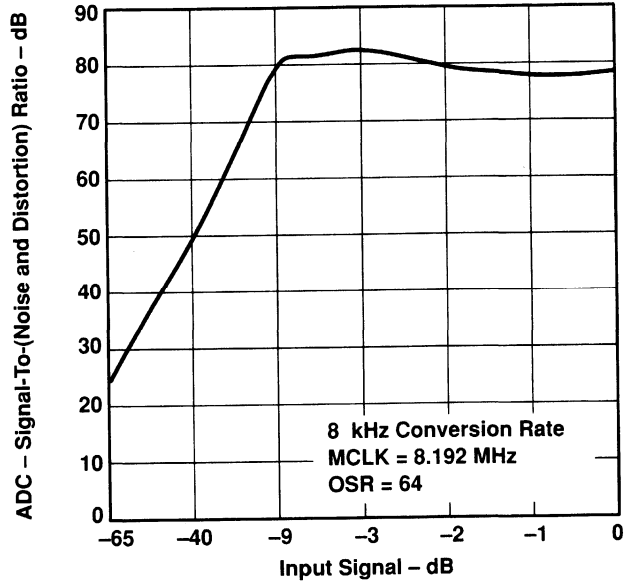


Figure 4-5.

**DAC SIGNAL-TO-NOISE RATIO
vs
INPUT SIGNAL**

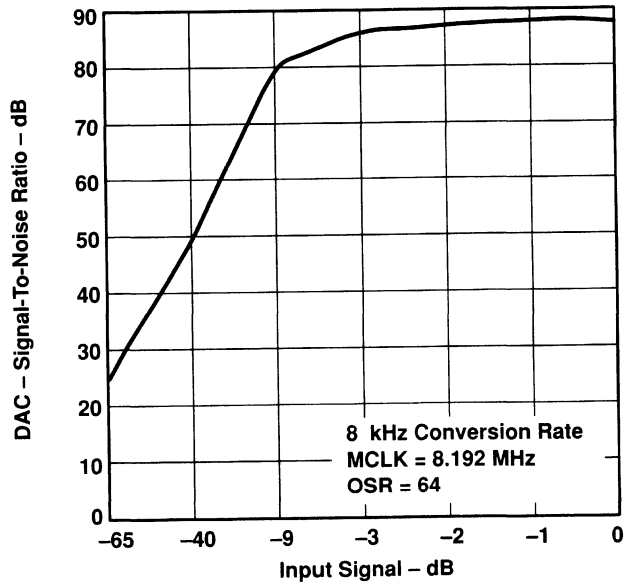


Figure 4-6.

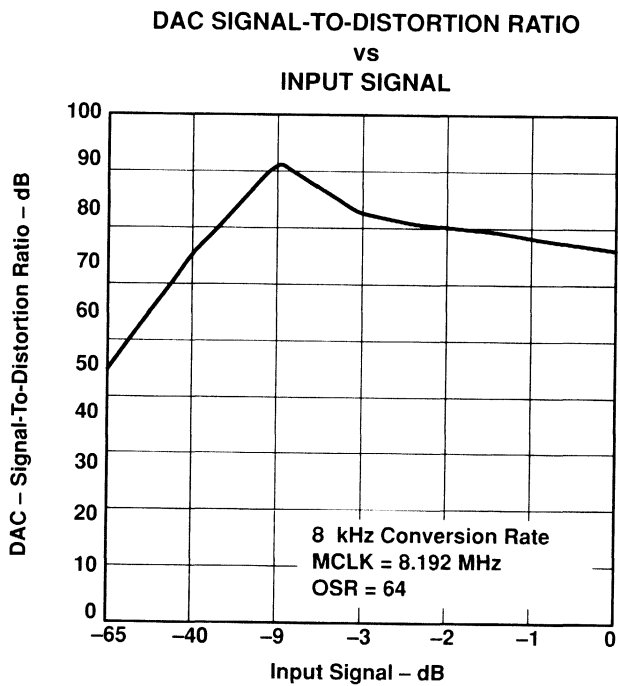


Figure 4-7.

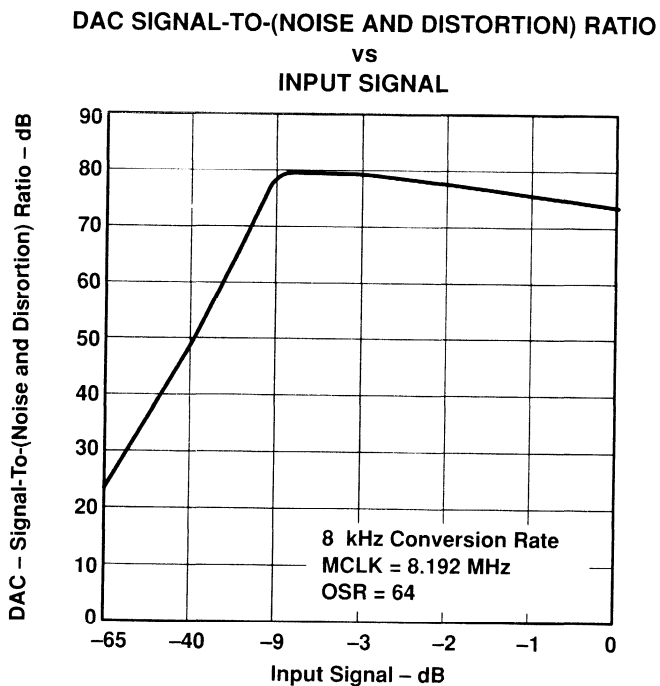
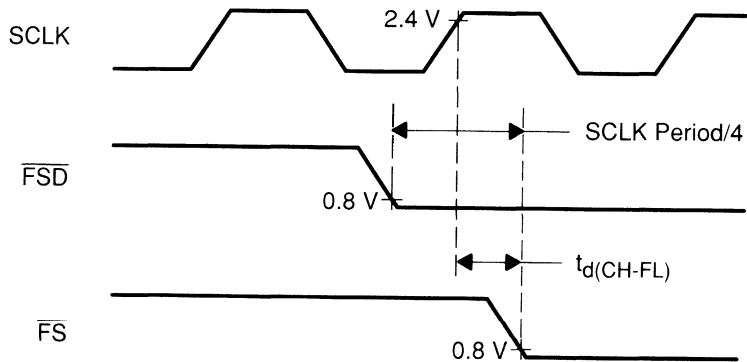


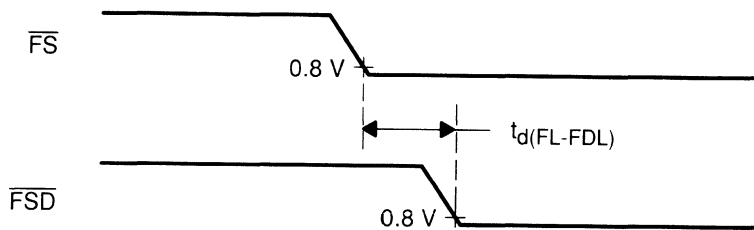
Figure 4-8.

5 Parameter Measurement Information



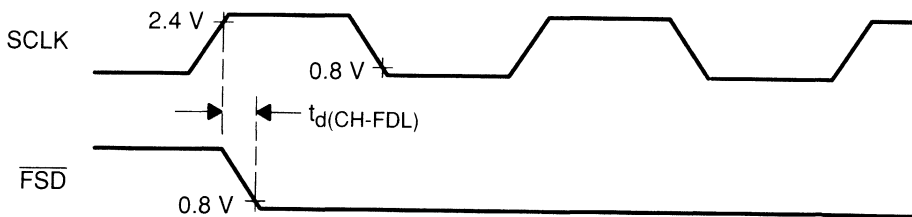
NOTE A: Timing shown is for the TLC320AD50C/52C operating as the master device.

Figure 5–1. Master $\overline{\text{FS}}$ and $\overline{\text{FSD}}$ Timing



NOTE A: Timing shown is for the TLC320AD50C/52C operating in the slave mode ($\overline{\text{FS}}$ and SCLK signals are generated externally). The programmed data value in the FSD register is 0.

Figure 5–2. Slave $\overline{\text{FS}}$ to $\overline{\text{FSD}}$ Timing



NOTE A: Timing shown is for the TLC320AD50C/52C operating in the slave mode ($\overline{\text{FS}}$ and SCLK signals are generated externally). There is a data value in the FSD register greater than 18 decimal.

Figure 5–3. Slave SCLK to $\overline{\text{FSD}}$ Timing

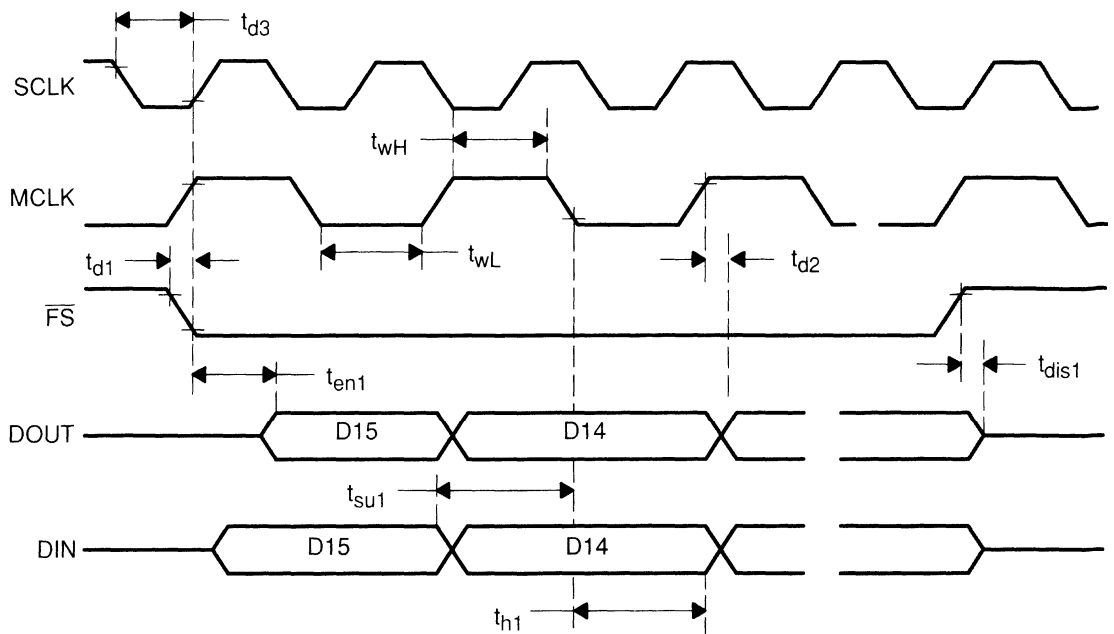


Figure 5-4. Serial Communication Timing (Master Mode)

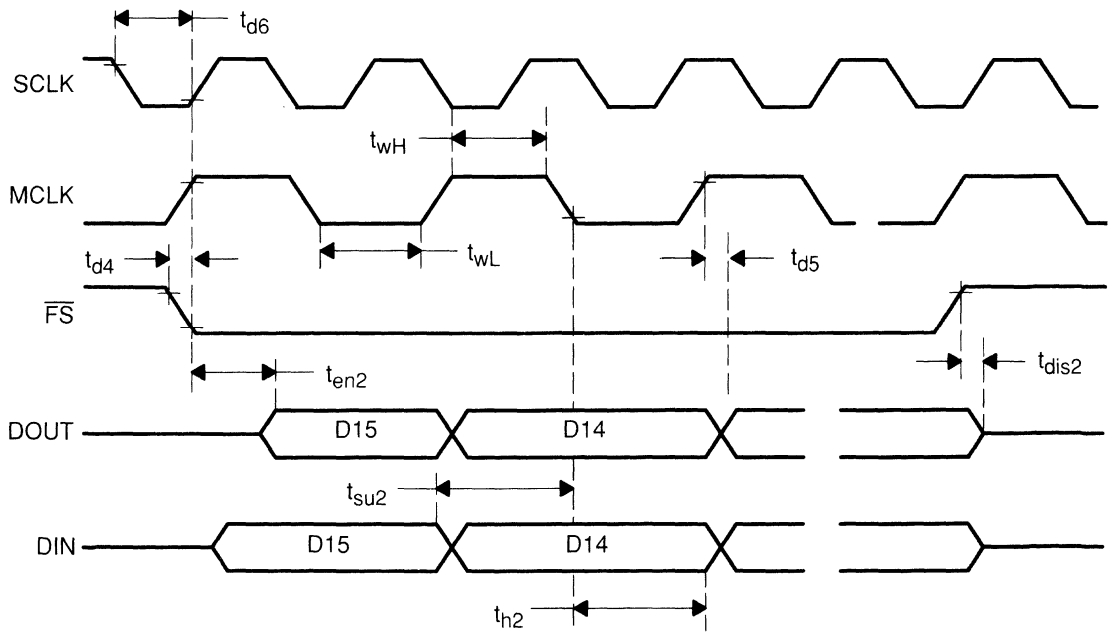


Figure 5-5. Serial Communication Timing (Slave Mode)

6 Register Set

Bits D12 through D8 in a secondary serial communication comprise the address of the register that is written with data carried in D7 through D0. D13 determines a read or write cycle to the addressed register. When low, a write cycle is selected.

The following table shows the register map.

Table 6–1. Register Map

REGISTER NO.	D15	D14	D13	D12	D11	D10	D9	D8	REGISTER NAME
0	0	0	0	0	0	0	0	0	No operation
1	0	0	0	0	0	0	0	1	Control 1
2	0	0	0	0	0	0	1	0	Control 2
3	0	0	0	0	0	0	1	1	Control 3
4	0	0	0	0	0	1	0	0	Control 4

6.1 Control 1 Register

Table 6–2. Control 1 Register

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	–	–	–	–	–	–	–	Software reset
0	–	–	–	–	–	–	–	Software reset not asserted
–	1	–	–	–	–	–	–	Software power down (analog and filters)
–	0	–	–	–	–	–	–	Software power down (not asserted)
–	–	1	–	–	–	–	–	Select AUXP and AUXM for ADC
–	–	0	–	–	–	–	–	Select INP and INM for ADC
–	–	–	0	–	–	–	–	Select INP and INM for monitor
–	–	–	1	–	–	–	–	Select AUXP and AUXM for monitor
–	–	–	–	1	1	–	–	Monitor amplifier gain = –18 dB (see Note 1)
–	–	–	–	1	0	–	–	Monitor amplifier gain = –8 dB (see Note 1)
–	–	–	–	0	1	–	–	Monitor amplifier gain = 0 dB (see Note 1)
–	–	–	–	0	0	–	–	Monitor amp mute
–	–	–	–	–	–	1	–	Digital loopback asserted
–	–	–	–	–	–	0	–	Digital loopback not asserted
–	–	–	–	–	–	–	1	16-bit DAC mode (hardware secondary requests)
–	–	–	–	–	–	–	0	Not 16-bit DAC mode (software secondary requests)

Default value: 0 0 0 0 0 0 0 0

NOTE 1: These gains are for a single-ended input. The gain is 6 dB lower with a differential input.

A software reset is a one-shot operation and this bit is cleared to 0 after reset. It is not necessary to write a 0 to end the master reset operation. Writing 0s to the reserved bits is suggested.

6.2 Control 2 Register

Table 6–3. Control 2 Register

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
X	–	–	–	–	–	–	–	FLAG output value
–	1	–	–	–	–	–	–	Phone mode enable
–	0	–	–	–	–	–	–	Phone mode disable
–	–	X	–	–	–	–	–	Decimator FIR overflow flag (valid only during read cycle)
–	–	–	1	–	–	–	–	16-bit ADC mode
–	–	–	0	–	–	–	–	Not-16-bit ADC mode
–	–	–	–	–	X	0	0	Reserved (TLC320AD50C only)
–	–	–	–	–	0	0	0	$\overline{\text{FSD}}$ enable (TLC320AD52C only)
–	–	–	–	–	1	–	–	$\overline{\text{FSD}}$ disable (TLC320AD52C only)
–	–	–	–	1	–	–	–	Analog loopback enabled
–	–	–	–	0	–	–	–	Analog loopback disabled

Default value: 00000000

Writing 0s to the reserved bits is suggested.

6.3 Control 3 Register

The following command contains the frame-sync delay (FSD) register address and loads D7 (MSB)–D0 into the FSD register. The data byte (D1–D0) determines the number of SCLKs between \overline{FS} and the delayed frame-sync signal, \overline{FSD} . The minimum data value for the register is decimal 18.

Table 6–4. Control 3 Register

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
–	–	X	X	X	X	X	X	Number of SCLKs between \overline{FS} and \overline{FSD}
X	X	–	–	–	–	–	–	Binary number of slave devices (3 maximum for TLC320AC50C, 1 maximum for TLC320AC52C)

Default value: 00000000

Writing 0s to the reserved bits is suggested.

6.4 Control 4 Register

Table 6–5. Control 4 Register

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
–	–	–	–	1	1	–	–	Analog input gain = mute
–	–	–	–	1	0	–	–	Analog input gain = 12 dB
–	–	–	–	0	1	–	–	Analog input gain = 6 dB
–	–	–	–	0	0	–	–	Analog input gain = 0 dB
–	–	–	–	–	–	1	1	Analog output gain = mute
–	–	–	–	–	–	1	0	Analog output gain = – 12 dB
–	–	–	–	–	–	0	1	Analog output gain = – 6 dB
–	–	–	–	–	–	0	0	Analog output gain = 0 dB
–	X	X	X	–	–	–	–	Sample frequency select (N): $f_s = MCLK/(128 \times N)$ or $MCLK/(512 \times N)$
1	–	–	–	–	–	–	–	External sample clock feature enabled
0	–	–	–	–	–	–	–	External sample clock feature disabled

Default value: 00000000

The value of the sample frequency divisor, N, is determined by the octal representation of bits D4 – D6. Hence, 001 = 1, 010 = 2, etc. By setting D4 – D6 to 000, N = 8 is selected.

7 Application Information

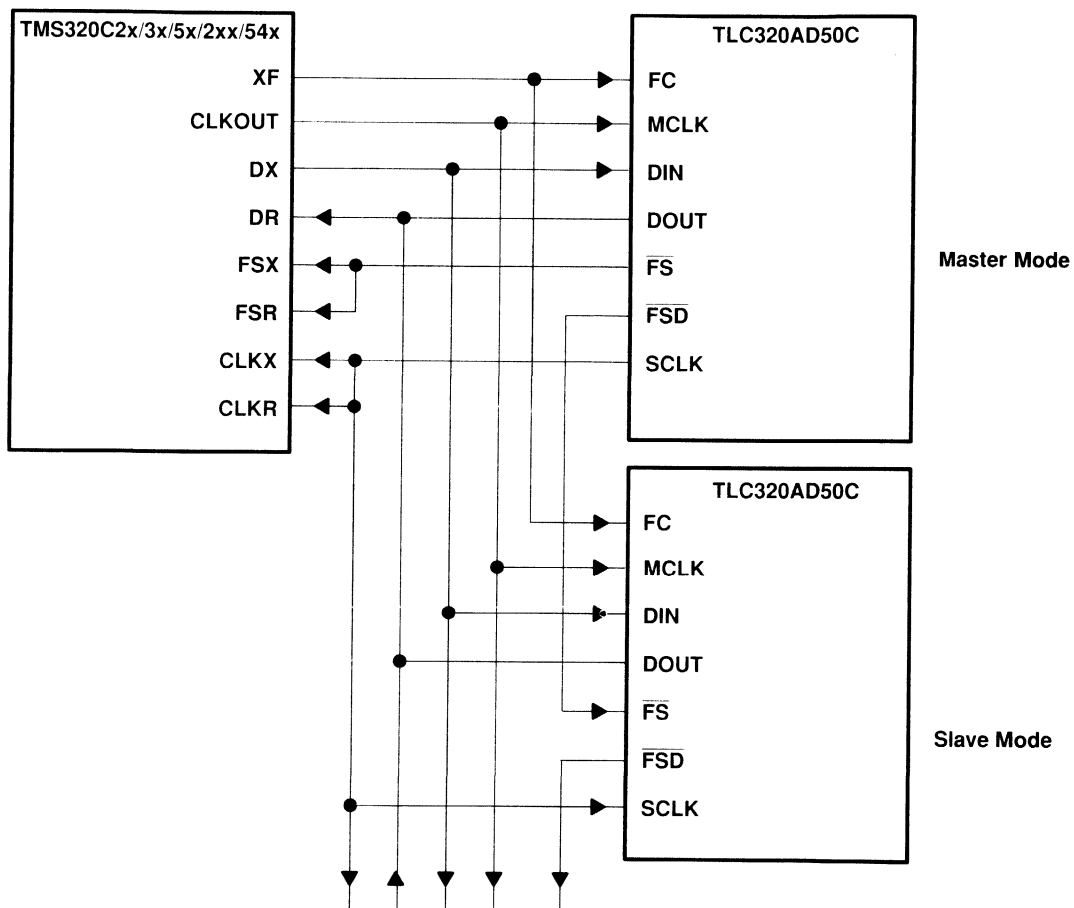


Figure 7–1. Master Device and Slave Device Connections (to DSP Interface)

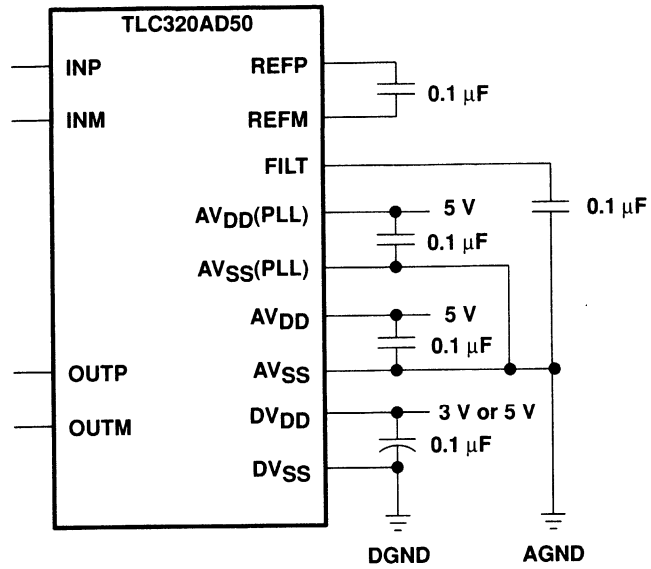


Figure 7-2. Power Supply Decoupling

TLC320AD55C ***Data Manual***

Sigma-Delta Analog Interface Circuit

SLAS085
July 1995



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Contents

<i>Section</i>	<i>Title</i>	<i>Page</i>
1	Introduction	4-423
1.1	Features	4-423
1.2	Functional Block Diagram	4-424
1.3	Terminal Assignments	4-425
1.4	Ordering Information	4-425
1.5	Terminal Functions	4-426
1.6	Definitions and Terminology	4-427
1.7	Register Functional Summary	4-428
2	Functional Description	4-429
2.1	Device Functions	4-429
2.1.1	Operating Frequencies	4-429
2.1.2	ADC Signal Channel	4-429
2.1.3	DAC Signal Channel	4-429
2.1.4	Serial Interface	4-429
2.1.5	Register Programming	4-429
2.1.6	Sigma-Delta ADC	4-430
2.1.7	Decimation Filter	4-430
2.1.8	Sigma-Delta DAC	4-430
2.1.9	Interpolation Filter	4-430
2.1.10	Switched-Capacitor Filter (SCF)	4-430
2.1.11	Analog/Digital Loopback	4-430
2.1.12	DAC Voltage Reference Enable	4-430
2.1.13	FIR Overflow Flag	4-430
2.2	Terminal Descriptions	4-431
2.2.1	Reset and Power-Down	4-431
2.2.2	Master Clock Circuit	4-432
2.2.3	Data Out (DOUT)	4-432
2.2.4	Data In (DIN)	4-432
2.2.5	Hardware Program Terminal (FC)	4-433
2.2.6	Frame-Sync	4-433
2.2.7	Multiplexed Analog Input	4-433
2.2.8	Analog Input	4-433
3	Serial Communications	4-435
3.1	Primary Serial Communication	4-435
3.2	Secondary Serial Communication	4-437
3.3	Conversion Rate Versus Serial Port	4-439
3.4	FIR Bypass Mode	4-440
3.5	Phone Mode Control	4-441

Contents (Continued)

<i>Section</i>	<i>Title</i>	<i>Page</i>
4	Specifications	4-443
4.1	Absolute Maximum Ratings Over Operating Free-Air Temperature Range ...	4-443
4.2	Recommended Operating Conditions	4-443
4.3	Recommended Operating Conditions, $DV_{DD} = 5\text{ V}$	4-443
4.4	Electrical Characteristics, $T_A = 25^\circ\text{C}$, $V_{DD}(\text{ADC}) = V_{DD}(\text{DAC}) = DV_{DD} = 5\text{ V}$, MCLK = 16.384 MHz, Fk = 8	4-444
4.4.1	Digital Inputs and Outputs, Outputs Not Loaded	4-444
4.4.2	ADC Path Filter	4-444
4.4.3	ADC Dynamic Performance	4-444
4.4.4	ADC Channel	4-445
4.4.5	DAC Path Filter	4-445
4.4.6	DAC Dynamic Performance	4-446
4.4.7	DAC Channel	4-446
4.4.8	Power Supplies, $V_{DD}(\text{ADC}) = V_{DD}(\text{DAC}) = DV_{DD} = 5\text{ V}$, No Load	4-447
4.4.9	Timing Requirements	4-447
5	Application Information	4-449
Appendix A	Register Set	4-451

List of Illustrations

<i>Figure</i>	<i>Title</i>	<i>Page</i>
1-1	Functional Block Diagram	4-424
1-2	Terminal Assignments	4-425
2-1	Reset Function	4-431
2-2	Internal Power-Down Logic	4-432
2-3	Differential Analog Input Configuration	4-433
3-1	Primary Serial Communication Timing	4-436
3-2	DAC and ADC Word Lengths	4-436
3-3	Hardware and Software Methods to Initiate a Secondary Request	4-437
3-4	Secondary DIN Format	4-437
3-5	Hardware FC Secondary Request	4-438
3-6	Software FC Secondary Request	4-439
3-7	FIR Bypass Timing	4-440
3-8	Phone Mode Timing	4-441
5-1	TLC320AD55C Application Schematic	4-449
5-2	TLC320AD55C I/O Buffer and V_{MID} Generator Schematic	4-450

List of Tables

<i>Table</i>	<i>Title</i>	<i>Page</i>
3-1	Least-Significant-Bit Control Function	4-438
3-2	Secondary Communication Data Format	4-439

1 Introduction

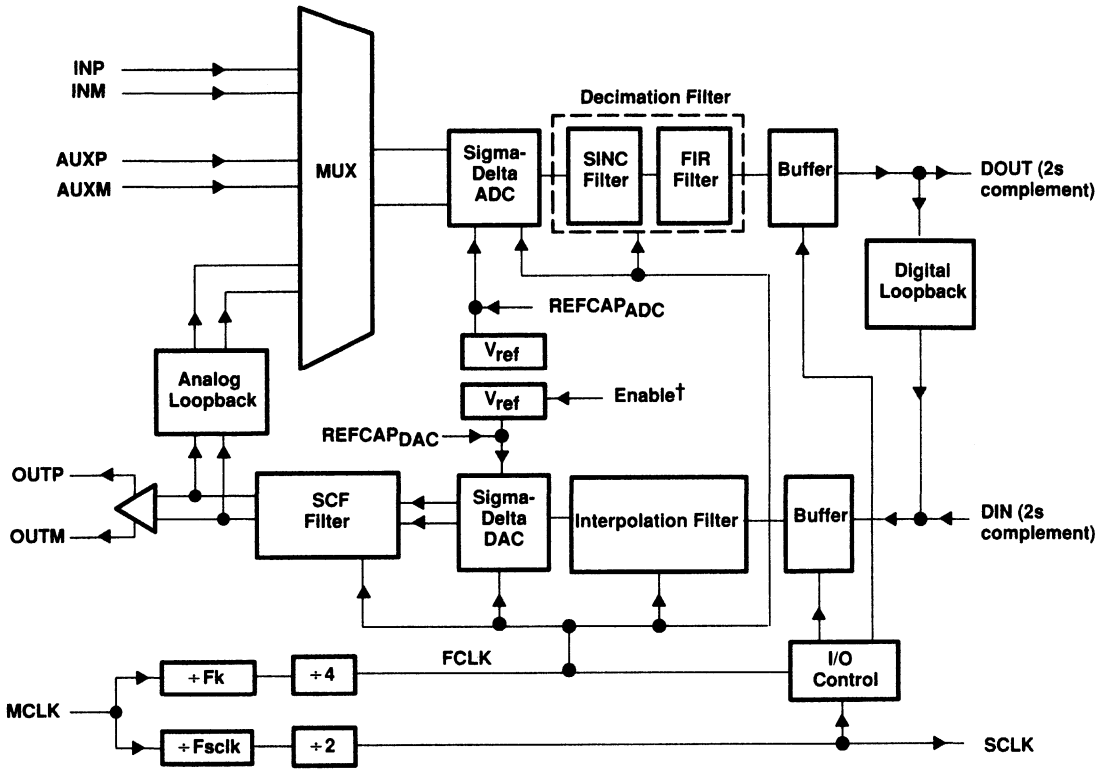
The TLC320AD55C provides high resolution low-speed signal conversion from digital-to-analog (D/A) and from analog-to-digital (A/D) using oversampling sigma-delta technology. This device consists of two, serial, synchronous conversion paths (one for each data direction) and includes an interpolation filter before the digital-to-analog converter (DAC) and a decimation filter after the analog-to-digital converter (ADC) (see Figure 1–1). Other overhead functions provide analog filtering and on-chip timing and control. The sigma-delta architecture produces high resolution, analog-to-digital and digital-to-analog conversion at low system speeds and low cost.

The options and the circuit configurations of this device can be programmed through the serial interface. The options include reset, power-down, communications protocol, serial clock rate, signal sampling rate, and test mode as outlined in Appendix A. The circuit configurations could include a selection of input ports to the ADC, analog loopback, digital loopback, decimator sinc filter output, decimator finite-duration impulse-response (FIR) filter output, interpolator sinc filter output, and interpolator FIR filter output. The TLC320AD55C is characterized for operation from 0°C to 70°C.

1.1 Features

- Single 5-V power supply
- Power dissipation (P_D) of 150 mW maximum in the operating mode
- Power-down mode to 1 mW
- General-purpose 16-bit signal processing
- 2s-complement format
- Serial port interface
- Minimum 80-dB harmonic distortion plus noise
- Differential architecture
- Internal reference voltage (V_{ref})
- Internal $64 \times$ oversampling
- Analog output with programmable gain of 1, 1/2, 1/4, and 0 (squelch)
- Phone-mode output control
- Variable conversion rate selected as $MCLK/(F_k \times 256)$, $F_k = 1, 2, 3, \dots, 256$
- System test mode:
 - Digital loopback test
 - Analog loopback test

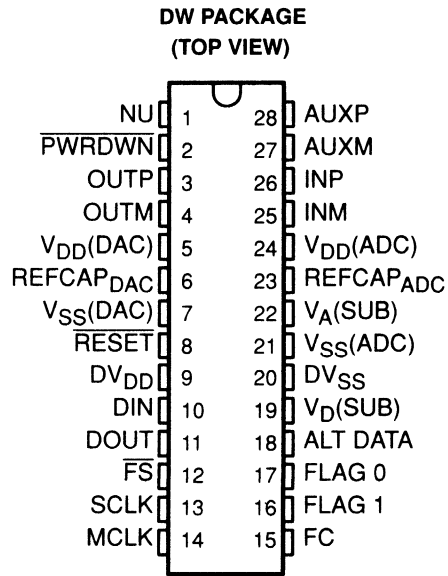
1.2 Functional Block Diagram



† See control 3 register in Appendix A.

Figure 1–1. Functional Block Diagram

1.3 Terminal Assignments



NU—Make no external connection

Figure 1–2. Terminal Assignments

1.4 Ordering Information

T _A	PACKAGE
	SMALL OUTLINE (DW)
0°C to 70°C	TLC320AD55CDW

1.5 Terminal Functions

TERMINALS NAME	NO.	I/O	DESCRIPTION
AUXM	27	I	Inverting input to auxiliary analog input
AUXP	28	I	Noninverting input to auxiliary analog input
ALT DATA	18	I	Signals on ALT DATA are routed to DOUT during secondary communication when phone mode is enabled.
DIN	10	I	Data input. DIN receives the DAC input data and command information from the DSP and is synchronized to SCLK.
DOUT	11	O	Data output. DOUT transmits the ADC output bits and is synchronized to SCLK. DOUT is at Hi-Z when \overline{FS} is not activated.
DV _{DD}	9	I	Digital power supply
DV _{SS}	20	I	Digital ground
FC	15	I	Function control. FC is sampled and latched on the rising edge of \overline{FS} for the primary serial communication. Refer to Section 3 Serial Communications for more details.
FLAG 0	17	O	During phone mode, FLAG 0 contains the value set in control 2 register.
FLAG 1	16	O	During phone mode, FLAG 1 contains the value set in control 2 register.
FS	12	O	Frame sync. When \overline{FS} goes low, the serial communication port is activated. In all serial transmission modes, \overline{FS} is held low during bit transmission. Refer to Section 3 Serial Communications for a detailed description.
INM	25	I	Inverting input to analog input
INP	26	I	Noninverting input to analog input
MCLK	14	I	Master clock. MCLK derives the internal clocks of the sigma-delta analog interface circuit.
OUTM	4	O	Inverting output of the DAC analog power amplifier. Functionally identical with and complementary to OUTP. OUTM and OUTP can drive 600 Ω differentially. OUTM should not be used alone for single-ended operation.
OUTP	3	O	Noninverting output of the DAC analog power amplifier. OUTM and OUTP can drive 600 Ω differentially. OUTP should not be used alone for single-ended operation.
PWRDWN	2	I	Power down. When PWRDWN is pulled low, the device goes into a power-down mode; the serial interface is disabled and most of the high-speed clocks are disabled. However, all of the registers' values are sustained and the device resumes full power operation without reinitialization when PWRDWN is pulled high again. PWRDWN resets the counters only and preserves the programmed register contents. Refer to Section 2.2.1.3 Software and Hardware Power-Down.
REFCAP _{ADC}	23	O	Analog-reference voltage connection for external capacitor for the ADC. The nominal voltage on REFCAP _{ADC} is 3.4 V. A buffer must be used when this voltage is used externally. REFCAP _{ADC} is not to be used as the mid-supply voltage reference for single-ended operation.
REFCAP _{DAC}	6	O	Analog-reference voltage connection for external capacitor for the DAC. The nominal voltage on REFCAP _{DAC} is 3.4 V. A buffer must be used when this voltage is used externally.
RESET	8	I	Reset. The reset function initializes all of the internal registers to their default values. The serial port can be configured to the default state accordingly. Refer to Appendix A Table A-2 Control 1 Register and Section 2.2.1 Reset and Power-Down for more detailed descriptions.
SCLK	13	O	Shift clock. SCLK is derived from MCLK and clocks serial data into DIN and out of DOUT.

NOTE 1: All digital inputs and outputs are TTL compatible unless otherwise noted.

1.5 Terminal Functions (Continued)

TERMINALS		I/O	DESCRIPTION
NAME	NO.		
V _A (SUB)	22	I	Analog substrate. V _A (SUB) must be grounded.
V _D (SUB)	19	I	Digital substrate. V _D (SUB) must be grounded.
V _{DD} (ADC)	24	I	Analog ADC path supply
V _{DD} (DAC)	5	I	Analog DAC path supply
V _{SS} (ADC)	21	I	Analog ADC path ground
V _{SS} (DAC)	7	I	Analog DAC path ground

NOTE 1: All digital inputs and outputs are TTL compatible unless otherwise noted.

1.6 Definitions and Terminology

Data Transfer Interval	The time during which data is transferred from DOUT and to DIN. The interval is 16 shift clocks and this data transfer is initiated by the falling edge of the frame-sync signal.
Signal Data	The input signal and all of the converted representations through the ADC channel and return through the DAC channel to the analog output. This is contrasted with the purely digital software control data.
Primary Communications	The digital data transfer interval. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.
Secondary Communications	The digital control and configuration data transfer interval into DIN and the register read data cycle from DOUT. The data transfer interval occurs when requested by hardware or software.
Frame Sync	The falling edge of the signal that initiates the data transfer interval. The primary frame sync starts the primary communications, and the secondary frame sync starts the secondary communications.
Frame Sync and Sampling Period	The time between falling edges of successive primary frame-sync signals.
f _s	The sampling frequency that is the reciprocal of the sampling period.
Frame-Sync Interval	The time period occupied by 16 shift clocks. It goes high on the sixteenth rising edge of SCLK after the falling edge of the frame sync.
ADC Channel	All signal processing circuits between the analog input and the digital conversion results at DOUT.
DAC Channel	All signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUTP and OUTM.
Host	Any processing system that interfaces to DIN, DOUT, SCLK, or \overline{FS} .
Dxx	A bit position in the primary data word (xx is the bit number).
DSxx	A bit position in the secondary data word (xx is the bit number).
d	The alpha character d is used to represent valid programmed or default data in the control register format (see secondary serial communications) when discussing other data bit portions of the register.
X	The alpha character X represents a don't-care bit position within the control register format.
FIR	Finite-duration impulse response.

1.7 Register Functional Summary

There are six data and control registers that are used as follows:

- Register 0 The No-op register. The 0 register allows secondary requests without altering any other register.
- Register 1 The control 1 register. The data in this register controls:
- The software reset
 - The software power-down
 - Selection of the normal or auxiliary analog inputs
 - The output amplifier gain (1, 1/2, 1/4, or squelch)
 - Selection of the analog loopback
 - Selection of the digital loopback
 - 16-bit or 15-bit mode of operation
- Register 2 The control 2 register. The data in this register:
- Contains the output flag indicating a decimator FIR filter overflow
 - Contains Flag 0 and Flag 1 output values for use in the phone mode
 - Selects the phone mode
 - Selects or bypasses the decimation FIR filter
 - Selects or bypasses the interpolater FIR filter
- Register 3 The Fk divide register. This register controls the filter clock rate and the sample period.
- Register 4 The Fsclk divide register. This register controls the shift (data) clock rate.
- Register 5 The control 3 register. This register enables and disables the DAC reference.

2 Functional Description

2.1 Device Functions

The following sections describe the functions of the device.

2.1.1 Operating Frequencies

The sampling (conversion) frequency is derived from the master clock (MCLK) input by the following equation:

$$f_s = \text{Sampling (conversion) frequency} = \frac{\text{MCLK frequency}}{(\text{Fk register value}) \times 256}$$

The inverse is the time between the falling edges of two successive primary frame-synchronization signals and it is the conversion period.

The input and output data clock (SCLK) is given by:

$$\text{SCLK frequency} = \frac{\text{MCLK frequency}}{(\text{Fsclk register value}) \times 2}$$

2.1.2 ADC Signal Channel

To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data.

The ADC converts the signal into discrete output digital words in 2s-complement format, corresponding to the analog-signal value at the sampling time. These 16-bit digital words, representing sampled values of the analog input signal, are clocked out of the serial port, DOUT, during the frame-sync interval (one word for each primary communication interval). During secondary communications, the data previously programmed into the registers can be read out with the appropriate register address, and the read bit set to 1. When a register read is not requested, all 16 bits are 0 in the secondary word.

2.1.3 DAC Signal Channel

DIN receives the 16-bit serial data word (2s complement) from the host during the primary communications interval and latches the data on the seventeenth rising edge of SCLK. The data are converted to an analog voltage by the DAC and then passed through a $(\sin x)/x$ correction circuit and a smoothing filter. An output buffer with three software-programmable gains (0 dB, -6 dB, and -12 dB) drives the differential outputs OUTP and OUTM. A squelch mode can also be programmed for the output buffer. During secondary communications, the configuration program data are read into the device control registers.

2.1.4 Serial Interface

The digital serial interface consists of the shift clock, the frame synchronization signal, the ADC-channel data output, and the DAC-channel data input. During the primary 16-bit frame synchronization interval, SCLK transfers the ADC channel results from DOUT and transfers 16-bit DAC data into DIN.

During the secondary frame-synchronization interval, the SCLK transfers the register read data from DOUT when the read bit is set to a one. In addition, SCLK transfers control and device parameter information into DIN. The functional sequence is shown in Figure 3-1.

2.1.5 Register Programming

All register programming occurs during secondary communications, and data are latched and valid on the rising edge of the frame-sync signal. When the default value for a particular register is desired, that register does not need to be addressed during secondary communications. The no-op command addresses the no-op register (register 0), and register programming does not take place during this communication.

DOUT is released from the high-impedance state on the falling edge of the primary or secondary frame-sync interval. In addition, each register can be read back during DOUT secondary communications by setting the read bit D13 to 1 in the addressed register (refer to Appendix A). When the register is in the read mode, no data can be written to the register during this cycle. To return this register to the write mode requires a subsequent secondary communication.

2.1.6 Sigma-Delta ADC

The sigma-delta ADC is a fourth-order, sigma-delta modulator with 64-times oversampling. The ADC provides high-resolution, low-noise performance using oversampling techniques.

2.1.7 Decimation Filter

The decimation filter reduces the digital data rate to the sampling rate. This is accomplished by decimating with a ratio of 1:64. The output of this filter is a sixteen-bit, 2s-complement data word clocking at the sample rate.

NOTE

The sample rate is determined through a programmable relationship of $MCLK/(F_k \times 256)$, $F_k = 1, 2, 3, \dots, 256$

2.1.8 Sigma-Delta DAC

The sigma-delta DAC is a fourth-order, sigma-delta modulator with 64-times oversampling. The DAC provides high-resolution, low-noise performance from a one-bit converter using oversampling techniques.

2.1.9 Interpolation Filter

The interpolation filter resamples the digital data at a rate of 64 times the incoming sample rate. The high-speed data output from this filter is then used in the sigma-delta DAC.

2.1.10 Switched-Capacitor Filter (SCF)

A switched-capacitor filter network is implemented on the analog output to provide low-pass operation with high rejection in the stop band.

2.1.11 Analog/Digital Loopback

The loopbacks provide a means of testing the ADC/DAC channels and can be used for in-circuit, system-level tests. The loopbacks feed the appropriate output to the corresponding input on the device.

The test capabilities include an analog loopback between the two analog paths and a digital loopback between the two digital paths. Each loopback is enabled by setting the D1 or D2 bit in control 1 register (see Appendix A).

2.1.12 DAC Voltage Reference Enable

The DAC voltage reference can be disabled through the control 3 register. This allows the use of an external voltage reference applied to the DAC channel modulator. By supplying an external reference, the user can scale the output voltage range of this channel. The internal reference value is 3.6 V which provides a 6-V, peak-to-peak, differential output. The ratio of an external reference to the internal reference determines the output voltage range of the DAC channel as shown in the following equation:

$$V_{O(PP)} = \frac{V(\text{EXT REF})}{3.6} \times 6 \text{ V}$$

NOTE

The distortion and noise specifications listed in Section 4 Specifications apply only under the following condition:

$$\frac{V(\text{EXT REF})}{3.6} \leq 1$$

2.1.13 FIR Overflow Flag

The decimator FIR filter provides an overflow flag to the control 2 register to indicate that the input to the filter has exceeded the range of the internal filter calculations. When this bit is set in the register, it remains set until the register is read by the user. Reading this value always resets the overflow flag.

2.2 Terminal Descriptions

The following sections describe the terminal functions.

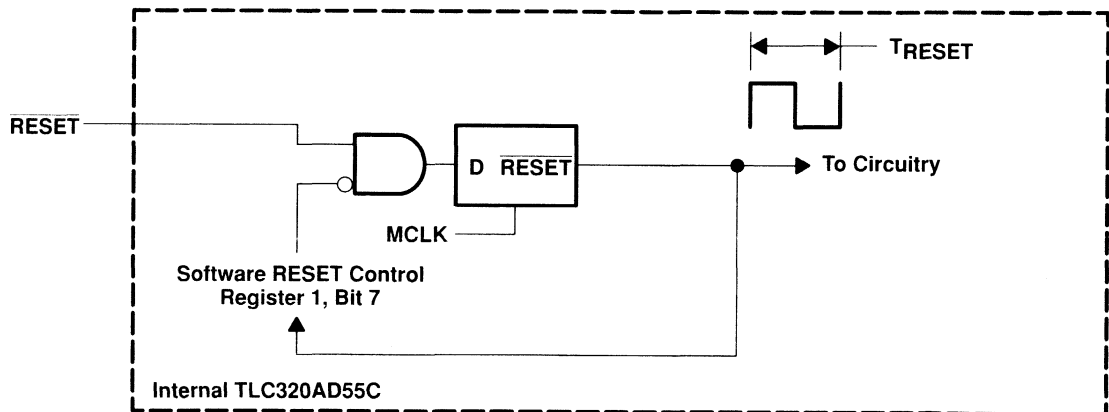
2.2.1 Reset and Power-Down

2.2.1.1 Reset

As shown in Figure 2–1, the TLC320AD55C resets both the internal counters and registers, including the programmed registers, in two ways:

- By applying a low-going reset pulse to the $\overline{\text{RESET}}$ terminal
- By writing to the programmable software reset bit (D07 in control 1 register)

$\overline{\text{PWRDWN}}$ resets the counters only and preserves the programmed register contents. The DAC resets to the 15-bit mode.



NOTE A: $\overline{\text{RESET}}$ to circuitry is at least 6 MCLK periods long and releases on the positive edge of MCLK.

Figure 2–1. Reset Function

2.2.1.2 Conditions of Reset

The two internal reset signals used for the reset and synchronization functions are:

- Counter reset – This signal resets all flip-flops and latches that are not externally programmed, with the exception of those generating the reset pulse itself. Additionally, this signal resets the software power-down bit.

Counter reset = $\overline{\text{RESET}}$ terminal or reset bit or $\overline{\text{PWRDWN}}$ terminal

- Register reset – This signal resets all flip-flops and latches that are not reset by the counter reset, except those generating the reset pulse itself.

Register reset = $\overline{\text{RESET}}$ terminal or reset bit

Both reset signals are at least six MCLK periods long (T_{RESET}) and release on the trailing edge of MCLK.

2.2.1.3 Software and Hardware Power-Down

Given the definitions above, the software-programmed power-down condition is cleared by programming the software bit (control 1 register bit 6) to a 0 or is cleared by cycling the power to the device, bringing $\overline{\text{PWRDWN}}$ low, or bringing $\overline{\text{RESET}}$ low (see Figure 2–2).

$\overline{\text{PWRDWN}}$ removes power to the entire chip. The software-programmable, power-down bit only removes power from the analog section of the chip, which allows a software power-up function. Cycling the power-down terminal from high to low and back to high resets all flip-flops and latches that are not externally programmed, thereby preserving the register contents with the exception that the software power-down bit is cleared.

When $\overline{\text{PWRDWN}}$ is not being used, it should be tied high [$V_{\text{DD}}(\text{ADC})$ is preferred].

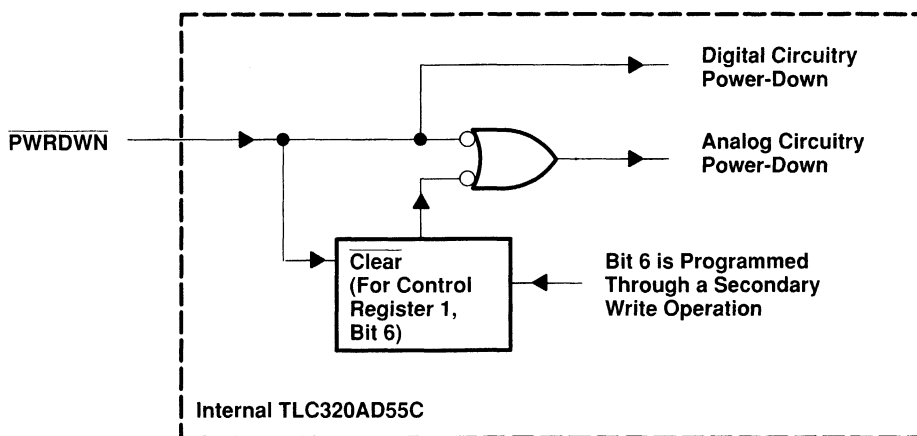


Figure 2–2. Internal Power-Down Logic

2.2.2 Master Clock Circuit

The clock circuit generates and distributes necessary clocks throughout the device. MCLK is the external master clock input. SCLK is derived from MCLK [$\text{SCLK} = \text{MCLK}/(\text{Fsclk} \times 2)$, $\text{Fsclk} = 1, 2, 3, \dots, 256$] in order to provide clocking of the serial communications between the device and a digital signal processor (DSP). The sample rate of the data paths is set as $\text{MCLK}/(\text{Fk} \times 256)$. Fk and Fsclk are programmable register values used as divisors of MCLK. The default value for the Fk and Fsclk register is 8 (decimal).

2.2.3 Data Out (DOUT)

DOUT is taken from the high-impedance state by the falling edge of the frame-sync signal. The most significant data bit then appears on DOUT.

DOUT is placed in a high-impedance state on the sixteenth rising edge of SCLK (internal or external) after the falling edge of the frame-sync signal. In the primary communication, the data word is the ADC conversion result. In the secondary communication, the data is the register read results when requested by the read/write ($\text{R}/\overline{\text{W}}$) bit with the eight MSBs set to zero (see the serial communications section). When a register read is not requested, the secondary word is all zeroes.

2.2.4 Data In (DIN)

In the primary communication, the data word is the input digital signal to the DAC channel. In the secondary communication, the data is the control and configuration data to set up the device for a particular function (see Section 3 Serial Communications).

2.2.5 Hardware Program Terminal (FC)

This input provides for hardware programming requests for secondary communication. It works in conjunction with the control bit D00 of the secondary data word. The signal on FC is latched 1/2 shift clock after the rising edge of the next internally generated primary frame-sync interval. FC should be tied low when not being used (see Section 3.2 Secondary Serial Communication).

2.2.6 Frame-Sync

The frame-sync signal indicates that the device is ready to send and receive data. The data transfer from DOUT and into DIN begins on the falling edge of the frame-sync signal.

The frame sync is generated internally and goes low on the rising edge of SCLK and remains low during the 16-bit data transfer.

2.2.7 Multiplexed Analog Input

The two differential analog inputs (INP and INM or AUXP and AUXM) are multiplexed into the sigma-delta modulator. The performance of the AUX channel is similar to the normal input channel.

2.2.8 Analog Input

The signal applied to the terminals INM and INP should be differential to preserve the device specifications (see Figure 2-3). A single-ended input signal should always be converted to a differential input signal prior to being used by the TLC320AD55C. The signal source driving the analog inputs (INM, INP, AUXM, AUXP) should have a low source-impedance for lowest noise performance and accuracy.

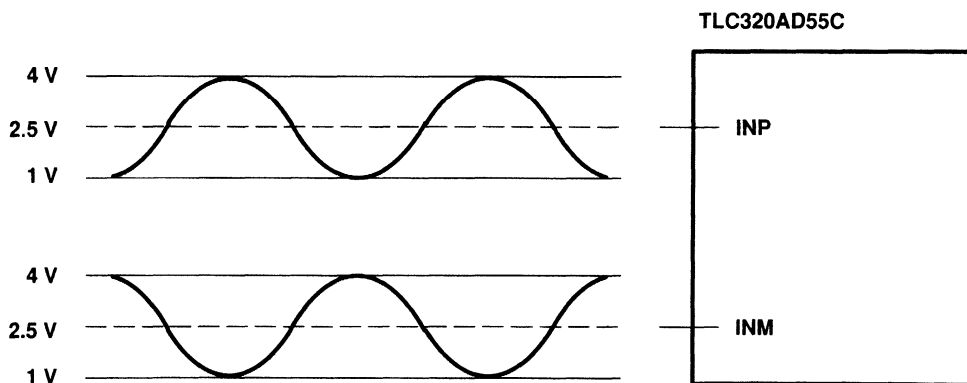


Figure 2-3. Differential Analog Input Configuration

3 Serial Communications

DOUT, DIN, SCLK, \overline{FS} , and FC are the serial communication signals. The digital output data from the ADC is taken from DOUT. The digital input data for the DAC is applied to DIN. The synchronizing clock for the serial communication data and the frame sync is taken from SCLK. The frame-synchronization pulse that encloses the ADC/DAC data transfer interval is taken from \overline{FS} . For signal (audio) data transmitted from the ADC or to the DAC, primary serial communication is used. To read or write words that control both the options and the circuit configurations of the device, secondary communication is used.

The purpose of the primary and secondary communications is to allow conversion data and control data to be transferred across the same serial port. A primary transfer is always dedicated to conversion data. A secondary transfer sets up and reads the register values described in Appendix A. A primary transfer occurs for every conversion period. A secondary transfer occurs only when requested. Two methods exist for requesting a secondary command. Terminal FC can request a secondary communication when it is asserted, or the LSB of the DAC data within a primary transfer can request a secondary communication. The selection of which method is enabled is provided in control 1 register (bit 0) as shown in Appendix A.

For all serial communications, the most significant bit is transferred first. For a 16-bit ADC word and a 16-bit DAC word, D15 is the most significant bit and D0 is the least significant bit. For a 15-bit DAC data word in the 16-bit primary communication, D15 is the most significant bit, D1 is the least significant bit, and D0 is used for the embedded function control. All digital data values are in 2s-complement format.

These logic signals are compatible with TTL-voltage levels and CMOS current levels.

3.1 Primary Serial Communication

Primary serial communication is used both to transmit and receive conversion signal data. The ADC word length is always 16 bits. The DAC word length depends on the status of D0 in the control 1 register. After power-up or reset, the device defaults to the 15-bit mode (not 16-bit mode). The DAC word length is 15 bits and the last bit of the primary 16-bit serial communication word is a function-control bit used to request secondary serial communications. In the 16-bit mode, all 16 bits of the primary communications word are used as data for the DAC and the hardware terminal FC must be used to request secondary communications.

Figure 3–1 shows the timing relationship for SCLK, \overline{FS} , DOUT and DIN in a primary communication. The timing sequence for this operation is as follows:

1. The TLC320AD55C takes \overline{FS} low.
2. One 16-bit word is transmitted from the ADC (DOUT) and one 16-bit word is received for the DAC (DIN).
3. The TLC320AD55C takes \overline{FS} high.

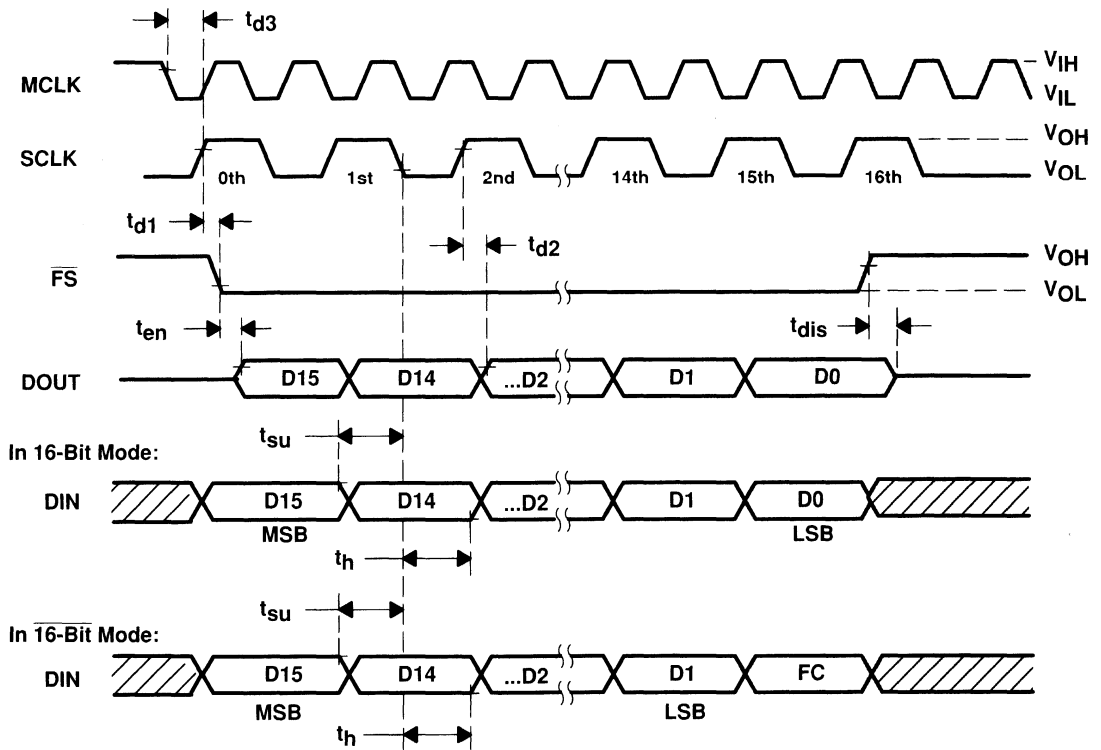


Figure 3–1. Primary Serial Communication Timing

When a secondary request is made through the LSB of the DAC data word ($\overline{16}$ -bit mode), the format shown in Figure 3–2 is used:

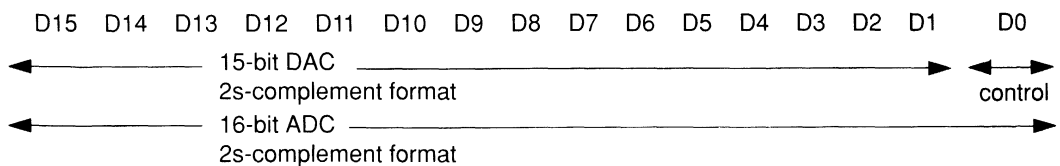


Figure 3–2. DAC and ADC Word Lengths

3.2 Secondary Serial Communication

Secondary serial communication reads or writes 16-bit words that program both the options and the circuit configurations of the device. All register programming occurs during secondary communications. Four primary and secondary communication cycles are required to program the four registers. When the default value for a particular register is desired, the user can omit addressing it during secondary communication. A no-op command addresses the no-op register (register 0), and no register programming takes place during this secondary communication.

There are two methods for initiating secondary communications (see Figure 3–3):

- 1) by asserting a high level on FC, or 2) by asserting the LSB of DIN 16-bit serial communication high while not in 16-bit mode (see control 1 register bit 0).

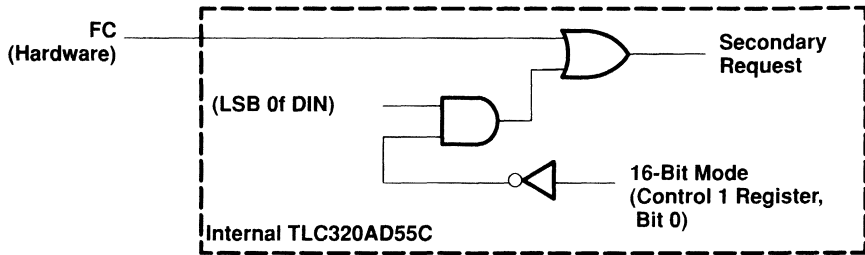


Figure 3–3. Hardware and Software Methods to Initiate a Secondary Request

1. Figures 3–5 and 3–6 show the two different methods by which FC requests secondary communication words as well as the timing for \overline{FS} , DOUT, DIN, and SCLK. The examples span two primary communication frames. Figure 3–5 shows the use of hardware function control.

During a secondary communication, a register can be written to or read from. When writing a value to a register, DIN contains the value to be written (see Figure 3–7). The data returned on DOUT is 00(hex). When performing a read function, DIN can still provide data to be written to an addressed register; however, DOUT contains the most recent value contained in the register addressed by DIN.

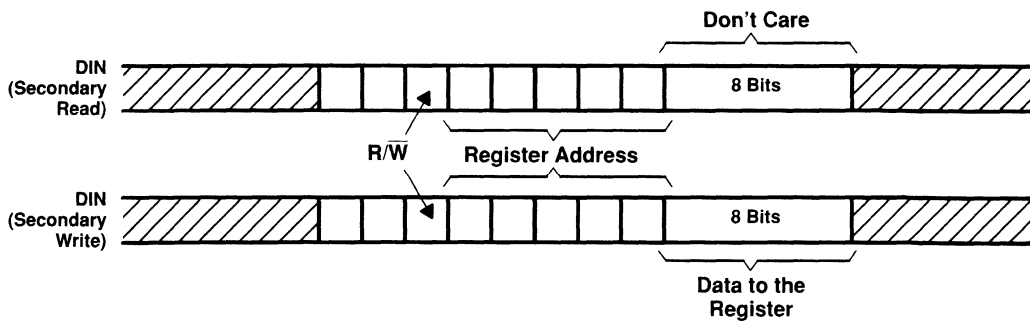


Figure 3–4. Secondary DIN Format

In Figure 3–5, FC clocks in and latches on the rising edge of frame sync (\overline{FS}). This causes the start of the secondary update 32 FCLKs (see Fk divide register, Appendix A) after the start of the primary communication frame. Read and write examples are shown for DIN and DOUT.

2. Figure 3–6 shows the use of software function control.

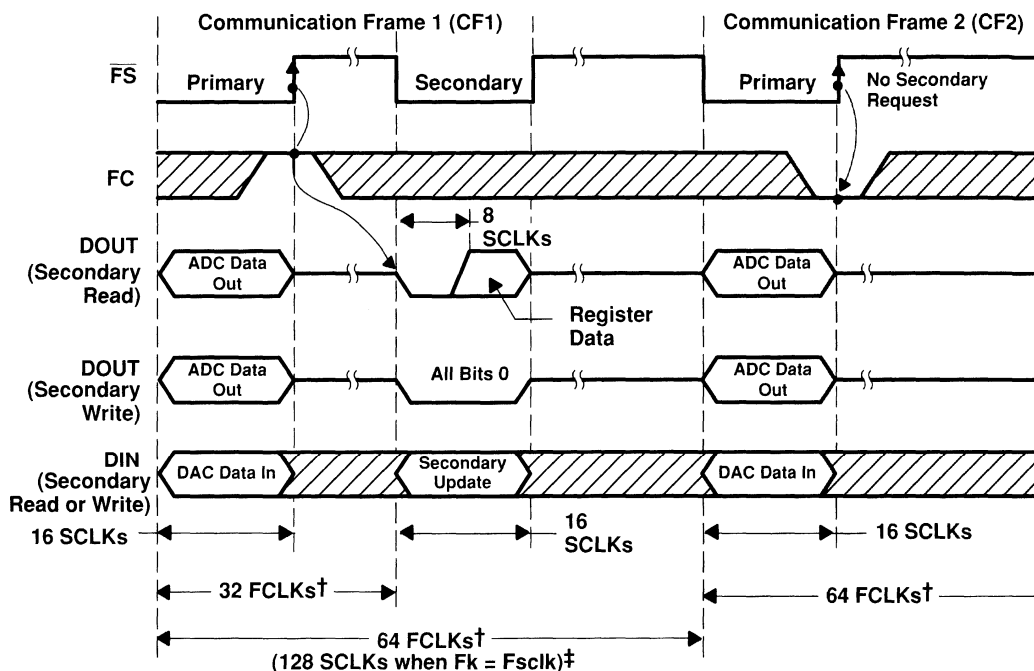
The software request for function control is typically used when the required resolution of the DAC channel is less than 16 bits. Then the least significant bit (D0) can be used for the secondary requests as shown in Table 3–1.

Table 3–1. Least-Significant-Bit Control Function

CONTROL BIT D0	CONTROL BIT FUNCTION
0	No operation (no-op)
1	Secondary communication request

On the falling edge of the next \overline{FS} , D15 through D1 is input to DIN or D15 through D0 is output to DOUT.

When a secondary communication request is made, \overline{FS} goes low for 32 FCLKs (see Fk divide register, Appendix A) after the beginning of the primary frame.

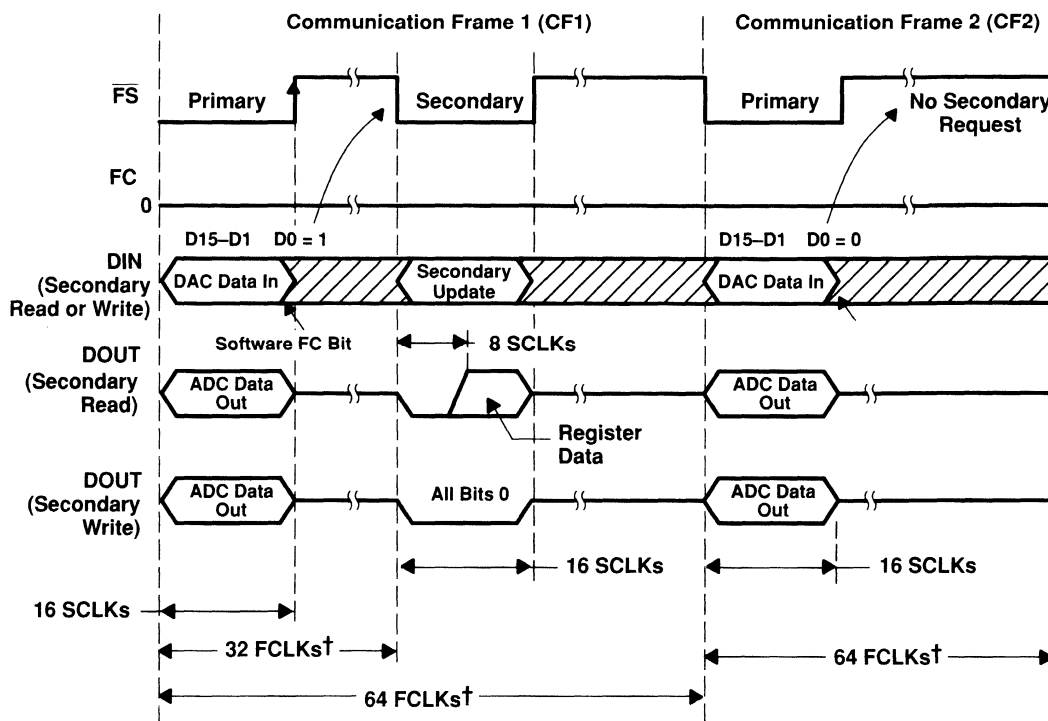


† See Fk divide register in Appendix A.

‡ For a selected MCLK, Fk and Fsclk: $SCLK = 2 Fk/Fsclk \times FCLK$

Figure 3–5. Hardware FC Secondary Request (Phone Mode Disabled)

In Figure 3–6, FC hardware terminal 15 is left in its nonasserted state (0). FC is asserted through software by embedding an asserted high level (1) in the LSB of the 16-bit primary word. This is possible when not in 16-bit mode (control 1 register bit 2 = 0) because the user is using only 15 bits of DAC information.



† See Fk divide register in Appendix A.

NOTE A: For a read cycle, the last 8 bits are don't care.

Figure 3–6. Software FC Secondary Request (Phone Mode Disabled)

Table 3–2 shows the secondary communications format. D13 is the R/W bit, the read/not-write bit.

D12 through D8 are address bits. The register map is specified in the register set section in Appendix A. D7 through D0 are data bits. The data bits are values for the specified register addressed by data bits D12 through D8.

Table 3–2. Secondary Communication Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	R/W	A	A	A	A	A	D	D	D	D	D	D	D	D

3.3 Conversion Rate Versus Serial Port

The SCLK frequency can be programmed independently from the FCLK frequency. This can create a problem with the interpretation of the serial port data. The serial port is designed to initiate a primary communication every 64 SCLKs. There must be an integer number of SCLKs ≥ 40 per sample period. Two examples follow to demonstrate the possible output of the serial port. SCLK must be fast enough to collect all data from each frame.

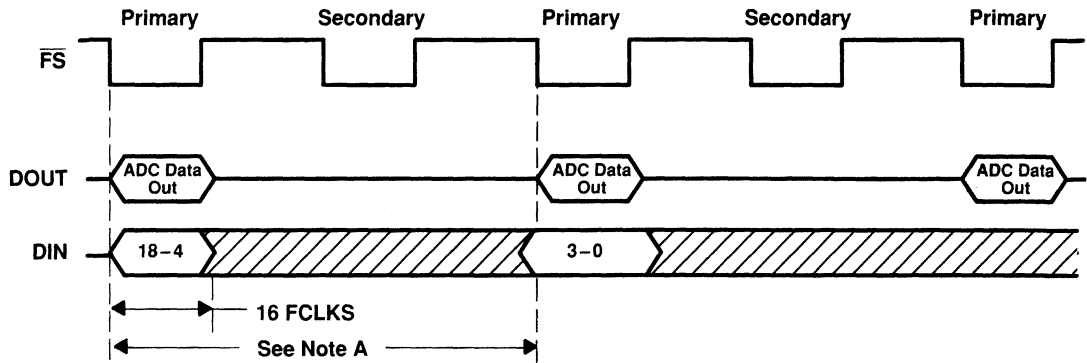
Example 1: $MCLK = 4.096 \text{ MHz}$, sample rate = 8 kHz, $8 \text{ kHz} = MCLK / (Fk \times 256)$, set $Fk = 2$, $SCLK = MCLK / (Fsclock \times 2)$, set $Fsclock = 2$, $SCLK = 1.024 \text{ MHz}$. With this configuration, $SCLK = \text{sample rate} \times 128$. Therefore, each primary communication is a valid sample.

Example 2: All variables above remain the same except $F_{sclk} = 1$, $SCLK = 2.048 \text{ MHz} = \text{sample rate} \times 256$. In this configuration, two consecutive primary communications represent the same data sample.

3.4 FIR Bypass Mode

An option is provided to bypass the FIR sections of the decimation filter and the interpolation filter. This is selected through the control 2 register. The sinc filters of the two paths cannot be bypassed.

The timing requirements for this mode of operation are shown in Figure 3–7.



NOTE A: The number of clocks between primary cycles is a function of FCLK. When either FIR is bypassed, this period is 16 FCLKs. See Fk divide register in Appendix A.

Figure 3–7. FIR Bypass Timing

3.5 Phone Mode Control

This function is provided for applications that need hardware control and monitor of external events. By allowing the device to drive two FLAG terminals (set through the control 2 register), the host digital signal processor (DSP) is capable of system control through the same serial port connection to the device. Along with this control is the capability for monitoring the value of the ALT DATA terminal during a secondary communication cycle. One application for this function is in monitoring ring detect or offhook detect from a phone answering system. The two FLAG terminals allow response to these incoming control signals. Figure 3–8 shows the timing associated with this operating mode.

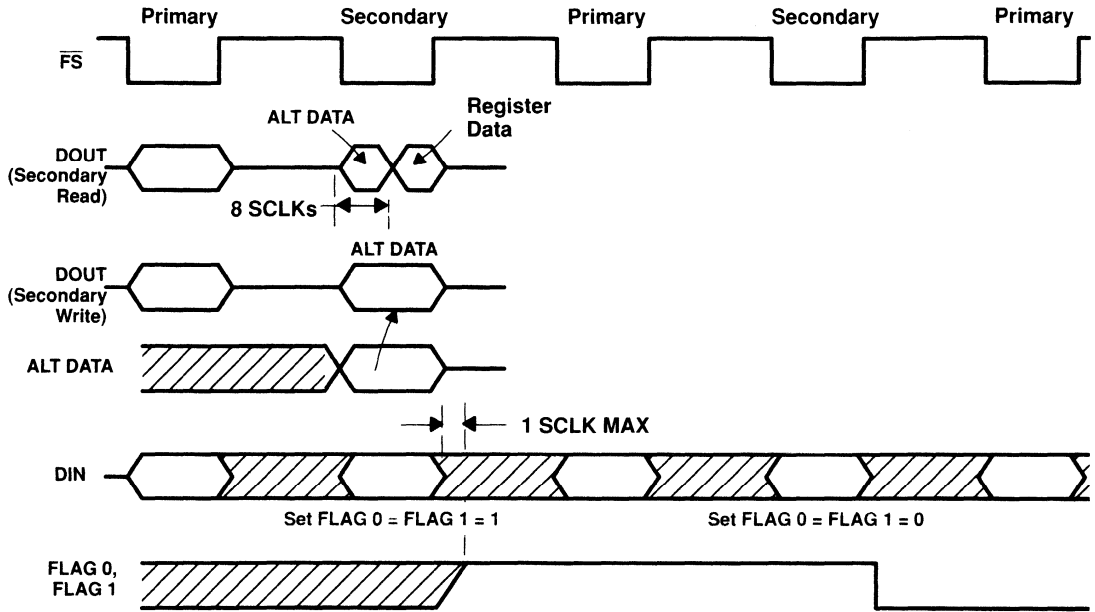


Figure 3–8. Phone Mode Timing

4 Specifications

4.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)[†]

Supply voltage range, DV_{DD} , $V_{DD}(\text{ADC, DAC})$ (see Note 1)	−0.3 V to 6.5 V
Output voltage range, $DOUT$, \overline{FS} , $SCLK$, $FLAG\ 0$, $FLAG\ 1$	−0.3 V to $DV_{DD} + 0.3$ V
Output voltage range, $OUTP$, $OUTM$	−0.3 V to $V_{DD} + 0.3$ V
Input voltage range, DIN , $PWRDWN$, $RESET$, $ALT\ DATA$, $MCLK$, FC	−0.3 V to $DV_{DD} + 0.3$ V
Input voltage range, INP , INM , $AUXP$, $AUXM$	−0.3 V to $V_{DD} + 0.3$ V
Case temperature for 10 seconds, T_C : DW package	260°C
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to $V_{SS}(\text{DAC})$ for DAC channel measurements and $V_{SS}(\text{ADC})$ for ADC channel measurements.

4.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{DD}(\text{ADC, DAC})$	4.5		5.5	V
Analog signal input voltage, V_I	Differential, (INP–INM) peak, for full scale operation		6	V
Load resistance for $OUTP$ and $OUTM$, R_L	0.3	10		k Ω
Load capacitance for $OUTP$ and $OUTM$, C_L			100	pF
ADC or DAC conversion rate (Nyquist)		8		kHz
Operating free-air temperature, T_A	0		70	°C

4.3 Recommended Operating Conditions, $DV_{DD} = 5$ V

	MIN	NOM	MAX	UNIT
Supply voltage, DV_{DD}	4.5		5.5	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
MCLK frequency (see Note 2), duty cycle = 50 ± 10%		16.384		MHz

NOTE 2: The default state for an 8 kHz conversion rate requires a 16.384 MHz MCLK frequency.

4.4 Electrical Characteristics, $T_A = 25^\circ\text{C}$, $V_{DD}(\text{ADC}) = V_{DD}(\text{DAC}) = DV_{DD} = 5\text{ V}$, $\text{MCLK} = 16.384\text{ MHz}$, $F_k = 8$ (unless otherwise noted)

4.4.1 Digital Inputs and Outputs, Outputs Not Loaded

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage, DOUT	$I_O = 360\ \mu\text{A}$	2.4	4.6		V
V_{OL} Low-level output voltage, DOUT	$I_O = 2\ \text{mA}$		0.2	0.4	V
I_{IH} High-level input current, any digital input	$V_{IH} = 5\ \text{V}$			10	μA
I_{IL} Low-level input current, any digital input	$V_{IL} = 0.8\ \text{V}$			10	μA
C_i Input capacitance			5		pF
C_o Output capacitance			5		pF

4.4.2 ADC Path Filter (see Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	20 Hz	-0.5	-0.15	0.2	dB
	200 Hz	-0.5	0.03	0.15	
	300 Hz to 3 kHz	-0.15	0	0.15	
	3.3 kHz	-0.35	-0.5	0.3	
	3.4 kHz	-1	-0.6	-0.1	
	4 kHz		-20	-14	
	$\geq 4.6\ \text{kHz}$			-40	

NOTE 3: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The analog input test signal is a sine wave with 0 dB = 6 $V_{I(PP)}$ as the reference level for the analog input signal. The passband is 0 to 3400 Hz.

4.4.3 ADC Dynamic Performance

4.4.3.1 ADC Signal-to-Noise (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio (SNR)	$V_I = -1\ \text{dB}$	80	85		dB
	$V_I = -9\ \text{dB}$	72	77		
	$V_I = -40\ \text{dB}$	40	45		
	$V_I = -65\ \text{dB}$	14	21		
	$V_{I(\text{AUXM}, \text{AUXP})} = -9\ \text{dB}$	72	78		

NOTE 4: The test condition is the digital equivalent of a 1020 Hz input signal with an 8 kHz conversion rate. The load impedance is 600 Ω . Input and output voltages are referred to $V_{DD}/2$.

4.4.3.2 ADC Signal-to-Distortion (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	$V_I = -1\ \text{dB}$	80	92		dB
	$V_I = -9\ \text{dB}$	80	94		
	$V_I = -40\ \text{dB}$	40	60		
	$V_I = -65\ \text{dB}$	15	40		
	$V_{I(\text{AUXM}, \text{AUXP})} = -9\ \text{dB}$	80	92		

NOTE 4: The test condition is the digital equivalent of a 1020 Hz input signal with an 8 kHz conversion rate. The load impedance is 600 Ω . Input and output voltages are referred to $V_{DD}/2$.

4.4.3.3 ADC Signal-to-Distortion+Noise (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total harmonic distortion+noise (THD+N)	$V_I = -9$ dB	80	83		dB
	$V_I = -1$ dB	72	76		
	$V_I = -40$ dB	40	45		
	$V_I = -65$ dB	14	20		
	$V_I(\text{AUXM, AUXP}) = -9$ dB	72	77		

NOTE 5: The test condition is a 1020 Hz input signal with an 8 kHz conversion rate. Input and output voltages are referred to $V_{DD}/2$.

4.4.4 ADC Channel

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic range			86		dB
Interchannel isolation		80			dB
Gain error	$V_I = -1$ dB at 1020 Hz			± 0.5	dB
Gain error, dc	INP = 3 V, INM = 2 V		± 0.6		dB
Off-set error, ADC converter			8		mV
CMRR Common-mode rejection ratio INM, INP or AUXM, AUXP	$V_I = 0$ dB at 1020 kHz	80			dB
Idle channel noise (on-chip reference)				50	$\mu\text{V rms}$
R_i Input resistance	$T_A = 25^\circ\text{C}$	70	100		$\text{k}\Omega$

4.4.5 DAC Path Filter (see Note 6)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	20 Hz	-0.5	0.08	0.15	dB
	200 Hz	-0.5	0.08	0.15	
	300 Hz to 3 kHz	-0.15	0.08	0.15	
	3.3 kHz	-0.35	0.11	0.3	
	3.4 kHz	-1	-0.48	-0.1	
	4 kHz		-20	-14	
	≥ 4.6 kHz			-40	

NOTE 6: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The nominal differential DAC channel peak-to-peak output voltage with this input condition is 6 V. The pass band is 0 to 3600 Hz.

4.4.6 DAC Dynamic Performance

4.4.6.1 DAC Signal-to-Noise (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio (SNR)	$V_O = 0$ dB	74	80		dB
	$V_O = -9$ dB	70	74		
	$V_O = -40$ dB	38	44		
	$V_O = -65$ dB	14	18		

NOTE 4: The test condition is the digital equivalent of a 1020 Hz input signal with an 8 kHz conversion rate. The load impedance is 600 Ω . Input and output voltages are referred to $V_{DD}/2$.

4.4.6.2 DAC Signal-to-Distortion (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	$V_O = 0$ dB	74	84		dB
	$V_O = -9$ dB	74	84		
	$V_O = -40$ dB	40	58		
	$V_O = -65$ dB	18	30		

NOTE 4: The test condition is the digital equivalent of a 1020 Hz input signal with an 8 kHz conversion rate. The load impedance is 600 Ω . Input and output voltages are referred to $V_{DD}/2$.

4.4.6.3 DAC Signal-to-Distortion + Noise (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total harmonic distortion+noise (THD+N)	$V_O = 0$ dB	72	78		dB
	$V_O = -9$ dB	68	74		
	$V_O = -40$ dB	38	44		
	$V_O = -65$ dB	14	20		

NOTE 4: The test condition is the digital equivalent of a 1020 Hz input signal with an 8 kHz conversion rate. The load impedance is 600 Ω . Input and output voltages are referred to $V_{DD}/2$.

4.4.7 DAC Channel

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic range			80		dB
Interchannel isolation		80			dB
Gain error, 0 dB	$V_O = 0$ dB at 1020 Hz			± 0.5	dB
Gain error, dc	Digital input offset = 1 V dc		± 0.2		dB
Idle channel broad-band noise	See Note 7			100	μ V rms
Idle channel narrow-band noise	0 – 4 kHz, See Note 7			40	μ V rms
V_{OO} Output offset voltage at OUT (differential)	DIN = All 0s		8		mV
V_O Analog output voltage, peak-to-peak, OUTP–OUTM (differential)	$R_L = 600$, With internal reference and full-scale digital input, (see Note 8)			6	V

NOTES: 7. The conversion rate is 8 kHz; the out-of-band measurement is made from 4800 Hz to $F_{MCLK}/2$.

8. The digital input to the DAC channel at DIN is in 2s complement.

4.4.8 Power Supplies, $V_{DD}(ADC) = V_{DD}(DAC) = DV_{DD} = 5\text{ V}$, No Load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{DD} (ADC)	Power supply current, ADC	Operating		12	20	mA
		Power-down		400		μA
I _{DD} (DAC)	Power supply current, DAC	Operating		16	24	mA
		Power-down		2.5		mA
I _{DD} (Digital)	Power supply current, digital	Operating		2	6	mA
		Power-down		300		μA
P _D	Power dissipation	Operating		150	250	mW
		Power-down		16	30	

4.4.9 Timing Requirements (see Notes 9 and 10)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{d1}	Delay time, SCLK↑ to \overline{FS} ↓	C _L = 20 pF		10	15	ns
t _{d2}	Delay time, SCLK↑ to DOUT			6	20	
t _{su}	Setup time, DIN before SCLK↓			20		
t _h	Hold time, DIN after SCLK↓				20	
t _{en}	Enable time, \overline{FS} ↓ to DOUT			10	25	
t _{dis}	Disable time, \overline{FS} ↑ to DOUT Hi-Z			20		
t _{d3}	Delay time MCLK↓ to SCLK↑			25	50	

NOTES: 9. Refer to Figure 3–1 for timing diagram.

10. When \overline{FS} occurs after SCLK, it shortens the MSB (D15) duration.

5 Application Information

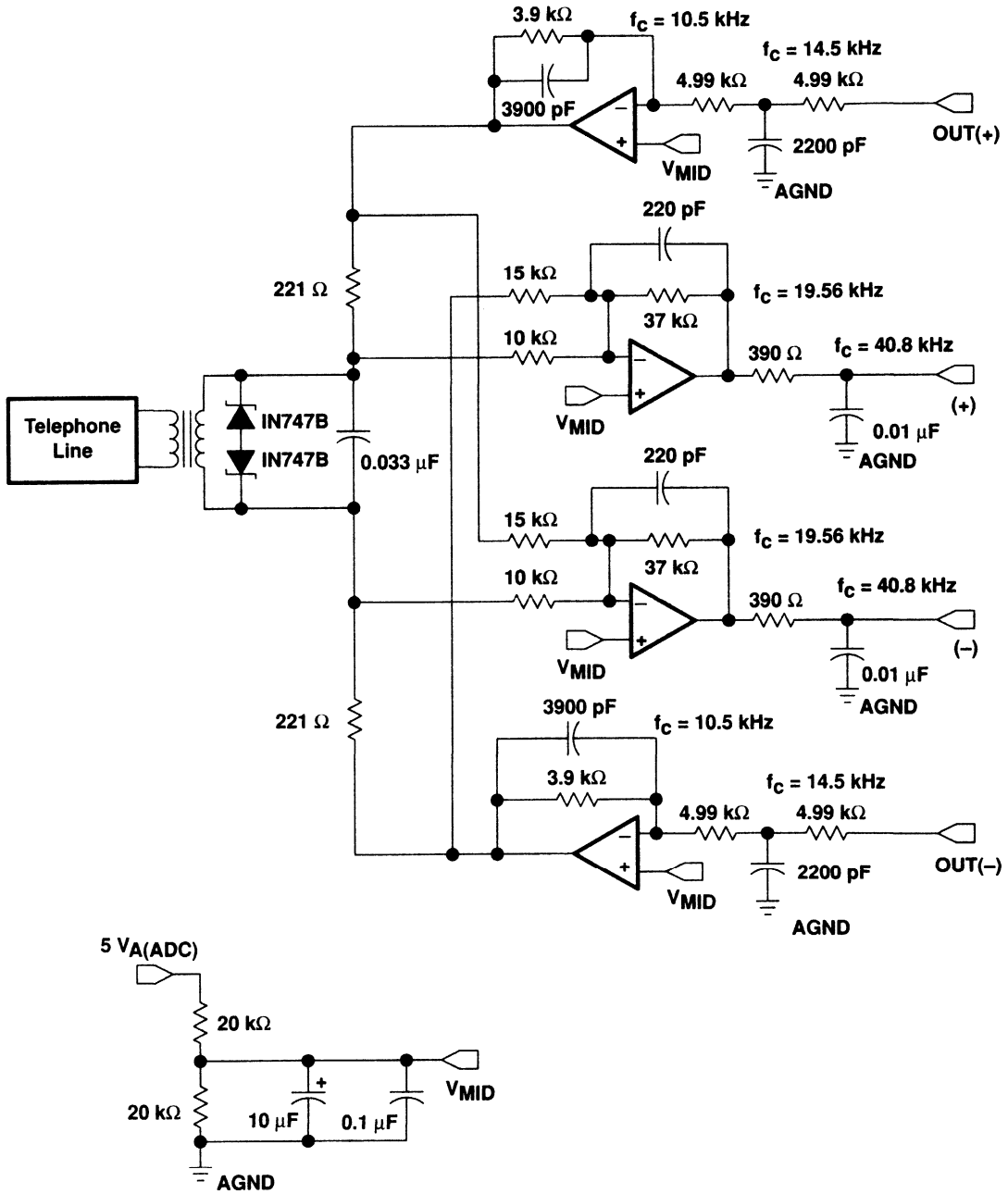


Figure 5-1. TLC320AD55C Application Schematic

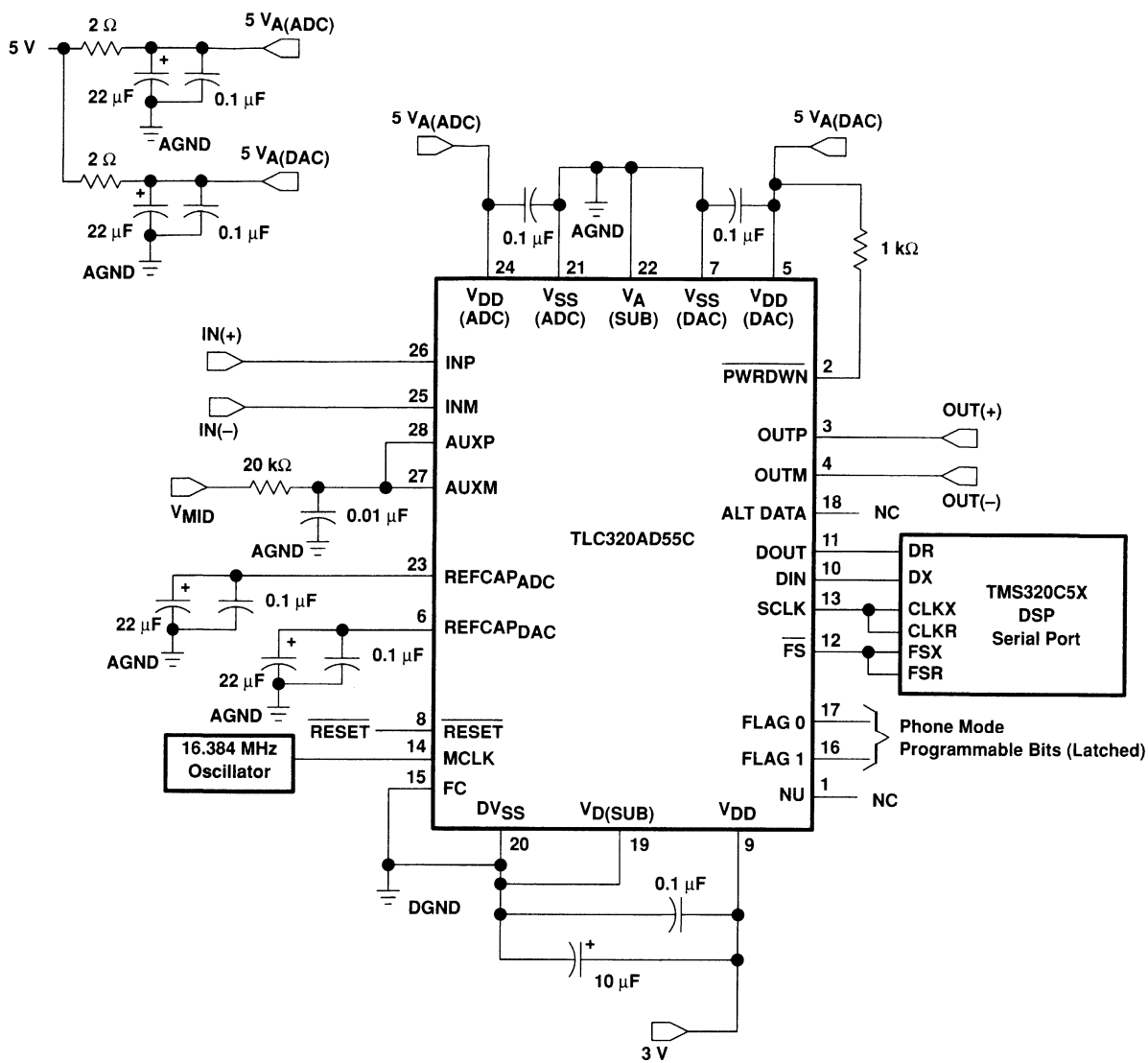


Figure 5-2. TLC320AD55C I/O Buffer and V_{MID} Generator Schematic

Appendix A Register Set

Data bits D12 through D8 in the secondary serial communication contain the address of the register, and data bits D7 through D0 contain the data that is to be written to the register. Data bit D13 determines a read or write cycle to the addressed register. When data bit D13 is low, a write cycle is selected.

The following table shows the register map:

Table A–1. Register Map

REGISTER NO.	D15	D14	D13	D12	D11	D10	D9	D8	REGISTER NAME
0	0	0	0	0	0	0	0	0	No operation
1	0	0	0	0	0	0	0	1	Control 1
2	0	0	0	0	0	0	1	0	Control 2
3	0	0	0	0	0	0	1	1	Fk divide
4	0	0	0	0	0	1	0	0	Fsclk divide
5	0	0	0	0	0	1	0	1	Control 3

Table A–2. Control 1 Register

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	–	–	–	–	–	–	–	Software reset
0	–	–	–	–	–	–	–	Software reset not asserted
–	1	–	–	–	–	–	–	Software power down (analog and filters)
–	0	–	–	–	–	–	–	Software power down (not asserted)
–	–	1	–	–	–	–	–	Select AUXP and AUXM
–	–	0	–	–	–	–	–	Select INP and INM
–	–	–	0	0	–	–	–	Analog output gain = 1
–	–	–	0	1	–	–	–	Analog output gain = 1/2
–	–	–	1	0	–	–	–	Analog output gain = 1/4
–	–	–	1	1	–	–	–	Analog output gain = 0 (squelch)
–	–	–	–	–	1	–	–	Analog loopback asserted
–	–	–	–	–	0	–	–	Analog loopback not asserted
–	–	–	–	–	–	1	–	Digital loopback asserted
–	–	–	–	–	–	0	–	Digital loopback not asserted
–	–	–	–	–	–	–	1	16-bit mode (hardware secondary requests)
–	–	–	–	–	–	–	0	Not 16-bit mode (software secondary requests)

Default register value: 00000000

The software reset is a one-shot operation and this bit is cleared to zero after reset. It is not necessary to write a zero to end the master reset operation.

Table A-3. Control 2 Register

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
X	X	-	-	-	-	-	-	Reserved
-	-	X	-	-	-	-	-	Decimator FIR overflow flag (valid only during read cycle)
-	-	-	X	-	-	-	-	FLAG 1 output value
-	-	-	-	X	-	-	-	FLAG 0 output value
-	-	-	-	-	1	-	-	Phone mode enabled
-	-	-	-	-	0	-	-	Phone mode disabled
-	-	-	-	-	-	0	-	Normal operation with decimator FIR filter
-	-	-	-	-	-	1	-	Bypass decimator FIR filter
-	-	-	-	-	-	-	0	Normal operation with interpolator filter
-	-	-	-	-	-	-	1	Bypass interpolator FIR filter

Default register value: 00000000

Writing zeros to the reserved bits is suggested.

Table A-4. Fk Divide Register

D7	D6	D5	D4	D3	D2	D1	D0	DIVIDE VALUE
1	1	1	1	1	1	1	1	255
			•			•		
			•			•		
			•			•		
1	0	0	0	0	0	0	0	128
			•			•		
			•			•		
			•			•		
0	0	1	0	0	0	0	0	32
			•			•		
			•			•		
			•			•		
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	256

Default register value: 00001000

The oversampling clock (FCLK) is set as $MCLK/(Fk \times 4)$. $MCLK/(Fk \times 256)$ is the sample frequency (conversion rate) for the converter. When Fk is programmed to zero, its value is interpreted as 256.

Table A-5. Fsclk Divide Register

D7	D6	D5	D4	D3	D2	D1	D0	DIVIDE VALUE
1	1	1	1	1	1	1	1	255
		•				•		
		•				•		
		•				•		
1	0	0	0	0	0	0	0	128
		•				•		
		•				•		
		•				•		
0	0	1	0	0	0	0	0	32
		•				•		
		•				•		
		•				•		
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	256

Default register value: 00001000

SCLK is set by $MCLK/(2 \times F_{sclk})$. SCLK is for the serial transfer of data to and from the TLC320AD55C. When Fsclk is programmed to zero, its value is interpreted as 256.

Table A-6. Control 3 Register

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
0	0	0	0	1	0	0	0	DAC reference disabled
0	0	0	0	0	0	0	0	DAC reference enabled

TLC320AD56C ***Data Manual***

Sigma-Delta Analog Interface Circuit

SLAS101A
September 1996



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Contents

<i>Section</i>	<i>Title</i>	<i>Page</i>
1	Introduction	4-461
1.1	Features	4-461
1.2	Functional Block Diagram	4-462
1.3	Terminal Assignments	4-463
1.4	Ordering Information	4-464
1.5	Terminal Functions	4-465
1.6	Definitions and Terminology	4-466
1.7	Register Functional Summary	4-467
2	Functional Description	4-469
2.1	Device Functions	4-469
2.1.1	Operating Frequencies	4-469
2.1.2	ADC Signal Channel	4-469
2.1.3	DAC Signal Channel	4-469
2.1.4	Serial Interface	4-469
2.1.5	Register Programming	4-469
2.1.6	Sigma-Delta ADC	4-470
2.1.7	Decimation Filter	4-470
2.1.8	Sigma-Delta DAC	4-470
2.1.9	Interpolation Filter	4-470
2.1.10	Digital Loopback	4-470
2.1.11	FIR Overflow Flag	4-470
2.2	Terminal Functions	4-470
2.2.1	Reset and Power-Down Functions	4-470
2.2.2	Master Clock Circuit	4-471
2.2.3	Data Out (DOUT)	4-471
2.2.4	Data In (DIN)	4-471
2.2.5	Hardware Program Terminal (FC)	4-471
2.2.6	Frame-Sync Function	4-472
2.2.7	Multiplexed Analog Input	4-472
2.2.8	Analog Input	4-472
2.2.9	Analog Output	4-472
3	Serial Communications	4-475
3.1	Primary Serial Communication	4-475
3.2	Secondary Serial Communication	4-477
3.3	Conversion Rate vs Serial Port	4-480
3.4	Phone Mode Control	4-480
4	Specifications	4-481
4.1	Absolute Maximum Ratings Over Operating Free-Air Temperature Range	4-481
4.2	Recommended Operating Conditions	4-481
4.2.1	Recommended Operating Conditions, $DV_{DD} = 5\text{ V}$, $AV_{DD} = 5\text{ V}$...	4-481
4.2.2	Recommended Operating Conditions, $DV_{DD} = 3\text{ V}$, $AV_{DD} = 5\text{ V}$...	4-481

Contents (Continued)

<i>Section</i>	<i>Title</i>	<i>Page</i>
4.3	Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, $DV_{DD} = 5\text{ V}$, $AV_{DD} = 5\text{ V}$	4-482
4.3.1	Digital Inputs and Outputs, $MCLK = 4.096\text{ MHz}$, $f_s = 8\text{ kHz}$, Outputs Not Loaded	4-482
4.3.2	Digital Inputs and Outputs, $MCLK = 4.096\text{ MHz}$, $f_s = 8\text{ kHz}$, Outputs Not Loaded, $DV_{DD} = 3\text{ V}$	4-482
4.3.3	ADC Path Filter, $MCLK = 4.096\text{ MHz}$, $f_s = 8\text{ kHz}$	4-482
4.3.4	ADC Dynamic Performance, $MCLK = 4.096\text{ MHz}$, $f_s = 8\text{ kHz}$	4-482
4.3.5	ADC Channel	4-484
4.3.6	DAC Path Filter, $MCLK = 8.192\text{ MHz}$, $f_s = 8\text{ kHz}$	4-484
4.3.7	DAC Dynamic Performance, $DV_{DD} = 5\text{ V}$ or 3 V	4-485
4.3.8	DAC Channel, $DV_{DD} = 5\text{ V}$ or 3 V	4-486
4.3.9	Power Supplies, No Load	4-486
4.3.10	Power-Supply Rejection	4-487
4.3.11	Timing Requirements	4-487
5	Application Information	4-491
Appendix A	Register Set	4-493

List of Illustrations

<i>Figure</i>	<i>Title</i>	<i>Page</i>
1-1.	Functional Block Diagram	4-462
1-2.	Terminal Assignments	4-463
1-3.	Terminal Assignments	4-464
2-1.	Internal Power-Down Logic	4-472
2-2.	Differential Analog-Input Configuration	4-473
3-1.	Primary Serial Communication Timing	4-476
3-2.	Hardware and Software Ways to Make a Secondary Request	4-477
3-3.	Hardware FC Secondary Request (Phone Mode Disabled)	4-478
3-4.	Software FC Secondary Request (Phone Mode Disabled)	4-479
3-5.	Phone Mode Timing	4-480
3-6.	Secondary DIN Format	4-480
4-1.	ADC Decimation Filter Response	4-488
4-2.	ADC Decimation Filter Passband Ripple	4-488
4-3.	DAC Interpolation Filter Response	4-489
4-4.	DAC Interpolation Passband Ripple	4-489
5-1.	Application Schematic For Single-Ended Input/Output	4-491
5-2.	Application Schematic For Differential Input/Output	4-492

List of Tables

<i>Table</i>	<i>Title</i>	<i>Page</i>
3-1.	Secondary Request Format	4-476
3-2.	Least Significant Bit Control Function	4-477
3-3.	Secondary Communication Data Format	4-479

1 Introduction

The TLC320AD56C provides high resolution low-speed signal conversion from digital-to-analog (D/A) and from analog-to-digital (A/D) using oversampling sigma-delta technology. This device consists of two serial synchronous conversion paths (one for each data direction) and includes an interpolation filter before the digital-to-analog converter (DAC) and a decimation filter after the analog-digital-converter (ADC) (see Figure 1–1). Other overhead functions provide on-chip timing and control. The sigma-delta architecture produces high resolution A/D and D/A conversion at low system speeds and low cost.

The options and the circuit configurations of this device can be programmed through the serial interface. The options include reset, power-down, communications protocol, serial clock rate, and test mode as outlined in Appendix A. The TLC320AD56C is characterized for operation from 0°C to 70°C.

1.1 Features

The TLC320AD56C includes the following features:

- Single 5-V power supply voltage or 5 V analog and 3 V digital supply voltages
- Power dissipation (P_D) of 150 mW maximum in the operating mode
- Power-down mode to 2.5 mW typical
- General-purpose 16-bit signal processing
- 2's-complement data format
- Typical dynamic range of 85 dB for the DAC and 87 dB for the ADC
- Minimum 79-dB total signal-to-(noise + distortion) for the ADC
- Minimum 80-dB total signal-to-(noise + distortion) for the DAC
- Differential architecture throughout the device
- Internal reference voltage (V_{ref})
- Internal 64X oversampling
- Serial port interface
- Phone-mode output control
- System test mode, digital loopback test mode
- Capable of supporting all V.34 sample rates by varying MCLK frequency
- Supports business audio applications
- Variable conversion rate selected as $MCLK/512$

1.2 Functional Block Diagram

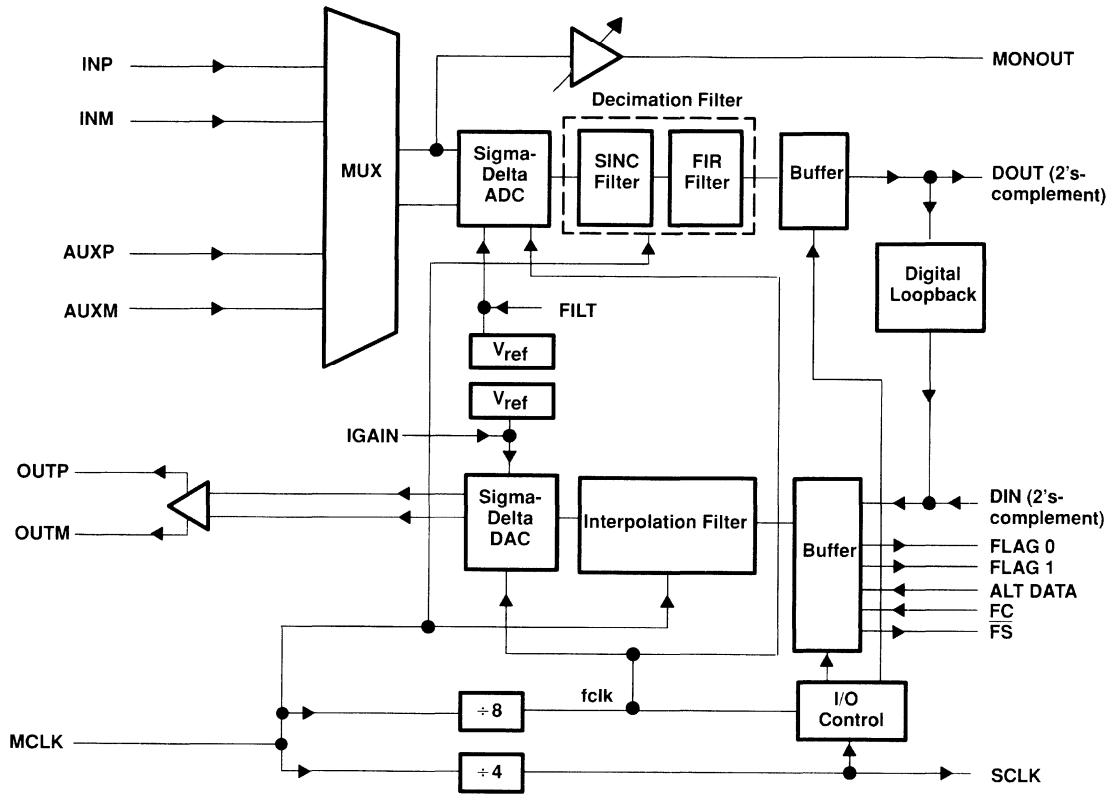
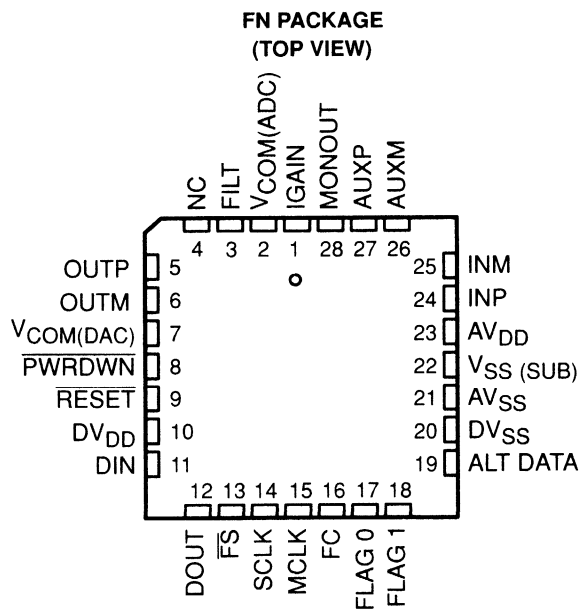


Figure 1-1. Functional Block Diagram

1.3 Terminal Assignments



NC – No internal connection

Figure 1–2. Terminal Assignments

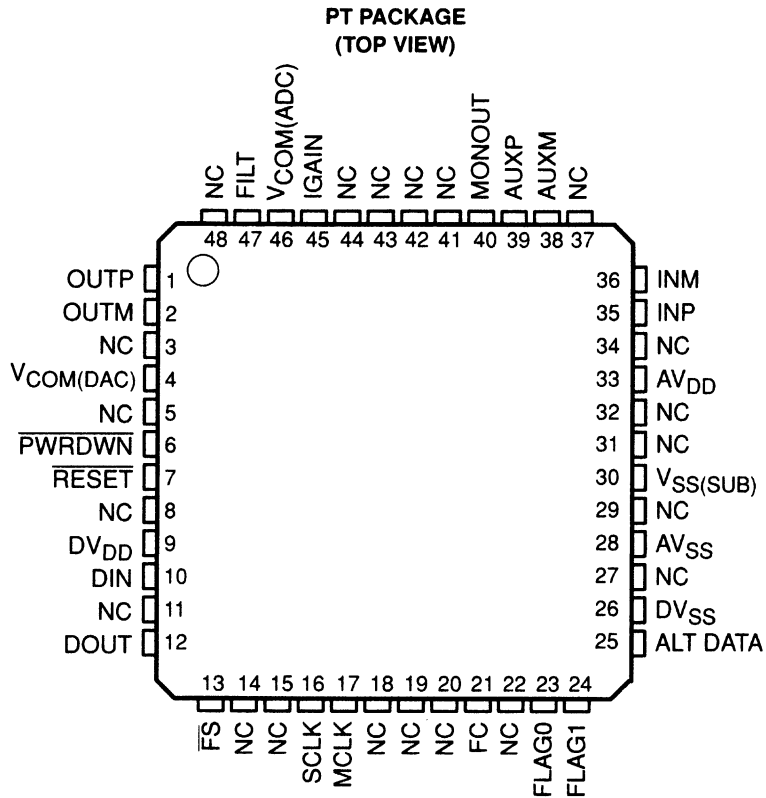


Figure 1–3. Terminal Assignments

1.4 Ordering Information

T _A	PACKAGE	
	CHIP CARRIER (FN)	QUAD FLAT PACK (PT)
0°C to 70°C	TLC320AD56CFN	TLC320AD56CPT

1.5 Terminal Functions

TERMINALS			I/O	DESCRIPTION
NAME	NUMBER			
	PT	FN		
ALT DATA	25	19	I	Signals on this terminal are routed to DOUT during secondary communication if phone mode is enabled.
AUXM	38	26	I	Inverting input to auxiliary analog input. AUXM requires an external RC antialias filter.
AUXP	39	27	I	Noninverting input to auxiliary analog input. Requires an external RC antialias filter.
AVDD	33	23	I	Analog ADC path supply (5 V only)
DIN	10	11	I	Data input. DIN receives the DAC input data and command information from the DSP and is synchronized to SCLK.
DOUT	12	12	O	Data output. DOUT transmits the ADC output bits and is synchronized to SCLK. This terminal is at high-Z when \overline{FS} is not activated.
DVDD	9	10	I	Digital power supply (5 V or 3 V)
DVSS	26	20	I	Digital ground
FC	21	16	I	Function code. FC is sampled and latched on the rising edge of \overline{FS} for the primary serial communication. Refer to the Serial Communications section for more details.
FLAG 0	23	17	O	Output flag 0. During phone mode, FLAG 0 contains the value set in Control 2 register.
FLAG 1	24	18	O	Output flag 1. During phone mode, FLAG 1 contains the value set in Control 2 register.
FILT	47	3	O	Bandgap filter. FILT is provided for decoupling of the bandgap reference, and provides 2.5 V to which the analog inputs or outputs can be referenced. The optimal capacitor value is 0.1 μ F (ceramic). This voltage node should be loaded only with a high-impedance dc load.
\overline{FS}	13	13	O	Frame sync. When \overline{FS} goes low, the serial communication port is activated. In all serial transmission modes, \overline{FS} is held low during bit transmission. Refer to section 3 <i>Serial Communications</i> for detailed description.
INM	36	25	I	Inverting input to analog modulator. INM requires an external RC antialias filter.
INP	35	24	I	Noninverting input to analog modulator. INP requires an external RC antialias filter.
IGAIN	45	1	O	Current gain reference scaling. IGAIN is provided for decoupling of the current gain reference and provides a 1.35-V reference. The optimal load is a 27-K resistor.
MCLK	17	15	I	Master clock. The master clock derives the internal clocks of the sigma-delta analog interface circuit.
MONOUT	40	28	O	Monitor output. MONOUT allows for monitoring of the analog input and is a high-impedance output. The gain or mute is selected using Control 2 register.
OUTM	2	6	O	Inverting current output of the DAC. OUTM is functionally identical with and complementary to OUTP. OUTM and OUTP current outputs can be loaded with 5 k Ω differentially or single-ended. This signal can also be used alone for single-ended operation.

NOTE 1: All digital inputs and outputs are TTL-compatible, unless otherwise noted for DVDD = 5 V.

1.5 Terminal Functions (Continued)

TERMINALS			I/O	DESCRIPTION
NAME	NUMBER			
	PT	FN		
OUTP	1	5	O	Noninverting current output of the DAC. OUTM and OUTP current outputs can be loaded with 5 k Ω differentially or single ended. This signal can also be used alone for single-ended operation.
PWRDWN	6	8	I	Power down. When this terminal is pulled low, the device goes into a power-down mode; the serial interface is disabled and most of the high-speed clocks are disabled. However, all the register values are sustained and the device resumes full power operation without reinitialization when this terminal is pulled high again. PWRDWN resets the counters only and preserves the programmed register contents. See subsection 2.21. <i>Reset and Power-Down Functions</i> .
RESET	7	9	I	Reset. The reset function is provided to initialize all the internal registers to their default values. The serial port can be configured to the default state accordingly. Refer to section 1.7 <i>Register Functional Summary</i> and subsection 2.2.1 <i>Reset and Power-Down Functions</i> for more detailed descriptions.
SCLK	16	14	O	Shift clock. The shift clock signal is derived from MCLK and is used to clock serial data into DIN and out of DOUT.
V _{SS(SUB)}	30	22	I	Analog substrate. This terminal must be grounded.
V _{COM(ADC)}	46	2	O	Common mode filter. This terminal is provided for decoupling of the common mode reference and provides a 2.5 V reference. The optimal capacitor value is 0.10 μ F. This node should be loaded only with a high-impedance dc load.
V _{COM(DAC)}	4	7	O	Common mode filter. This terminal is provided for decoupling of the common mode reference and provides a 2.5 V reference. The optimal capacitor value is 0.10 μ F. This node should be loaded only with a high-impedance dc load.
AV _{SS}	28	21	I	Analog ground

NOTE 1: All digital inputs and outputs are TTL-compatible, unless otherwise noted for DV_{DD} = 5 V.

1.6 Definitions and Terminology

Data Transfer Interval This is time during which data is transferred from DOUT and to DIN. This interval is 16 shift clocks and this data transfer is initiated by the falling edge of the frame-sync signal.

Signal Data This refers to the input signal and all of the converted representations through the ADC channel and return through the DAC channel to the analog output. This is contrasted with the purely digital software control data.

Primary Communications This refers to the digital data transfer interval. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.

Secondary Communications This refers to the digital control and configuration data transfer interval into DIN and the register read data cycle from DOUT. The data transfer interval occurs when requested by hardware or software.

Frame Sync Frame sync refers only to the falling edge of the signal that initiates the data transfer interval. The primary frame sync starts the primary communications, and the secondary frame sync starts the secondary communications.

Frame Sync and Sampling Period	The time between the falling edges of successive primary frame-sync signals.
f_s	The sampling frequency that is the reciprocal of the sampling period.
Frame-Sync Interval	The time period occupied by 16 shift clocks. It goes high on the sixteenth rising edge of SCLK after the falling edge of the frame sync.
ADC Channel	This term refers to all signal processing circuits between the analog input and the digital conversion results at DOUT.
DAC Channel	This term refers to all signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUTP and OUTM.
Host	Any processing system that interfaces to DIN, DOUT, SCLK, or \overline{FS} .
Dxx	Bit position in the primary data word (xx is the bit number).
DSxx	Bit position in the secondary data word (xx is the bit number).
d	The alpha character d represents valid programmed or default data in the control register format (see section 3.2 <i>Secondary Serial Communications</i>) when discussing other data bit portions of the register.
X	The alpha character X represents a do-not-care bit position within the control register format.
FIR	Finite duration impulse response.

1.7 Register Functional Summary

There are three data and control registers that are used as follows:

Register 0 The No-Op register. The 0 address allows secondary requests without altering any other register.

Register 1 The Control 1 register. The data in this register controls:

- The software reset
- The software power down
- Selection of the normal or auxiliary analog inputs
- Selection of the digital loopback
- 16-bit or 15-bit mode of operation
- Selection of monitor amp output

Register 2 The Control 2 register. The data in this register:

- Contains the output flag indicating a decimator FIR filter overflow
- Contains Flag 0 and Flag 1 output values for use in the phone mode
- Selects the phone mode

2 Functional Description

2.1 Device Functions

The functions of the TLC320AD56C are described in the following sections.

2.1.1 Operating Frequencies

The sampling (conversion) frequency is derived from the master clock (MCLK) input by equation 1.

$$f_s = \text{Sampling (conversion) frequency} = \frac{\text{MCLK}}{512} \quad (1)$$

The inverse is the time between the falling edges of two successive primary frame synchronization signals and is the conversion period.

2.1.2 ADC Signal Channel

To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data.

The input signal is filtered and applied to the ADC input. The ADC converts the signal into discrete output digital words in 2s-complement format, corresponding to the analog signal value at the sampling time. These 16-bit digital words, representing sampled values of the analog input signal, are clocked out of the serial port during the frame-sync interval, (DOUT), one word for each primary communication interval. During secondary communications, the data previously programmed into the registers can be read out with the appropriate register address, and the read bit set to 1. When no register read is requested, all 16 bits are 0 in the secondary word.

2.1.3 DAC Signal Channel

DIN receives the 16-bit serial data word (2's complement) from the host during the primary communications interval and latches the data on the seventeenth rising edge of SCLK. The data are converted to an analog current by the sigma-delta DAC comprised of a digital interpolation filter, and a digital 1-bit modulator. The DACs differential outputs OOUTP and OOUTM are a current output-type, (which requires resistive loading 5k Ω maximum). These outputs are then connected to the external low pass filter, as shown in the application schematics in Figure 3–7 and Figure 3–8 to complete the signal reconstruction. This filter can be incorporated in the data access arrangement (DAA) for modem applications.

2.1.4 Serial Interface

The digital serial interface consists of the shift clock, the frame synchronization signal, the ADC-channel data output, and the DAC-channel data input. During the primary 16-bit frame synchronization interval, the SCLK transfers the ADC channel results from DOUT and transfers 16-bit DAC data into DIN.

During the secondary frame synchronization interval, the SCLK transfers the register read data from DOUT when the read bit is set to a 1. In addition, the SCLK transfers control and device parameter information into DIN. The functional sequence is shown in Figure 3–1.

2.1.5 Register Programming

All register programming occurs during secondary communications, and data is latched and valid on the rising edge of the frame-sync signal. When the default value for a particular register is desired, that register does not need to be addressed during the secondary communications. The no-op command addresses the pseudo-register (register 0), and no register programming takes place during this communications.

DOUT is released from the high-impedance state on the falling edge of the primary or secondary frame-sync interval. In addition, each register can be read back during DOUT secondary communications by setting the read bit D13 to 1 in the appropriate register. When the register is in the read mode, no data can be written to the register during this cycle. To return this register to the write mode requires a subsequent secondary communication.

2.1.6 Sigma-Delta ADC

The sigma-delta ADC is a fourth-order sigma-delta modulator with 64 times oversampling. The ADC provides high resolution and low noise performance using oversampling techniques.

2.1.7 Decimation Filter

The decimation filter reduces the digital data rate to the sampling rate. This is accomplished by decimating with a ratio of 1:64. The output of this filter is a sixteen-bit 2's-complement data word clocking at the sample rate selected.

NOTE

The sample rate is determined through a relationship of $MCLK/512$.

2.1.8 Sigma-Delta DAC

The sigma-delta DAC is a fourth-order sigma-delta modulator with 64 times oversampling. The DAC provides high-resolution, low-noise performance from a 1-bit converter using oversampling techniques. The TLC320AD56C is a current-output DAC and requires a load resistor for current-to-voltage conversion (see Figures 3–7 and 3–8).

2.1.9 Interpolation Filter

The interpolation filter resamples the digital data at a rate of 64 times the incoming sample rate. The high-speed data output from this filter is then used in the sigma-delta DAC.

2.1.10 Digital Loopback

The digital loopback provides a means of testing the ADC/DAC channels and can be used for in-circuit system-level tests. The loopback feeds the ADC output to the DAC input on the IC.

Digital loopback is enabled by setting the appropriate bit in Control 1 register (see Appendix A).

2.1.11 FIR Overflow Flag

The decimator FIR filter provides an overflow flag to the Control 2 register to indicate that the input to the filter has exceeded the range of the internal filter calculations. When this bit is set in the register, it will remain set until the register is read by the user. Reading this value will always reset the overflow flag.

2.2 Terminal Functions

The terminal functions are described in the following sections.

2.2.1 Reset and Power-Down Functions

2.2.1.1 Reset

The TLC320AD56C resets the internal counters and registers, including the programmed registers, in one of two ways:

1. By applying a low-going reset pulse to the reset terminal
2. By writing to the programmable software reset bit (D07 in Control 1 register)

\overline{PWRDWN} resets the counters only and preserves the programmed register contents. The \overline{PWRDWN} terminal must be kept low 20 ms after the power supplies have settled.

2.2.1.2 Conditions of Reset

The two internal reset signals used for the reset and synchronization functions are:

1. Counter Reset – This signal resets all flip-flops and latches that are not externally programmed, with the exception of those generating the reset pulse itself. Additionally, this signal resets the software power-down bit. A counter reset is initiated with the $\overline{\text{RESET}}$ terminal or RESET bit or PWRDWN terminal.
2. Register Reset – This signal resets all flip-flops and latches that are not reset by the counter reset, except those generating the reset pulse itself. A register reset is initiated with the $\overline{\text{RESET}}$ terminal or RESET bit.

Both reset signals should be at least six master clock periods long, T_{RESET} , and should release on the trailing edge of the master clock.

2.2.1.3 Software and Hardware Power Down

Given the definitions above, the software programmed power-down condition is cleared by clearing the software bit (Control 1 register, bit 6) to a 0 or by cycling the power to the device or bringing $\overline{\text{RESET}}$ low.

The output of the monitor amplifier maintains its midpoint voltage during hardware and software power downs to minimize pops and clicks.

$\overline{\text{PWRDWN}}$ powers down the entire chip. Cycling the power-down terminal from high to low and back high resets all flip-flops and latches that are not externally programmed, thereby preserving the register contents.

When $\overline{\text{PWRDWN}}$ is not used, it should be tied high.

2.2.2 Master Clock Circuit

The clock circuit generates and distributes necessary clocks throughout the device. MCLK is the external master clock input. SCLK is derived from MCLK in order to provide clocking of the serial communications between the device and a digital signal processor (DSP). The sample rates of the data paths are set to $\text{MCLK}/512$.

2.2.3 Data Out (DOUT)

DOUT is taken from the high-impedance state by the falling edge of frame sync. The most significant data bit then appears on DOUT.

DOUT is placed in a high-impedance state on the sixteenth rising edge of SCLK after the falling edge of frame sync. In the primary communication, the data word is the ADC conversion result. In the secondary communication, the data is the register read results when requested by the read/write ($\overline{\text{R/W}}$) bit with the eight MSBs set to 0 (see Section 3 *Serial Communications*). If no register read is requested, the secondary word is all zeroes.

2.2.4 Data In (DIN)

In the primary communication, the data word is the input digital signal to the DAC channel. In the secondary communication, the data is the control and configuration data to set up the device for a particular function. (see section 3 *Serial Communications*).

2.2.5 Hardware Program Terminal (FC)

FC provides for hardware programming requests for secondary communication. It works in conjunction with the control bit D00 of the secondary data word. The signal on FC is latched 1/2 shift clock after the rising edge of the next internally generated primary frame-sync interval. The FC terminal should be tied low when not used (see Section 3.2 *Secondary Serial Communication* and Table 3–2).

2.2.6 Frame-Sync Function

The frame-sync signal indicates that the device is ready to send and receive data. The data transfer from DOUT and into DIN begins on the falling edge of the frame-sync signal.

The frame sync is generated internally and goes low on the rising edge of SCLK and remains low during the 16-bit data transfer.

2.2.7 Multiplexed Analog Input

The two differential analog inputs (INP and INM or AUXP and AUXM) are multiplexed into the sigma-delta modulator. The performance of the AUX channel is similar to the normal input channel. A simple RC antialiasing filter must be connected to AUXP and AUXM (also INP and INM when used).

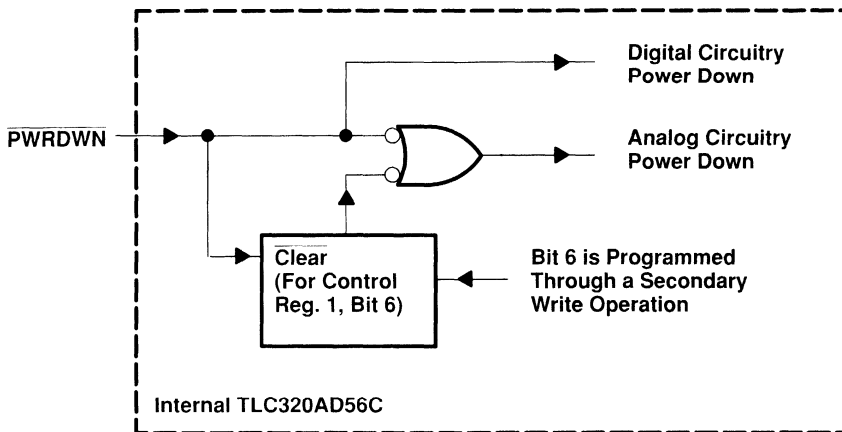


Figure 2–1. Internal Power-Down Logic

2.2.8 Analog Input

The signal applied to the terminals INM and INP (shown in Figure 2–2) should be differential to preserve the device specifications. A single-ended input signal should always be converted to a differential input signal prior to being used by the TLC320AD56C (see section 5 *Application Information*). The signal source driving the analog inputs (INM, INP, AUXM, AUXP) should have a low source impedance for lowest noise performance and accuracy. To obtain maximum dynamic range, the input signal should be centered at midsupply. A simple RC antialiasing filter must be connected to INP and INM (also AUXP and AUXM if used). A suitable tradeoff for the cutoff frequency (f_{co}) of the antialiasing filter is $f_{co} = 3 \times f_s$. With this cutoff frequency, the attenuation within the band of interest ($0 - f_s/2$) is less than 0.1 dB.

2.2.9 Analog Output

The analog output swing across the OUPM and OUTM terminals depends on the value of the resistor used from the IGAIN terminal to analog ground and the resistor load across the OUPM and OUTM terminals. Both resistors can be used to set the output voltage swing and then gained to the desired value in the external DAC output filter as shown in Figure 5–1 and Figure 5–2. With this external filter, the gain of the DAC channel is -2.5 dB.

The resistor on the IGAIN terminal sets up the output current pumped and the resistor across OUPM and OUTM is the load which converts the current output of the DAC to a voltage. Hence, the voltage swing across OUPM and OUTM depends on the ratio of the load resistor to the value of the resistor from the IGAIN terminal to analog ground. With 0 dB digital code applied to the DAC channel, the IGAIN resistor set at $27 \text{ k}\Omega$, and a load resistor of $5 \text{ k}\Omega$, the output swing across OUPM and OUTM is -10.5 dB. The ratio of IGAIN resistance to load resistance can be adjusted to get the desired voltage swing. For the best distortion performance, it is recommended that the output swing be limited to -6 dB relative to $6 V_{pp}$.

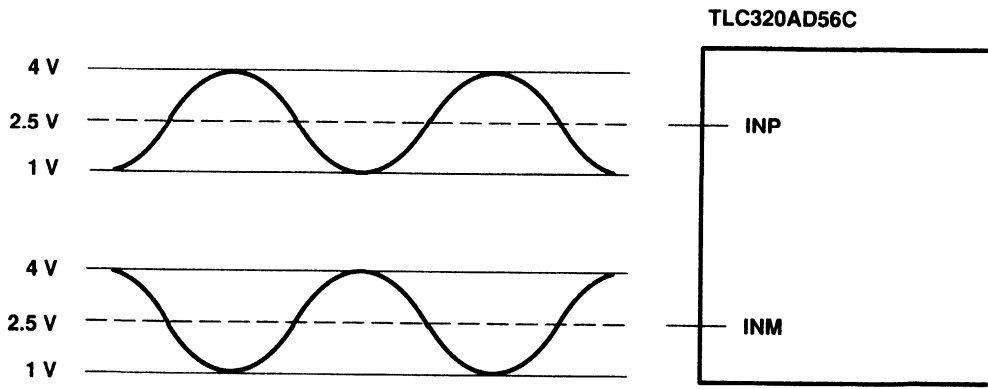


Figure 2-2. Differential Analog-Input Configuration

3 Serial Communications

DOUT, DIN, SCLK, \overline{FS} , and FC are the serial communication signals. The digital output data from the ADC is taken from DOUT. The digital input data for the DAC is applied to DIN. The synchronizing clock for the serial communication data and the frame sync is taken from SCLK. The frame synchronization pulse that encloses the ADC/DAC data transfer interval is taken from \overline{FS} . For an audio signal data transmitted from the ADC or to the DAC, primary serial communication is used. To read or write words that control both the options and the circuit configurations of the device, secondary communication is used.

The purpose of the primary and secondary communications is to allow conversion data and control data to be transferred across the same serial port. A primary transfer is always dedicated to conversion data. A secondary transfer is used to set up and read the register values described in Appendix A. A primary transfer occurs for every conversion period. A secondary transfer occurs only when requested. Two methods exist for requesting a secondary command. The FC terminal can be used to request a secondary communication by asserting it, or the least significant bit (LSB) of the DAC data within a primary transfer can request a secondary communication. The selection of which method is enabled is provided in Control 1 register (bit D0) as shown in Appendix A.

For all serial communications, the most significant bit (MSB) is transferred first. For a 16-bit ADC word and a 16-bit DAC word, D15 is the MSB and D0 is the LSB. For a 15-bit DAC data word in the 16-bit primary communication, D15 is the MSB, D1 is the LSB, and D0 is used for the embedded function control. All digital data values are in 2s-complement format.

These logic signals are compatible with TTL-voltage levels and CMOS current levels (when $V_{DD} = 5\text{ V dc}$). These logic signals are also compatible with a 3-V supply.

3.1 Primary Serial Communication

A primary serial communication transmits and receives conversion signal data. The ADC word length is always 16 bits. The DAC word length depends on the status of D0 in the Control 1 register. After power up or reset, the device defaults to a 15-bit mode (not 16-bit mode). The DAC word length is 15 bits and the last bit of the primary 16-bit serial communication word is a function control bit used to request secondary serial communications. In 16-bit mode, all 16 bits of the primary communications word are used as data for the DAC and the hardware terminal FC must be used to request secondary communications.

Figure 3–1 shows the timing relationship for SCLK, \overline{FS} , DOUT and DIN in a primary communication. The timing sequence for this operation is as follows:

1. \overline{FS} is brought low by the TLC320AD56C.
2. One 16-bit word is transmitted from the ADC (DOUT) and one 16-bit word is received for the DAC (DIN).
3. \overline{FS} is brought high by the TLC320AD56C signaling the end of the conversion.

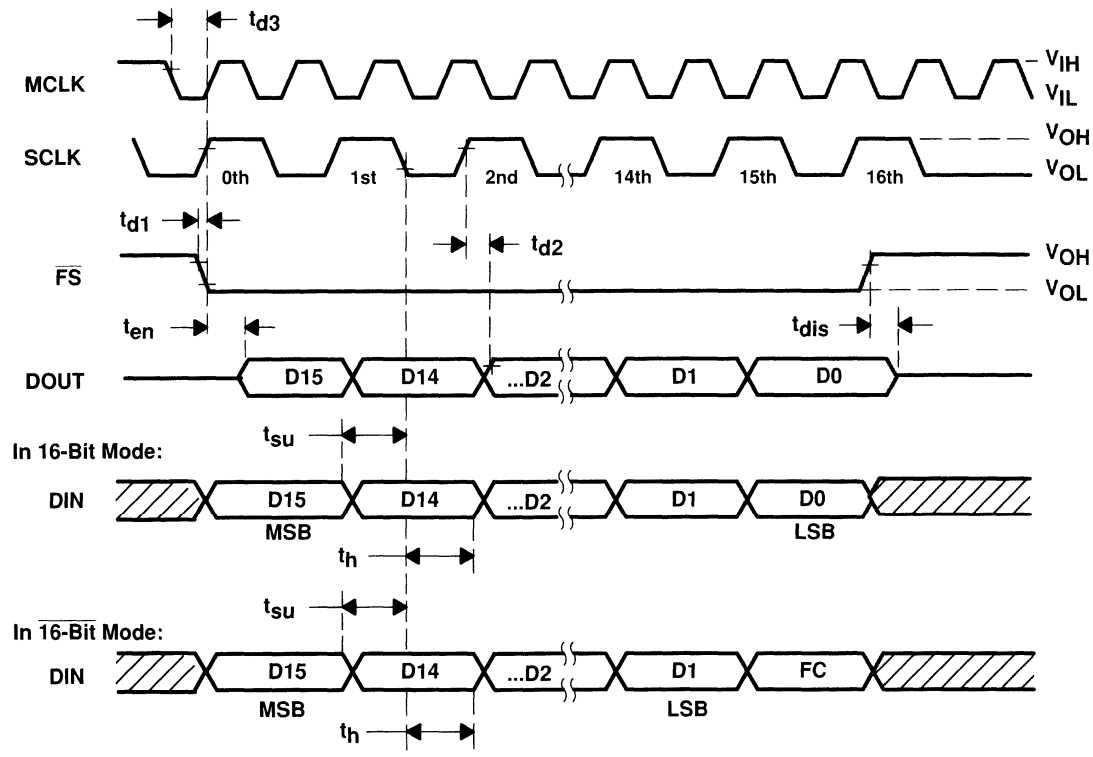


Figure 3–1. Primary Serial Communication Timing

When a secondary request is made through the LSB of the DAC data word ($\overline{16}$ -bit mode), the format in Table 3–1 is used.

Table 3–1. Secondary Request Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
←----- 15-bit DAC -----→														←----- control -----→	
2's-complement format															
←----- 16-bit ADC -----→															
2's-complement format															

3.2 Secondary Serial Communication

Secondary serial communication is used to read or write 16-bit words that program both the options and the circuit configurations of the device. All register programming occurs during secondary communications. Two primary and secondary communication cycles are required to program the two registers. When the default value for a particular register is desired, then the user could omit addressing it during secondary communication. The NOOP command addresses a pseudo-register, register 0, and no register programming takes place during this secondary communication.

There are two methods for initiating secondary communications. They are 1) by asserting a high signal level on FC, or 2) by asserting the LSB of the DIN 16-bit serial communication high while not in 16-bit mode (see Control 1 register, bit 0).

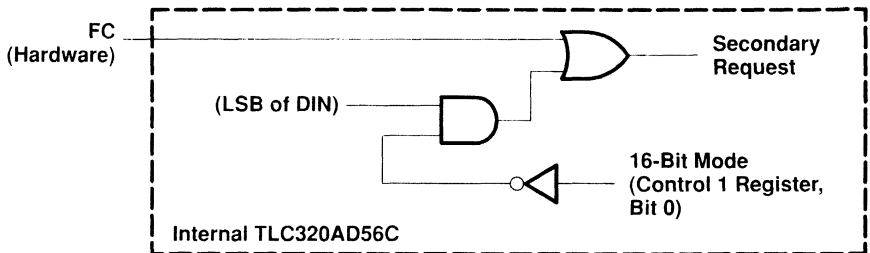


Figure 3–2. Hardware and Software Ways to Make a Secondary Request

1. Figures 3–3 and 3–4 show the two different ways FC requests secondary communication words as well as the timing for \overline{FS} , DOUT, DIN, and SCLK. The examples span two primary communication frames. Figure 3–3 shows the use of hardware function control.

During a secondary communication, a register may be written to or read from. When writing a value to a register, the DIN line contains the value to be written. The data returned on DOUT is 00H. When performing a read function, the DIN line may still provide data to be written to an addressed register; however, the DOUT line contains the most recent value in the register addressed by DIN.

In Figure 3–3, FC is clocked in and latched on the rising edge of frame sync (\overline{FS}). This causes the start of the secondary information 32 FCLKs after the start of the primary communication frame. Read and write examples are shown for DIN and DOUT.

2. Figure 3–4 shows the use of software function control.

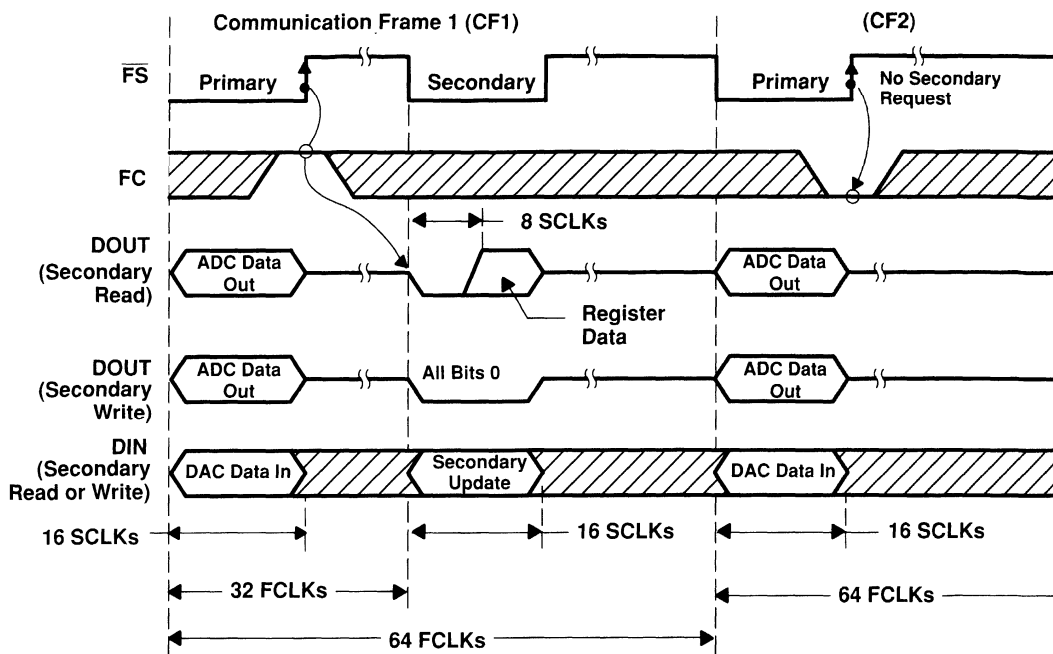
The software request is typically used when the required resolution of the DAC channel is less than 16 bits. Then the least significant bit (D0) can be used for the secondary requests as shown in Table 3–2.

Table 3–2. Least Significant Bit Control Function

Control Bit D0	Control Bit Function
0	No operation (NOOP)
1	Secondary communication request

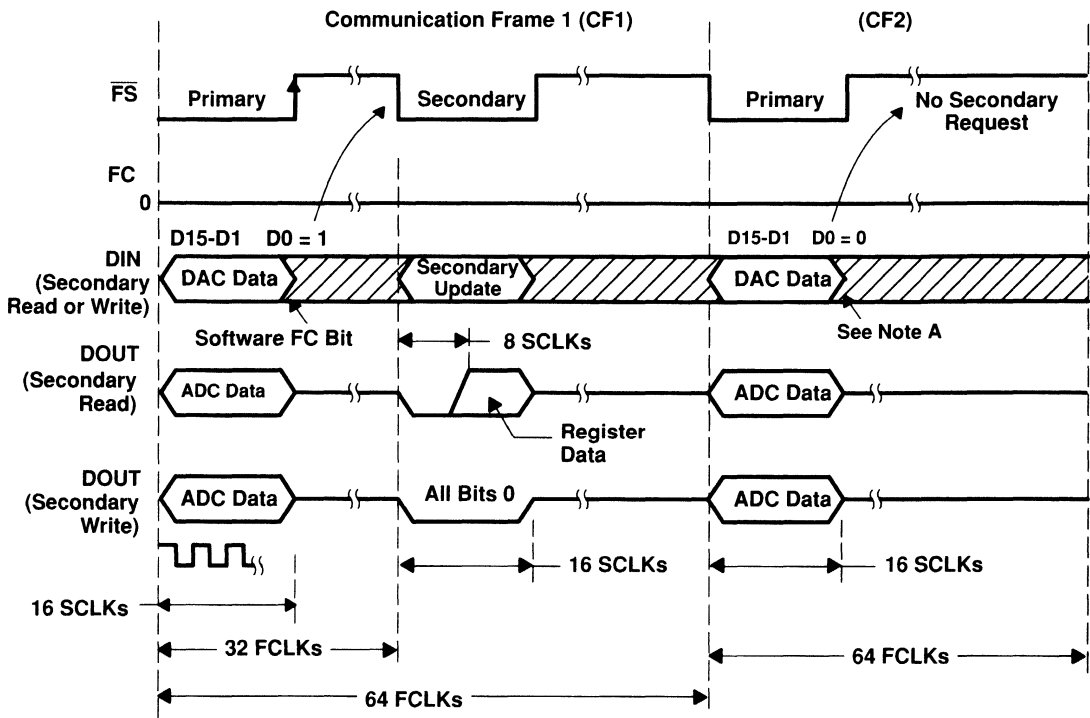
On the falling edge of the next \overline{FS} , D15–D1 is input to DIN or D15–D0 is output to DOUT.

When a secondary communication request is made, \overline{FS} goes low 32 FCLKs after the beginning of the primary frame.



**Figure 3–3. Hardware FC Secondary Request
(Phone Mode Disabled)**

In Figure 3–4, FC hardware terminal 15 is left in its unasserted state (0). FC is asserted through software by embedding an asserted high level (1) in the LSB of the 16-bit primary word. This is possible when not in 16-bit mode (Control 1 register, bit 2 = 0) because the user is using only 15 bits of DAC information.



NOTE A: For a read cycle, the last 8 bits are do-not-care bits.

Figure 3-4. Software FC Secondary Request (Phone Mode Disabled)

Table 3-3 shows the secondary communications format. D13 is the read/not-write (R/\bar{W}) bit.

D12-D8 are address bits. The register map is specified in the register set section in Appendix A. D7-D0 are data bits. The data bits are the new values for the specified register addressed by D12-D8.

Table 3-3. Secondary Communication Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
—	—	R/\bar{W}	A	A	A	A	A	D	D	D	D	D	D	D	D

3.3 Conversion Rate vs Serial Port

The SCLK frequency is set by the frequency of MCLK. There is a 2-stage clock divider that sets the SCLK frequency as $MCLK/4$.

3.4 Phone Mode Control

Phone mode control is provided for applications that need hardware control and monitoring of external events. By allowing the device to drive two FLAG terminals (set through the Control 2 register), the host (DSP) is capable of system control through the same serial port that connects to the device. Along with this control is the capability of monitoring the value of the ALT DATA terminal during a secondary communication cycle. One application for this function is in monitoring RING DETECT or OFFHOOK DETECT from a phone answering system. The two FLAG terminals allow response to these incoming control signals. Figure 3-6 shows the timing associated with this operating mode.

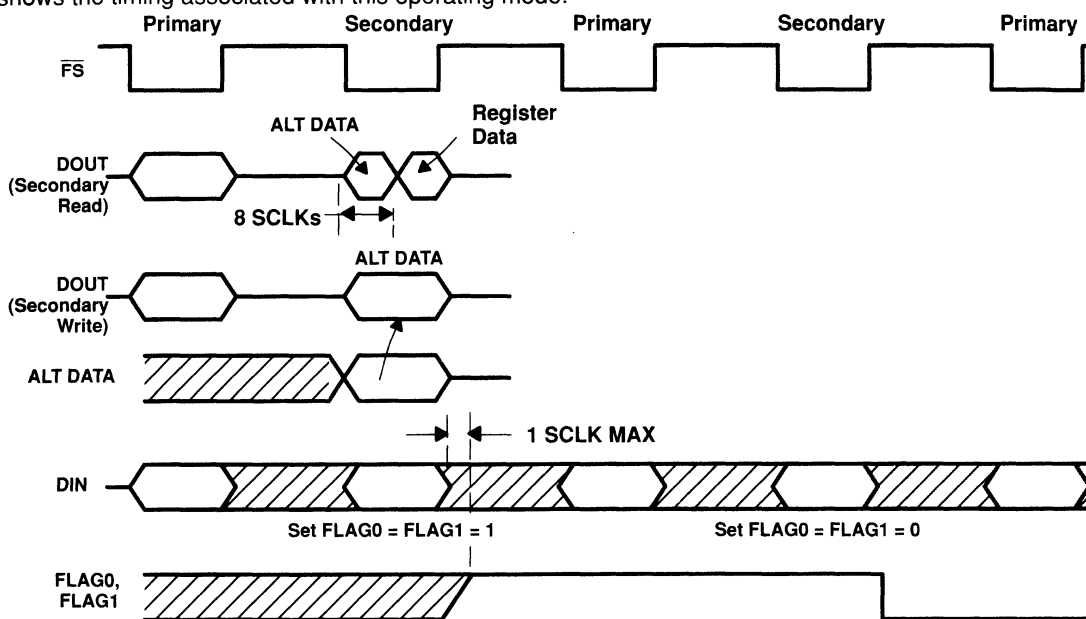


Figure 3-5. Phone Mode Timing

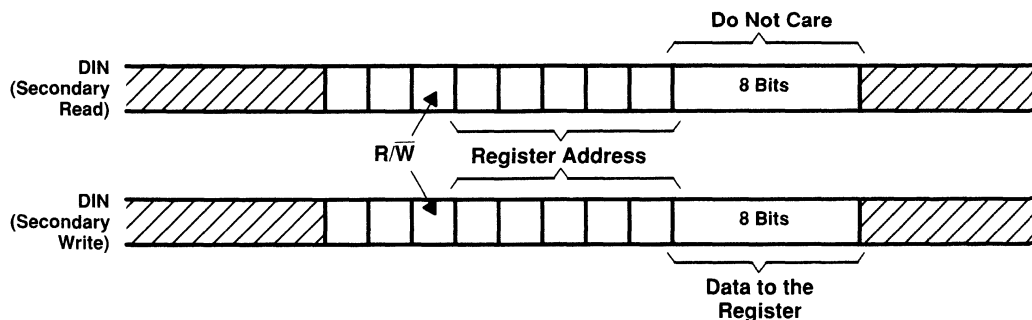


Figure 3-6. Secondary DIN Format

4 Specifications

4.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, DV_{DD} , AV_{DD} (see Note 1)	−0.3 V to 7 V
Output voltage range, DO_{UT} , \overline{FS} , $SCLK$, $FLAG0$, $FLAG1$	−0.3 V to $DV_{DD} + 0.3$ V
Output voltage range, $OUTP$, $OUTM$	−0.3 V to $V_{DD} + 0.3$ V
Input voltage range, DIN , \overline{PWRDWN} , \overline{RESET} , $ALT\ DATA$, MCLK, FC	−0.3 V to $DV_{DD} + 0.3$ V
Input voltage range, INP , INM , $AUXP$, $AUXM$	−0.3 V to $V_{DD} + 0.3$ V
Case temperature for 10 seconds, T_C : DW package	260°C
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

4.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, AV_{DD} (see Note 2)	4.75		5.25	V
Analog signal input voltage, $V_{I(\text{analog})}$	Differential, $(INP - INM)$ peak, for full scale operation			6 V
Resistance, $IGAIN$, $R_{(IGAIN)}$	20	27	54	k Ω
Load resistance, $OUTP$, $OUTM$, R_L	$5/27 \times R_{(IGAIN)}$			k Ω
ADC or DAC conversion rate (sample rate)		8	22.05	kHz
Operating free-air temperature, T_A	0		70	°C

4.2.1 Recommended Operating Conditions, $DV_{DD} = 5$ V, $AV_{DD} = 5$ V

	MIN	NOM	MAX	UNIT
Supply voltage, DV_{DD} (see Note 2)	4.5		5.5	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
MCLK frequency (see Note 3)		4.096	11.29	MHz

4.2.2 Recommended Operating Conditions, $DV_{DD} = 3$ V, $AV_{DD} = 5$ V

	MIN	NOM	MAX	UNIT
Supply voltage, DV_{DD} (see Note 2)	2.7	3	3.3	V
High-level input voltage, V_{IH}	1.8			V
Low-level input voltage, V_{IL}			0.6	V
MCLK frequency (see Note 3)		4.096	11.29	MHz

NOTES: 2. Voltages at analog inputs and outputs and V_{DD} are with respect to the V_{SS} terminal.

3. The default state for an 8-kHz conversion rate requires a 4.096-MHz MCLK frequency.

4.3 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, $DV_{DD} = 5\text{ V}$, $AV_{DD} = 5\text{ V}$ (Unless Otherwise Noted)

4.3.1 Digital Inputs and Outputs, $MCLK = 4.096\text{ MHz}$, $f_s = 8\text{ kHz}$, Outputs Not Loaded

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, DOUT $I_O = 360\ \mu\text{A}$	2.4	4.6		V
V_{OL}	Low-level output voltage, DOUT $I_O = 2\text{ mA}$		0.2	0.4	V
I_{IH}	High-level input current, any digital input $V_{IH} = 5\text{ V}$			10	μA
I_{IL}	Low-level input current, any digital input $V_{IL} = 0.8\text{ V}$			10	μA
C_i	Input capacitance		5		pF
C_o	Output capacitance		5		pF

4.3.2 Digital Inputs and Outputs, $MCLK = 4.096\text{ MHz}$, $f_s = 8\text{ kHz}$, Outputs Not Loaded, $DV_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, DOUT $I_O = 360\ \mu\text{A}$	2			V
V_{OL}	Low-level output voltage, DOUT $I_O = 2\text{ mA}$			0.4	V
I_{IH}	High-level input current, any digital input $V_{IH} = 3.3\text{ V}$			10	μA
I_{IL}	Low-level input current, any digital input $V_{IL} = 0.6\text{ V}$			10	μA
C_i	Input capacitance		5		pF
C_o	Output capacitance		5		pF

4.3.3 ADC Path Filter, $MCLK = 4.096\text{ MHz}$, $f_s = 8\text{ kHz}$ (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	0 to 300 Hz	-0.5		0.2	dB
	300 Hz to 3 kHz	-0.35		0.2	
	3.3 kHz	-0.4		0.3	
	3.6 kHz			-3	
	4 kHz			-40	
	$\geq 4.4\text{ kHz}$			-74	

NOTE 4: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The analog input test signal is a sine wave with $0\text{ dB} = 6\text{ V}_{I(\text{PP})}$ as the reference level for the analog input signal. The -1 dB pass band is 0 to 3400 Hz for an 8-kHz sample rate. This pass band scales linearly with the sample rate.

4.3.4 ADC Dynamic Performance, $MCLK = 4.096\text{ MHz}$, $f_s = 8\text{ kHz}$

4.3.4.1 ADC Signal-to-Noise (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio (SNR)	$V_I = -1\text{ dB}$		86		dB
	$V_I = -3\text{ dB}$	80	84		
	$V_I = -6\text{ dB}$	76	81		
	$V_I = -9\text{ dB}$	73	78		
	$V_I = -40\text{ dB}$	42	47		
	$V_I = -65\text{ dB}$	17	22		
	$V_{AUX} = -9\text{ dB}$	73	78		

NOTE 5: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output voltages are referred to $AV_{DD}/2$.

4.3.4.2 ADC Signal-to-Distortion (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	$V_I = -1$ dB		78		dB
	$V_I = -3$ dB	74	79		
	$V_I = -6$ dB	77	82		
	$V_I = -9$ dB	80	85		
	$V_I = -40$ dB	65	70		
	$V_I = -65$ dB	42	47		
	$V_{AUX} = -9$ dB	80	85		

NOTE 5: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output voltages are referred to $V_{DD}/2$.

4.3.4.3 ADC Signal-to-Distortion, $DV_{DD} = 3$ V (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	$V_I = -1$ dB		79		dB
	$V_I = -3$ dB	90	95		
	$V_I = -6$ dB	92	100		
	$V_I = -9$ dB	94	103		
	$V_I = -40$ dB	68	76		
	$V_I = -65$ dB	42	52		
	$V_{AUX} = -9$ dB	94	103		

NOTE 5: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output voltages are referred to $V_{DD}/2$.

4.3.4.4 ADC Signal-to-Distortion+Noise (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total harmonic distortion + noise (THD+N)	$V_I = -1$ dB		77		dB
	$V_I = -3$ dB	73	78		
	$V_I = -6$ dB	73	78		
	$V_I = -9$ dB	72	77		
	$V_I = -40$ dB	41	46		
	$V_I = -65$ dB	16	21		
	$V_{AUX} = -9$ dB	72	77		

NOTE 5: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output voltages are referred to $V_{DD}/2$.

4.3.4.5 ADC Signal-to-Distortion+Noise, $DV_{DD} = 3\text{ V}$ (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total harmonic distortion + noise (THD+N)	$V_I = -1\text{ dB}$		78		dB
	$V_I = -3\text{ dB}$	79	84		
	$V_I = -6\text{ dB}$	76	81		
	$V_I = -9\text{ dB}$	73	78		
	$V_I = -40\text{ dB}$	42	47		
	$V_I = -65\text{ dB}$	17	22		
	$V_{AUX} = -9\text{ dB}$	73	78		

NOTE 5: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output voltages are referred to $V_{DD}/2$.

4.3.5 ADC Channel

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(PP)}$ Peak-to-peak input voltage			6		V
Dynamic range			87		dB
Interchannel isolation			110		
E_G Gain error	$V_I = -1\text{ dB}$ at 1020 Hz		± 0.3		
$E_{O(ADC)}$ ADC converter offset error			5		mV
CMRR Common-mode rejection ratio at INM, INP or AUXM, AUXP	$V_I = 0\text{ dB}$ at 1020 kHz		80		dB
Idle channel noise (on-chip reference)			30	75	$\mu\text{V rms}$
R_i Input resistance	$T_A = 25^\circ\text{C}$		100		$\text{k}\Omega$
Channel delay			$17/f_s$		s

4.3.6 DAC Path Filter, $MCLK = 8.192\text{ MHz}$, $f_s = 8\text{ kHz}$ (see Note 6)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	0 to 300 Hz	-0.5		0.2	dB
	300 Hz to 3 kHz	-0.25		0.25	
	3.3 kHz	-0.35		0.3	
	3.6 kHz			-3	
	4 kHz			-40	
	$\geq 4.4\text{ kHz}$			-74	

NOTE 6: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is $6 V_{I(PP)}$. The -1 dB pass band is 0 to 3400 Hz for an 8-kHz sample rate. This pass band scales linearly with the sample rate.

4.3.7 DAC Dynamic Performance, $DV_{DD} = 5\text{ V}$ or 3 V

4.3.7.1 DAC Signal-to-Noise (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio (SNR)	$V_O = 0\text{ dB}$	80	85		dB
	$V_O = -9\text{ dB}$	72	77		
	$V_O = -40\text{ dB}$	41	46		
	$V_O = -65\text{ dB}$	16	21		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at the output of a single pole RC filter with a cutoff frequency of 32 kHz. The test is conducted in 16-bit mode.

4.3.7.2 DAC Signal-to-Distortion (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	$V_O = 0\text{ dB}$	86	92		dB
	$V_O = -9\text{ dB}$	90	96		
	$V_O = -40\text{ dB}$	60	66		
	$V_O = -65\text{ dB}$	40	46		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at the output of a single pole RC filter with a cutoff frequency of 32 kHz. The test is conducted in 16-bit mode.

4.3.7.3 DAC Signal-to-Distortion+Noise (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total harmonic distortion + noise (THD+N)	$V_O = 0\text{ dB}$	80	84		dB
	$V_O = -9\text{ dB}$	72	76		
	$V_O = -40\text{ dB}$	41	45		
	$V_O = -65\text{ dB}$	16	20		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at the output of a single pole RC filter with a cutoff frequency of 32 kHz. The test is conducted in 16-bit mode.

4.3.8 DAC Channel, $DV_{DD} = 5\text{ V}$ or 3 V

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dynamic range				85		dB
Interchannel isolation				108		
E_G Gain error, 0 dB	$V_O = 0\text{ dB}$ at 1020 Hz			± 0.5		
Idle channel broad-band noise	See Note 8			70	150	$\mu\text{V rms}$
Idle channel narrow-band noise	0 – 4 kHz,	See Note 8		2	20	$\mu\text{V rms}$
Channel delay				$18/f_S$		s
V_{OO} Output offset voltage at OUT (differential)	DIN = zero code			2		mV
V_O Analog output voltage, OUTP–OUTM	With internal reference and full-scale digital input, See Note 9	Differential	$\frac{9.6 \times R_{LOAD}}{R_{(IGAIN)}}$			V_{PP}

- NOTES: 8. The conversion rate is 8 kHz; the out-of-band measurement is made from 4400 Hz to 3 MHz.
9. The digital input to the DAC channel at DIN is in 2's complement format. The TLC320AD56C is a current DAC and requires a load resistor for current-to-voltage conversion. This output voltage is across the load resistor (see Figures 5–1 and 5–2).

4.3.9 Power Supplies, No Load (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD} (analog) Power supply current, ADC	Operating		18	25	mA
	Power down		0.5		mA
I_{DD} (digital1) Power supply current, digital	Operating		2	5	mA
	Power down		3		μA
I_{DD} (digital2) Power supply current, digital, $DV_{DD} = 3.3\text{ V}$	Operating		1		mA
	Power down		3		μA
P_D Power dissipation	Operating		100	150	mW
	Power down		2.5	5	

4.3.10 Power-Supply Rejection (see Note 10)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{DD1}	Supply-voltage rejection ratio, ADC channel, DV _{DD}	f _i = 0 to 30 kHz		55		dB
V _{DD2}	Supply-voltage rejection ratio, DAC channel, DV _{DD}	f _i = 0 to 30 kHz		55		dB
V _{DD3}	Supply-voltage rejection ratio, ADC channel, AV _{DD}	f _i = 0 to 30 kHz		50		dB
V _{DD4}	Supply-voltage rejection ratio, DAC channel, AV _{DD}	Single ended, f _i = 0 to 30 kHz		50		dB
		Differential, f _i = 0 to 30 kHz		55		dB

† All typical values are at 25°C.

NOTE 10: Power supply rejection measurements are made with both the ADC and the DAC channels idle and a 200-mV peak-to-peak signal applied to the appropriate supply.

4.3.11 Timing Requirements (see Figure 3–1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{d1}	Delay time, SCLK↑ to \overline{FS} ↓	C _L = 20 pF			0	ns
t _{d2}	Delay time, SCLK↑ to DOUT valid				20	
t _{su}	DIN setup time before SCLK low			20		
t _h	DIN hold time after SCLK high				20	
t _{en}	Enable time, \overline{FS} ↓ to DOUT valid				25	
t _{dis}	Disable time, \overline{FS} ↑ to DOUT Hi-Z			20		
t _{d3}	Delay time, MCLK↓ to SCLK↑				50	
t _{wH}	Pulse duration, MCLK high			32		
t _{wL}	Pulse duration, MCLK low		20			

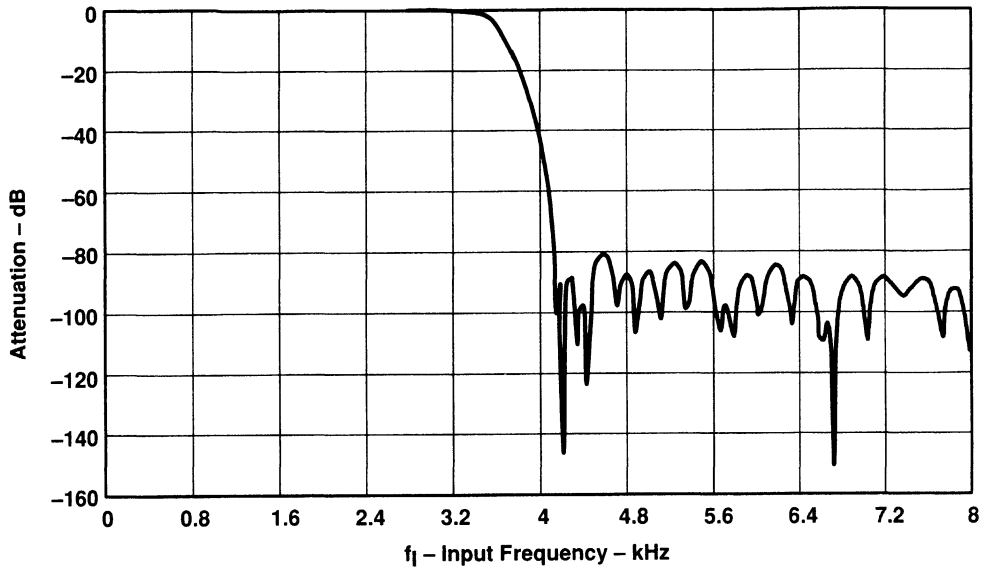


Figure 4-1. ADC Decimation Filter Response

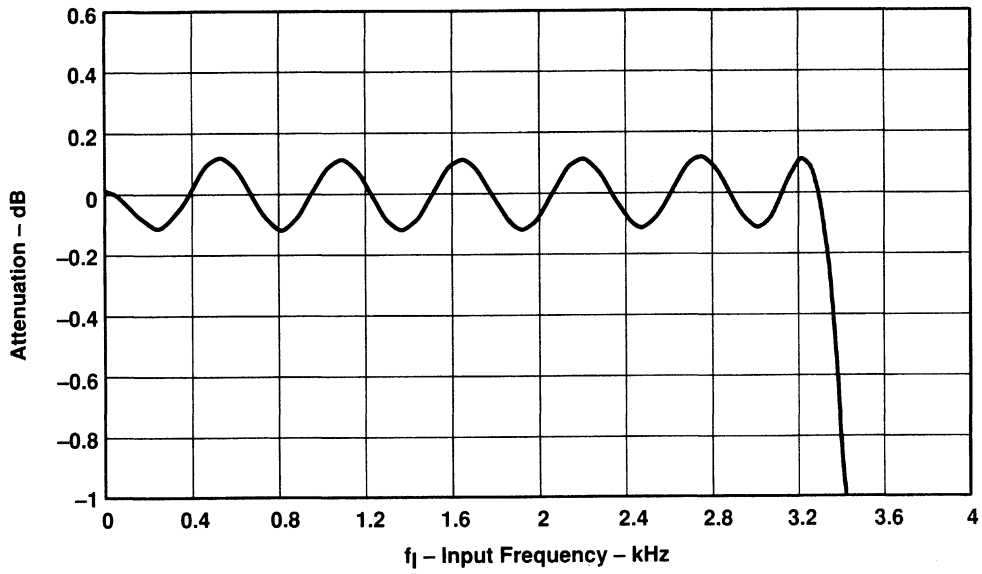


Figure 4-2. ADC Decimation Passband Ripple

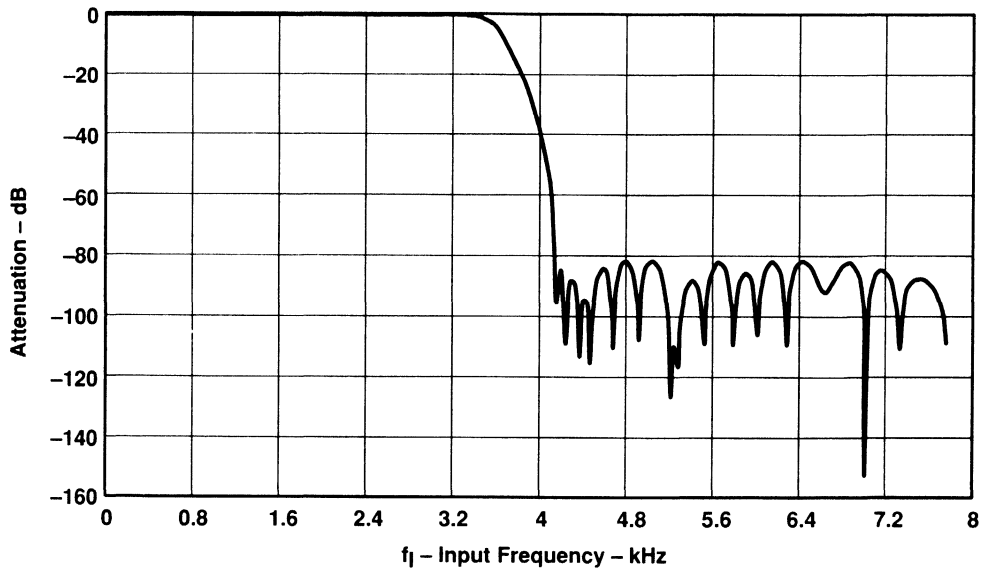


Figure 4-3. DAC Interpolation Filter Response

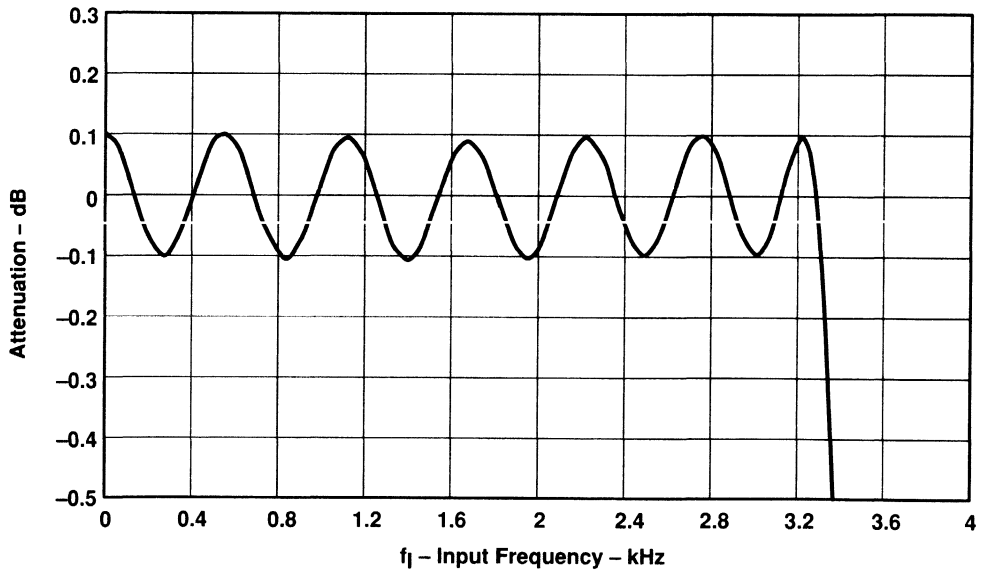


Figure 4-4. DAC Interpolation Passband Ripple

5 Application Information

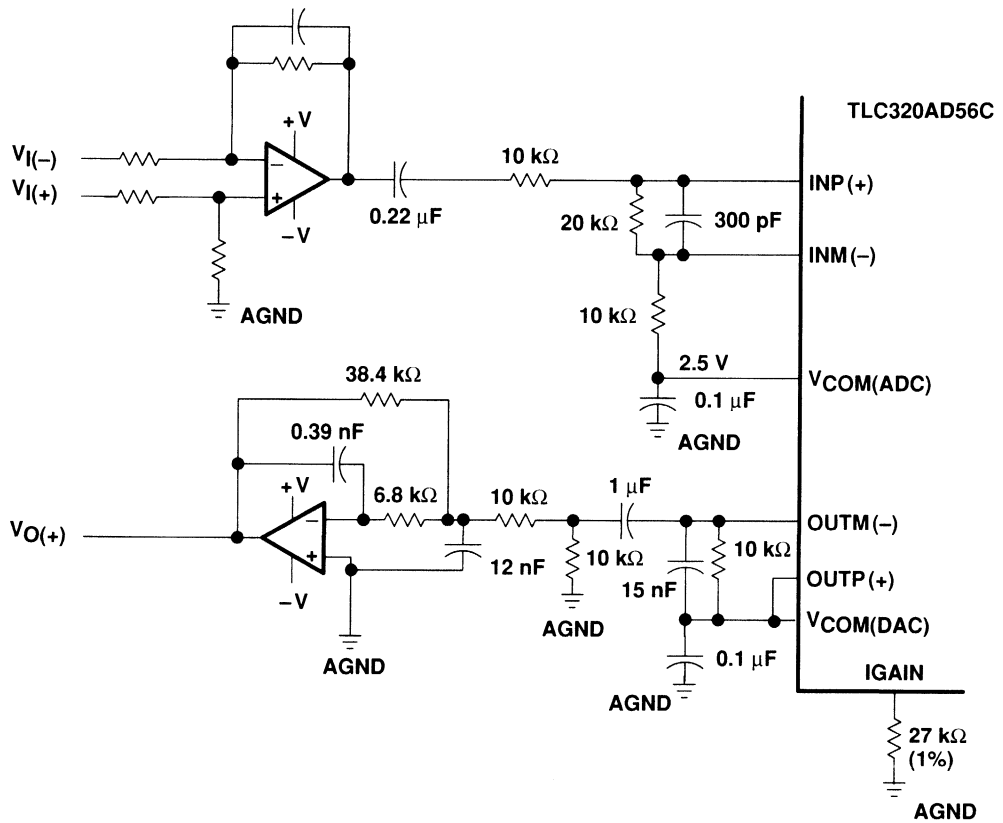


Figure 5-1. Application Schematic For Single-Ended Input/Output

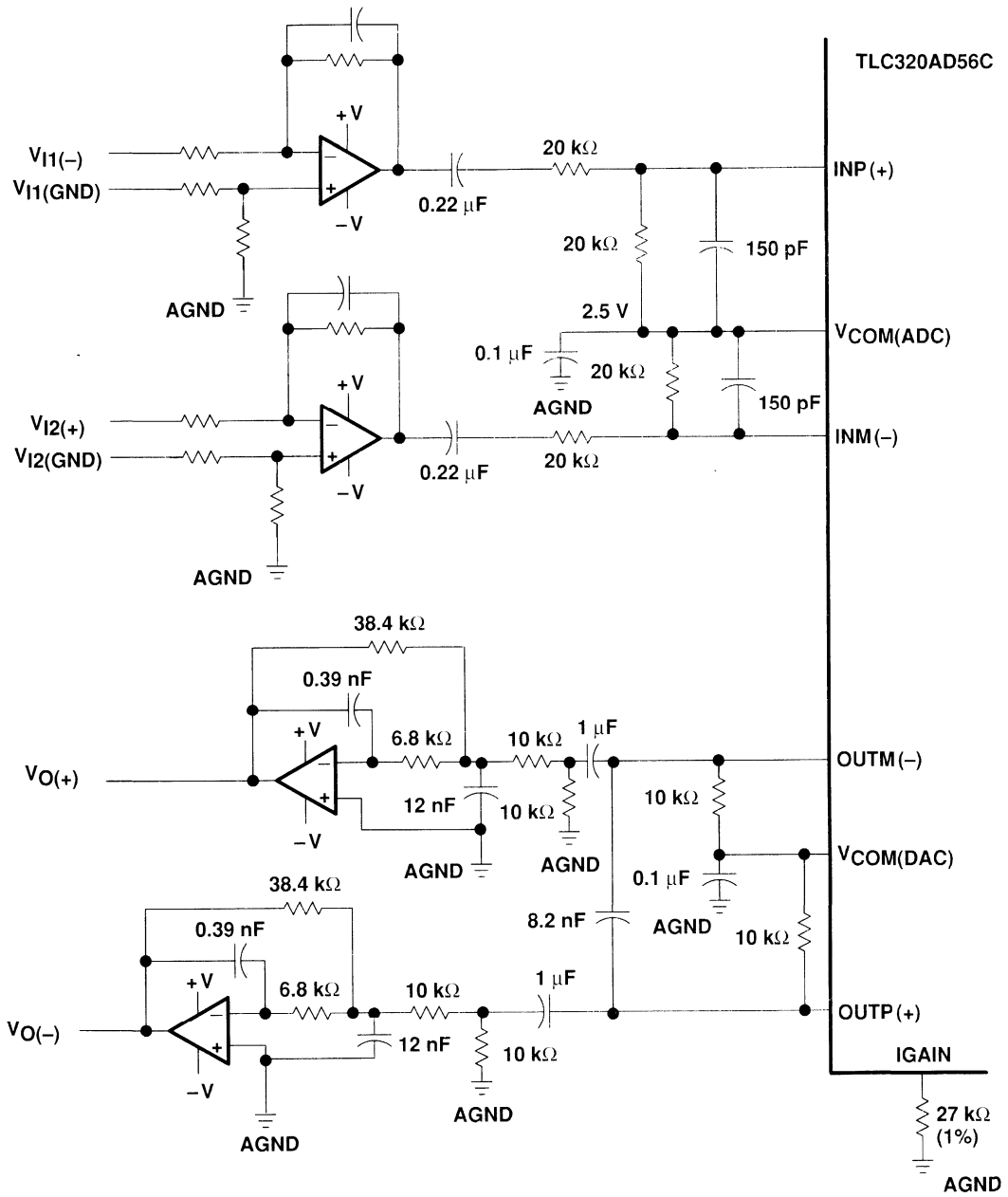


Figure 5-2. Application Schematic For Differential Input/Output

Appendix A Register Set

Bits D12 through D8 in a secondary serial communication comprise the address of the register that is written with the data carried in D7 through D0. D13 determines a read or write cycle to the addressed register. When low, a write cycle is selected.

Table A–1 shows the register map.

Table A–1. Data and Control Registers

REGISTER NO.	BITS								REGISTER NAME	
	D15	D14	D13	D12	D11	D10	D9	D8		
0	0	0	0	0	0	0	0	0	0	No operation
1	0	0	0	0	0	0	0	0	1	Control 1
2	0	0	0	0	0	0	1	0		Control 2

Table A–2. Control 1 Register

BITS								DESCRIPTION
D7	D6	D5	D4	D3	D2	D1	D0	
1	–	–	–	–	–	–	–	Software reset
0	–	–	–	–	–	–	–	Software reset not asserted
–	1	–	–	–	–	–	–	Software power down (analog and filters)
–	0	–	–	–	–	–	–	Software power down (not asserted)
–	–	1	–	–	–	–	–	Select AUXP and AUXM
–	–	0	–	–	–	–	–	Select INP and INM
–	–	–	0	–	–	–	–	Select INP and INM for monitor
–	–	–	1	–	–	–	–	Select AUXP and AUXM for monitor
–	–	–	–	1	1	–	–	Monitor amp gain = – 18 dB (see Note B)
–	–	–	–	1	0	–	–	Monitor amp gain = – 8 dB (see Note B)
–	–	–	–	0	1	–	–	Monitor amp gain = 0 dB (see Note B)
–	–	–	–	0	0	–	–	Monitor amp mute
–	–	–	–	–	–	1	–	Digital loopback asserted
–	–	–	–	–	–	0	–	Digital loopback not asserted
–	–	–	–	–	–	–	1	16-bit mode (hardware secondary requests)
–	–	–	–	–	–	–	0	Not 16-bit mode (software secondary requests)

NOTES: A. Default value: 00000000

B. These gains are for a single-ended input. The gain is 6 dB lower with a differential input.

The software reset is a one-shot operation and this bit is cleared to 0 after reset. It is not necessary to write a zero to end the master reset operation. Writing 0s to the reserved bits is suggested.

Table A-3. Control 2 Register

BITS								DESCRIPTION
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	X	-	-	-	-	-	Decimator FIR overflow flag (valid only during read cycle)
-	-	-	X	-	-	-	-	FLAG 1 output value (valid only during read cycle)
-	-	-	-	X	-	-	-	FLAG 0 output value (valid only during read cycle)
-	-	-	-	-	1	-	-	Phone mode enabled
-	-	-	-	-	0	-	-	Phone mode disabled
X	X	-	-	-	-	X	X	Reserved

NOTES: A. Default value: 00000000

B. X = do not care

Writing 0s to the reserved bits is suggested.

TLC320AD75C ***Data Manual***

20-Bit Sigma-Delta Stereo ADA Circuit

SLAS144
February 1997



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Contents

<i>Section</i>	<i>Title</i>	<i>Page</i>
1	Introduction	4-501
1.1	Features	4-501
1.2	Functional Block Diagram	4-502
1.3	System Block Diagram	4-503
1.4	Terminal Assignments	4-504
1.5	Ordering Information	4-504
1.6	Terminal Functions	4-505
2	Detailed Description	4-507
2.1	Power-Down and Reset Functions	4-507
2.1.1	ADC Power Down	4-507
2.1.2	Reset Function for ADC	4-507
2.1.3	Reset/Initialization for DAC	4-508
2.2	Differential Input to the ADC	4-509
2.3	Sigma-Delta Modulator for the ADC	4-509
2.4	Decimation Filter	4-509
2.5	High-Pass Filter	4-509
2.6	Master Clock	4-510
2.6.1	Master-Clock Circuit for ADC	4-510
2.6.2	Master-Clock Circuit for DAC	4-510
2.7	Test	4-511
2.8	Master Mode for ADC	4-511
2.9	Slave Mode for ADC	4-511
2.10	Digital-Audio-Data Interface for DAC	4-511
2.11	Serial-Control Interface for DAC	4-513
2.11.1	Serial-Control-Data Input	4-513
2.12	DAC De-emphasis Filter	4-513
2.13	Digital Filter Mute for DAC	4-513
2.14	DAC Digital Attenuation/Soft Mute	4-514
2.15	Sigma-Delta DAC Modulator	4-515
2.16	DAC Interpolation Filter	4-515
2.17	DAC PWM Output (L2–L1 and R2–R1)	4-515
2.18	DAC Control Register Set	4-516
2.19	Auto-Resynchronization Functionality	4-517
3	Specifications	4-519
3.1	Absolute Maximum Ratings Over Operating Free-Air Temperature Range	4-519
3.2	Recommended Operating Conditions	4-519
3.3	Electrical Characteristics, $AV_{DD} = LV_{DD} = V_{DD1} = V_{DD2} = PV_{DDL} =$ $PV_{DDR} = XV_{DD} = 5\text{ V}$, $V_{35A} = V_{35D} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$	4-520
3.3.1	Digital Interface	4-520
3.3.2	Analog Interface	4-520
3.3.3	ADC Performance, $f_s = 44.1\text{ kHz}$, Bandwidth = 22.05 kHz	4-521
3.3.4	DAC Performance, 20-Bit Mode, $f_s = 44.1\text{ kHz}$, Bandwidth = 22.05 kHz	4-521

Contents (Continued)

<i>Section</i>	<i>Title</i>	<i>Page</i>
3.3.5	ADC Inputs	4-521
3.3.6	ADC High-Pass Filter, $f_s = 44.1$ kHz	4-521
3.3.7	ADC Decimation Filter, $f_s = 44.1$ kHz	4-521
3.3.8	DAC Filter Characteristics, $f_s = 44.1$ kHz	4-522
3.3.9	Power Supply Current, $f_s = 44.1$ kHz	4-522
3.4	ADC Switching Characteristics	4-522
3.5	DAC Timing Requirements	4-523
4	Parameter Measurement Information	4-525
5	Application Information	4-527
5.1	Circuit And Layout Considerations	4-533
5.2	PCB Footprint	4-533

List of Illustrations

<i>Figure</i>	<i>Title</i>	<i>Page</i>
Figure 2–1	ADC Start-Up Timing	4–508
Figure 2–2	DAC-Reset Timing Relationships	4–508
Figure 2–3	Differential Analog-Input Configuration	4–509
Figure 2–4	ADC Audio-Data Serial Timing – Master Mode	4–511
Figure 2–5	ADC Audio-Data Serial Timing – Slave Mode	4–511
Figure 2–6	Audio Data Serial Timing – ADC and All DAC Modes	4–512
Figure 2–7	Control-Data Input Timing	4–513
Figure 2–8	De-emphasis Filter Characteristics	4–513
Figure 2–9	Digital Attenuation Characteristics	4–514
Figure 2–10	DAC Digital Attenuation Operation With Tapered Gain Response	4–514
Figure 2–11	Oversampling Noise Power With and Without Noise Shaping	4–515
Figure 4–1	ADC Audio-Data Serial Timing	4–525
Figure 4–2	DAC Control-Data Serial Timing	4–525
Figure 5–1	TLC320AD75C Application Schematic	4–530
Figure 5–2	A-Weighted Function	4–532
Figure 5–3	Land Pattern for PCB Layout	4–533

List of Tables

<i>Table</i>	<i>Title</i>	<i>Page</i>
Table 2–1	ADC Master Clock to Sample-Rate Comparison	4–510
Table 2–2	DAC Master Clock to Sample-Rate Comparison	4–510
Table 2–3	Attenuation Mode Register	4–516
Table 2–4	System Mode Register	4–517
Table 5–1	TLC320AD75C Schematic Components	4–527
Table 5–2	A-Weighted Data	4–532

1 Introduction

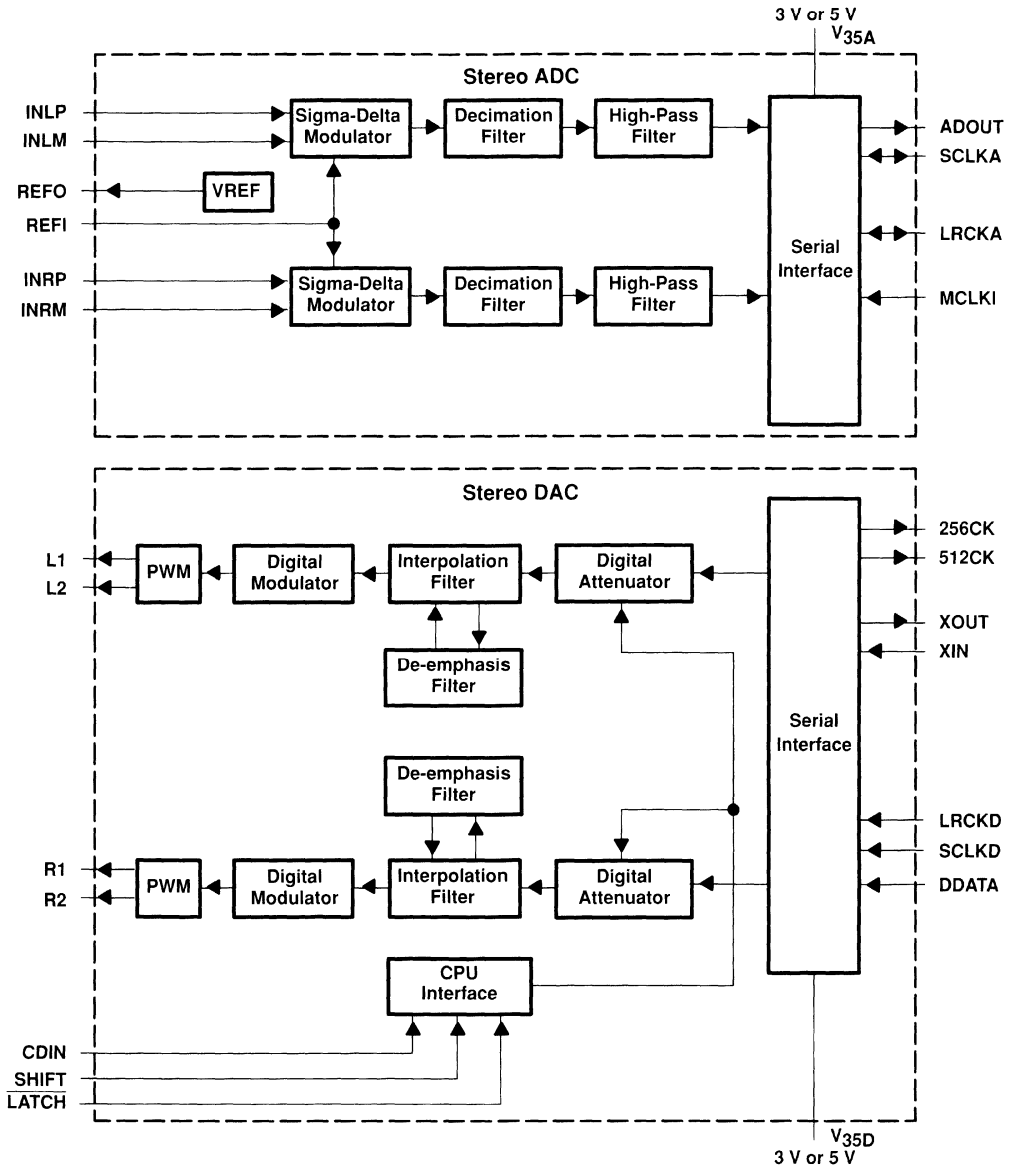
The TLC320AD75C is a high-performance stereo 20-bit analog-to-digital and digital-to-analog converter (ADA) using sigma-delta technology to provide four concurrent 20-bit resolution conversions from both analog-to-digital (A/D) and digital-to-analog (D/A) signal paths. Additional functions provided are digital attenuation, digital de-emphasis filtering, soft mute, and on-chip timing and control. Control words from a host controller or processor are used to implement these functions.

The TLC320AD75C is characterized for operation from 0°C to 70°C.

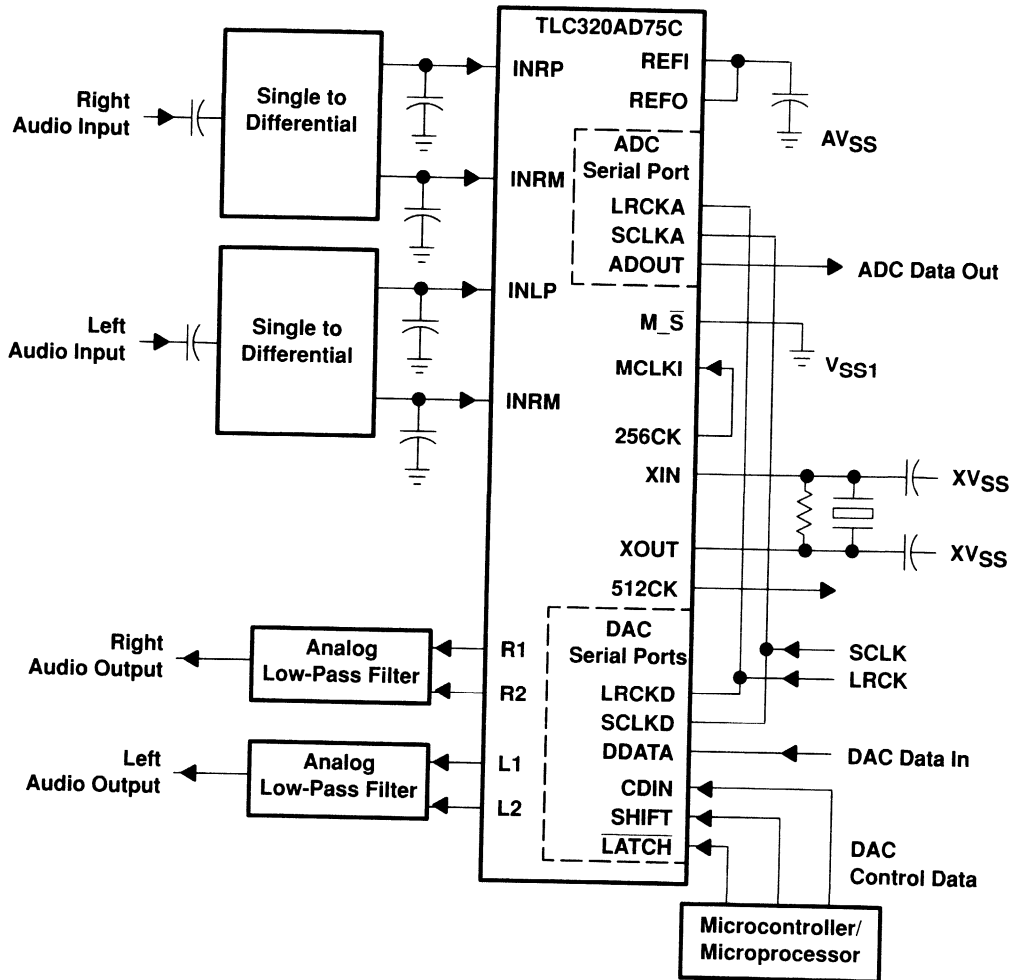
1.1 Features

- Single 5-V (Analog/Digital) Power Level and 3.3-V to 5-V Digital Interface Level
- Sample Rates up to 48 kHz
- 20-Bit Resolution Conversions
- Signal-to-Noise Ratio (EIAJ) of 100 dB for the ADC
- Total Harmonic Distortion + Noise of 0.0017% for the ADC
- Signal-to-Noise Ratio (EIAJ) of 104 dB for the DAC
- Total Harmonic Distortion + Noise of 0.0013% for the DAC
- Internal Voltage Reference (V_{ref})
- Serial Port Interface
- Differential Architecture
- DAC Provides PWM Output
- Digital De-emphasis Filtering for 32-, 44.1-, and 48-kHz Sample Rates for the DAC
- Digital Attenuation/Soft Mute Function for the DAC
- Small 56-Pin DL Plastic Small-Outline Package

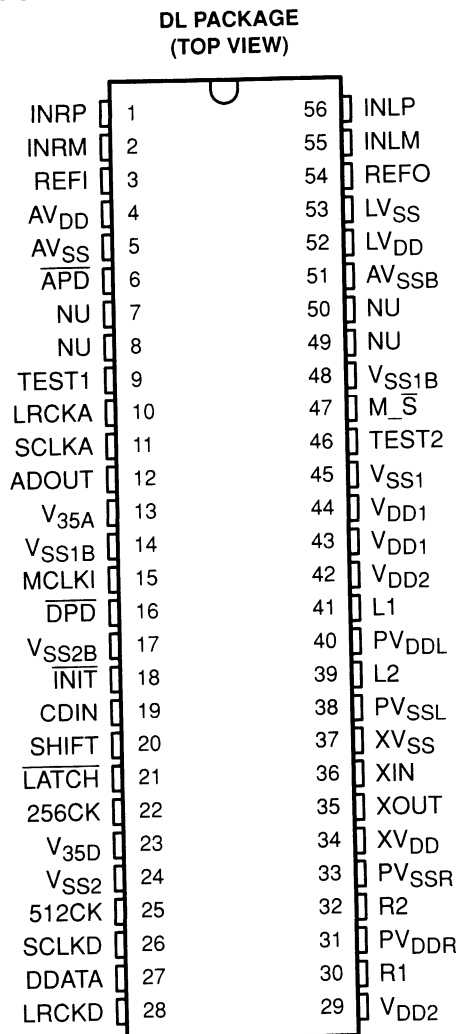
1.2 Functional Block Diagram



1.3 System Block Diagram



1.4 Terminal Assignments



1.5 Ordering Information

T _A	PACKAGE
	SMALL OUTLINE (DL)
0°C to 70°C	TLC320AD75CDL

1.6 Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ADOUT	12	O	20-bit ADC data output. ADOUT provides the MSB first in 2's-complement data format and is left justified within the 32-bit packet for each channel. The output level is 3.3 V for $V_{35A} = 3.3$ V (see Figure 2–6).
\overline{APD}	6	I	Analog power-down mode. \overline{APD} disables the ADC analog modulators. The ADC single-bit modulator outputs become invalid, rendering the outputs of the digital filters invalid. When \overline{APD} is pulled high, normal operation of the device is resumed.
AVDD	4		Analog power supply voltage for ADC modulators
AVSS	5		Analog ground for ADC modulators
AVSSB	51		Analog substrate ground for ADC modulators
CDIN	19	I	Attenuation mode and system control mode input for DAC. CDIN is a 24-bit stream with a 16-bit data word followed by an 8-bit device address. This stream is configured with the MSB first (see Section 2.15, <i>Sigma-Delta DAC Modulator</i>).
DDATA	27	I	DAC input data in 2's-complement data format. MSB/LSB first and 20-bit/16-bit input formats are selectable by using the DAC control registers (see Section 2.15, <i>Sigma-Delta DAC Modulator</i>).
\overline{DPD}	16	I	Digital power-down mode. The \overline{DPD} shuts down the ADC digital decimation filters and clock generators, and provides a digital reset. All digital outputs of the ADC function, are brought to unasserted states. When \overline{DPD} is pulled high, normal operation of the device is resumed. When in slave mode operation, after the rising edge of \overline{DPD} , the ADC system is synchronized.
\overline{INIT}	18	I	Initial DAC reset signal. The DAC device is activated on the rising edge of \overline{INIT} . When \overline{INIT} is brought low, the DAC is reset when LRCKD is present.
INLM	55	I	Inverting input for the left channel analog modulator
INLP	56	I	Noninverting input for the left channel analog modulator
INRM	2	I	Inverting input for the right channel analog modulator
INRP	1	I	Noninverting input for the right channel analog modulator
\overline{LATCH}	21	I	Latch signal for the DAC control serial data. Attenuation/system-control data loads into the internal registers when \overline{LATCH} is brought low.
LRCKA	10	I/O	Left/right clock for ADC. LRCKA signifies whether the serial data is associated with the left channel ADC (when LRCKA is high) or the right channel ADC (when LRCKA is low). LRCKA is normally connected to LRCKD. LRCKA is output when configured in master mode.
LRCKD	28	I	Left/right clock for DAC. LRCKD signifies whether the serial data is associated with the left channel DAC (when LRCKD is high) or the right channel DAC (when LRCKD is low). LRCKD is normally connected to LRCKA.
LVDD	52		Digital power supply for analog modulators. LVDD is normally connected to AVDD through a 50- Ω resistor.
LVSS	53		Digital ground for analog modulators. LVSS is normally connected to AVSS through a 50- Ω resistor.
L1	41	O	Left channel DAC PWM output 1
L2	39	O	Left channel DAC PWM output 2
MCLKI	15	I	Master clock input for ADC. MCLKI operates at 256 times the sample rate (i.e. 256 times LRCKA). MCLKI is normally connected to 256CK through a 50- Ω resistor.

Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
M \bar{S}	47	I	Master/slave selection. The ADC serial port is configured as master mode when M \bar{S} is pulled high. M \bar{S} is connected to V $_{SS1}$ for slave mode.
NU	7, 8, 49, 50	–	Not used
PVDDL	40		PWM power supply for left channel DAC
PVDDR	31		PWM power supply for right channel DAC
PVSSL	38		PWM ground for left channel DAC
PVSSR	33		PWM ground for right channel DAC
REFI	3	I	Input reference voltage. REFI provides reference voltage for the ADC modulator (normally connected to REFO).
REFO	54	O	Internal ADC reference voltage (normally connected to REFI).
R1	30	O	Right channel DAC PWM output 1
R2	32	O	Right channel DAC PWM output 2
SCLKA	11	I/O	Shift clock for the ADC. The shift clock clocks serial data out of the ADC, and operates at 64 times the sample rate (i.e. 64 times LRCKA). SCLKA is normally connected to SCLKD. SCLKA is output when configured in master mode.
SCLKD	26	I	Shift clock for the DAC. The shift clock clocks serial audio data into the DAC, and operates at 64 times the sample rate (i.e. 64 times LRCKD). SCLKD is normally connected to SCLKA.
SHIFT	20	I	Shift data. SHIFT clocks the control data (CDIN) into the internal control registers for the DAC.
TEST1	9	I	Factory test terminal1. TEST1 should be connected to V $_{SS1}$ for normal operation.
TEST2	46	I	Factory test terminal2. TEST2 should be connected to V $_{SS1}$ for normal operation.
XIN	36	I	Oscillator input terminal for 512 times the DAC sample rate. XIN derives all of the key logic signals of the DAC device. (XIN can also be driven by an external oscillator.)
XOUT	35	O	Oscillator output terminal for 512 times the DAC sample rate
VDD1	43, 44		Digital power supply for ADC
VDD2	29, 42		Digital power supply voltage for DAC
VSS1	45		Digital ground for ADC digital filters
VSS1B	14, 48		Digital substrate ground for ADC
VSS2	24		Digital ground for the DAC
VSS2B	17		Digital substrate ground for DAC
V35A	13		Digital power supply for ADC interface logic. V35A is connected to 3 V or 5 V.
V35D	23		Digital power supply for DAC interface logic. V35D is connected to 3 V or 5 V.
XVDD	34		Oscillator power-supply voltage for DAC
XVSS	37		Oscillator circuit ground for DAC
256CK	22	O	256 times sample rate clock output. 256CK is normally connected to MCLKI through a 50- Ω resistor. 256CK is the XIN frequency divided by two.
512CK	25	O	512 times sample rate clock output (output level is 3.3 V for V35D = 3.3 V). 512CK is a buffered version of XIN (master clock input).

2 Detailed Description

The sigma-delta ADC converter consists of an oversampling analog modulator and digital decimation filter.

The sigma-delta DAC incorporates an interpolation finite impulse-response (FIR) filter and oversampled modulator. The pulse-width-modulation (PWM) digital output feeds an external low-pass filter to recover the analog audio signal.

Two control registers configure the DAC. The attenuation register controls the attenuation range, de-emphasis enable, and mute selection. The system register controls the data format and de-emphasis filter-sample rate.

2.1 Power-Down and Reset Functions

2.1.1 ADC Power Down

The power-down state is comprised of a separate digital and analog power down for the ADC. The power consumption of each is detailed in the electrical characteristics section.

The digital power-down mode shuts down the digital filters and clock generators. When the digital power-down terminal is pulled high, normal operation of the device is initiated. In slave mode, the conversion process must synchronize to an input on LRCKA as well as SCLKA. Therefore, the conversion process is not initiated until the first rising edges of both SCLKA and LRCKA are detected after $\overline{\text{DPD}}$ is pulled high. This synchronizes the conversion cycle; all conversions are performed at a fixed LRCKA rate after the initial synchronization. After $\overline{\text{DPD}}$ is brought high, the output of the digital filters remains invalid for 26 LRCKA cycles which consists of group delays of the decimation and high-pass filter.

The analog power-down mode disables the analog modulators. The single-bit modulator outputs become invalid, which renders the outputs of the digital filters invalid. When the $\overline{\text{APD}}$ terminal is brought high, the modulators are brought back online; however, the settling time of the modulator stage is normally 100 ms.

2.1.2 Reset Function for ADC

The conversion process is not initiated until the first rising edges of both SCLKA and LRCKA are detected after $\overline{\text{DPD}}$ is pulled high. This synchronizes the conversion cycle; all conversions are performed at a fixed LRCKA rate after the initial synchronization.

During general operation of the ADC, $\overline{\text{APD}}$ is recommended to be pulled high ($\overline{\text{APD}}$ is not needed for a reset). When using the analog power-down mode ($\overline{\text{APD}}$ low), the following timing procedure is required to start all of the ADC since the analog modulator portion which includes the external portion needs to be settled after $\overline{\text{APD}}$ is high.

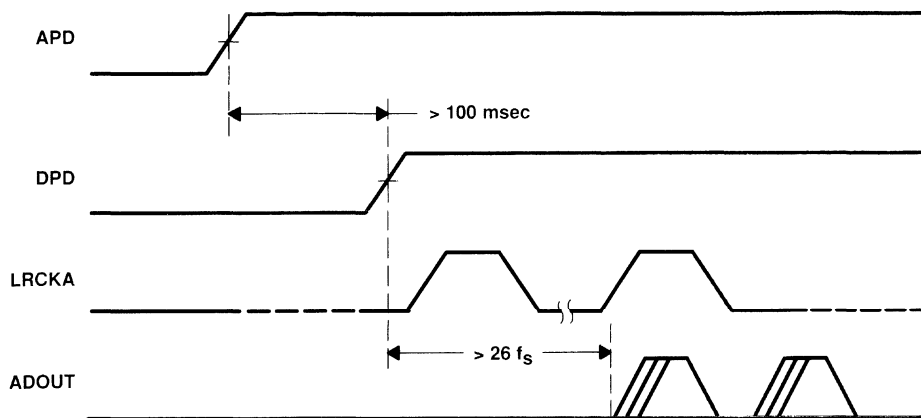


Figure 2-1. ADC Start-Up Timing

2.1.3 Reset/Initialization for DAC

When $\overline{\text{INIT}}$ is brought low, an internal reset signal becomes active approximately 120 cycles of the sampling frequency (f_s) after the falling edge of $\overline{\text{INIT}}$. Under this condition, all internal circuits are initialized and the PWM output is held at zero data (50% duty cycle). When $\overline{\text{INIT}}$ is brought high, the internal reset signal goes inactive for a maximum of five LRCKD periods after the rising edge of $\overline{\text{INIT}}$. At this point, internal clocks are synchronous with LRCKD and the PWM output is valid (see Figure 2-2). LRCKD must be applied for proper initialization.

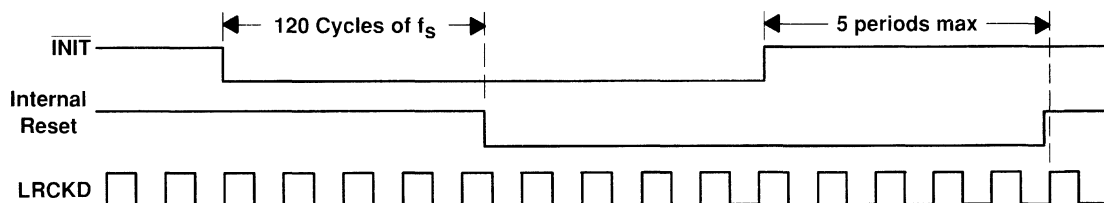


Figure 2-2. DAC-Reset Timing Relationships

2.2 Differential Input to the ADC

The input to the ADC is differential in order to provide common-mode noise rejection and increase the input dynamic range. Figure 2–3 shows the analog input signals used in a differential configuration to achieve a $6.4 V_{I(PP)}$ differential swing with a $3.2 V_{I(PP)}$ swing per input line.

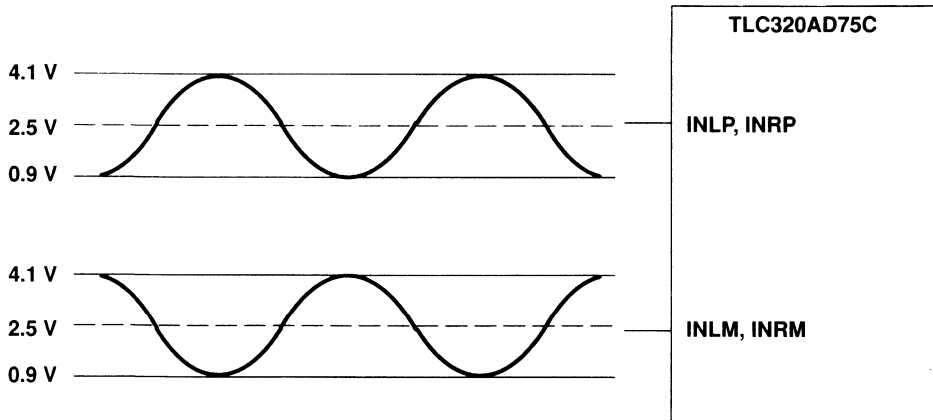


Figure 2–3. Differential Analog-Input Configuration

2.3 Sigma-Delta Modulator for the ADC

The modulator is a fourth-order sigma-delta modulator with 64 times oversampling. The ADC provides high-resolution, low-noise performance from a 1-bit converter using oversampling techniques.

2.4 Decimation Filter

The decimation filter after the sigma-delta ADC modulator reduces the digital data rate to the sampling rate of LRCKA. This is accomplished by decimating with a ratio of 1:64.

2.5 High-Pass Filter

The high-pass filter removes dc from the input of the ADC. The output of this filter is a 2's-complement data word of 20 bits serially clocked out. If the input value exceeds the full range of the converter, the output of the high-pass filter is held at the appropriate extreme until the input returns to the analog input range of the TLC320AD75C.

2.6 Master Clock

2.6.1 Master-Clock Circuit for ADC

The master-clock circuit generates and distributes necessary clocks throughout the device. MCLKI is the external master-clock input. The sample rate of the data paths is set as $LRCKA = MCLKI/256$. With a fixed oversampling ratio of $64 \times f_s$, the effect of changing MCLKI is shown in Table 2–1.

Table 2–1. ADC Master Clock to Sample-Rate Comparison

MCLKI (MHz)	SCLKA (MHz)	LRCKA (kHz)
12.2880	3.0720	48
11.2896	2.8224	44.1
8.1920	2.0480	32

When the TLC320AD75C is in master mode ($M_{\bar{S}}$ is pulled high) SCLKA is derived from MCLKI in order to provide clocking of the serial communications between the sigma-delta audio ADC and a digital signal processor (DSP) or control logic. This is equivalent to a clock running at $64 \times LRCKA$.

When the TLC320AD75C is in slave mode ($M_{\bar{S}}$ is connected to V_{SS1}), SCLKA is externally derived. For SCLKA use of a clock running at 64 times LRCKA is recommended.

2.6.2 Master-Clock Circuit for DAC

The timing and control circuit generates and distributes necessary clocks throughout the TLC320AD75C. XIN is the oscillator input terminal or can receive an external master-clock input. The sample rate of the data paths is set as $LRCKD = XIN/512$. With a fixed oversampling ratio of $32\times$ and each PWM output value requiring 16 XIN cycles, the effect of changing XIN is shown in Table 2–2.

Table 2–2. DAC Master Clock to Sample-Rate Comparison

XIN (MHz)	256CK (MHz)	LRCKD (kHz)
24.5760	12.2880	48.0
22.5792	11.2896	44.1
16.3840	8.1920	32.0

The DAC can be operated at any conversion rate between 48 kHz and 32 kHz by choosing the appropriate master-clock frequency. Some of the functions of the converter, such as the deemphasis filter, operate only at the frequencies shown in Table 2–2.

2.7 Test

TEST1 and TEST2 are reserved for factory test and are tied to digital ground (V_{SS1}).

2.8 Master Mode for ADC

Configured as the master device ($M_{\overline{S}}$ is connected to V_{DD1}), the TLC320AD75C generates LRCKA and SCLKA from MCLKI. These signals are provided for synchronizing the serial port of a digital signal processor (DSP) or other control devices.

LRCKA is generated internally from MCLKI. The frequency of LRCKA is fixed at the sampling frequency, f_s ($MCLKI/256$). During the high period of LRCKA, the left channel data is serially shifted to the output; during the low period, the right channel data is shifted to the output (ADOUT). The conversion cycle is synchronized with the rising edge of LRCKA.

Figure 2–4 (master mode) shows 20-bit data, MSB first, ADOUT data shifted out of the TLC320AD75 during the first 20 SCLKA periods of the 32 SCLKA periods for both left and right channel data.

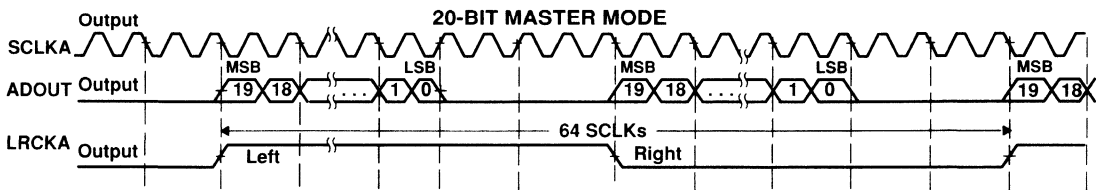


Figure 2–4. ADC Audio-Data Serial Timing – Master Mode

2.9 Slave Mode for ADC

Configured as a slave device ($M_{\overline{S}}$ is connected to V_{SS1}), the TLC320AD75C receives LRCKA and SCLKA as inputs. The conversion cycle is synchronized to the rising edge of LRCKA, and the data is synchronized to the falling edge of SCLKA. SCLKA must meet the setup requirements specified in the recommended operating conditions section. Synchronization of the slave mode is accomplished with the rising edge of \overline{DPD} .

The slave mode is shown in Figure 2–5. SCLKA and LRCKA are externally generated and sourced. The first rising edges of SCLKA and LRCKA after the rising edge of \overline{DPD} initiate the conversion cycle (see Section 2.8, *Master Mode for ADC* for signal functions).

Figure 2–5 (slave mode) shows 20-bit data, MSB first, and ADOUT data shifted out of the TLC320AD75 during the first 20 SCLKA periods of the 32 SCLKA periods for both left and right channel data.

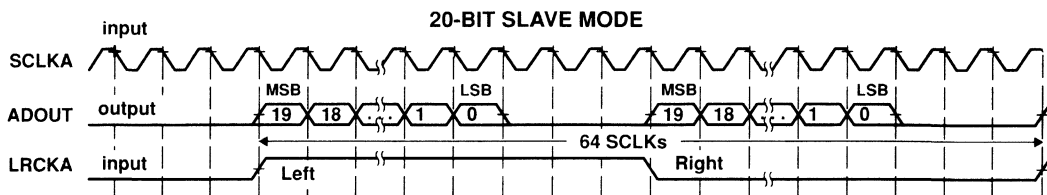


Figure 2–5. ADC Audio-Data Serial Timing – Slave Mode

2.10 Digital-Audio Data Interface for DAC

The conversion cycle is synchronized to the rising edge of LRCKD, and the data must meet the setup requirements specified in the timing requirements table. The input data is 16 or 20 bits with the MSB or LSB first as selected in the system register. The recommended SCLKD frequency is $64 \times f_s$. Figure 2–6 illustrates the input timing.

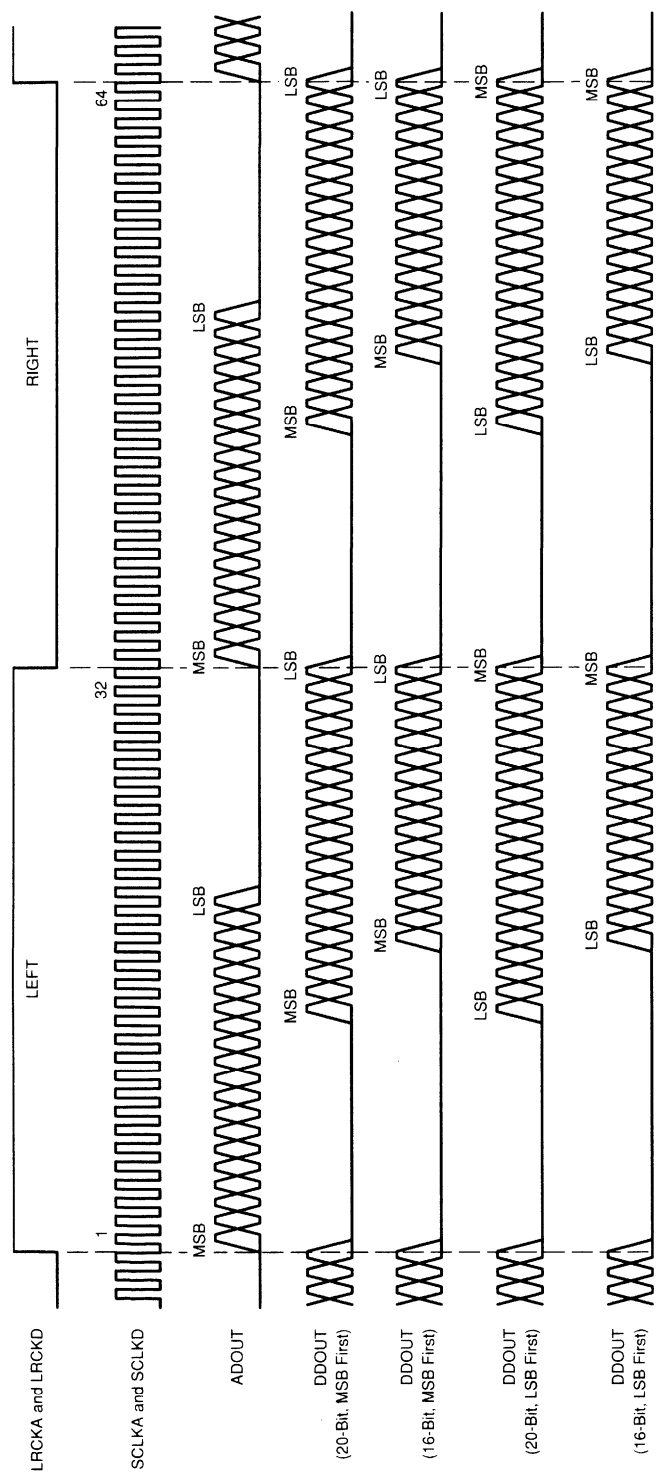


Figure 2-6. Audio-Data Serial Timing – ADC and All DAC Modes

2.11 Serial-Control Interface for DAC

The TLC320AD75C uses the most-significant-bit-first format. Therefore, for a 16-bit data word, D16 is the most significant bit (MSB) and D1 is the least significant bit (LSB).

2.11.1 Serial-Control-Data Input

The 16-bit control-data input implements the device-control functions. The TLC320AD75C has two registers for this data: the system register and the attenuation register. The system register contains most of the system configuration information, and the attenuation register controls the audio output level and deemphasis. Figure 2–7 illustrates the input timing for CDIN, SHIFT, and $\overline{\text{LATCH}}$. The data loads internally during the low level of $\overline{\text{LATCH}}$. The shift clock must be high or low for the $\overline{\text{LATCH}}$ setup time before $\overline{\text{LATCH}}$ goes low.

As shown in Figure 2–7, CDIN is a 24-bit data stream consisting of 16 bits of control data D16 through D1 followed by 8 bits of device, address A8 through A1. When the TLC320AD75C receives address >E7h, the control data is latched into the device by $\overline{\text{LATCH}}$. For all other addresses, the data is ignored.

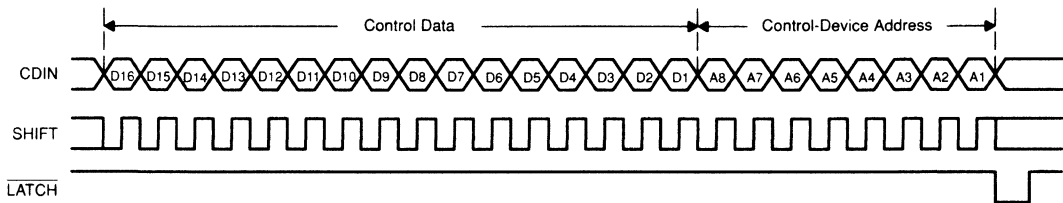


Figure 2–7. Control-Data Input Timing

2.12 DAC De-emphasis Filter

Three sets of de-emphasis-filter coefficients support the three sampling rates (f_s): 32 kHz, 44.1 kHz, and 48 kHz. Internal system-register values select the filter coefficients. The internal register values enable or disable the filter. Figure 2–8 illustrates the de-emphasis filtering characteristics.

Many audio sources have been recorded with pre-emphasis characteristics that are the inverse of the characteristics shown in Figure 2–8. This device provides reconstruction of the original frequency response.

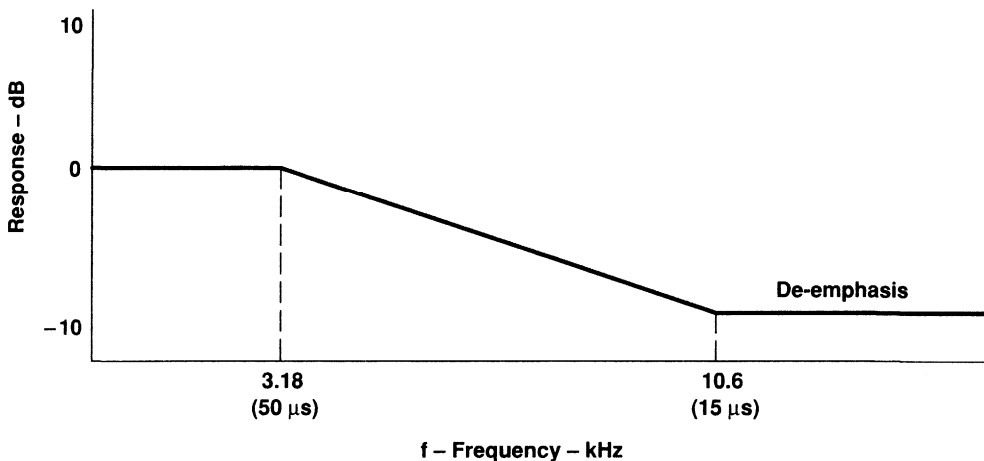


Figure 2–8. De-emphasis Filter Characteristics

2.13 Digital Filter Mute for DAC

When the mute bit in the attenuation register is set to 1, the DAC digital filter mute is active. The output of the digital filter is 0 + dc offset. Operation of the digital filter is normal during mute.

2.14 DAC Digital Attenuation/Soft Mute

A value selected in the internal attenuation register determines the attenuation of the digital-audio data input. The attenuation value is 12 bits long with a valid range of hex values from 400h to 000h. A data value of 001h corresponds to an attenuation value of -60 dB and a data value of 400h corresponds to 0 dB. The attenuation function is nonlinear. Figure 2-9 illustrates the attenuation function in dB. The default attenuation value is 400h (refer to the attenuator mode register for more detailed description).

$$\text{Attenuation} = 20 \log \left(\frac{\text{attenuation data}}{1024} \right)$$

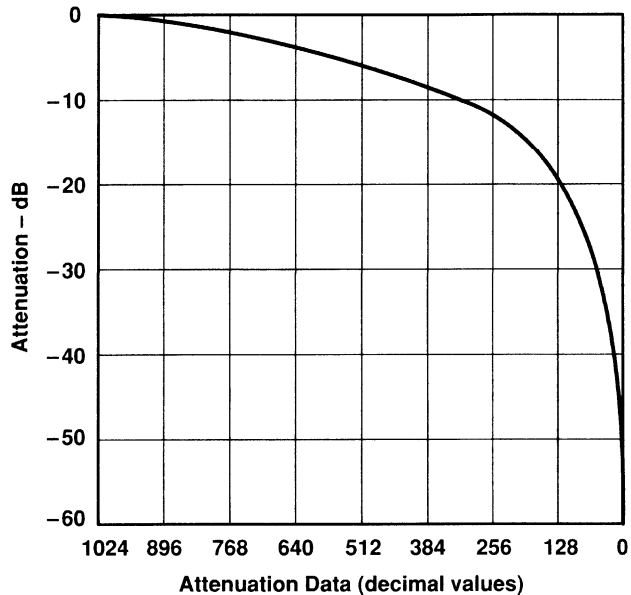


Figure 2-9. Digital Attenuation Characteristics

The attenuation operation of the DAC has a tapered gain response. It takes time $T = 1024/f_s$ (sec) to reach the actual 000H data output after an ATT = 000H data transfer from 400H data as shown in Figure 2-10.

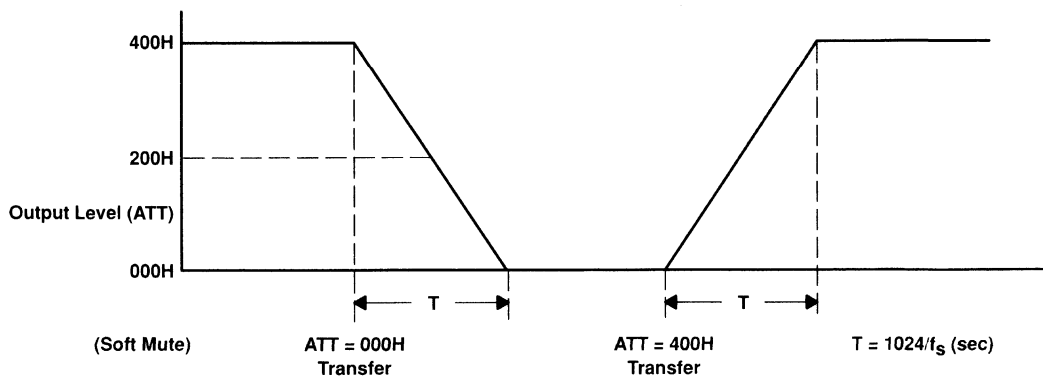
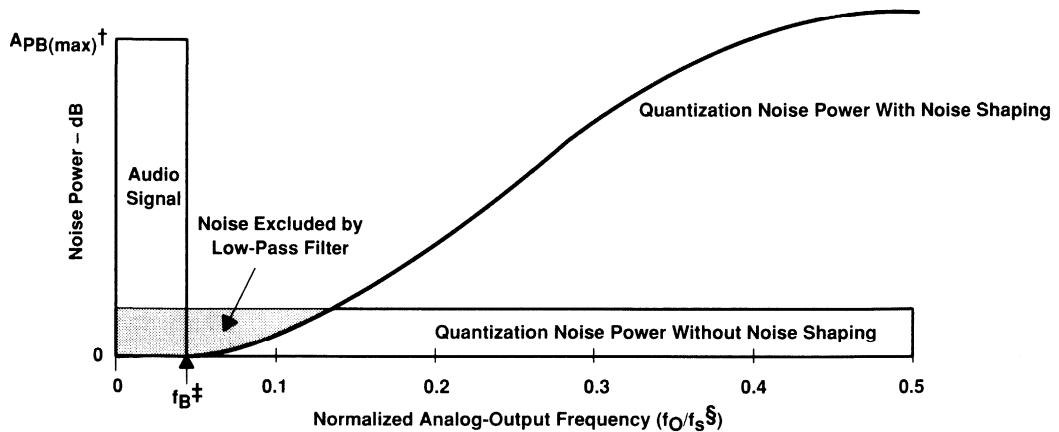


Figure 2-10. DAC Digital Attenuation Operation with Tapered Gain Response

2.15 Sigma-Delta DAC Modulator

The DAC uses a third-order modulator with 32 times oversampling. The DAC provides high-resolution, low-noise performance using a 15-value PWM output as shown in Figure 2–11.



$^\dagger APB(max)$ is the passband maximum amplitude.

$^\ddagger f_B$ is the highest frequency of interest within the baseband.

$^\S f_O$ is the output frequency at the external low-pass filter output.

Figure 2–11. Oversampling Noise Power With and Without Noise Shaping

2.16 DAC Interpolation Filter

The interpolation filter used prior to the DAC increases the digital-data rate from the LRCKD speed to the oversampled rate by interpolating with a ratio of 1:32. The oversampling modulator receives the output of this filter with de-emphasis as an option.

2.17 DAC PWM Output (L2–L1 and R2–R1)

The L2–L1 and the R2–R1 output pairs are PWM signals with the L2–L1 differential pulse duration determining the left-channel analog voltage and the R2–R1 differential pulse duration determining the right-channel analog voltage.

Each DAC left and right output consists of 15 levels of PWM and provides a differential signal as the input to two external differential amplifiers configured as a low-pass filter to produce the left and right audio outputs.

2.18 DAC Control Register Set

Tables 2–3 and 2–4 list the bit functions.

Table 2–3. Attenuation Mode Register†

D16–D5	D4	D3	D2	D1	DESCRIPTION	
0h	-	-	-	-	DAC attenuation (D5 = MSB, D16 = LSB)	Muted
1h	-	-	-	-		Digital attenuation, –60.2 dB
2h	-	-	-	-		Digital attenuation, –54.2 dB
3h	-	-	-	-		Digital attenuation, –50.7 dB
1FFh	-	-	-	-		Digital attenuation, –6.04 dB
200h	-	-	-	-		Digital attenuation, –6.02 dB
201h	-	-	-	-		Digital attenuation, –6.02 dB
3FFh	-	-	-	-		Digital attenuation, –0.01 dB
400h	-	-	-	-		Digital attenuation, 0 dB
-	0	-	-	-		D/F mute
-	1	-	-	-	Muted	
-	-	0	-	-	De-emphasis enable	No de-emphasis
-	-	1	-	-		De-emphasis selected
-	-	-	0	-	DAC register select	Attenuator-mode register
-	-	-	1	-		System-mode register
-	-	-	-	0	DAC mode	Normal
-	-	-	-	1		Factory test only

† The initialization value is 0400h.

Table 2–4. System Mode Register†

D16	D15	D14	D13	D12–D5	D4	D3	D2	D1	DESCRIPTION	
0	-	-	-	-	-	-	-	-	Reserved	
-	0	-	-	-	-	-	-	-	Resynchronize	Off
-	1	-	-	-	-	-	-	-		On
-	-	0	0	-	-	-	-	-	Sample rate/ de-emphasis selection	44.1 kHz
-	-	0	1	-	-	-	-	-		Reserved
-	-	1	0	-	-	-	-	-		48 kHz
-	-	1	1	-	-	-	-	-		32 kHz
-	-	-	-	0	-	-	-	-	Reserved	
-	-	-	-	-	0	-	-	-	Input-data word width	20 bits audio data
-	-	-	-	-	1	-	-	-		16 bits audio data
-	-	-	-	-	-	0	-	-	Input D-data protocol	MSB first
-	-	-	-	-	-	1	-	-		LSB first
-	-	-	-	-	-	-	0	-	DAC register select	Attenuator-mode register
-	-	-	-	-	-	-	1	-		System-mode register
-	-	-	-	-	-	-	-	0	DAC mode	Normal
-	-	-	-	-	-	-	-	1		Factory test only

† The initialization value is 0000h.

2.19 Auto-Resynchronization Functionality

The TLC320AD75C has an auto-resynchronization function to keep the entire conversion cycle for the ADC portion and DAC portion respectively checking the LRCK cycle of the f_s rate. When the ADC is in slave mode, the ADC portion has a window of ± 4 clocks of the internal $64 f_s$ clock to check the LRCK cycle with the f_s rate detecting the rising edge of LRCK within this window. When an error is detected on the LRCK cycle, the ADC conversion cycle is resynchronized with an external LRCK cycle at the next rising edge of LRCK. This resynchronization occurs automatically and the ADC portion continues processing based on the new conversion cycle timing.

The DAC portion has a window of ± 2 clocks of the internal $128 f_s$ clock to check the LRCK cycle detecting the rising edge of the LRCK clock. When an error is detected, the conversion cycle of the DAC is resynchronized with an external LRCK cycle automatically and the DAC portion continues processing based on the new conversion cycle timing. (The external LRCK rate should be the same as the f_s rate. This functionality is to ensure the TLC320AD75C conversion operation even if LRCK has a timing problem due to noise injection for example.)

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage range, AV_{DD} , LV_{DD} (see Note 1)	-0.3 V to 6.5 V
Supply voltage range, V_{DD1} , V_{35A} (see Note 2)	-0.3 V to 6.5 V
Supply voltage range, $PV_{DD(L/R)}$, V_{DD2} , V_{35D} , XV_{DD} (see Note 3)	-0.3 V to 6.5 V
Analog input voltage range, INLP, INLM, INRP, INRM	-0.3 V to $AV_{DD} + 0.3$ V
Digital input voltage range	-0.3 V to $V_{DD1/2} + 0.3$ V
Output voltage range, V_O : L1, L2, R1, R2	-0.3 V to $AV_{DD} + 0.3$ V
Operating free-air temperature range, T_A	-0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Case temperature for 10 seconds	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values for maximum ratings are with respect to AV_{SS} .
 2. Voltage values for maximum ratings are with respect to V_{SS1} .
 3. Voltage values for maximum ratings are with respect to V_{SS2} .

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Analog supply voltage, AV_{DD} (see Note 4)	4.75	5	5.25	V
Digital supply voltage, V_{DD1}	4.75	5	5.25	V
Analog logic supply voltage, LV_{DD}	4.75	5	5.25	V
Reference voltage at REFI		3.2		V
Digital supply voltage, V_{35A} , V_{35D}	3	3.3	5.25	V
Digital supply voltage, V_{DD2}	4.75	5	5.25	V
Digital supply voltage, PV_{DDL} , PV_{DDR}	4.75	5	5.25	V
Clock supply voltage, XV_{DD}	4.75	5	5.25	V
Setup time, SCLKA/SCLKD↑ before LRCKA/LRCKD valid, t_{su1} (see Figure 4–2)	50			ns
Setup time, LRCKA/LRCKD valid before SCLKA/SCLKD↑, t_{su2} (see Figure 4–2)	50			ns
Load resistance at ADOUT, R_L	8			k Ω
Operating free-air temperature, T_A	0		70	°C

NOTE 4: Voltages at analog inputs and outputs and AV_{DD} are with respect to AV_{SS} .

3.3 Electrical Characteristics, $V_{DD} = LV_{DD} = V_{DD1} = V_{DD2} = PV_{DDL} = PV_{DDR} = XV_{DD} = 5\text{ V}$, $V_{35A} = V_{35D} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

3.3.1 Digital Interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2	3.3		V
V_{IH}	High-level input voltage	XIN	4.5	5		V
V_{IL}	Low-level input voltage			0.2	0.8	V
V_{IL}	Low-level input voltage	XIN		0.2	0.8	V
V_{OH}	High-level output voltage	ADOUT	$I_{OH} = 0.4\text{ mA}$	2.6	3.2	V
		512CK	$I_{OH} = 0.4\text{ mA}$	2.6	3.2	
		256CK	$I_{OH} = 0.4\text{ mA}$	4.5	4.9	
		L1, L2, R1, R2	$I_{OH} = 0.4\text{ mA}$	4.5	4.9	
		XOUT	$I_{OH} = 1.2\text{ mA}$	4.5	4.9	
V_{OL}	Low-level output voltage	ADOUT	$I_{OL} = 2\text{ mA}$	0.2	0.4	V
		512CK	$I_{OL} = 2\text{ mA}$	0.2	0.4	
		256CK	$I_{OL} = 2\text{ mA}$	0.2	0.4	
		L1, L2, R1, R2	$I_{OL} = 2\text{ mA}$	0.2	0.5	
		XOUT	$I_{OL} = 1.2\text{ mA}$	0.2	0.5	
I_{IH}	High-level input current, any digital input			0.1		μA
I_{IL}	Low-level input current, any digital input			0.1		μA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

3.3.2 Analog Interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(\text{analog})}$	Analog input voltage, ADC	Differential		6.4		V
		0 to peak		3.2		V
Z_i	Input impedance, ADC			200		$\text{k}\Omega$

3.3.3 ADC Performance, $f_s = 44.1$ kHz, Bandwidth = 22.05 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			20		Bits
DYNAMIC PERFORMANCE					
Signal to noise (EIAJ)	INLP = INRP = 2.5 V dc INLM = INRM = 2.5 V dc	96	100		dB
Dynamic range	- 60 dB input		100		dB
Signal to noise + distortion (THD + N)	- 0.5 dB input		0.0017%	0.003%	
Total harmonic distortion (THD)			0.001%		
Interchannel isolation			120		dB
DC ACCURACY					
Absolute gain error			±0.2		dB
	- 0.5 dB IN		±0.2	±0.5	dB
Interchannel gain mismatch			±0.2		dB
Offset drift			0		LSB/°C

3.3.4 DAC Performance, 20-Bit Mode, $f_s = 44.1$ kHz, Bandwidth = 22.05 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution	See Note 5		20		bits
Signal-to-noise ratio	See Note 5	100	104		dB
Signal-to-noise + distortion (THD + N)	See Note 5			0.0013%	0.0025%

NOTE 5: These specifications are measured at the output (V_O) of the external low-pass filter.

3.3.5 ADC Inputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Input voltage range	Differential		6.4		V
	0 to peak		3.2		
Input impedance			200		k Ω

3.3.6 ADC High-Pass Filter, $f_s = 44.1$ kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband (-3 dB)			0.86		Hz
Passband	5 Hz		-0.12		dB
Group delay			$1/f_s$		s

3.3.7 ADC Decimation Filter, $f_s = 44.1$ kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband ripple	20.03 kHz		±0.01		dB
Stopband attenuation	24.07 kHz	80			dB
Group delay			$25/f_s$		s

3.3.8 DAC Filter Characteristics, $f_s = 44.1$ kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	$f_s = 20$ kHz		± 0.002		dB
Stop-band attenuation	$f_s = 24.1$ kHz	75			dB
Group delay			$29/f_s$		s

3.3.9 Power Supply Current, $f_s = 44.1$ kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DD(A)}$ Power-supply current, analog (ADC)	AV_{DD} and LV_{DD}		29	40	mA
$I_{DD(AD)}$ Power-supply current, digital (ADC)	V_{DD1} and V_{35A}		22	30	mA
$I_{DD(DA1)}$ Power-supply current, digital (DAC)	V_{DD2} and V_{35D}		20	25	mA
$I_{DD(DA2)}$ Power-supply current, PWM/OSC (DAC)	PV_{DDL} , PV_{DDR} , and XV_{DD}		17	25	mA
$I_{DD(AST)}$ Power-down current, analog (ADC)	AV_{DD} and LV_{DD}		250		μ A
$I_{DD(DST)}$ Power-down current, digital (ADC)	V_{DD1} and V_{35A}		150		μ A
P_D Power dissipation			400		mW
$PSRR$ Power-supply rejection ratio	0 to 24 kHz		75		dB
	24 kHz to 2.798 MHz		85		dB

3.4 ADC Switching Characteristics (see Figures 2–1 and 4–1)

PARAMETER	MIN	TYP	MAX	UNIT
f_{MCKI} Input clock frequency, MCKI		11.3	12.8	MHz
$t_d(MDD)$ Delay time, $SCLKA\downarrow$ to $ADOUT$, master mode	0		50	ns
$t_d(MIRD)$ Delay time, $SCLKA\downarrow$ to $LRCKA$, master mode	-20		20	ns
$t_d(SDD1)$ Delay time, $LRCKA$ to $ADOUT$, slave mode			50	ns
$t_d(SDD2)$ Delay time, $SCLKA\downarrow$ to $ADOUT$, slave mode			50	ns

3.5 DAC Timing Requirements (see Figures 4–1 and 4–2, and Note 6)

		MIN	TYP	MAX	UNIT
f_{XIN}	Input frequency, XIN clock		22.6	25.6	MHz
t_{w1}	Pulse duration, SCLKD	155	177		ns
t_{w2}	Pulse duration, SHIFT	100			ns
t_{w3}	Pulse duration, \overline{LATCH}	100			ns
t_{su3}	Setup time, DDATA valid before SCLKD \uparrow	20			ns
t_{h1}	Hold time, DDATA valid after SCLKD \uparrow	20			ns
t_{su4}	Setup time, CDIN valid before SHIFT \uparrow	20			ns
t_{h2}	Hold time, CDIN valid after SHIFT \uparrow	20			ns
t_{su5}	Setup time, \overline{LATCH} \uparrow before SHIFT \uparrow	100			ns
t_{h3}	Hold time, \overline{LATCH} \downarrow after SHIFT \uparrow	80			ns

NOTE 6: All timing measurements were taken at the $V_{DD}/2$ voltage level.

4 Parameter Measurement Information

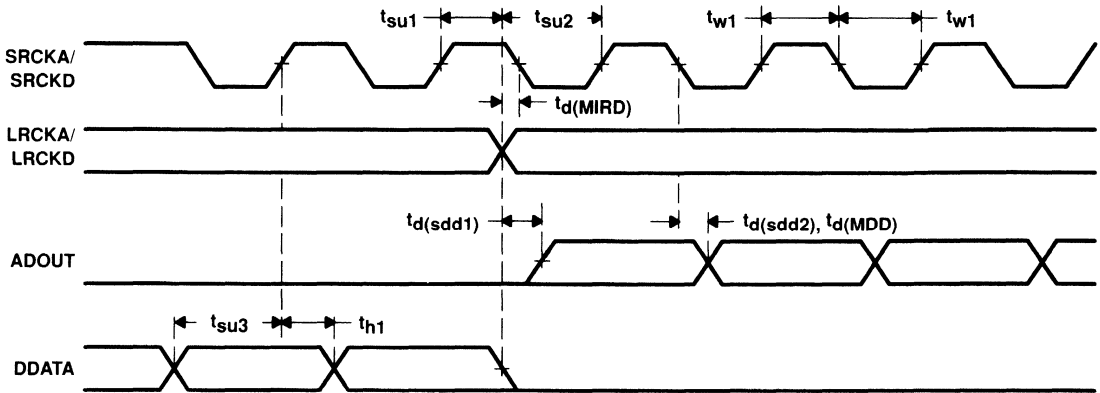


Figure 4-1. ADC Audio-Data Serial Timing

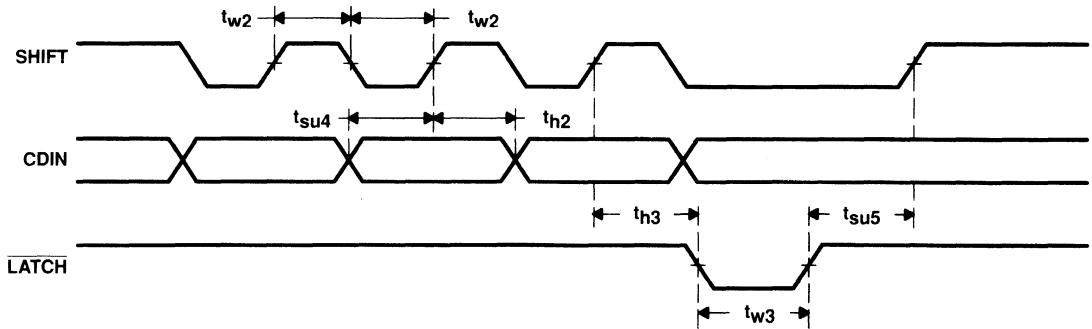


Figure 4-2. DAC Control-Data Serial Timing

5 Application Information

Table 5–1. TLC320AD75C Schematic Components

SYMBOL	DESCRIPTION
C1	220- μ F capacitor
C2	4700-pF capacitor
C3	4700-pF capacitor
C4	220- μ F capacitor
C5	47- μ F capacitor
C6	22- μ F capacitor
C7	0.1- μ F capacitor
C8	100- μ F capacitor
C9	0.1- μ F capacitor
C10	220- μ F capacitor
C12	220- μ F capacitor
C13	18-pF capacitor
C14	12-pF capacitor
C15	220- μ F capacitor
C16	47- μ F capacitor
C17	0.1- μ F capacitor
C18	4700- μ F capacitor
C19	4700- μ F capacitor
C20	200-pF capacitor
C21	100- μ F capacitor
C22	0.1- μ F capacitor
C23	200-pF capacitor
C24	100-pF capacitor
C25	47- μ F capacitor
C26	22- μ F capacitor
C27	220- μ F capacitor
C28	220- μ F capacitor
C29	47- μ F capacitor
C30	100-pF capacitor
C31	47- μ F capacitor
C32	30-pF capacitor
C33	120-pF capacitor
C34	30-pF capacitor
C35	30-pF capacitor
C36	120-pF capacitor

Table 5–1. TLC320AD75C Schematic Components (Continued)

SYMBOL	DESCRIPTION
C37	30-pF capacitor
C38	100- μ F capacitor
C39	100- μ F capacitor
C40	4700-pF capacitor
C41	1200-pF capacitor
C42	1200-pF capacitor
C43	4700-pF capacitor
C44	47- μ F capacitor
C45	47- μ F capacitor
C46	100- μ F capacitor
C47	100- μ F capacitor
C48	47- μ F capacitor
C49	47- μ F capacitor
C50	0.1- μ F capacitor
C51	0.1- μ F capacitor
C52	0.1- μ F capacitor
C53	47- μ F capacitor
C54	220- μ F capacitor
C55	0.1- μ F capacitor
R1	50- Ω resistor
R2	50- Ω resistor
R3	50- Ω resistor
R4	50- Ω resistor
R5	50- Ω resistor
R6	50- Ω resistor
R7	50- Ω resistor
R8	50- Ω resistor
R9	50- Ω resistor
R10	50- Ω resistor
R11	50- Ω resistor
R12	50- Ω resistor
R13	50- Ω resistor
R14	1-M Ω resistor
R15	50- Ω resistor
R16	50- Ω resistor
R17	50- Ω resistor
R18	5-k Ω resistor
R19	620- Ω resistor
R20	10-k Ω resistor
R21	5-k Ω resistor

Table 5–1. TLC320AD75C Schematic Components (Continued)

SYMBOL	DESCRIPTION
R22	4.7-k Ω resistor
R23	5-k Ω resistor
R24	620- Ω resistor
R25	68-k Ω resistor
R26	33-k Ω resistor
R27	18-k Ω resistor
R28	33-k Ω resistor
R29	18-k Ω resistor
R30	68-k Ω resistor
R31	68-k Ω resistor
R32	33-k Ω resistor
R33	18-k Ω resistor
R34	33-k Ω resistor
R35	18-k Ω resistor
R36	68-k Ω resistor
R37	1.5-k Ω resistor
R38	1.5-k Ω resistor
R39	1.5-k Ω resistor
R40	1.5-k Ω resistor
R41	100- Ω resistor
R42	100- Ω resistor
R43	100- Ω resistor
R44	100- Ω resistor
R45	330-k Ω resistor
R46	330-k Ω resistor
R47	10-k Ω resistor
R48	10-k Ω resistor
R49	10-k Ω resistor
R50	10-k Ω resistor

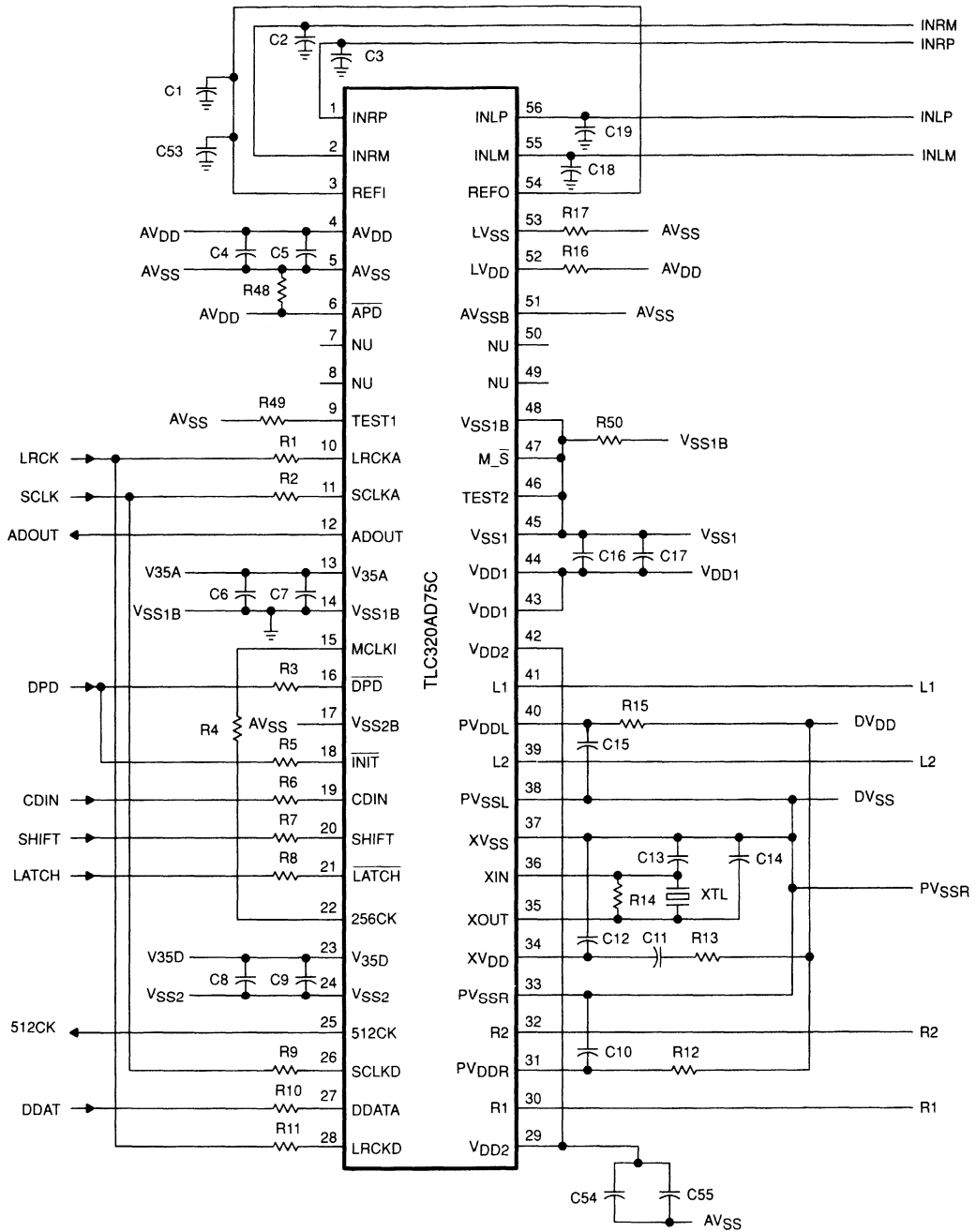


Figure 5-1. TLC320AD75C Application Schematic

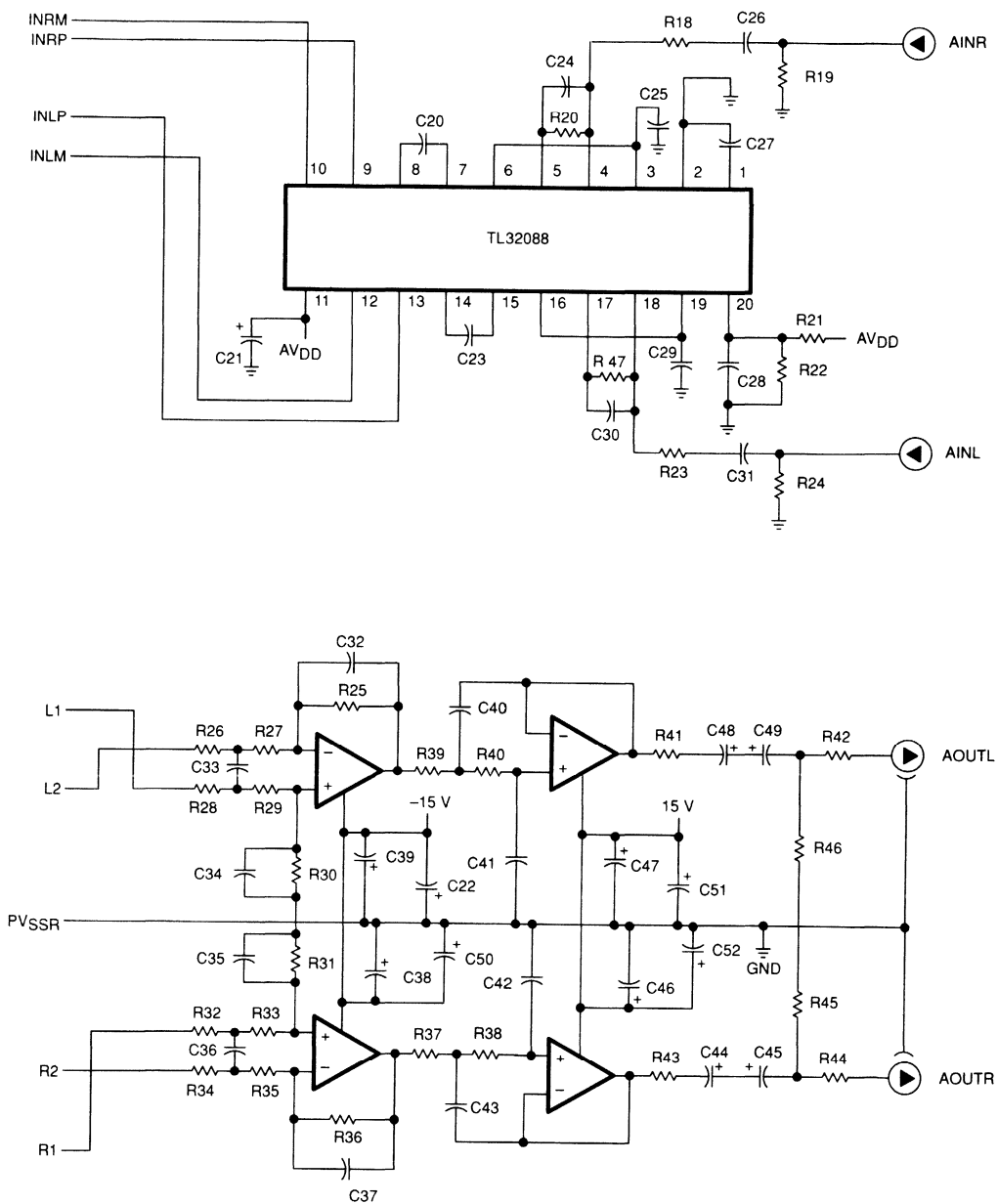


Figure 5-1. TLC320AD75C Application Schematic (Continued)

Table 5–2. A-Weighted Data

FREQUENCY	A WEIGHTING (dB)	FREQUENCY	A WEIGHTING (dB)
25	-44.6 ± 2	800	-0.1 ± 1
31.5	-39.2 ± 2	1000	0 ± 0
40	-34.5 ± 2	1250	0.6 ± 1
50	-30.2 ± 2	1600	1.0 ± 1
63	-26.1 ± 2	2000	1.2 ± 1
80	-22.3 ± 2	2500	1.2 ± 1
100	-19.1 ± 1	3150	1.2 ± 1
125	-16.1 ± 1	4000	1.0 ± 1
160	-13.2 ± 1	5000	0.5 ± 1
200	-10.8 ± 1	6300	-0.1 ± 1
250	-8.6 ± 1	8000	-1.1 ± 1
315	-6.5 ± 1	10000	-2.4 ± 1
400	-4.8 ± 1	12500	-4.2 ± 2
500	-3.2 ± 1	16000	-6.5 ± 2
630	-1.9 ± 1		

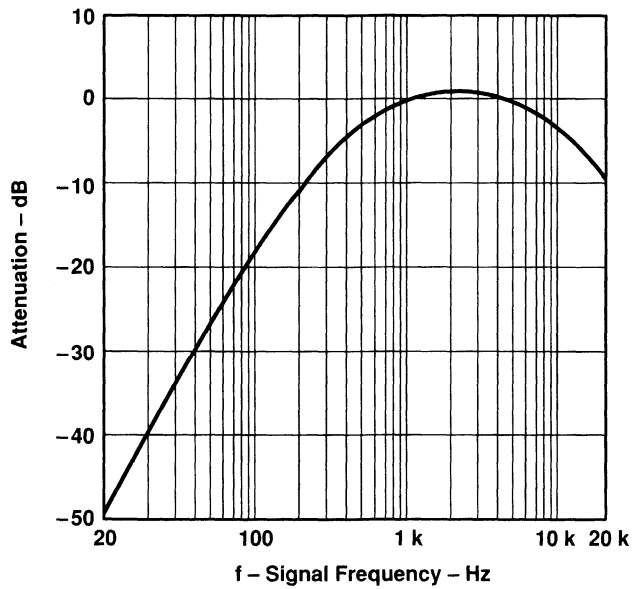


Figure 5–2. A-Weighted Function

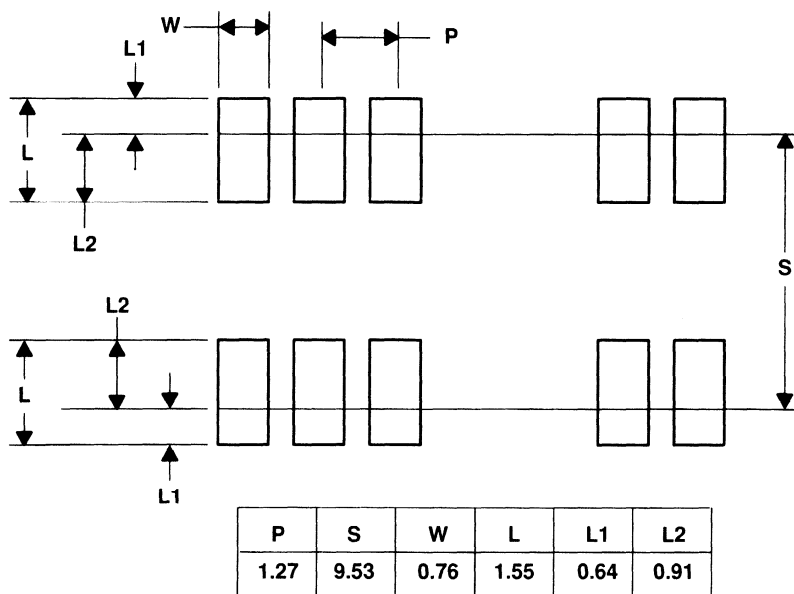
5.1 Circuit And Layout Considerations

The designer should follow these guidelines for the best device performance.

- Separate digital and analog ground planes should be used. All digital device functions should be over the digital ground plane, and all analog device functions should be over the analog ground plane. The ground planes should be connected at only one point to the direct power supply, and this is usually at the connector edge of the board.
- A single crystal-controlled clock should synchronously generate all digital signals.
- All power supply lines should include a 0.1- μ F and a 1- μ F capacitor. When clock noise is excessive, a toroidal inductance of 10 μ H should be placed in series with XV_{DD} before connecting to DV_{DD} .
- The digital input control signals should be buffered when they are generated off of the card.
- Clock jitter should be minimized, and precautions taken to prevent clock overshoot. This minimizes any high-frequency coupling to the analog output.

5.2 PCB Footprint

Figure 5–3 shows the printed-circuit-board (PCB) land pattern for the TLC320AD75C small-outline package.



NOTE A: All linear dimensions are in millimeters.

Figure 5–3. Land Pattern for PCB Layout

TLC320AD80C ***Data Manual***

Audio Processor Subsystem

SLAS141
November 1997



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Contents

<i>Section</i>	<i>Title</i>	<i>Page</i>
1	Introduction	4-541
1.1	Features	4-541
1.2	Applications	4-542
1.3	Functional Block Diagram	4-543
1.4	Terminal Assignments	4-544
1.5	Ordering Information	4-544
1.6	Terminal Functions	4-545
2	Functional Description	4-547
2.1	Audio Input Ports	4-548
2.1.1	Serial PCM Data Ports	4-548
2.1.2	Analog Audio Input Ports	4-551
2.1.3	Audio Source Selection Procedure	4-552
2.1.4	Audio Input Port Mute and Capacitor Precharge Mode	4-553
2.2	Analog Audio Outputs	4-553
2.2.1	Variable Stereo Audio Outputs	4-553
2.2.2	External Stereo Audio Output	4-554
2.2.3	Wideband Multiplexer Output	4-554
2.3	Volume/Balance/Mute Control	4-554
2.3.1	Volume Control	4-554
2.4	Sigma-Delta DAC	4-555
2.4.1	Interpolator/Modulator	4-555
2.4.2	Continuous Time and Switched Capacitor Filters	4-555
2.5	Serial Control Port	4-555
2.5.1	Serial Control Port Description	4-555
2.5.2	Serial Control Command Format	4-556
2.5.3	Power-Down/Reset	4-557
2.6	Software Interface	4-557
3	Specifications	4-559
3.1	Absolute maximum ratings over operating free-air temperature range	4-559
3.2	Recommended Operating Conditions	4-559
3.2.1	Static Digital Specifications, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} + 5\%$	4-559
3.2.2	Power Supplies, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} + 5\%$	4-560

Contents (Continued)

<i>Section</i>	<i>Title</i>	<i>Page</i>
3.3	Electrical Characteristics	4-560
3.3.1	Analog Audio Channel Performance, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} + 5\%$	4-560
3.3.2	Volume Control and Output Drivers Performance, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} + 5\%$	4-561
3.3.3	Monaural Decoder Performance, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} + 5\%$, $f_S = 32\text{ kHz}$	4-561
3.3.4	Wideband Multiplexer Performance, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} + 5\%$	4-562
3.3.5	PCM Audio Channel Performance, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} + 5\%$, $f_S = 48\text{ kHz}$	4-562
3.3.6	DAC Interpolation Filter, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} + 5\%$, $f_S = 48\text{ kHz}$	4-562
3.4	Timing Requirements, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} + 5\%$, $f_S = 48\text{ kHz}$...	4-563
3.4.1	Serial PCM Data Port	4-563
3.4.2	Serial Control Interface, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} + 5\%$,	4-563
4	Application Information	4-565
4.1	Schematic	4-567
Appendix A	Register Set	4-569

List of Illustrations

<i>Figure</i>	<i>Title</i>	<i>Page</i>
2-1	Philips I ² S Protocol Serial PCM Data Format	4-549
2-2	Left-Justified Serial PCM Data Format	4-550
2-3	Right-Justified Serial PCM Data Format	4-551
2-4	Left-Justified DSP Serial PCM Data Format (Inverted BCLK)	4-551
2-5	Serial Interface Timing	4-546
3-1	Serial Port Timing	4-564
3-2	SPI Serial Control Port Timing	4-566
4-1	De-Emphasis 75 μ s Low-Pass Filter at 2.12 kHz	4-565
4-2	Application Schematic	4-566

List of Tables

<i>Table</i>	<i>Title</i>	<i>Page</i>
2-1	Serial Port Signals	4-549
2-2	Control Register 00h Allowable Settings	4-550
2-3	Master Clock (MCLK) Rates Supported For Various Sample Rates (LRCLK) ..	4-551
4-1	Digital Interface Capacitive Loading, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} + 5\%$, $f_S = 48\text{ kHz}$	4-565

1 Introduction

The TLC320AD80 is an audio processing subsystem designed to meet the audio needs of a broad range of set-top box applications. This device includes a high-performance stereo audio DAC, analog volume and balance control, analog TV monaural decoder, de-emphasis filter, and an analog wide-band multiplexer. The sigma-delta DAC performs data conversion with 85-dB performance. The architecture provides much flexibility, giving the user the option to use all or a subset of the functional blocks.

There are two serial digital interfaces for digital audio data and four analog audio inputs. The analog output of the device can be selected to be the output of the DAC, the output of the TV baseband filter, or pass-through of one of the analog inputs.

The digital interfaces enable ease of use by providing compatibility with the industry standard I²S digital audio port, and with the SPI™ serial control interface. In addition, the digital audio interface supports additional interface protocols.

1.1 Features

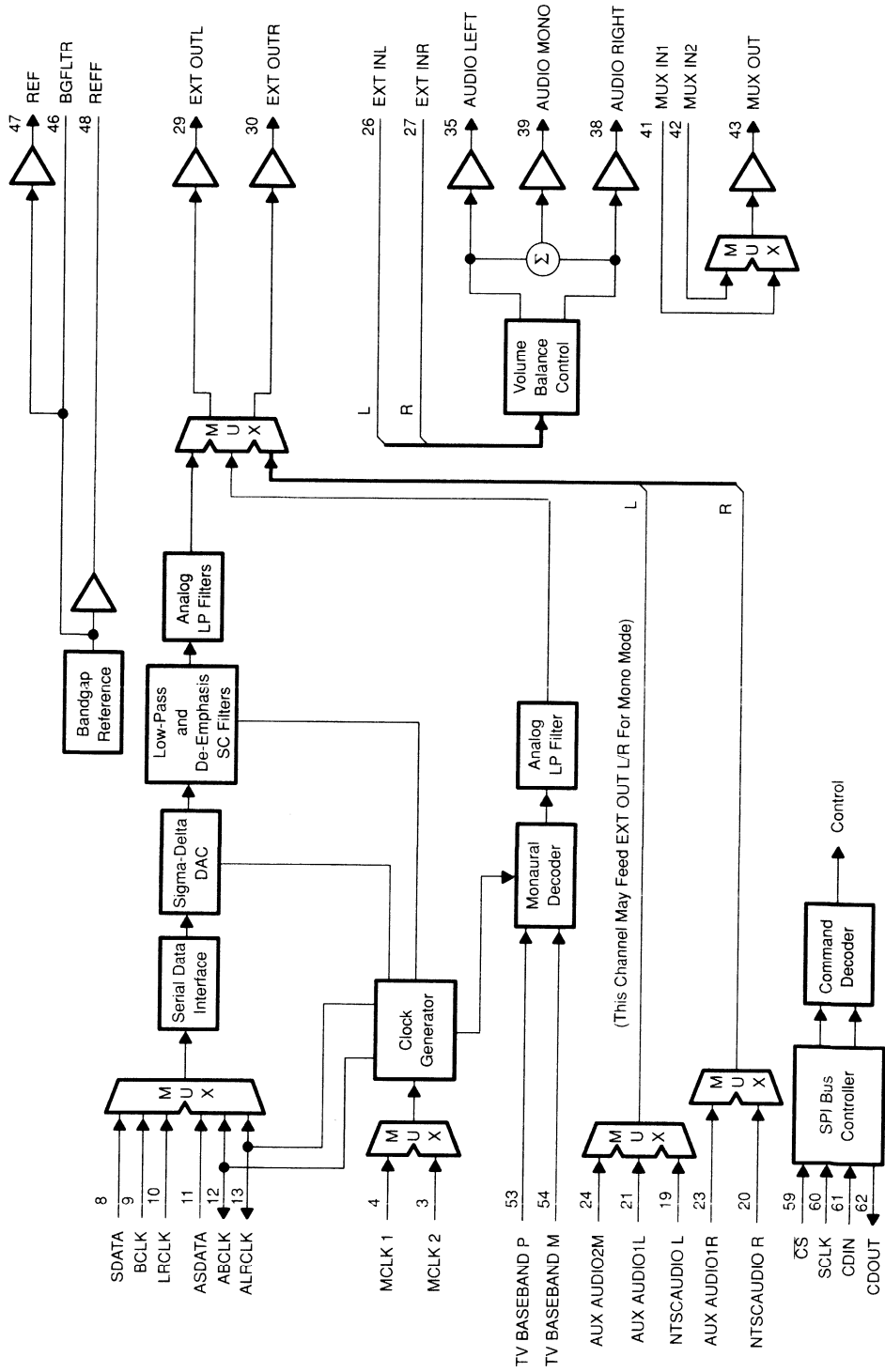
- Highly Integrated Analog Audio Functions
- Flexible Architecture Allows Variable Interconnects Between Functions
- Sigma-Delta DAC With 16-Bit Resolution and 82-dB Performance Typical
- Internal Monaural Decoder for TV Baseband Audio
- Four Analog Audio Inputs: Two Stereo and Two Mono
- Volume and Balance Control: 69 Step at 1 dB per Step With Mute
- Selectable 50/15 ms De-Emphasis Analog Filter
- Uncommitted Wide-Band Analog 2:1 Multiplexer
- Multiplexed Analog Output can Select the Output of the DAC or Analog Data Pass-Through From One of the Analog Audio Inputs
- Two Flexible Digital Serial Data Ports (Philips I²S Protocol, Left-Justified, and Right-Justified Formats)
- SPI Bus-Compatible Serial Control Port
- Sample Rates Supported in DAC: 8 kHz to 48 kHz
- Digital Serial Ports Support 16-Bit or 18-Bit PCM Digital Audio Data Format
- Analog Stereo Inputs can be Configured as Mono Inputs Through the Left Channel
- Analog Output With 600-Ω Load Drive and Short Circuit Protection
- Internal Voltage Reference
- TTL/CMOS Compatible
- Single 5-V Power Supply, 64-Pin TQFP Package

SPI™ is a trademark of Motorola Inc.

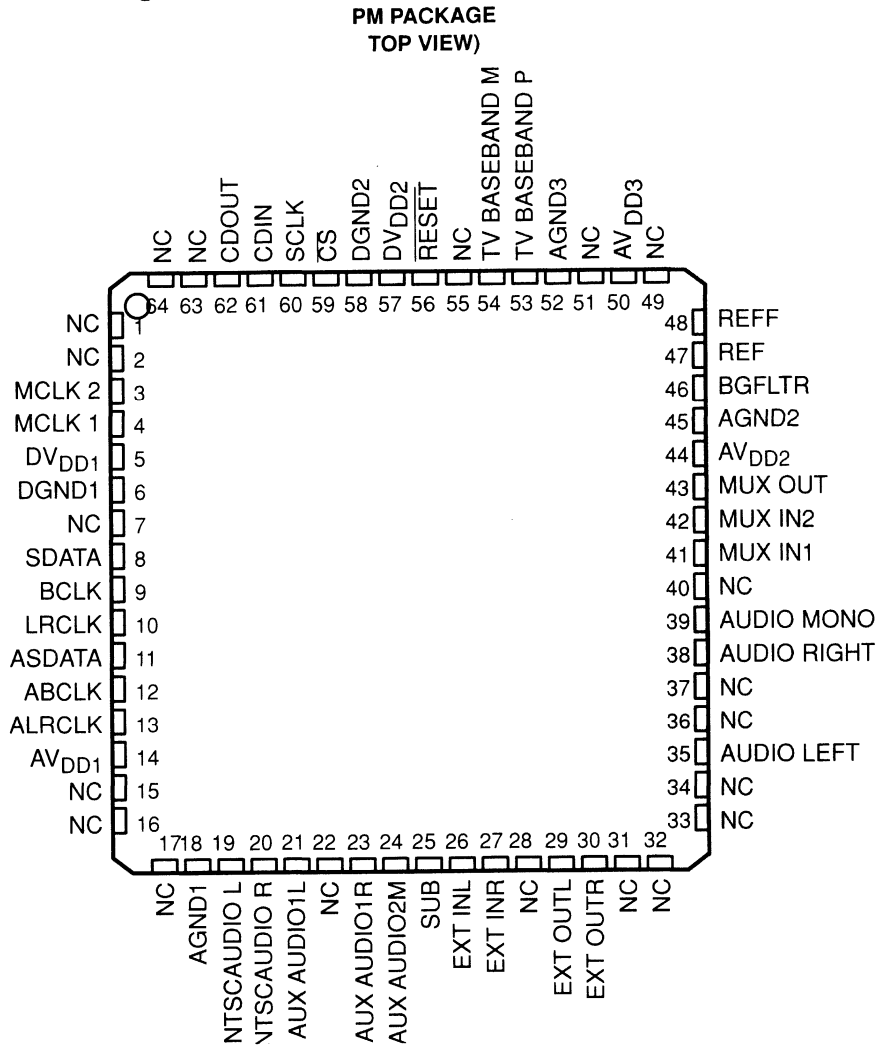
1.2 Applications

- Direct Broadcast Satellite (DBS) Set-Top Boxes
- Digital Cable or Telco Set-Top Boxes
- High Definition Television (HDTV), Digital Audio Broadcast Receivers
- Video Laser Disks, Video CD, and CD-I Players

1.3 Functional Block Diagram



1.4 Terminal Assignments



1.5 Ordering Information

T _A	PACKAGE
	CHIP CARRIER (PM)
0°C to 70°C	TLC320AD80CPM

1.6 Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND1	18	I	Analog ground for sigma-delta DAC
AGND2	45	I	Analog ground for analog audio output drivers
AGND3	52	I	Analog ground for bandgap reference
AUDIO LEFT	35	O	Left channel line-level analog audio output. The AUDIO LEFT output driver provides line level signals (1 V _{rms} max) for line output. The AUDIO LEFT output is capable of driving a 600-Ω load.
AUDIO MONO	39	O	Monaural variable line-level analog audio output. The AUDIO MONO output signal is the sum of the AUDIO RIGHT and AUDIO LEFT outputs divided by 2. The output is capable of driving a 10-kΩ load.
AUDIO RIGHT	38	O	Right channel variable line-level analog audio output. The AUDIO RIGHT output driver provides line level signals (1 V _{rms} max) for line output. The AUDIO RIGHT output is capable of driving a 600-Ω load.
AUX AUDIO1L	21	I	Left channel auxiliary analog audio input 1
AUX AUDIO1R	23	I	Right channel auxiliary analog audio input 1
AUX AUDIO2M	24	I	Mono channel auxiliary analog audio input 2
ABCLK	12	I/O	Auxiliary serial bit clock input. The ABCLK bit clock signal clocks the serial PCM data (ASDATA) into the TLC320AD80.
ALRCLK	13	I/O	Auxiliary left/right channel indicator. ALRCLK signifies whether the serial PCM data is associated with the left channel DAC or the right channel DAC.
ASDATA	11	I	Auxiliary serial PCM data input port. ASDATA can be configured as 16 or 18 bits with the most significant bit (MSB) first, 2's complement format.
AV _{DD1}	14	I	Analog 5-V power supply for the sigma-delta DAC
AV _{DD2}	44	I	Analog 5-V power supply for the analog audio output drivers
AV _{DD3}	50	I	Analog 5-V power supply for the bandgap reference
BCLK	9	I	Serial bit clock input. BCLK clocks the serial PCM data (SDATA) into the device.
BGFLTR	46	I	Bandgap reference filter. BGFLTR provides for noise filtering of the internal bandgap reference (2.25 V). BGFLTR requires a 0.1 μF capacitor to analog ground. This voltage node should be loaded only with a high-impedance dc load.
CDIN	61	I	SPI bus serial control data input. Data is transferred MSB first. CDIN specifies the channel specific attenuation and mute, serial PCM data format and rates, de-emphasis mode, audio input port selection, and stereo or monaural analog inputs.
CDOUT	62	O	SPI bus serial control data output port
CS	59	I	SPI bus chip select input (active low)
DGND1	6	I	Digital ground for the sigma-delta DAC
DGND2	58	I	Digital ground for the serial interface
DV _{DD1}	5	I	Digital 5-V power supply for the sigma-delta DAC
DV _{DD2}	57	I	Digital 5-V power supply for the serial interface
EXT INL	26	I	Left channel external analog audio input
EXT INR	27	I	Right channel external analog audio input

1.6 Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EXT OUTL	29	O	Left channel fixed line level analog audio output. The EXT OUTL output driver provides line level signals ($1 V_{RMS}$ max) for line output. The EXT OUTL output is capable of driving a 10-k Ω load.
EXT OTR	30	O	Right channel fixed line level analog audio output. The EXT OTR output driver provides line level signals ($1 V_{RMS}$ max) for line output. The EXT OTR output is capable of driving a 10-k Ω load.
LRCLK	10	I	Left/right channel indicator. LRCLK signifies whether the serial PCM data (SDATA) is associated with the left channel DAC or the right channel DAC.
MCLK 1	4	I	Master clock, sigma-delta DAC oversampling clock input. The TLC320AD80 defaults to MCLK 1. The TLC320AD80 can run off of MCLK 1 or MCLK 2.
MCLK 2	3	I	Auxiliary master clock, DAC oversampling clock input. The TLC320AD80 can run off of either MCLK 1 or MCLK 2.
MUX IN1	41	I	Wideband multiplexer input 1
MUX IN2	42	I	Wideband multiplexer input 2
MUX OUT	43	O	Wideband multiplexer output. The multiplexer can output one of two inputs (MUX IN1, MUX IN2) or perform an audio mute. The MUX OUT output is capable of driving a 600- Ω load.
NTSCAUDIO L	19	I	Left channel NTSC analog audio input
NTSCAUDIO R	20	I	Right channel NTSC analog audio input
REF	47	I	Voltage reference. The REF voltage provides a common mode reference of 2.25 V for all audio output drivers. The REF voltage can also be used as an external common mode reference with the restriction that only a high-impedance dc load should be applied. REF should be bypassed with a 0.1 μ F capacitor.
REFF	48	I	Voltage reference filter. REFF is provided for low-pass filtering of the internal voltage reference (3.2 V) for the sigma-delta DAC. REFF should be bypassed with 10 μ F and 0.1 μ F capacitors. This voltage node should be loaded only with a high-impedance dc load.
RESET	56	I	Power down/reset. When RESET is held low, the TLC320AD80 is placed in a power-down state. The TLC320AD80 is reset on the rising edge of RESET.
SCLK	60	I	SPI bus serial clock input. Control input data (CDIN) must be valid on the rising edge of SCLK. SCLK may be continuous or gated.
SDATA	8	I	Serial PCM data input port. SDATA can be configured as 16 or 18 bits with the MSB first, 2s complement format.
SUB	25	I	Substrate ground connected to AGND plane.
TV BASEBAND P	53	I	TV aural baseband multiplex noninverting input
TV BASEBAND M	54	I	TV aural baseband multiplex inverting input

2 Functional Description

The TLC320AD80 is an audio processing subsystem that includes a high-performance stereo audio DAC, analog volume and balance control, analog TV monaural decoder, de-emphasis filter, and an analog wide-band multiplexer. The sigma-delta DAC performs data conversion with 85-dB performance. The architecture provides much flexibility with the option to use all or some of the functional blocks.

The digital interfaces enable ease of use by providing compatibility with the industry standard I²S digital audio port, and with the SPI serial control interface. The digital audio serial interface also supports additional interface protocols and 16-bit or 18-bit data formats.

The analog interface provides much flexibility. Four analog audio sources are supported including two stereo audio sources, a TV baseband audio signal, and one mono source. In addition, the inputs to the volume and balance and the wideband mux are external to the chip. This allows the option to connect intermediate analog functions between functional blocks. As a default, these connections should include dc blocking capacitors to eliminate analog offsets. Finally, the primary analog output of the device is provided by a multiplexer. This allows selection from one of the following sources: the DAC, the output of the monaural decoder, or pass-through of one of the analog inputs. The multiplexer also allows the two stereo inputs to be used as mono inputs. In this case, the left channel is routed into both the left and right outputs.

The TLC320AD80 integrates several audio functions into one device. Following is a brief description of the device. Subsections of this chapter describe the details. The functions include:

- Sigma-delta stereo DAC
- 50/15 ms de-emphasis analog filter
- Analog volume and analog balance control
- Output multiplexer to select between the various audio sources
- TV baseband monaural audio decoder
- Additional uncommitted 2:1 mono multiplexer
- Two flexible digital audio input ports
- A SPI compatible serial control interface
- Voltage reference with buffered output

The DAC audio input can be selected from either of the digital serial ports. Several sample rates are supported. In addition, a software-selectable 50/15 μ s de-emphasis filter is provided in the analog section of the DAC. The output of the DAC is fed into the output multiplexer. The aforementioned serial ports provide several timing protocols (Phillips I²S, left justified, right justified, DSP mode), each with 16-bit or 18-bit data formats.

The TV baseband monaural decoder receives differential audio inputs from two external terminals (TV BASEBAND P, TV BASEBAND M). The output of this decoder is fed into the output multiplexer. The decoder is a differential eighth order elliptic switched capacitor filter used to reject high frequency audio signals that may be present in the NTSC audio broadcast multiplex. Proper operation of this section requires that the master clock (MCLK) correspond to an audio sample rate of 32 kHz.

The analog volume and balance control receives inputs from external terminals. The output of this section provides independent stereo and mono outputs on three terminals. All three outputs are also short-circuit protected. The functionality of this block provides either ganged or individual gain control for the left and the right channel. There are 69 volume settings which range from 6 dB to -62 dB of gain in 1 dB/step increments.

The external connections to this function allow for dc blocking capacitors to be included on the board, thus eliminating dc offsets present on the source. A typical implementation would connect the output of the analog multiplexer (EXT OUTL, EXT OUTR) to the input of this function.

The analog output multiplexer allows selection of the several analog sources input to the device. One of these audio sources is the output of the DAC. The others are the output of the TV monaural decoder, either of the two stereo analog inputs, or auxiliary mono input. Mono sources are sent to both right and left channels. The output of this multiplexer provides stereo outputs on two terminals, each with 10 k Ω drive capability. Both terminals are short-circuit protected.

The master clock for the device is derived from an external clock source. Control register 01h selects MCLK 1, or MCLK 2 to be the master clock source. This clock is then used to clock the DAC, the digital audio serial ports, and the monaural decoder, switched-capacitor filter. The serial ports can be selected independent from the MCLK 1 and MCLK 2 selection. However, the clock rate of the selected clock source partly determines the sampling rate of the device. Refer to Table 2–1, and the description of control register 00h.

The TLC320AD80 also provides an uncommitted 2:1 mono analog multiplexer. The inputs and outputs of this device are connected to external terminals.

The voltage reference is used internally for the analog sections of the device. The external terminals must be connected to decoupling capacitors. In addition, the reference terminals can be externally buffered for use with external support circuitry.

2.1 Audio Input Ports

The audio inputs consist of: two digital serial interfaces, two stereo analog inputs, one analog TV baseband audio input, and one mono analog input. The TV baseband audio input is a differential input. All other analog inputs are single-ended.

The audio input is selected by programming control register 01h. Only one of these inputs is active at any one time. The others are disabled. That is, if an analog input is selected, then the digital serial interfaces are inactive.

The two digital serial interfaces provide the input to the DAC through a digital multiplexer. These interfaces support several serial protocols including I²S, left-justified, and right-justified formats. The data format is 16-bit or 18-bit precision, with MSB first. There is also a DSP-compatible mode available.

All single-ended analog inputs can be passed through to the main output of the device by means of an analog multiplexer. The differential TV baseband audio input (TV BASEBAND P, TV BASEBAND M) feeds a monaural decoder which then feeds the same multiplexer.

2.1.1 Serial PCM Data Ports

The device includes two serial ports used to transfer digital audio data from an external digital source to the DAC: The AUX serial port (ASDATA, ABCLK, and ALRCLK) can be configured to operate in either master or slave mode. The main serial PCM port (SDATA, BCLK, and LRCLK) always operates in the slave mode. Note, that the only exclusion is that the AUX port does not support the DSP mode when configured as master.

Configuration of these serial ports is accomplished by means of the SPI-compatible control serial interface port. Specifically, the protocol (Philips I²S protocol, left-justified, right-justified, or DSP mode), and data format (16-bit or 18-bit) are selected by programming control register 00h. The multiplexer selection is programmed with control register 01h which will also enable or disable these serial data ports.

2.1.1.1 Main Serial PCM Port

The main serial PCM (SDATA, BCLK, and LRCLK) port always operates in slave mode. That is, all clocks are inputs to the device. The LRCLK and BCLK clocks must be synchronous with MCLK.

A typical set-top-box application would connect this input to an MPEG/AC3 audio decoder.

2.1.1.2 Aux Serial PCM Data Port

The aux serial port (ASDATA, ABCLK, and ALRCLK) operates in either the master or slave mode. The master mode supports all the documented interface protocols with the exception of the DSP mode. The slave mode supports all documented protocols without exception.

The aux serial PCM data port receives non-compressed data from an auxiliary audio source. The slave mode is identical to the clock mode of main serial PCM port. In the master mode, this device generates the required BCLK and LRCLK clocks synchronously with the applied MCLK.

2.1.1.3 Serial Interface Protocols Supported

The serial ports comprise the signals in Table 2–1.

Table 2–1. Serial Port Signals

MAIN PORT	AUXILIARY PORT	DESCRIPTION
SDATA	ASDATA	PCM audio data. 16-bit or 18-bit data precision
BCLK	ABCLK	Bit clock. Rate is equal to 32x, 48x, or 64x the sample rate
LRCLK	ALRCLK	Left/right clock. Rate is equal to the sample rate

Figure 2–1 through Figure 2–4 are for a bit clock (BCLK) set to 48 × the sample rate and 16-bit data precision. All serial protocols supported are shown.

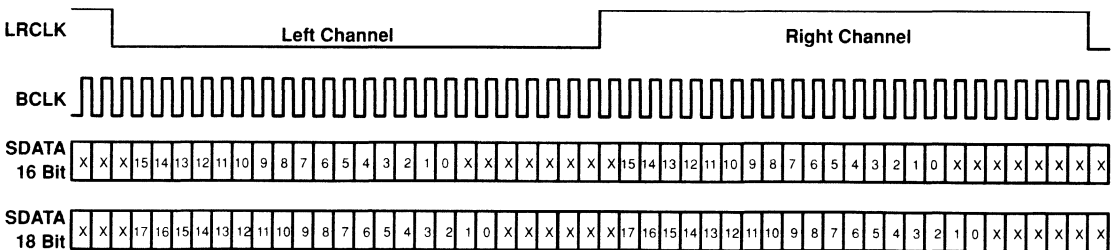


Figure 2–1. Philips I²S Protocol Serial PCM Data Format

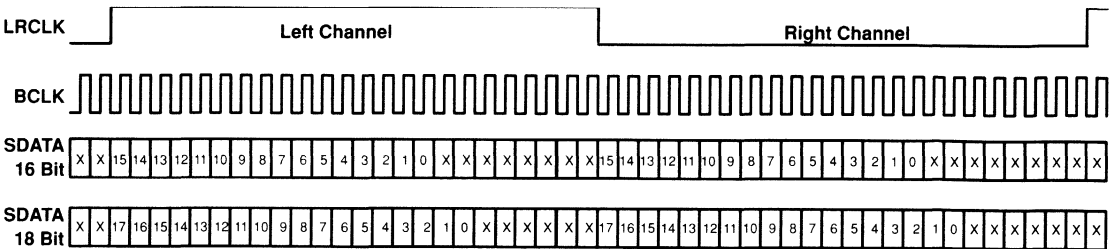


Figure 2–2. Left-Justified Serial PCM Data Format

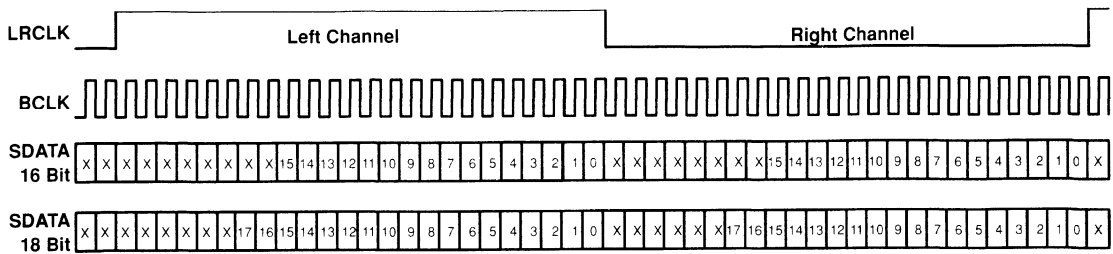


Figure 2–3. Right-Justified Serial PCM Data Format

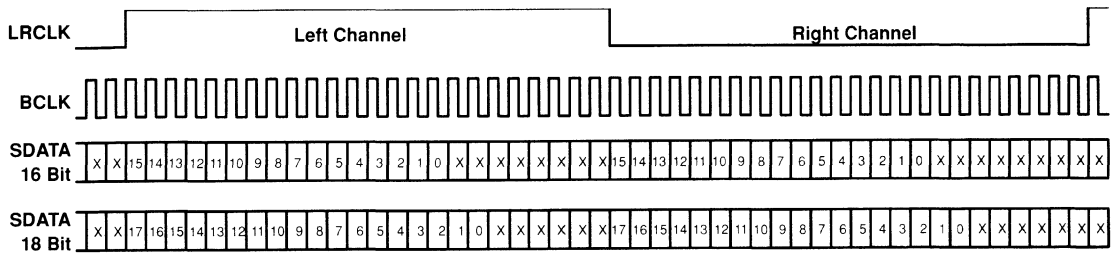


Figure 2–4. Left-Justified DSP Serial PCM Data Format (Inverted BCLK)

Table 2–2. Control Register 00h Allowable Settings

PRECISION	MCLK	BCLK	DIVIDER	JUSTIFICATION
16-Bit	256 ×	64 ×	4	Left, right, I ² S
16-Bit	256 ×	32 ×	8	Left, right, I ² S
16-Bit	384 ×	64 ×	6	Left, right, I ² S
16-Bit	384 ×	48 ×	8	Left, right, I ² S
16-Bit	384 ×	32 ×	12	Left, right, I ² S
16-Bit	512 ×	64 ×	8	Left, right, I ² S
16-Bit	512 ×	32 ×	16	Left, right, I ² S
16-Bit	256 ×	64 ×	4	Left, right, I ² S
18-Bit	384 ×	64 ×	6	Left, right, I ² S
18-Bit	384 ×	48 ×	8	Left, right, I ² S
18-Bit	512 ×	64 ×	8	Left, right, I ² S

Table 2-3. Master Clock (MCLK) Rates Supported For Various Sample Rates (LRCLK)

LRCLK (kHz)	MCLK (MHz)		
	256 × LRCLK	384 × LRCLK	512 × LRCLK
48	12.288	18.432	N/A
44.1	11.2896	16.9344	N/A
32	8.192	12.288	N/A
24	6.144	9.216	N/A
22.05	5.6448	8.4672	N/A
16	N/A	N/A	8.192
12	N/A	N/A	6.144
11.025	N/A	N/A	5.6448
8	N/A	N/A	4.096

2.1.2 Analog Audio Input Ports

The main analog audio input ports consist of two stereo audio inputs, one mono audio input, and one TV baseband audio input. The stereo inputs and the mono input can be passed through to the output (EXT OUTL, EXT OUTF) by means of the analog output multiplexer. The TV baseband audio is a differential input that feeds an internal monaural decoder before it is sent to the same output multiplexer.

The secondary analog audio inputs consist of one stereo input to the volume and balance control and two mono inputs to the wideband multiplexer. These inputs are intended primarily for interconnecting functional blocks by means of dc blocking capacitors. However, it also provides the user with the ability to combine internal functions with additional external analog functions. All inputs should be connected through dc-blocking capacitors.

2.1.2.1 Stereo Analog Input Ports

The two stereo audio input ports (NTSCAUDIO L, NTSCAUDIO R, AUX AUDIO1L, AUX AUDIO1R) are single-ended inputs. These inputs are sent to the output multiplexer without additional analog processing. The output of the multiplexer can be externally connected to another functional block such as the volume and balance control. These stereo inputs also have the ability to function in mono mode. In this mode, the left channel of the selected input is sent to both the left and right outputs (EXT OUTL, EXT OUTF). Control register 01h is used to program the mono or stereo mode for these inputs.

A typical application would connect the NTSC audio input to the output of a MTS stereo decoder. The AUX AUDIO1 port would be connected to an alternate nonbroadcast audio source.

2.1.2.2 Mono Analog Input Port

The one mono audio port (AUX MONO 2M) is a single-ended input. This input is sent to the output multiplexer without additional analog processing. However, the output of the multiplexer can be externally connected to another functional block such as the volume and balance control. This input is internally applied to both the left and right audio channels.

A typical application would connect the AUX MONO 2M input to receive the second audio program (SAP) channel output of an MTS stereo decoder.

2.1.2.3 TV Audio Baseband Input

The TV baseband audio audio port (TV BASEBAND P, TV BASEBAND M) is a mono differential input. This input feeds an internal a monaural decoder used to extract the mono (left and right) signal from the TV baseband. The output of the monaural decoder is sent to the output multiplexer.

The monaural decoder is a differential, eighth-order switched-capacitor filter. Proper operation requires that the master clock (MCLK 1 or MCLK 2) and control register settings correspond to a sample rate of 32 kHz. These settings ensure the filter requirements for proper stopband rejection. The purpose of the filter is to reject specific signals from the NTSC audio broadcast multiplex. The signals rejected include the 15.73425 kHz BTSC stereo pilot tone, left and right stereo subcarriers, SAP channel, Pro channel, and data channel as allowed by the FCC.

A typical connection would connect this input to the output of a TV IF detector. Therefore, composite TV aural baseband signal would be demodulated by the TV analog IF detector (without an MTS stereo decoder) and then input to the TLC320AD80.

A passive single pole low-pass filter with a 3-dB bandwidth of 2.12 kHz should be connected to the TV baseband differential input to provide the required 75 μ s de-emphasis filter. This external filter also acts as an anti-aliasing filter for the internal switched capacitor monaural decoder.

2.1.2.4 Volume and Balance External Analog Input

This stereo audio input (EXT INL, EXT INR) is primarily intended to receive the external stereo audio output (EXT OUTL, EXT OUTR) of the TLC320AD80. However, the user has the option to connect additional analog functions in between these ports. The input should be ac-coupled to remove dc offsets that may be present in the incoming signal.

The input resistance of this port varies as a function of the volume control setting. The input resistance is lowest (≥ 20 k Ω) when the volume control is at its maximum setting of 6 dB. The input resistance is reduced to approximately 2 k Ω when the capacitor precharge mode is selected from control register 01h. The capacitor precharge mode is provided to charge and discharge the external ac coupling capacitor quickly, overriding the input resistance of the volume control setting.

2.1.2.5 Wideband Multiplexer Analog Inputs

The MUX IN1 and MUX IN2 signals are the analog inputs to an uncommitted wideband multiplexer. A typical application would use this multiplexer to provide source selection for the input to a channel 3/4 RF modulator.

2.1.3 Audio Source Selection Procedure

Changing the audio source selection between any two of the six audio inputs can produce an audible click depending on the difference between the corresponding signal values at the time of switching. This difference between signals could be as large as 2.8 V peak-to-peak which would produce a very loud audible click. This audible click can be eliminated on the variable audio outputs (AUDIO RIGHT, AUDIO LEFT, and AUDIO MONO) by using the zero crossing mute function in conjunction with source selection changes. This procedure will not eliminate audible clicks on the fixed audio outputs (EXT OUTR, EXT OUTL) since the zero crossing mute function is located in the volume control block.

Prior to each audio source selection change, the audio output should be muted by writing 00h to volume control register 03h. The output signal follows the currently selected audio input until the next zero crossing occurs which activates the mute. After a recommended time delay of 4096 LRCLK cycles, the audio source can be changed by writing to control register 01h. The capacitor precharge mode and the audio input port mute should also be enabled by setting bit D1 to 1 and clearing bit D0 to 0 of control register 01h. After a second recommended time delay of 512 LRCLK cycles, the precharge mode and audio input port mute should be disabled and then the audio can be unmuted by restoring the original volume control setting to control registers 03h and 04h. The output signal remains muted until the next zero crossing occurs and then follows the newly selected audio input. The second delay time of 512 LRCLK cycles is required to allow

enough time for the voltage across the capacitors connecting the external stereo output to the external stereo input to reach a steady state condition.

A similar approach is required to prevent audible clicks on the output of the wideband multiplexer. Prior to each multiplexer input selection change, the multiplexer output should be muted by clearing bit D5 to 0 of control register 02h. The output signal follows the currently selected multiplexer input until the next zero crossing occurs which activates the mute. After a recommended time delay of 4096 LRCLK cycles, the multiplexer input selection can be changed by writing to bit D2 of control register 01h. The multiplexer output can then be unmuted by setting bit D5 to 1 of control register 02h. The output signal remains muted until the next zero crossing occurs and then follows the newly selected multiplexer input.

2.1.4 Audio Input Port Mute and Capacitor Precharge Mode

The sigma-delta DAC and the monaural decoder may introduce offset errors that could cause audible clicks or pops to occur during volume control changes. To prevent this audible noise, the external audio output (EXT OUTL, EXT OUTF) should be connected to the external audio inputs (EXT INL, EXT INR) through ac coupling capacitors to remove this offset error.

During source selection changes, sufficient time needs to be provided to allow the voltage across these external capacitors to reach a steady state condition before returning the audio to an unmuted condition. In order to minimize this required settling time, the input resistance of the external audio inputs can be reduced by a factor of 10 by selecting the capacitor precharge mode. The input resistance of this port normally varies as a function of the volume control setting. The input resistance is lowest ($\geq 20 \text{ k}\Omega$) when the volume control is at its maximum setting of 6 dB. When the capacitor precharge mode is selected by setting control register 01h to 1, the input resistance is reduced to approximately $2 \text{ k}\Omega$.

The audio input port mute should be enabled when using the capacitor precharge mode by clearing bit D0 of control register 01h to 0. When the audio input port mute is enabled, the serial PCM audio data is disabled (forced to 0) at the input to the sigma-delta DAC, the differential input to the monaural decoder is shorted, and the remaining analog audio inputs are muted. This removes the signal content but not the offset error of a particular audio channel which is necessary in the capacitor precharge mode since the time constant may be insufficient to find the long term average of the selected audio signal.

The audio input port mute feature may also be used in conjunction with the volume control mute to provide increased audio mute attenuation for the serial PCM audio inputs. This improved mute attenuation occurs following 30 LRCLK cycles when the 0 input data propagates to the output of the sigma-delta DAC. The serial PCM audio data is enabled and disabled at the beginning of an audio sample period (rising edge of LRCLK) for an audio input port mute or unmute operation. The serial PCM data must be re-enabled prior to requesting an unmuted volume control setting to provide the audio signal necessary to perform a zero crossing unmute at the volume control stage.

2.2 Analog Audio Outputs

The TLC320AD80 analog outputs consist of two stereo outputs and two mono outputs. All are single-ended analog outputs.

2.2.1 Variable Stereo Audio Outputs

The variable stereo audio output (AUDIO LEFT, AUDIO RIGHT) provides the output of the volume and balance functional block. This output is intended as the final output of the TLC320AD80. In addition, one of the mono outputs (AUDIO MONO) is derived from this stereo audio pair. The AUDIO MONO output is the summation of the AUDIO LEFT and AUDIO RIGHT channels divided by 2.

The variable stereo audio output (AUDIO LEFT, AUDIO RIGHT) provides the selected audio input after application of the volume control. The full-scale analog output of each channel is typically 2.8 V peak-to-peak. These analog outputs can drive load impedances as low as 600Ω and are short circuit protected to 10 mA.

A typical set-top-box application would connect AUDIO MONO output to one of the inputs of the wideband multiplexer after applying external 75 μ s pre-emphasis. If selected by the wideband multiplexer, the monaural audio output would then be processed by the channel 3/4 RF modulator and then connected to an external TV or VCR receiver (with a coaxial cable). The full-scale analog output is typically 2.8 V peak-to-peak. This analog output (AUDIO MONO) can drive load impedances as low as 10 k Ω and is short circuit protected to 7 mA.

2.2.2 External Stereo Audio Output

The external stereo output (EXT OUTL, EXT OTR) provides the output of the analog multiplexer (connected to the analog inputs, the DAC, and the monaural decoder). A typical connection would ac couple this output to the volume and balance external inputs. Alternate connections may include external analog functions located before the volume and balance input.

The selected audio input is output at a fixed volume of 0 dB on the external stereo audio output (EXT OUTL, EXT OTR). The full-scale analog output of each channel is typically 2.8 V peak-to-peak. The analog outputs can drive load impedances as low as 10 k Ω and are short circuit protected to 7 mA.

2.2.3 Wideband Multiplexer Output

The wideband multiplexer output is a single-ended output provided by the wide-band multiplexer. The inputs and output of this multiplexer are provided by external terminals. A typical application would use this function to provide source selection for a channel 3/4 RF modulator. The modulator would then be connected to a TV or VCR by means of a coaxial cable.

The wideband multiplexer can output one of two inputs (MUX IN1 AND MUX IN2) or perform an audio mute. A typical connection would connect one input to the composite TV baseband audio signal. The other input would connect to the AUDIO MONO output of the TLC320AD80 with external 75 μ s pre-emphasis. This feature allows remodulating an analog audio program which was broadcast in stereo without sacrificing the stereo content.

The wideband multiplexer has a 3-dB bandwidth greater than 90 kHz to provide a flat response for the SAP channel of a TV aural baseband signal. The volume control mute does not have any effect on the wideband multiplexer output. The wideband multiplexer has an independent mute control located at bit D5 of control register 02h. The full-scale analog output is typically 2.8 V peak-to-peak. The analog output can drive load impedances as low as 600 Ω and is short circuit protected to 10 mA.

2.3 Volume/Balance/Mute Control

The inputs and outputs of the volume and balance control are provided by external terminals. The inputs to this block (EXT INL, EXT INR) are typically ac-coupled to the EXT OUTL and EXT OTR outputs. The outputs consist of a stereo pair (AUDIO LEFT, AUDIO RIGHT) and a mono output (AUDIO MONO). The volume of the left and right audio channels can be controlled independently for stereo balance control. The lowest volume control setting corresponds to audio mute.

2.3.1 Volume Control

The TLC320AD80 provides a volume control range from 6 dB to -62 dB in 1 dB increments. Volume changes can be executed in each channel (left or right) independently or in ganged mode. All volume transitions take effect at zero-crossing to avoid clicks during volume transitions.

Volume control changes are programmed by means of control registers 03h and 04h (see *Appendix A, Register Set*). These changes will take effect during zero crossing of the data on a given channel. A zero crossing is defined by when the relative magnitude of the signal is zero (i.e., equal to the V_{ref} voltage level). However, if no zero crossing occurs within 4096 LRCLK periods, the gain is forced to change. Independent left channel and right channel zero crossing detectors are provided to minimize pops or clicks on stereo signals.

The time-out feature of 4096 LRCLK periods can be eliminated by setting D7 of control register 04h, in which case the data values must have a zero crossing for the next gain setting to be sent to the amplifier. This feature is useful in applications where severe data latency is either expected or needed and an audio pop is to be avoided. Many other multimedia applications such as acoustic echo cancellation will benefit from this feature.

The 70th volume control setting corresponds to audio mute. Mute provides greater than 80 dB of attenuation from a full-scale audio output.

It is possible for an audible click or pop to occur immediately after a zero crossing unmute. If an audio amplifier needs to slew rate limit immediately after being unmuted to catch up with a rapidly changing audio input, then that amplifier may subsequently overshoot causing an audible click or pop. By utilizing the programmable volume control feature of the TLC320AD80, a soft mute function can be implemented in software that eliminates this potential cause of audible noise. A soft mute would provide a gradual attenuation change over an appropriate time interval when entering a muted condition rather than an allowing an abrupt change to occur. The original volume control setting would be gradually restored upon leaving a muted condition.

2.4 Sigma-Delta DAC

The sigma-delta DAC contains an interpolation filter and single bit modulator with 64 times oversampling. The switched-capacitor and continuous time analog filter which follows, provides the smoothed analog signal output.

2.4.1 Interpolator / Modulator

The interpolation filter receives 16-bit or 18-bit data at the sample rate and interpolates new values at a rate of 64-times the sample rate. These values are provided to the sigma-delta modulator for noise shaping. The output of the digital modulator is a one bit data stream which is sent to a switched capacitor filter.

2.4.2 Continuous Time and Switched Capacitor Filters

The switched capacitor filter performs the low-pass filter function. The filter characteristics are stated in the specification section. The corner frequency of this filter is directly proportional to the selected sample rate. The continuous time filter is used to reduce the switching frequency energy of the switched capacitor filter, and any remaining high frequency energy. This switched-capacitor filter also provides the selectable 50/15 μ s de-emphasis under control of register 02h.

2.5 Serial Control Port

The SPI-compatible serial port controls all the programmable states of the TLC320AD80. The 4-wire SPI compatible interface is composed of a serial clock (SCLK), an active low chip select (\overline{CS}), a command data input (CDIN), and a command data output (CDOOUT). There are five 8-bit control registers within the TLC320AD80.

2.5.1 Serial Control Port Description

The serial control port is activated when the active low \overline{CS} signal is asserted. The \overline{CS} input must be asserted low prior to a data transfer and must remain low for the duration of the transfer as shown in Figure 2–5.

The serial command data input (CDIN) is sampled with the rising edge of SCLK. The CDIN data is MSB first and unsigned.

While the \overline{CS} input is low, the SCLK input must idle high when there is no valid data to be transferred. The first byte of CDIN data after \overline{CS} activation is the serial control command. The serial control command includes a 4-bit control register address [D(3–0)] and a control port direction bit (D7). The second byte of data is the register data.

The \overline{CS} input must make a low to high transition in order to specify a new control register address. When the \overline{CS} input is set to 1, the serial command data output (CDOOUT) is placed in a high-impedance state. When the \overline{CS} input is cleared to 0, the CDOOUT output is held low during nonvalid data intervals.

The serial control port is activated when the \overline{CS} signal (active low) goes low. The \overline{CS} line must be low prior to data transactions and must remain low for the duration of the transaction. The serial command data input (CDIN) is sampled on the rising edge of SCLK. The CDIN data is MSB first and unsigned. While the \overline{CS} input is low, the SCLK input must idle high when there is no valid data to be transferred. The first byte of CDIN data after \overline{CS} activation is set up as a serial control command. The serial control command includes a 4-bit control register address [D(3–0)] and a control port direction bit (D7). The second byte of data is set up as control register data. The \overline{CS} input must make a low-to-high transition in order to specify a new control register address. When the \overline{CS} input goes high, the serial command data output (CDOOUT) is placed in a high-impedance state. When the \overline{CS} input goes low, the CDOOUT output is held low during nonvalid data intervals.

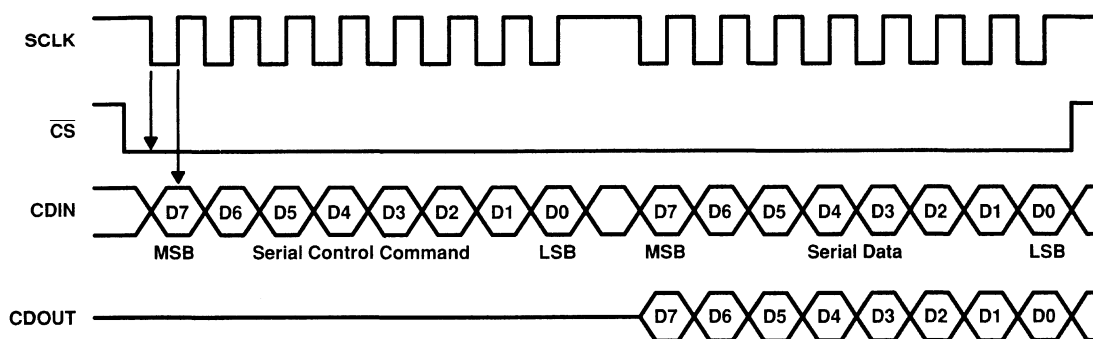


Figure 2–5. Serial Interface Timing

2.5.2 Serial Control Command Format

The serial control command format is shown below.

D7	D6	D5	D4	D3	D2	D1	D0
WR	Unused			ADDR(3–0)			

The serial control command fields are defined as:

WR – Serial interface direction

When this bit is 1:

- The serial interface is in write mode.
- Serial data is sent control register specified in the serial control command

When this bit is 0:

- The serial interface is in read mode.
- The control register data is output to CDOOUT according to the control register address.

ADDR(3–0) – Control register address specifies the TLC320AD80 register being accessed.

2.5.3 Power-Down/Reset

When the $\overline{\text{RESET}}$ terminal is held low, the TLC320AD80C is put in a power-down condition. During power down, the sigma-delta DACs are disabled to conserve power and the digital output drivers (ABCLK, ALRCLK, and CDOUT) are placed in a high-impedance state. When powered down, the analog audio outputs settle near V_{ref} (2.25 V).

There are two ways in which to initialize the TLC320AD80C.

- The TLC320AD80C begins reset and initialization on the rising edge of the $\overline{\text{RESET}}$ signal. A stable clock waveform having a frequency within the specified allowable frequency range (see Timing Requirements section) must be present at the master clock (MCLK1) input prior to the rising edge of the $\overline{\text{RESET}}$ signal for proper operation. In order to prevent the occurrence of audible pops or clicks from the TLC320AD80C, the $\overline{\text{RESET}}$ terminal must be kept low 500 ms after the power supplies have settled. This provides adequate time for the 2.25-V based line outputs to charge the large output capacitors on the analog audio outputs while minimizing any audible pops.
- Set bit D0 of control register 02h to 1.

To maximize the initialization cycle accuracy, the TLC320AD80C should not be continually polled. This initialization cycle takes about 500 ms to complete following the rising edge of $\overline{\text{RESET}}$.

The power-down mode can also be selected by setting bit D0 of control register 02h to 1. In this software controlled power-down mode the sigma-delta DACs, the monaural decoder, and the audio input amplifiers are all disabled to conserve power. The external audio outputs (EXT OUTF, EXT OUTL) are muted to hold the output voltage at V_{ref} . Since muting the external audio output can cause an audible click, a zero crossing mute should be performed prior to initiating a software power-down.

2.6 Software Interface

Control of the TLC320AD80 is accomplished by means of the SPI serial interface and the control registers described in Appendix A.

3 Specifications

3.1 Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, AV_{DD} (see Note 1)	–0.3 V to 6 V
Supply voltage range, DV_{DD} (see Note 2)	–0.3 V to 6 V
Analog input voltage	–0.3 V to $AV_{DD} + 0.3$ V
Digital input voltage	–0.3 V to $DV_{DD} + 0.3$ V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values for maximum ratings are with respect to AGND.
2. Voltage values for maximum ratings are with respect to DGND.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNITS
Analog supply voltage, AV_{DD} (see Note 3)	4.75	5	5.25	V
Digital supply voltage, DV_{DD}	4.75	5	5.25	V
Operating free-air temperature, T_A	0		70	°C
Storage temperature, T_{Stg}	–65		150	°C

NOTE 3: Voltages at analog inputs and outputs and V_{CC} are with respect to the AGND terminal.

3.2.1 Static Digital Specifications, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} + 5\%$

	TEST CONDITIONS	MIN	NOM	MAX	UNITS
High-level input voltage, V_{IH}				2	V
Low-level input voltage, V_{IL}		0.8			V
High-level output voltage, V_{OH}	$I_O = -1$ mA	2.4		DV_{DD}	V
Low-level output voltage, V_{OL}	$I_O = 4$ mA			0.4	V
Input leakage current		–10		10	μA
Output leakage current		–10		10	μA
Leakage current, digital I/O terminals	Input mode	–10		10	μA

3.2.2 Power Supplies, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} + 5\%$

	TEST CONDITIONS	MIN	NOM	MAX	UNITS
Power supply current (see Note 4)	Normal		52	90	mA
	Power-down mode		19		mA
Power supply rejection	1 kHz		40		dB
	1 MHz		30		dB

NOTE 4: Power supply current rating for line outputs driving 10-k Ω load.

3.3 Electrical Characteristics

3.3.1 Analog Audio Channel Performance, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} \pm 5\%$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Full-scale input voltage		All analog audio inputs	2.66	2.8	2.94	V_{PP}
Common mode input voltage		All analog audio inputs	2.1	2.25	2.4	V
Input impedance	Resistance	All analog audio inputs	20			k Ω
	Capacitance	All analog audio inputs		15		pF
3-dB Bandwidth		All analog audio inputs except the TV BASEBAND P or TV BASEBAND M inputs	20			kHz
Signal-to-noise ratio (SNR)		A-weighted, referenced to 0-dB f_s , All analog audio inputs except the TV BASEBAND P or TV BASEBAND M inputs	80	85		dB
Total harmonic distortion (THD)		A-weighted, referenced to 0-dB f_s			0.02%	
Frequency response		20 Hz to 20 kHz	-0.8		0.2	dB
Deviation from linear phase		20 Hz to 20 kHz		± 1.5		degrees

3.3.2 Volume Control and Output Drivers Performance, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} \pm 5\%$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Volume control	Range	Total continuous control range		68		dB
	Step resolution	Differential error	0.5	1	1.5	dB
	Volume integral error	Deviation from ideal volume setting		± 2		dB
	Gain tracking	Left and right channel gain matching		± 1		dB
	Mute attenuation	Relative to volume setting of 0 dB	-80	-90		dB
Full-scale output voltage		All analog audio outputs, maximum volume	2.66	2.8	2.94	V_{PP}
Common mode output voltage		All analog audio outputs	2.1	2.25	2.4	V
Output resistance (open loop)		All analog audio outputs		300		Ω
Output drive capability	Output load resistance	Short circuit protected, AUDIO RIGHT, AUDIO LEFT, MUX OUT	600			Ω
		Short circuit protected, AUDIO MONO, EXT OTR, EXT OUTL	10			k Ω
	Output load capacitance	Short circuit protected, AUDIO RIGHT, AUDIO LEFT			300	pF
		Short circuit protected, AUDIO MONO, EXT OTR, EXT OUTL, MUX OUT			100	pF
V_{ref} Output reference voltage		2.1	2.25	2.4	V	
Output reference current				100		μA
Audio channel separation (relative to 0 dB)	EXT OUTL, EXT OTR			80		dB
	AUDIO LEFT, AUDIO RIGHT			80		dB

3.3.3 Monaural Decoder Performance, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} \pm 5\%$, $f_s = 32\text{ kHz}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
3-dB Bandwidth		TV BASEBAND P or TV BASEBAND M inputs only, MCLK = 256 x 32 kHz or 384 x 32 kHz		14		kHz
Signal-to-noise ratio (SNR)		A-weighted, referenced to -3 dB, $f_s = 50\text{ Hz}$ to 14 kHz		54		dB
Total harmonic distortion (THD)		A-weighted, referenced to -3 dB, $f_s = 50\text{ Hz}$ to 14 kHz		50		dB
BTSC filter	-3-dB Passband	TV baseband input filter referenced to 0 dB	14			kHz
	Passband ripple			+0.5		dB
	Stopband		15.73425			kHz
	Stopband rejection		-44	-50		dB

3.3.4 Wideband Multiplexer Performance, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} \pm 5\%$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
3-dB Bandwidth	MUX IN1 or MUX IN2 inputs	90			kHz
Signal-to-noise ratio (SNR)	Unweighted, referenced to 0 dB, $f_S = 50\text{ Hz to }47\text{ kHz}$	70	85		dB
Total harmonic distortion (THD)	Unweighted, referenced to 0 dB, $f_S = 50\text{ Hz to }47\text{ kHz}$			0.1%	
Frequency response	50 Hz to 47 kHz		± 0.35		dB
Deviation from linear phase	50 Hz to 47 kHz		± 2		degrees

3.3.5 PCM Audio Channel Performance, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} \pm 5\%$, $f_S = 48\text{ kHz}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DAC resolution (see Note 5)		16			Bits
Signal-to-noise ratio (SNR) (see Note 5)	A-weighted, referenced to -3 dB , f_S	76	82		dB
Total harmonic distortion (THD) (see Note 5)	A-weighted, referenced to -3 dB , f_S		0.02%		
Total harmonic distortion + noise (THD+N) (see Note 5)	A-weighted, referenced to -3 dB , f_S	-70	-74		dB
Total harmonic distortion + noise (THD+N) without de-emphasis	A-weighted, referenced to -3 dB , f_S	62	66		dB
Signal-to-intermodulation distortion			-74		dB
Frequency response	0 to $0.4 f_S$	-0.5		0.5	dB
Deviation from linear phase	0 to $0.4 f_S$		± 1.4		degrees
Crosstalk isolation		-72	-78		dB
Audible out of band energy	$0.55 f_S$ to 22 kHz		-60		dB
Total out of band energy	$0.55 f_S$ to 3 MHz		-45		dB
De-emphasis, $50/15\ \mu\text{s}$	Pole location	$f_S = 32, 44.1, \text{ and } 48\text{ kHz}$ only		3.18	kHz
	Zero location	$f_S = 32, 44.1, \text{ and } 48\text{ kHz}$ only		10.6	kHz
	Attenuation	$f_S = 32, 44.1, \text{ and } 48\text{ kHz}$ only, $20 \log(15/50)$		-10.5	dB

NOTE 5: Measurements are performed with de-emphasis enabled.

3.3.6 DAC Interpolation Filter, $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} \pm 5\%$, $f_S = 48\text{ kHz}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Passband	$f_S = \text{Audio sample rate}$	0		$0.4 f_S$	kHz
Passband ripple				± 0.1	dB
Transition band		$0.4 f_S$		$0.6 f_S$	kHz
Stopband		$>0.6 f_S$			kHz
Stopband attenuation		74			dB
Group delay			$30/f_S$		sec
Group delay variation versus frequency			$0.1/f_S$		sec

3.4 Timing Requirements, $T_A = 25\text{ }^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} \pm 5\%$, $f_s = 48\text{ kHz}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input frequency, MCLK1, MCLK2		4.096		18.432	MHz
f_s Audio sample rate		8		48	kHz
t_{su1} Setup time, PCM data	Relative to the rising edge of BCLK			60	ns
t_{h1} Hold time, PCM data	Relative to the rising edge of BCLK			0	ns
t_{su2} Setup time, LRCLK	Relative to the rising edge of BCLK			60	ns
t_{h2} Hold time, LRCLK	Relative to the rising edge of BCLK			0	ns

3.4.1 Serial PCM Data Port (see Figures 3–1 and 3–2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$t_c(\text{BCLK})$ Cycle time, BCLK				60	ns
$t_r(\text{BCLK})$ Rise time, BCLK				0	ns
$t_f(\text{BCLK})$ Fall time, BCLK				0	ns
$t_{su}(\text{LRCLK})$ Setup time, LRCLK \downarrow before BCLK \uparrow				0	ns
$t_h(\text{LRCLK})$ Hold time, LRCLK \uparrow after BCLK \uparrow				0	ns
$t_{su}(\text{SDATA})$ Setup time, SDATA before BCLK \uparrow				0	ns
$t_h(\text{SDATA})$ Hold time, SDATA after BCLK \uparrow				0	ns
$t_d(\text{SDATA})$ Delay time, SDATA valid after BCLK \downarrow				0	ns
$t_{wL}(\text{BCLK})$ Pulse duration, BCLK low				60	ns
$t_{wH}(\text{BCLK})$ Pulse duration, BCLK high				60	ns
$t_{wL}(\text{MCLK})$ Pulse duration, MCLK low				60	ns
$t_{wH}(\text{MCLK})$ Pulse duration, MCLK high				60	ns
$t_r(\text{MCLK})$ Rise time, MCLK				0	ns
$t_f(\text{MCLK})$ Fall time, MCLK				0	ns

3.4.2 Serial Control Interface, $T_A = 25\text{ }^\circ\text{C}$, $AV_{DD} = DV_{DD} = 5\text{ V} \pm 5\%$, (see Figure 3–3)

DESCRIPTION	MIN	TYP	MAX	UNITS
f_{SCLK} Input frequency, SCLK			3	MHz
$t_c(\text{SCLK})$ Cycle time, SCLK	333			ns
$t_{wL}(\text{SCLK})$ Pulse width, SCLK low	100			ns
$t_{wH}(\text{SCLK})$ Pulse width, SCLK high	100			ns
$t_{su}(\text{CS})$ Setup time, $\overline{\text{CS}}\downarrow$ before SCLK \downarrow	150			ns
$t_h(\text{CS})$ Hold time, $\overline{\text{CS}}\uparrow$ after SCLK \uparrow	150			ns
$t_{su}(\text{CDIN})$ Setup time, CDIN before SCLK \uparrow	50			ns
$t_h(\text{CDIN})$ Hold time, CDIN after SCLK \uparrow	50			ns
$t_d(\text{CDOOUT})$ Delay time, CDOOUT after SCLK \downarrow			30	ns
$t_h(\text{CDOOUT})$ Hold time, CDOOUT after SCLK \downarrow		5		ns
$t_r(\text{SCLK})$ Rise time, SCLK			100	ns
$t_f(\text{SCLK})$ Fall time, SCLK			100	ns

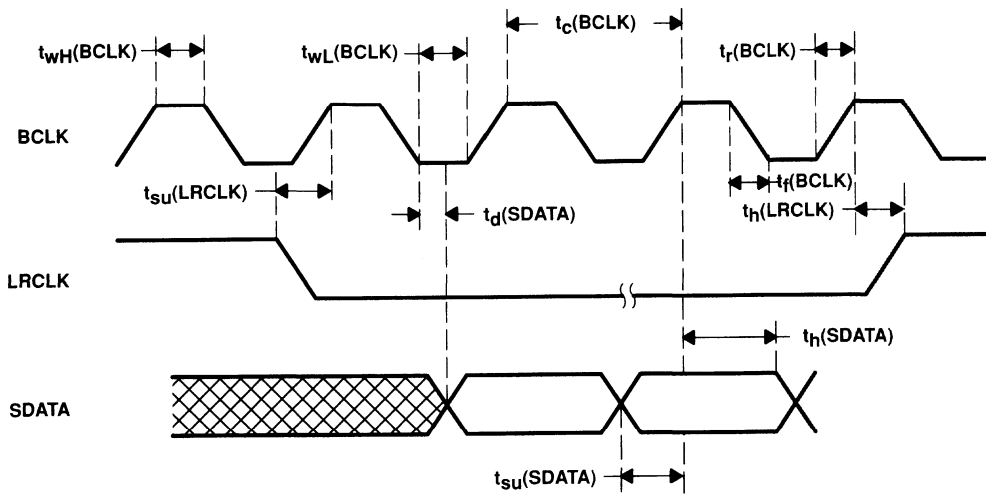


Figure 3-1. Serial Port Timing

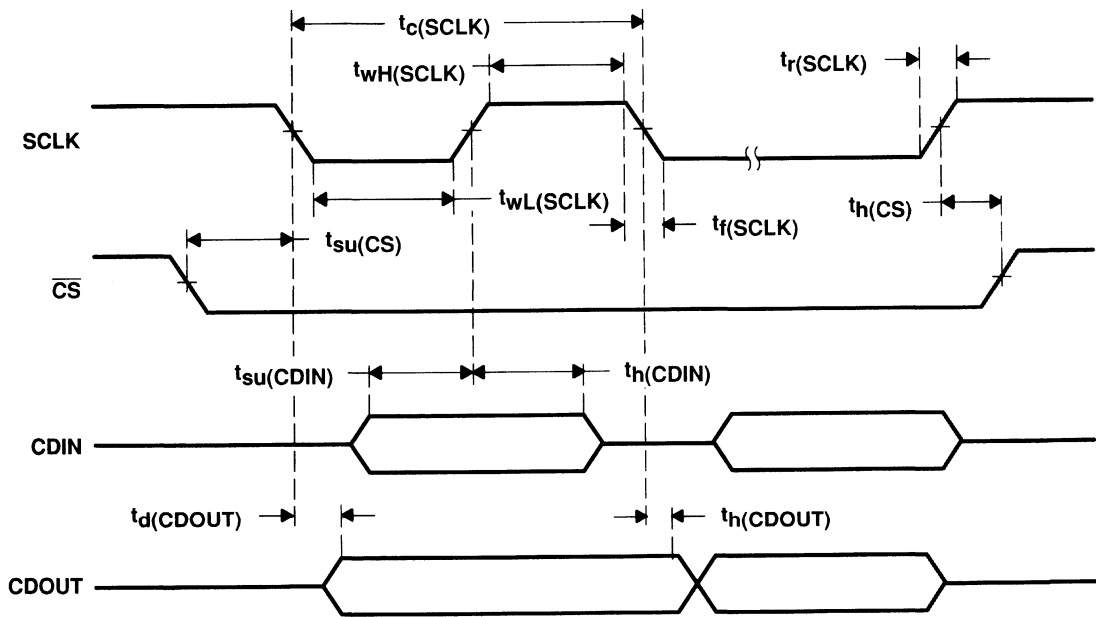


Figure 3-2. SPI Serial Control Port Timing

4 Application Information

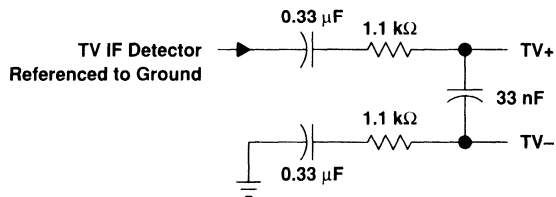


Figure 4–1. De-Emphasis 75 μ s Low-Pass Filter at 2.12 kHz

Table 4–1. Digital Interface Capacitive Loading, $T_A = 25^\circ\text{C}$,
 $AV_{DD} = DV_{DD} = 5\text{ V} \pm 5\%$, $f_s = 48\text{ kHz}$

TERMINAL NAME		NO.	I/O	TYPICAL CAPACITIVE LOAD
SDATA	44	I	5 pF	
BCLK	1	I	5 pF	
LRCLK	2	I	5 pF	
ASDATA	3	I	5 pF	
ABCLK	4	I	5 pF	
ABCLK	40	I	5 pF	
ALRCLK	5	I	5 pF	
ALRCLK	50	I	5 pF	
MCLK	41	I	5 pF	
AMCLK	40	I	5 pF	
CDOUT	39	O	5 pF	
CDIN	38	I	5 pF	
SCLK	37	I	5 pF	
CS	36	I	TBD	
RESET	33	I	TBD	

NOTE 1: ALRCLK and ABCLK are programmable as either inputs or outputs.

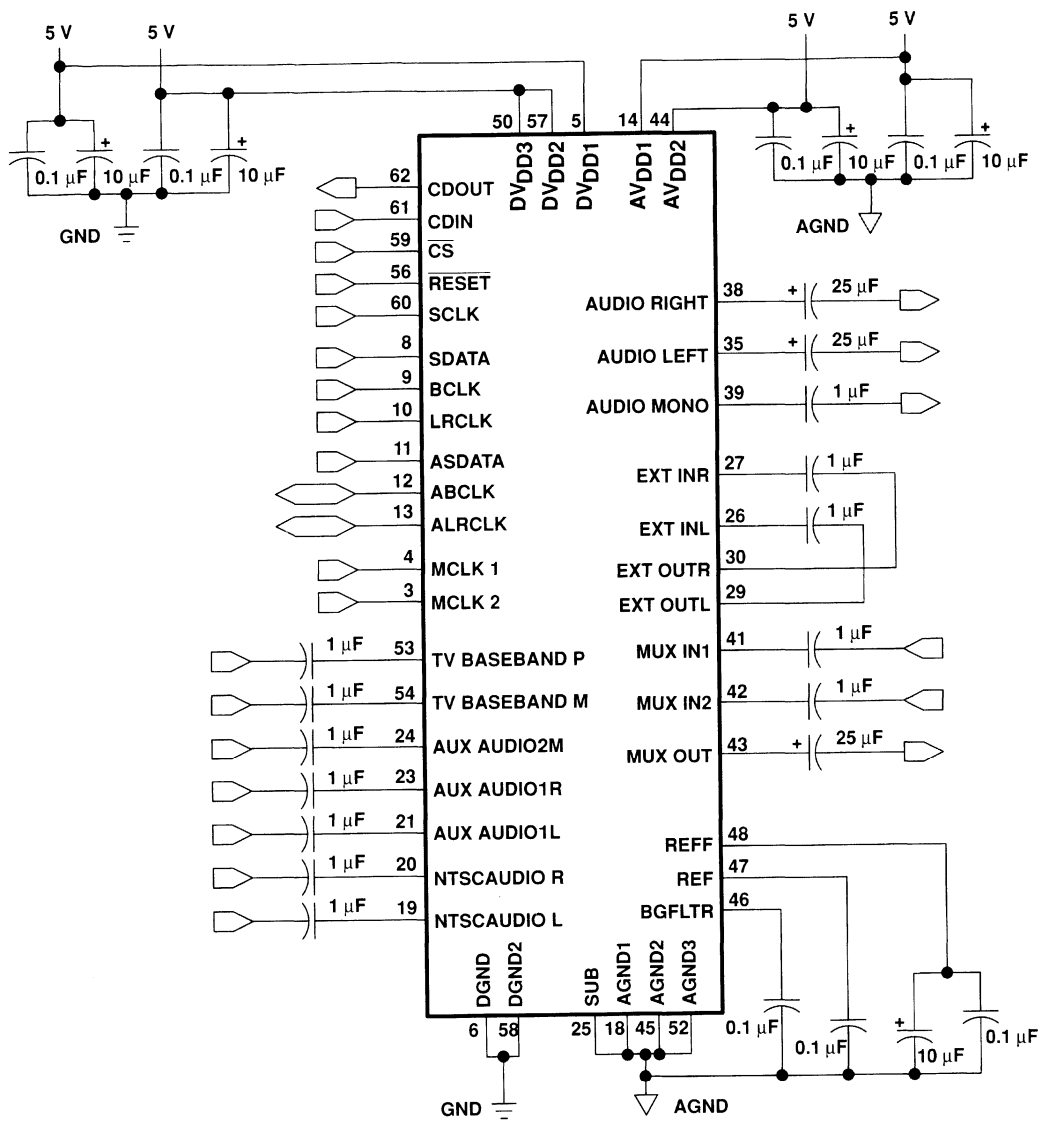
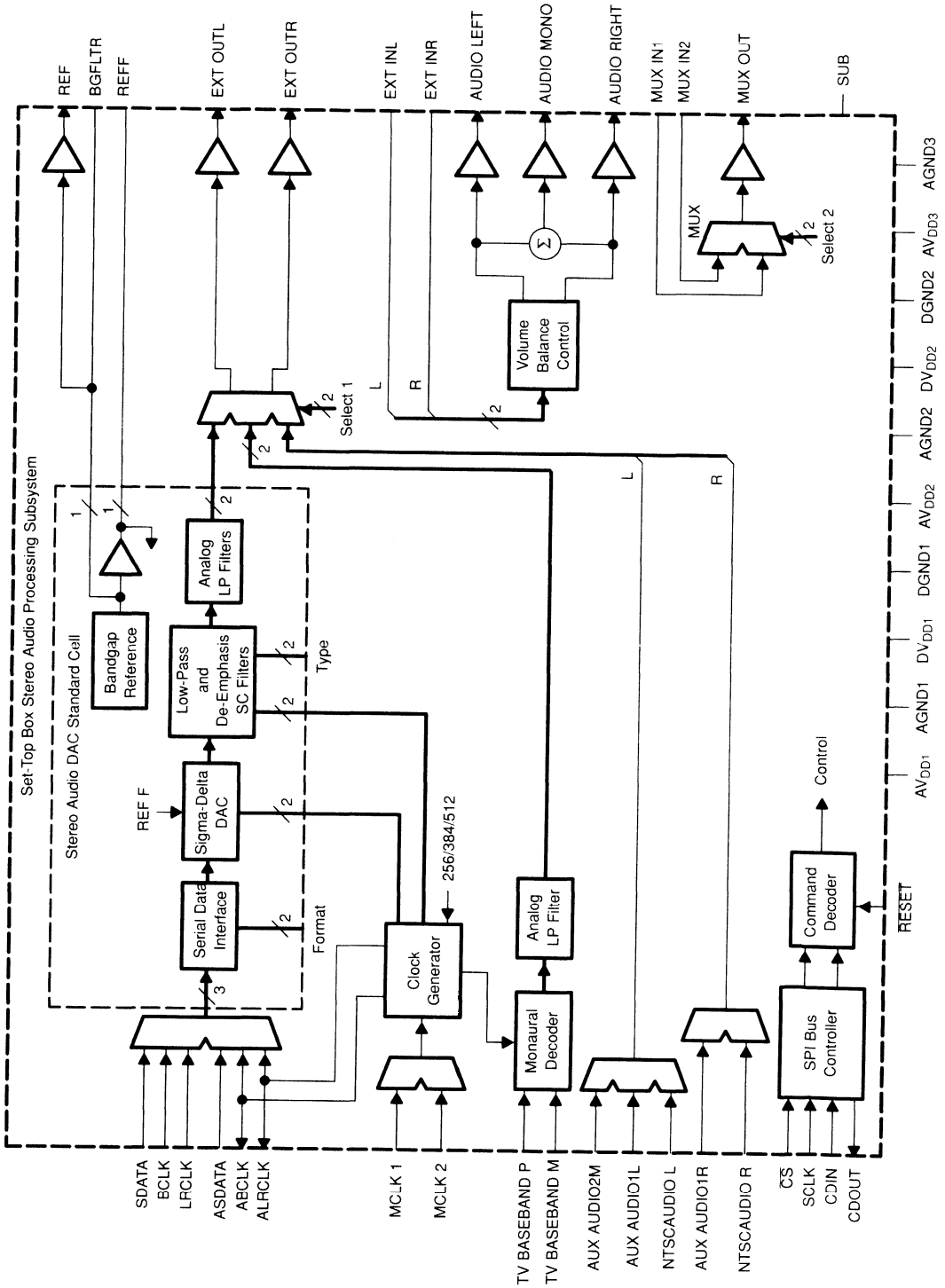


Figure 4-2. Application Schematic

NOTE: If the TLC320AD80 is to be used in applications where high voltage may be present, as with TV monitors or sets, it is recommended to add either external diodes (1N5347A) or transient suppressors (Motorola SA5.0A) from any input and/or output terminals (that connect directly to external TV monitors or sets) to the circuit board ground.

4.1 Schematic



Appendix A Register Set

Control of the TLC320AD80 is accomplished by means of the SPI serial interface and the control registers described in this section.

There are five control registers used to control the various functions of the device: volume control, multiplexer selections, serial interface, modes of operation, etc.

Table A–1. Serial PCM Data Format Control Register (Control Register 00h)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION	
0	0	–	–	–	–	–	–	Serial PCM data format	Philips I ² S protocol
0	1	–	–	–	–	–	–		Right justified
1	0	–	–	–	–	–	–		Left justified
1	1	–	–	–	–	–	–		Left justified DSP (inverted BCLK)
–	–	0	–	–	–	–	–	Serial PCM data precision	16 bits
–	–	1	–	–	–	–	–		18 bits
–	–	–	0	0	–	–	–	MCLK rate	256 x LRCLK (22.05 kHz ≤ LRCLK ≤ 48 kHz)
–	–	–	0	1	–	–	–		384 x LRCLK (22.05 kHz ≤ LRCLK ≤ 48 kHz)
–	–	–	1	0	–	–	–		512 x LRCLK (8 kHz ≤ LRCLK ≤ 16 kHz)
–	–	–	1	1	–	–	–	Reserved	
–	–	–	–	–	0	0	–	Bit clock (BCLK) rate	64 x LRCLK
–	–	–	–	–	0	1	–		48 x LRCLK (384x mode only)
–	–	–	–	–	1	0	–		32 x LRCLK (16-bit mode only)
–	–	–	–	–	1	1	–	Reserved	
–	–	–	–	–	–	–	x	Reserved	

The default value at reset is 00h.

Table A–2. Source Selection Control Register (Control Register 01h)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION	
0	0	0	0	–	–	–	–	Main audio input port select	NTSC AUDIO (stereo)
0	0	0	1	–	–	–	–		NTSC AUDIO (mono)
0	0	1	0	–	–	–	–		AUX AUDIO1 (stereo)
0	0	1	1	–	–	–	–		AUX AUDIO1 (mono)
0	1	0	0	–	–	–	–		Reserved
0	1	0	1	–	–	–	–		AUX AUDIO2 (mono)
0	1	1	0	–	–	–	–		Reserved
0	1	1	1	–	–	–	–		TV aural baseband multiplex (mono)
1	0	0	0	–	–	–	–		Main serial PCM data (slave mode)
1	0	0	1	–	–	–	–		Reserved
1	0	1	0	–	–	–	–		Aux serial PCM data (slave mode)
1	0	1	1	–	–	–	–		Aux serial PCM data (master mode) (see Note 1)
1	1	x	x	–	–	–	–		Reserved
–	–	–	–	0	–	–	–		Master clock input port select
–	–	–	–	1	–	–	–	MCLK 2	
–	–	–	–	–	0	–	–	Wideband mux input port select	MUX IN1
–	–	–	–	–	1	–	–		MUX IN2
–	–	–	–	–	–	0	–	Capacitor precharge mode	Disabled
–	–	–	–	–	–	1	–		Enabled
–	–	–	–	–	–	–	0	Audio input port mute	Enabled
–	–	–	–	–	–	–	1		Disabled

The default value at reset is 00h.

NOTE 1: All serial PCM data formats except DSP.

Table A-3. Control Register 02h

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION	
0	0	-	-	-	-	-	-	De-emphasis mode	50/15 μ s (LRCLK = 48 kHz)
0	1	-	-	-	-	-	50/15 μ s (LRCLK = 44.1 kHz)		
1	0	-	-	-	-	-	50/15 μ s (LRCLK = 32 kHz)		
1	1	-	-	-	-	-	None		
-	-	0	-	-	-	-	-	Wideband mux output mute	Enabled
-	-	1	-	-	-	-	-		Disabled
-	-	-	0	-	-	-	-	Volume/mute gating enabler	Zero crossing or time out
-	-	-	1	-	-	-	-		Zero crossing only
-	-	-	-	x	-	-	-	Reserved	
-	-	-	-	-	x	-	-	Reserved	
-	-	-	-	-	-	0	-	Reset	Normal mode
-	-	-	-	-	-	1	-		Clear DAC digital filter
-	-	-	-	-	-	-	0	Power down with ext out mute	Device enabled
-	-	-	-	-	-	-	1		Device powered down

The default value at reset is 00h.

Table A-4. Left Volume Control Register (Control Register 03h)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION	
0	-	-	-	-	-	-	-	Volume control mode	Ganged left/right control on left
1	-	-	-	-	-	-	-		Independent left/right control
-	0	0	0	0	0	0	0	Left volume control	-90 dB (mute)
-	0	0	0	0	0	0	1		-62 dB
-	0	0	0	0	0	1	0		-61 dB
-	0	1	1	1	1	1	0		-1 dB
-	0	1	1	1	1	1	1		0 dB
-	1	0	0	0	0	0	0		1 dB
-	1	0	0	0	1	0	1		6 dB
-	1	0	0	0	1	1	x	Reserved	
-	1	1	1	1	x	x	x	Reserved	

The default value at reset is 00h.

Table A-5. Right Volume Control Register (Control Register 04h)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION	
x	-	-	-	-	-	-	-	Reserved	
-	0	0	0	0	0	0	0	Right volume control	
-	0	0	0	0	0	0	1		-90 dB (mute)
-	0	0	0	0	0	1	0		-62 dB
-	0	1	1	1	1	1	0		-61 dB
-	0	1	1	1	1	1	1		-1 dB
-	1	0	0	0	0	0	0		0 dB
-	1	0	0	0	1	0	1		1 dB
-	1	0	0	0	1	1	x	6 dB	
-	1	0	0	0	1	1	x	Reserved	
-	1	1	1	1	x	x	x	Reserved	

The default value at reset is 00h.

General Information	1
General Purpose ADCs	2
General Purpose DACs	3
DSP AICs and CODECs	4
Special Functions	5
Video Interface Palettes	6
Digital Imaging Sensor Products	7
Mechanical Information	8

Contents

	Page
TL7726 :	5-3
TLC04, MF4A-50, TLC14, MF4A-100 :	5-7
TLC2932 :	5-19
TLC2933 :	5-41
TL32088 :	5-61

5

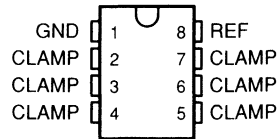
Special Functions

TL7726C, TL7726I, TL7726Q HEX CLAMPING CIRCUITS

SLAS078B – SEPTEMBER 1993 – REVISED OCTOBER 1996

- Protects Against Latch-Up
- 25-mA Current Sink in Active State
- Less Than 1-mW Dissipation in Standby Condition
- Ideal for Applications in Environments Where Large Transient Spikes Occur
- Stable Operation for All Values of Capacitive Load
- No Output Overshoot

D OR P PACKAGE
(TOP VIEW)



description

The TL7726C, TL7726I, and TL7726Q each consist of six identical clamping circuits that monitor an input voltage with respect to a reference value, REF. For an input voltage (V_I) in the range of GND to $< REF$, the clamping circuits present a very high impedance to ground, drawing current of less than $10 \mu A$. The clamping circuits are active for $V_I < GND$ or $V_I > REF$ when they have a very low impedance and can sink up to 25 mA.

These characteristics make the TL7726C, TL7726I, and TL7726Q ideal as protection devices for CMOS semiconductor devices in environments where there are large positive or negative transients to protect analog-to-digital converters in automotive or industrial systems. The use of clamping circuits provides a safeguard against potential latch-up.

The TL7726C is characterized for operation over the temperature range of $0^\circ C$ to $70^\circ C$. The TL7726I is characterized for operation over the temperature range of $-40^\circ C$ to $85^\circ C$. The TL7726Q is characterized for operation over the temperature range of $-40^\circ C$ to $125^\circ C$.

AVAILABLE OPTIONS

OPERATING TEMPERATURE RANGE	DEVICE	PACKAGE
$0^\circ C - 70^\circ C$	TL7726CD	8-pin SO
$0^\circ C - 70^\circ C$	TL7726CP	8-pin DIP
$-40^\circ C - 85^\circ C$	TL7726ID	8-pin SO
$-40^\circ C - 85^\circ C$	TL7726IP	8-pin DIP
$-40^\circ C - 125^\circ C$	TL7726QD	8-pin SO
$-40^\circ C - 125^\circ C$	TL7726QP	8-pin DIP



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 **TEXAS
INSTRUMENTS**

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TL7726C, TL7726I, TL7726Q HEX CLAMPING CIRCUITS

SLAS078B – SEPTEMBER 1993 – REVISED OCTOBER 1996

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Reference voltage, V_{ref}	6 V
Clamping current, I_{JK}	± 50 mA
Junction temperature, T_J	150°C
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A :	
TL7726C	0°C to 70°C
TL7726I	-40°C to 85°C
TL7726Q	-40°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR	$T_A = 70^\circ\text{C}$	$T_A = 85^\circ\text{C}$	$T_A = 125^\circ\text{C}$
	POWER RATING	ABOVE $T_A \leq 25^\circ\text{C}$	POWER RATING	POWER RATING	POWER RATING
D	728 mW	5.8 mW/°C	467 mW	380 mW	148 mW
P	900 mW	8 mW/°C	540 mW	420 mW	100 mW

recommended operating conditions

		MIN	MAX	UNIT
Reference voltage, V_{ref}		4.5	5.5	V
Input clamping current, I_{JK}	$V_I \geq V_{ref}$		25	mA
	$V_I \leq \text{GND}$	-25		

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{JK+} Positive clamp voltage	$I_I = 20$ mA	V_{ref}		$V_{ref} + 200$	mV
V_{JK-} Negative clamp voltage	$I_I = 20$ mA	-200		0	mV
I_Z Reference current	$V_{ref} = 5$ V		25	60	μA
I_I Input current	$V_{ref} - 50$ mV $\leq V_I \leq V_{ref}$			10	μA
	$\text{GND} \leq V_I \leq 50$ mV	-10			μA
	50 mV $\leq V_I \leq V_{ref} - 50$ mV	-1		1	μA

† All typical values are at $T_A = 25^\circ\text{C}$.

switching characteristics specified at $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_s Settling time	$V_I(\text{system}) = \pm 13$ V, $R_I = 600 \Omega$, $t_t < 1 \mu\text{s}$, Measured at 10% to 90%, See Figure 1		30	μs



PARAMETER MEASUREMENT INFORMATION

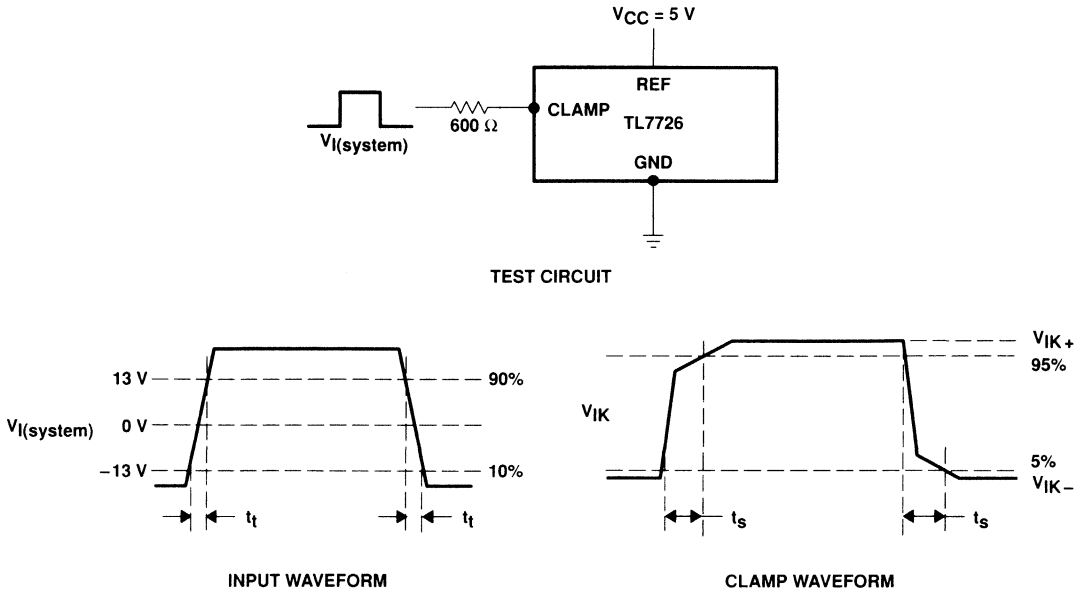


Figure 1. Switching Characteristics

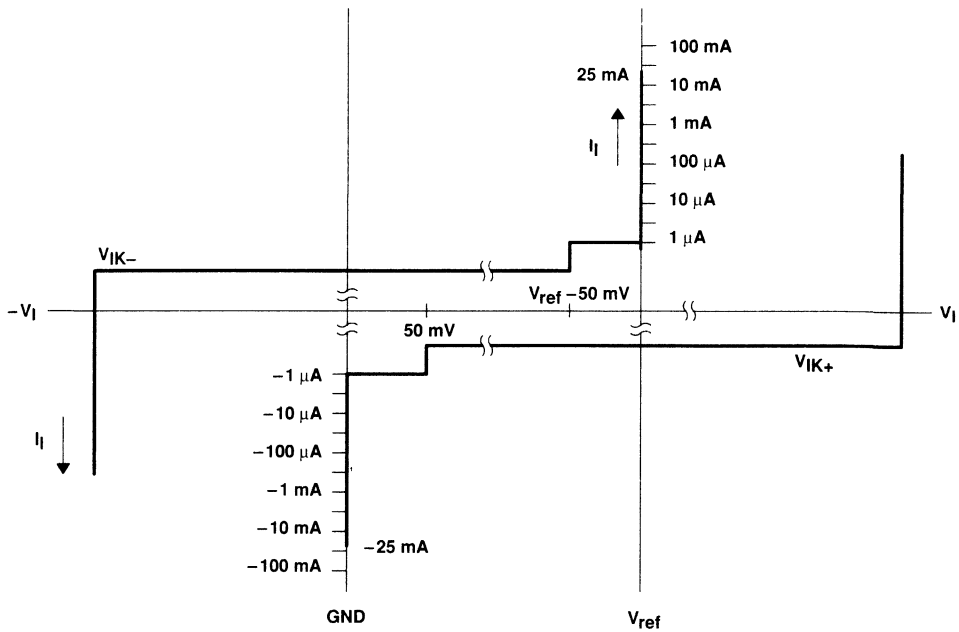
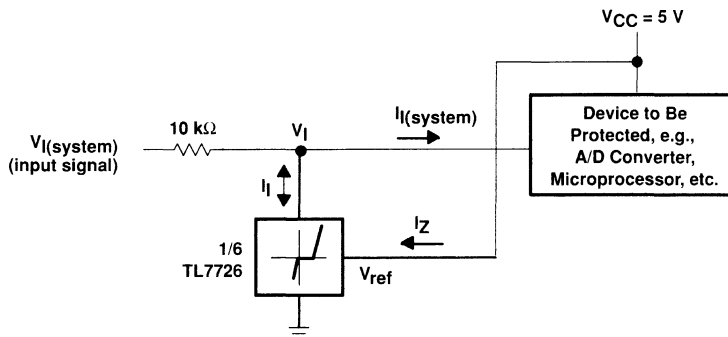


Figure 2. Tolerance Band for Clamping Circuit

TL7726C, TL7726I, TL7726Q HEX CLAMPING CIRCUITS

SLAS078B – SEPTEMBER 1993 – REVISED OCTOBER 1996

APPLICATION INFORMATION



Example: If $I_I \gg I_{I(\text{system})}$, i.e., $V_{I(\text{system})} > V_{\text{ref}} + 200 \text{ mV}$

where:

$I_{I(\text{system})}$ = Input current to the device being protected

$V_{I(\text{system})}$ = Input voltage to the device being protected

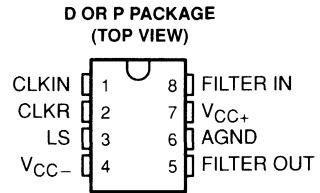
then the maximum input voltage

$$\begin{aligned} V_{I(\text{system})\text{max}} &= V_{\text{ref}} + I_{I\text{max}}(10\text{k}\Omega) \\ &= 5 \text{ V} + 25 \text{ mA}(10\text{k}\Omega) \\ &= 5 \text{ V} + 250 \text{ V} \\ &= 255 \text{ V} \end{aligned}$$

Figure 3. Typical Application

TLC04/MF4A-50, TLC14/MF4A-100
BUTTERWORTH FOURTH-ORDER LOW-PASS
SWITCHED-CAPACITOR FILTERS
 SLAS021A – NOVEMBER 1986 – REVISED MARCH 1995

- **Low Clock-to-Cutoff-Frequency Ratio Error**
 TLC04/MF4A-50 . . . $\pm 0.8\%$
 TLC14/MF4A-100 . . . $\pm 1\%$
- **Filter Cutoff Frequency Dependent Only on External-Clock Frequency Stability**
- **Minimum Filter Response Deviation Due to External Component Variations Over Time and Temperature**
- **Cutoff Frequency Range From 0.1 Hz to 30 kHz, $V_{CC\pm} = \pm 2.5$ V**
- **5-V to 12-V Operation**
- **Self Clocking or TTL-Compatible and CMOS-Compatible Clock Inputs**
- **Low Supply-Voltage Sensitivity**
- **Designed to be Interchangeable With National MF4-50 and MF4-100**



description

The TLC04/MF4A-50 and TLC14/MF4A-100 are monolithic Butterworth low-pass switched-capacitor filters. Each is designed as a low-cost, easy-to-use device providing accurate fourth-order low-pass filter functions in circuit design configurations.

Each filter features cutoff frequency stability that is dependent only on the external-clock frequency stability. The cutoff frequency is clock tunable and has a clock-to-cutoff frequency ratio of 50:1 with less than $\pm 0.8\%$ error for the TLC04/MF4A-50 and a clock-to-cutoff frequency ratio of 100:1 with less than $\pm 1\%$ error for the TLC14/MF4A-100. The input clock features self-clocking or TTL- or CMOS-compatible options in conjunction with the level shift (LS) terminal.

The TLC04C/MF4A-50C and TLC14C/MF4A-100C are characterized for operation from 0°C to 70°C . The TLC04I/MF4A-50I and TLC14I/MF4A-100I are characterized for operation from -40°C to 85°C . The TLC04M/MF4A-50M and TLC14M/MF4A-100M are characterized over the full military temperature range of -55°C to 125°C .

AVAILABLE OPTIONS

T _A	CLOCK-TO-CUTOFF FREQUENCY RATIO	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	50:1	TLC04CD/MF4A-50CD	TLC04CP/MF4A-50CP
	100:1	TLC14CD/MF4A-100CD	TLC14CP/MF4A-100CP
-40°C to 85°C	50:1	TLC04ID/MF4A-50ID	TLC04IP/MF4A-50IP
	100:1	TLC14ID/MF4A-100ID	TLC14IP/MF4A-100IP
-55°C to 125°C	50:1		TLC04MP/MF4A-50MP
	100:1		TLC14MP/MF4A-100MP

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC04CDR/MF4A-50CDR).

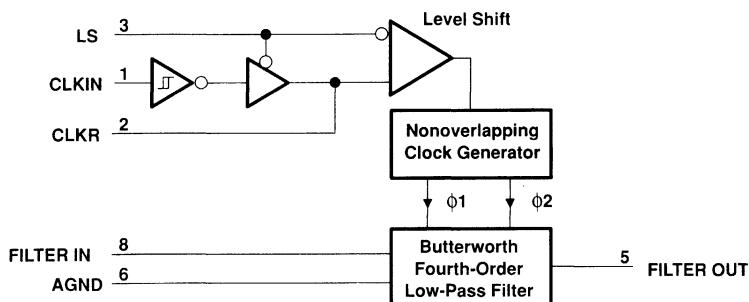
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TLC04/MF4A-50, TLC14/MF4A-100 BUTTERWORTH FOURTH-ORDER LOW-PASS SWITCHED-CAPACITOR FILTERS

SLAS021A – NOVEMBER 1986 – REVISED MARCH 1995

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	6	I	Analog ground. The noninverting input to the operational amplifiers of the Butterworth fourth-order low-pass filter.
CLKIN	1	I	Clock in. CLKIN is the clock input terminal for CMOS-compatible clock or self-clocking options. For either option, LS is at V_{CC-} . For self-clocking, a resistor is connected between CLKIN and CLKR and a capacitor is connected from CLKIN to ground.
CLKR	2	I	Clock R. CLKR is the clock input for a TTL-compatible clock. For a TTL clock, LS is connected to midsupply and CLKIN can be left open, but it is recommended that it be connected to either V_{CC+} or V_{CC-} .
FILTER IN	8	I	Filter input
FILTER OUT	5	O	Butterworth fourth-order low-pass filter output
LS	3	I	Level shift. LS accommodates the various input clocking options. For CMOS-compatible clocks or self-clocking, LS is at V_{CC-} and for TTL-compatible clocks, LS is at midsupply.
V_{CC+}	7	I	Positive supply voltage terminal
V_{CC-}	4	I	Negative supply voltage terminal

TLC04/MF4A-50, TLC14/MF4A-100
BUTTERWORTH FOURTH-ORDER LOW-PASS
SWITCHED-CAPACITOR FILTERS
 SLAS021A – NOVEMBER 1986 – REVISED MARCH 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC\pm}$ (see Note 1)	± 7 V
Operating free-air temperature range, T_A :	TLC04C/MF4A-50C, TLC14C/MF4A-100C 0°C to 70°C
	TLC04I/MF4A-50I, TLC14I/MF4A-100I -40°C to 85°C
	TLC04M/MF4A-50M, TLC14M/MF4A-100M -55°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the AGND terminal.

recommended operating conditions

	TLC04/MF4A-50		TLC14/MF4A-100		UNIT
	MIN	MAX	MIN	MAX	
Positive supply voltage, V_{CC+}	2.25	6	2.25	6	V
Negative supply voltage, V_{CC-}	-2.25	-6	-2.25	-6	V
High-level input voltage, V_{IH}	2		2		V
Low-level input voltage, V_{IL}	0.8		0.8		V
Clock frequency, f_{clock} (see Note 2)	$V_{CC\pm} = \pm 2.5$ V		5	1.5×10^6	Hz
	$V_{CC\pm} = \pm 5$ V		5	2×10^6	
Cutoff frequency, f_{CO} (see Note 3)	0.1	40×10^3	0.05	20×10^3	Hz
Operating free-air temperature, T_A	TLC04C/MF4A-50C, TLC14C/MF4A-100C		0	70	°C
	TLC04I/MF4A-50I, TLC14I/MF4A-100I		-40	85	
	TLC04M/MF4A-50M, TLC14M/MF4A-100M		-55	125	

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.

3. The cutoff frequency is defined as the frequency where the response is 3.01 dB less than the dc gain of the filter.

electrical characteristics over recommended operating free-air temperature range, $V_{CC+} = 2.5$ V, $V_{CC-} = -2.5$ V, $f_{clock} \leq 250$ kHz (unless otherwise noted)

filter section

PARAMETER	TEST CONDITIONS	TLC04/MF4A-50		TLC14/MF4A-100		UNIT	
		MIN	TYP‡	MAX	MIN		TYP‡
V_{OO} Output offset voltage		25		50		mV	
V_{OM} Peak output voltage	$R_L = 10$ k Ω	V_{OM+}	1.8	2	1.8	2	V
		V_{OM-}	-1.25	-1.7	-1.25	-1.7	
I_{OS} Short-circuit output current	Source	-0.5		-0.5		mA	
	Sink	4		4			
I_{CC} Supply current	$f_{clock} = 250$ kHz	1.2	2.25	1.2	2.25	mA	

‡ All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 4: $I_{OS(source)}$ is measured by forcing the output to its maximum positive voltage and then shorting the output to the V_{CC-} terminal. $I_{OS(sink)}$ is measured by forcing the output to its maximum negative voltage and then shorting the output to the V_{CC+} terminal.



TLC04/MF4A-50, TLC14/MF4A-100
BUTTERWORTH FOURTH-ORDER LOW-PASS
SWITCHED-CAPACITOR FILTERS

SLAS021A – NOVEMBER 1986 – REVISED MARCH 1995

electrical characteristics over recommended operating free-air temperature range, $V_{CC+} = 5\text{ V}$, $V_{CC-} = -5\text{ V}$, $f_{\text{clock}} \leq 250\text{ kHz}$ (unless otherwise noted)

filter section

PARAMETER		TEST CONDITIONS	TLC04/MF4A-50			TLC14/MF4A-100			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OO}	Output offset voltage		150			200			mV
V_{OM}	Peak output voltage	$R_L = 10\text{ k}\Omega$	3.75	4.3		3.75	4.5		V
			-3.75	-4.1		-3.75	-4.1		
I_{OS}	Short-circuit output current	$T_A = 25^\circ\text{C}$, See Note 4	-2			-2			mA
			5			5			
I_{CC}	Supply current	$f_{\text{clock}} = 250\text{ kHz}$	1.8	3		1.8	3	mA	
k_{SVS}	Supply voltage sensitivity (see Figures 1 and 2)		-30			-30			dB

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 4: $I_{OS(\text{source})}$ is measured by forcing the output to its maximum positive voltage and then shorting the output to the V_{CC-} terminal. $I_{OS(\text{sink})}$ is measured by forcing the output to its maximum negative voltage and then shorting the output to the V_{CC+} terminal.

clocking section

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		$V_{CC+} = 10\text{ V}$, $V_{CC-} = 0$	6.1	7	
		$V_{CC+} = 5\text{ V}$, $V_{CC-} = 0$		3.1	3.5	4.4
V_{IT-}	Negative-going input threshold voltage	$V_{CC+} = 10\text{ V}$, $V_{CC-} = 0$	1.3	3	3.8	V
			$V_{CC+} = 5\text{ V}$, $V_{CC-} = 0$	0.6	1.5	
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	$V_{CC+} = 10\text{ V}$, $V_{CC-} = 0$	2.3	4	7.6	V
			$V_{CC+} = 5\text{ V}$, $V_{CC-} = 0$	1.2	2	
V_{OH}	High-level output voltage	$V_{CC} = 10\text{ V}$ $I_O = -10\text{ }\mu\text{A}$	9			V
			4.5			
V_{OL}	Low-level output voltage	$V_{CC} = 10\text{ V}$ $I_O = 10\text{ }\mu\text{A}$	1			V
			0.5			
	Input leakage current	$V_{CC} = 10\text{ V}$ $V_{CC} = 5\text{ V}$ LS at midsupply, $T_A = 25^\circ\text{C}$	2			μA
			2			
I_O	Output current	$V_{CC} = 10\text{ V}$ $V_{CC} = 5\text{ V}$ CLKR and CLKIN shortened to V_{CC-}	-3			mA
			-7			
		$V_{CC} = 10\text{ V}$ $V_{CC} = 5\text{ V}$ CLKR and CLKIN shortened to V_{CC+}	-0.75			mA
			-2			
		3		7		
		0.75		2		

† All typical values are at $T_A = 25^\circ\text{C}$.



TLC04/MF4A-50, TLC14/MF4A-100
BUTTERWORTH FOURTH-ORDER LOW-PASS
SWITCHED-CAPACITOR FILTERS
 SLAS021A – NOVEMBER 1986 – REVISED MARCH 1995

operating characteristics over recommended operating free-air temperature range, $V_{CC+} = 2.5\text{ V}$, $V_{CC-} = -2.5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLC04/MF4A-50			TLC14/MF4A-100			UNIT	
		MIN	TYP†	MAX	MIN	TYP†	MAX		
Maximum clock frequency, f_{max}	See Note 2	1.5	3		1.5	3		MHz	
Clock-to-cutoff-frequency ratio (f_{clock}/f_{co})	$f_{clock} \leq 250\text{ kHz}$, $T_A = 25^\circ\text{C}$	49.27	50.07	50.87	99	100	101	Hz/Hz	
Temperature coefficient of clock-to-cutoff frequency ratio	$f_{clock} \leq 250\text{ kHz}$	±25			±25			ppm/°C	
Frequency response above and below cutoff frequency (see Note 5)	$f_{co} = 5\text{ kHz}$, $f_{clock} = 250\text{ kHz}$, $T_A = 25^\circ\text{C}$	$f = 6\text{ kHz}$	-7.9	-7.57	-7.1				dB
		$f = 4.5\text{ kHz}$	-1.7	-1.46	-1.3				
	$f_{co} = 5\text{ kHz}$, $f_{clock} = 250\text{ kHz}$, $T_A = 25^\circ\text{C}$	$f = 3\text{ kHz}$				-7.9	-7.42	-7.1	dB
		$f = 2.25\text{ kHz}$				-1.7	-1.51	-1.3	
Dynamic range (see Note 6)	$T_A = 25^\circ\text{C}$	80			78			dB	
Stop-band frequency attenuation at $2 f_{co}$	$f_{clock} \leq 250\text{ kHz}$	24	25		24	25		dB	
Voltage amplification, dc	$f_{clock} \leq 250\text{ kHz}$, $RS \leq 2\text{ k}\Omega$	-0.15	0	0.15	-0.15	0	0.15	dB	
Peak-to-peak clock feedthrough voltage	$T_A = 25^\circ\text{C}$	5			5			mV	

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.

5. The frequency responses at f are referenced to a dc gain of 0 dB.

6. The dynamic range is referenced to 1.06 V rms (1.5 V peak) where the wideband noise over a 30-kHz bandwidth is typically 106 μV rms for the TLC04/MF4A-50 and 135 μV rms for the TLC14/MF4A-100.

operating characteristics over recommended operating free-air temperature range, $V_{CC+} = 5\text{ V}$, $V_{CC-} = -5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLC04/MF4A-50			TLC14/MF4A-100			UNIT	
		MIN	TYP†	MAX	MIN	TYP†	MAX		
Maximum clock frequency, f_{max}	See Note 2	2	4		2	4		MHz	
Clock-to-cutoff-frequency ratio (f_{clock}/f_{co})	$f_{clock} \leq 250\text{ kHz}$, $T_A = 25^\circ\text{C}$	49.58	49.98	50.38	99	100	101	Hz/Hz	
Temperature coefficient of clock-to-cutoff frequency ratio	$f_{clock} \leq 250\text{ kHz}$	±15			±15			ppm/°C	
Frequency response above and below cutoff frequency (see Note 5)	$f_{co} = 5\text{ kHz}$, $f_{clock} = 250\text{ kHz}$, $T_A = 25^\circ\text{C}$	$f = 6\text{ kHz}$	-7.9	-7.57	-7.1				dB
		$f = 4.5\text{ kHz}$	-1.7	-1.44	-1.3				
	$f_{co} = 5\text{ kHz}$, $f_{clock} = 250\text{ kHz}$, $T_A = 25^\circ\text{C}$	$f = 3\text{ kHz}$				-7.9	-7.42	-7.1	dB
		$f = 2.25\text{ kHz}$				-1.7	-1.51	-1.3	
Dynamic range (see Note 6)	$T_A = 25^\circ\text{C}$	86			84			dB	
Stop-band frequency attenuation at $2 f_{co}$	$f_{clock} \leq 250\text{ kHz}$	24	25		24	25		dB	
Voltage amplification, dc	$f_{clock} \leq 250\text{ kHz}$, $RS \leq 2\text{ k}\Omega$	-0.15	0	0.15	-0.15	0	0.15	dB	
Peak-to-peak clock feedthrough voltage	$T_A = 25^\circ\text{C}$	7			7			mV	

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.

5. The frequency responses at f are referenced to a dc gain of 0 dB.

6. The dynamic range is referenced to 2.82 V rms (4 V peak) where the wideband noise over a 30-kHz bandwidth is typically 142 μV rms for the TLC04/MF4A-50 and 178 μV rms for the TLC14/MF4A-100.



TLC04/MF4A-50, TLC14/MF4A-100
BUTTERWORTH FOURTH-ORDER LOW-PASS
SWITCHED-CAPACITOR FILTERS

SLAS021A – NOVEMBER 1986 – REVISED MARCH 1995

TYPICAL CHARACTERISTICS

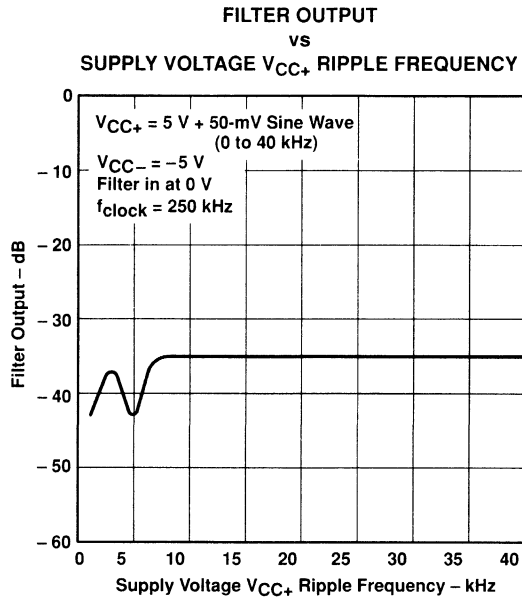


Figure 1

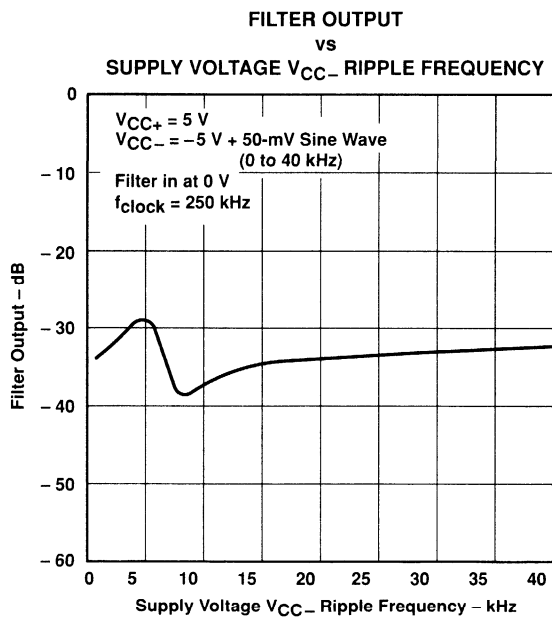


Figure 2

APPLICATION INFORMATION

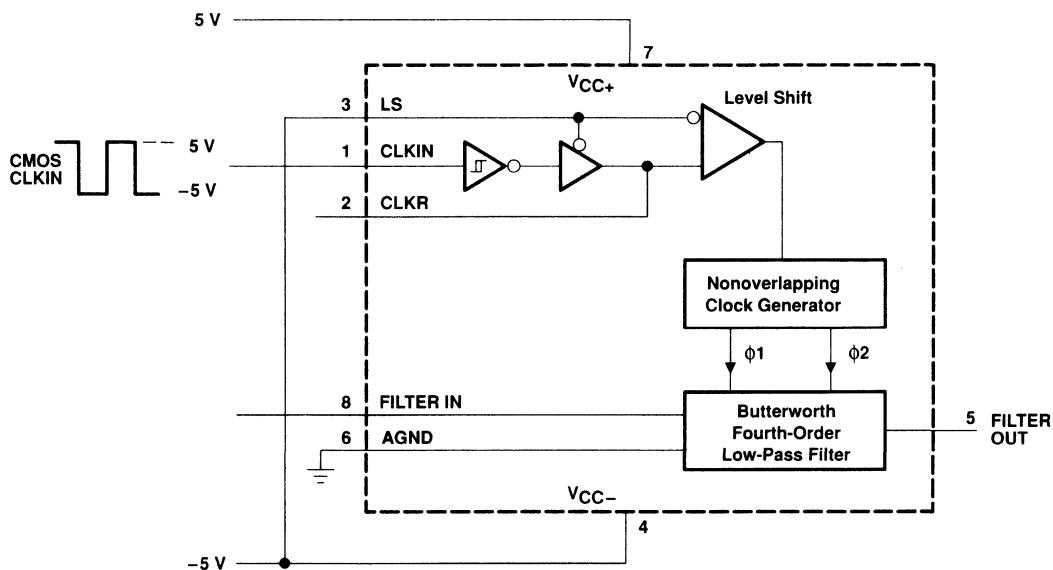


Figure 3. CMOS-Clock-Driven Dual-Supply Operation

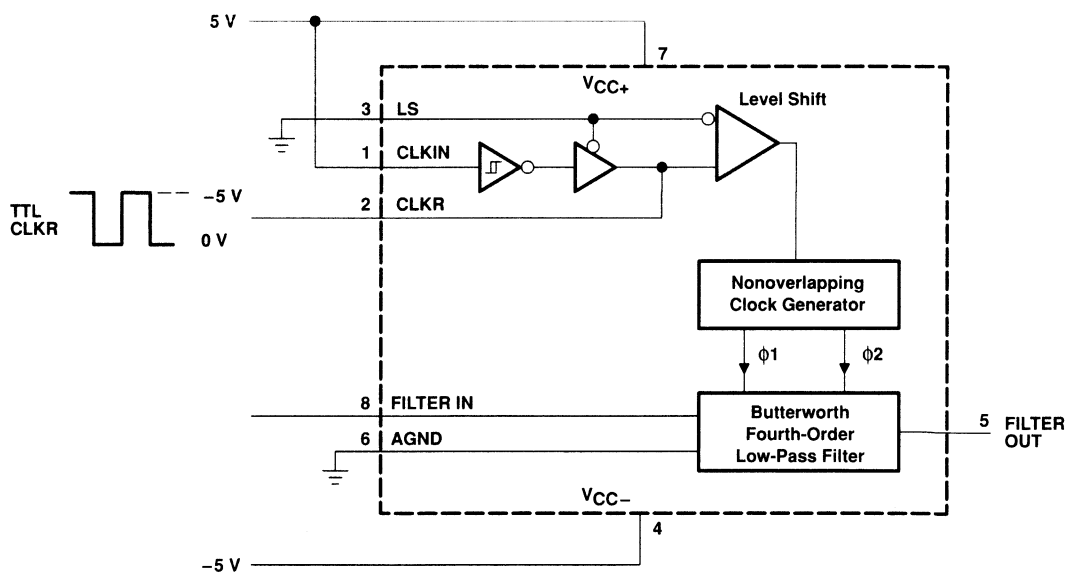
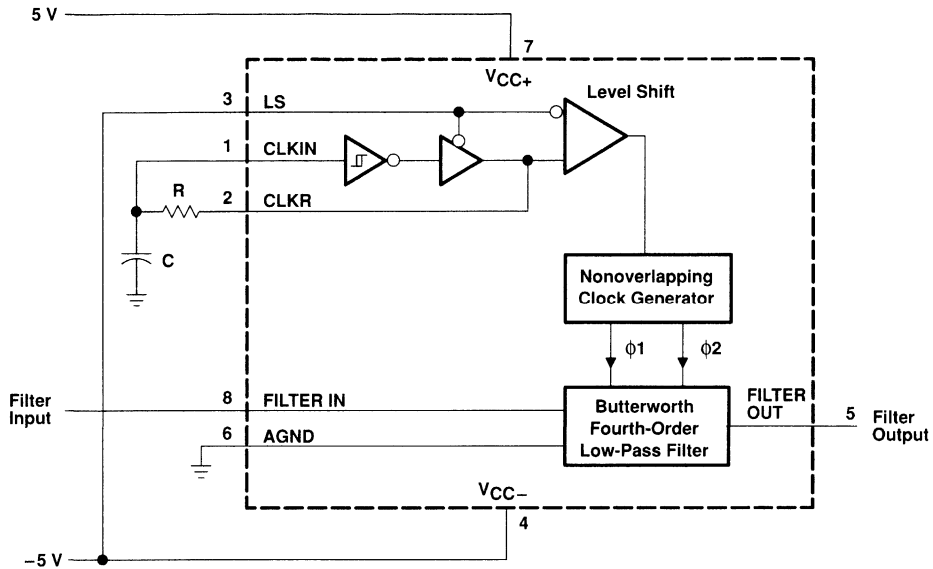


Figure 4. TTL-Clock-Driven Dual-Supply Operation

TLC04/MF4A-50, TLC14/MF4A-100
BUTTERWORTH FOURTH-ORDER LOW-PASS
SWITCHED-CAPACITOR FILTERS

SLAS021A – NOVEMBER 1986 – REVISED MARCH 1995

APPLICATION INFORMATION



$$f_{\text{clock}} = \frac{1}{RC \times \ln \left[\left(\frac{V_{CC} - V_{IT-}}{V_{CC} - V_{IT+}} \right) \left(\frac{V_{IT+}}{V_{IT-}} \right) \right]}$$

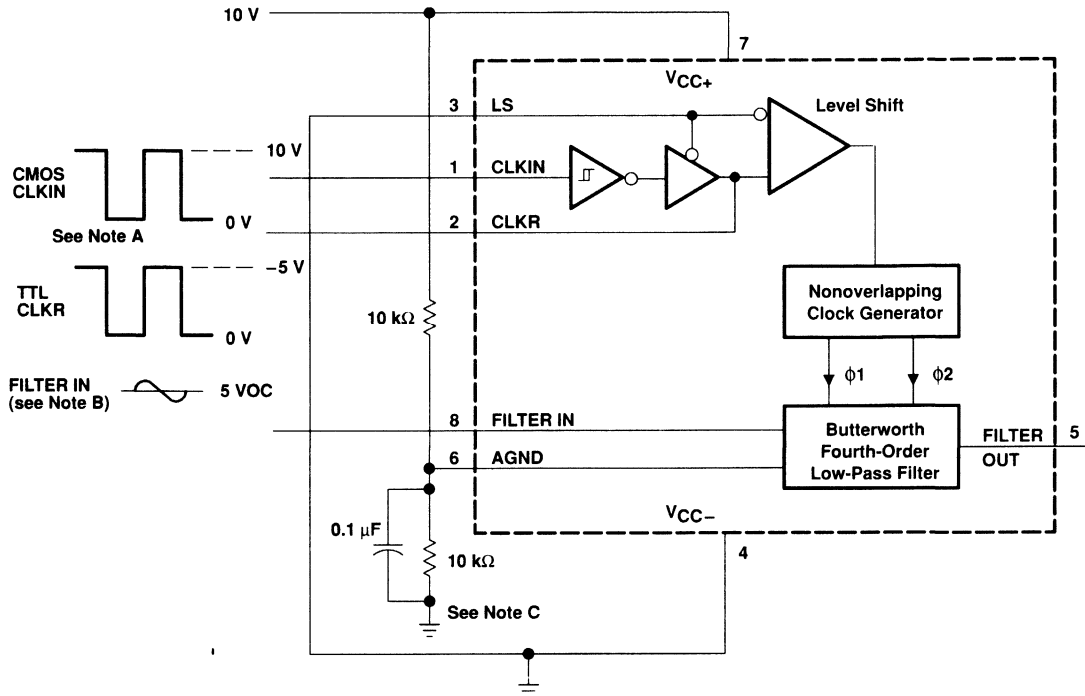
For $V_{CC} = 10 \text{ V}$

$$f_{\text{clock}} = \frac{1}{1.69 RC}$$

Figure 5. Self-Clocking Through Schmitt-Trigger Oscillator Dual-Supply Operation

TLC04/MF4A-50, TLC14/MF4A-100
BUTTERWORTH FOURTH-ORDER LOW-PASS
SWITCHED-CAPACITOR FILTERS
 SLAS021A – NOVEMBER 1986 – REVISED MARCH 1995

APPLICATION INFORMATION

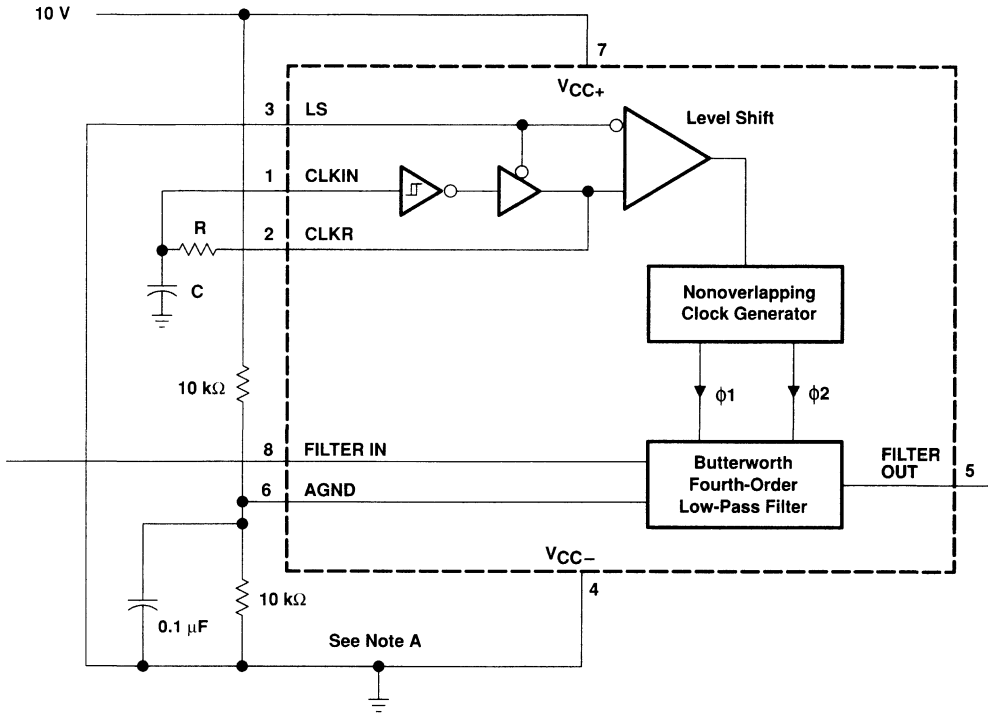


- NOTES: A. The external clock used must be of CMOS level because the clock is input to a CMOS Schmitt trigger.
 B. The filter input signal should be dc-biased to midsupply or ac-coupled to the terminal.
 C. AGND must be biased to midsupply.

Figure 6. External-Clock-Driven Single-Supply Operation

TLC04/MF4A-50, TLC14/MF4A-100
BUTTERWORTH FOURTH-ORDER LOW-PASS
SWITCHED-CAPACITOR FILTERS
 SLAS021A – NOVEMBER 1986 – REVISED MARCH 1995

APPLICATION INFORMATION



$$f_{\text{clock}} = \frac{1}{RC \times \ln \left[\left(\frac{V_{CC-} - V_{IT-}}{V_{CC-} - V_{IT+}} \right) \left(\frac{V_{IT+}}{V_{IT-}} \right) \right]}$$

For $V_{CC} = 10 \text{ V}$

$$f_{\text{clock}} = \frac{1}{1.69 RC}$$

NOTE A: AGND must be biased to midsupply.

Figure 7. Self Clocking Through Schmitt-Trigger Oscillator Single-Supply Operation

APPLICATION INFORMATION

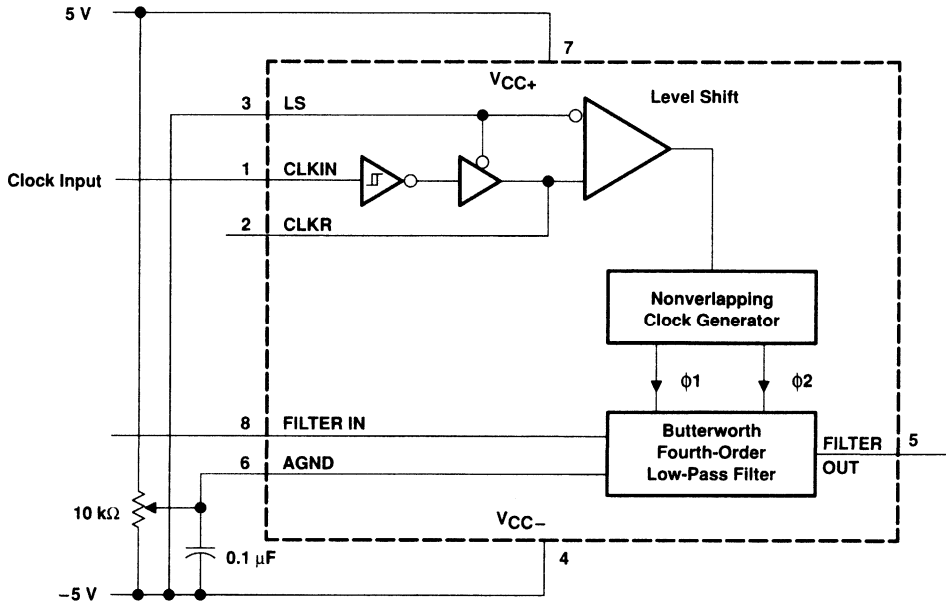
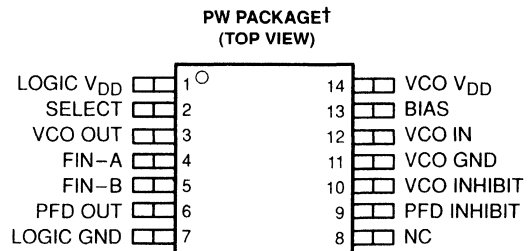


Figure 8. DC Offset Adjustment

TLC2932I HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS097E – SEPTEMBER 1994 – REVISED MAY 1997

- **Voltage-Controlled Oscillator (VCO) Section:**
 - Complete Oscillator Using Only One External Bias Resistor (R_{BIAS})
 - Lock Frequency:
 - 22 MHz to 50 MHz ($V_{DD} = 5\text{ V} \pm 5\%$, $T_A = -20^\circ\text{C}$ to 75°C , $\times 1$ Output)
 - 11 MHz to 25 MHz ($V_{DD} = 5\text{ V} \pm 5\%$, $T_A = -20^\circ\text{C}$ to 75°C , $\times 1/2$ Output)
 - Output Frequency . . . $\times 1$ and $\times 1/2$ Selectable
- **Phase-Frequency Detector (PFD) Section Includes a High-Speed Edge-Triggered Detector With Internal Charge Pump**
- **Independent VCO, PFD Power-Down Mode**
- **Thin Small-Outline Package (14 terminal)**
- **CMOS Technology**
- **Typical Applications:**
 - Frequency Synthesis
 - Modulation/Demodulation
 - Fractional Frequency Division
- **Application Report Available†**
- **CMOS Input Logic Level**

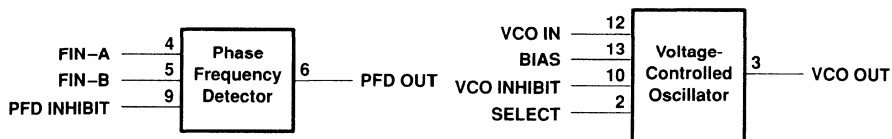


† Available in tape and reel only and ordered as the TLC2932IPWLE.
NC – No internal connection

description

The TLC2932I is designed for phase-locked-loop (PLL) systems and is composed of a voltage-controlled oscillator (VCO) and an edge-triggered-type phase frequency detector (PFD). The oscillation frequency range of the VCO is set by an external bias resistor (R_{BIAS}). The VCO has a 1/2 frequency divider at the output stage. The high-speed PFD with internal charge pump detects the phase difference between the reference frequency input and signal frequency input from the external counter. Both the VCO and the PFD have inhibit functions, which can be used as a power-down mode. The TLC2932I is suitable for use as a high-performance PLL due to the high speed and stable oscillation capability of the device.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (PW)
-20°C to 75°C	TLC2932IPWLE

† TLC2932 Phase-Locked-Loop Building Block With Analog Voltage-Controlled Oscillator and Phase Frequency Detector (SLAA011).

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TLC2932I

HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS097E – SEPTEMBER 1994 – REVISED MAY 1997

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
FIN-A	4	I	Input reference frequency $f_{(REF IN)}$ is applied to FIN-A.
FIN-B	5	I	Input for VCO external counter output frequency $f_{(FIN-B)}$. FIN-B is nominally provided from the external counter.
LOGIC GND	7		GND for the internal logic.
LOGIC V _{DD}	1		Power supply for the internal logic. This power supply should be separate from VCO V _{DD} to reduce cross-coupling between supplies.
NC	8		No internal connection.
PFD INHIBIT	9	I	PFD inhibit control. When PFD INHIBIT is high, PFD output is in the high-impedance state, see Table 3.
PFD OUT	6	O	PFD output. When the PFD INHIBIT is high, PFD output is in the high-impedance state.
BIAS	13	I	Bias supply. An external resistor (R _{BIAS}) between VCO V _{DD} and BIAS supplies bias for adjusting the oscillation frequency range.
SELECT	2	I	VCO output frequency select. When SELECT is high, the VCO output frequency is $\times 1/2$ and when low, the output frequency is $\times 1$, see Table 1.
VCO IN	12	I	VCO control voltage input. Nominally the external loop filter output connects to VCO IN to control VCO oscillation frequency.
VCO INHIBIT	10	I	VCO inhibit control. When VCO INHIBIT is high, VCO OUT is low (see Table 2).
VCO GND	11		GND for VCO.
VCO OUT	3	O	VCO output. When the VCO INHIBIT is high, VCO output is low.
VCO V _{DD}	14		Power supply for VCO. This power supply should be separated from LOGIC V _{DD} to reduce cross-coupling between supplies.

detailed description

VCO oscillation frequency

The VCO oscillation frequency is determined by an external resistor (R_{BIAS}) connected between the VCO V_{DD} and the BIAS terminals. The oscillation frequency and range depends on this resistor value. The bias resistor value for the minimum temperature coefficient is nominally 3.3 k Ω with 3-V at the VCO V_{DD} terminal and nominally 2.2 k Ω with 5-V at the VCO V_{DD} terminal. For the lock frequency range refer to the recommended operating conditions. Figure 1 shows the typical frequency variation and VCO control voltage.

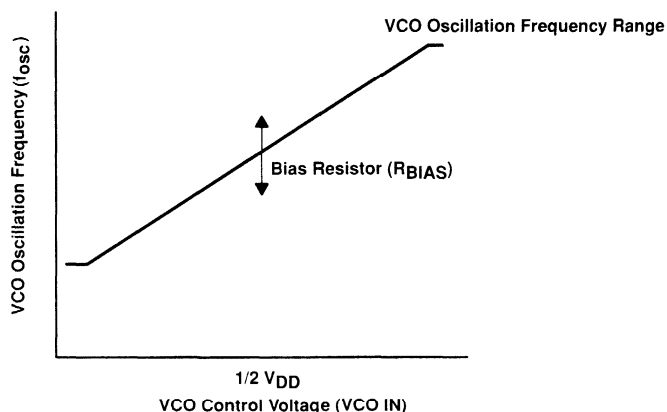


Figure 1. VCO Oscillation Frequency

TLC2932I HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS097E – SEPTEMBER 1994 – REVISED MAY 1997

VCO output frequency 1/2 divider

The TLC2932I SELECT terminal sets the f_{osc} or $1/2 f_{osc}$ VCO output frequency as shown in Table 1. The $1/2 f_{osc}$ output should be used for minimum VCO output jitter.

Table 1. VCO Output 1/2 Divider Function

SELECT	VCO OUTPUT
Low	f_{osc}
High	$1/2 f_{osc}$

VCO inhibit function

The VCO has an externally controlled inhibit function which inhibits the VCO output. A high level on the VCO INHIBIT terminal stops the VCO oscillation and powers down the VCO. The output maintains a low level during the power-down mode, refer to Table 2.

Table 2. VCO Inhibit Function

VCO INHIBIT	VCO OSCILLATOR	VCO OUTPUT	$I_{DD}(VCO)$
Low	Active	Active	Normal
High	Stopped	Low level	Power Down

PFD operation

The PFD is a high-speed, edge-triggered detector with an internal charge pump. The PFD detects the phase difference between two frequency inputs supplied to FIN-A and FIN-B as shown in Figure 2. Nominally the reference is supplied to FIN-A, and the frequency from the external counter output is fed to FIN-B.

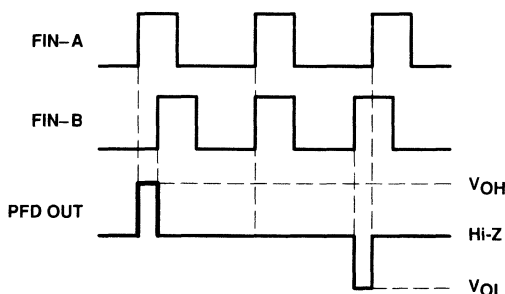


Figure 2. PFD Function Timing Chart

PFD output control

A high level on the PFD INHIBIT terminal places the PFD output in the high-impedance state and the PFD stops phase detection as shown in Table 3. A high level on the PFD INHIBIT terminal also can be used as the power-down mode for the PFD.

Table 3. VCO Output Control Function

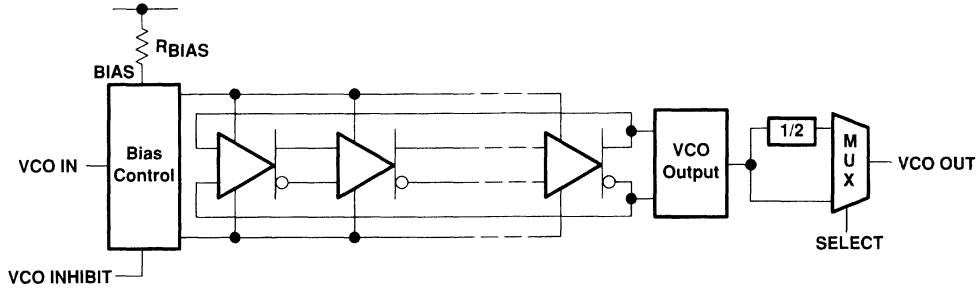
PFD INHIBIT	DETECTION	PFD OUTPUT	$I_{DD}(PFD)$
Low	Active	Active	Normal
High	Stopped	Hi-Z	Power Down

TLC29321 HIGH-PERFORMANCE PHASE-LOCKED LOOP

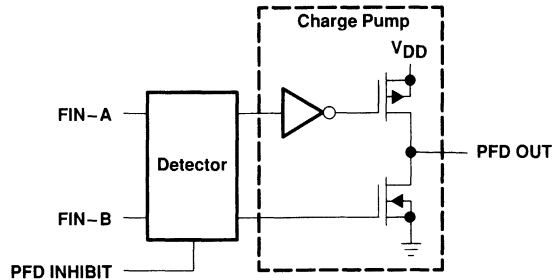
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schematics

VCO block schematic



PFDD block schematic



absolute maximum ratings†

Supply voltage (each supply), V_{DD} (see Note 1)	7 V
Input voltage range (each input), V_I (see Note 1)	-0.5 V to $V_{DD} + 0.5$ V
Input current (each input), I_I	± 20 mA
Output current (each output), I_O	± 20 mA
Continuous total power dissipation, at (or below) $T_A = 25^\circ\text{C}$ (see Note 2)	700 mW
Operating free-air temperature range, T_A	-20°C to 75°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network GND.

2. For operation above 25°C free-air temperature, derate linearly at the rate of $5.6 \text{ mW}/^\circ\text{C}$.

TLC29321 HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS097E – SEPTEMBER 1994 – REVISED MAY 1997

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (each supply, see Note 3)	$V_{DD} = 3\text{ V}$	2.85	3	3.15	V
	$V_{DD} = 5\text{ V}$	4.75	5	5.25	
Input voltage, V_I (inputs except VCO IN)		0		V_{DD}	V
Output current, I_O (each output)		0		± 2	mA
VCO control voltage at VCO IN		0.9		V_{DD}	V
Lock frequency ($\times 1$ output)	$V_{DD} = 3\text{ V}$	14		21	MHz
	$V_{DD} = 5\text{ V}$	22		50	
Lock frequency ($\times 1/2$ output)	$V_{DD} = 3\text{ V}$	7		10.5	MHz
	$V_{DD} = 5\text{ V}$	11		25	
Bias resistor, R_{BIAS}	$V_{DD} = 3\text{ V}$	2.2	3.3	4.3	k Ω
	$V_{DD} = 5\text{ V}$	1.5	2.2	3.3	

NOTE 3: It is recommended that the logic supply terminal (LOGIC V_{DD}) and the VCO supply terminal (VCO V_{DD}) should be at the same voltage and separated from each other.

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2\text{ mA}$	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.3	V
V_{IT}	Input threshold voltage at SELECT, VCO INHIBIT		0.9	1.5	2.1	V
I_I	Input current at SELECT, VCO INHIBIT	$V_I = V_{DD}$ or GND			± 1	μA
$Z_i(\text{VCO IN})$	Input impedance	VCO IN = $1/2 V_{DD}$		10		M Ω
$I_{DD}(\text{INH})$	VCO supply current (inhibit)	See Note 4		0.01	1	μA
$I_{DD}(\text{VCO})$	VCO supply current	See Note 5		5	15	mA

NOTES: 4. Current into VCO V_{DD} , when VCO INHIBIT = V_{DD} , PFD is inhibited.

5. Current into VCO V_{DD} , when VCO IN = $1/2 V_{DD}$, $R_{BIAS} = 3.3\text{ k}\Omega$, VCO INHIBIT = GND, and PFD is inhibited.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2\text{ mA}$	2.7			V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.2	V
I_{OZ}	High-impedance-state output current	PFD INHIBIT = high, $V_I = V_{DD}$ or GND			± 1	μA
V_{IH}	High-level input voltage at FIN-A, FIN-B		2.7			V
V_{IL}	Low-level input voltage at FIN-A, FIN-B				0.5	V
V_{IT}	Input threshold voltage at PFD INHIBIT		0.9	1.5	2.1	V
C_i	Input capacitance at FIN-A, FIN-B			5		pF
Z_i	Input impedance at FIN-A, FIN-B			10		M Ω
$I_{DD}(Z)$	High-impedance-state PFD supply current	See Note 6		0.01	1	μA
$I_{DD}(\text{PFD})$	PFD supply current	See Note 7		0.1	1.5	mA

NOTES: 6. Current into LOGIC V_{DD} , when FIN-A, FIN-B = GND, PFD INHIBIT = V_{DD} , no load, and VCO OUT is inhibited.

7. Current into LOGIC V_{DD} , when FIN-A, FIN-B = 1 MHz ($V_{I(PP)} = 3\text{ V}$, rectangular wave), NC = GND, no load, and VCO OUT is inhibited.



TLC2932I

HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS097E – SEPTEMBER 1994 – REVISED MAY 1997

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 3\text{ V}$
(unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Operating oscillation frequency	$R_{BIAS} = 3.3\text{ k}\Omega$, VCO IN = $1/2 V_{DD}$	15	19	23	MHz
$t_{s(fosc)}$	Time to stable oscillation (see Note 8)	Measured from VCO INHIBIT↓			10	μs
t_r	Rise time	$C_L = 15\text{ pF}$, See Figure 3		7	14	ns
		$C_L = 50\text{ pF}$, See Figure 3		14		
t_f	Fall time	$C_L = 15\text{ pF}$, See Figure 3		6	12	ns
		$C_L = 50\text{ pF}$, See Figure 3		10		
Duty cycle at VCO OUT		$R_{BIAS} = 3.3\text{ k}\Omega$, VCO IN = $1/2 V_{DD}$	45%	50%	55%	
$\alpha(f_{osc})$	Temperature coefficient of oscillation frequency	$R_{BIAS} = 3.3\text{ k}\Omega$, VCO IN = $1/2 V_{DD}$, $T_A = -20^\circ\text{C}$ to 75°C		0.04		$\%/^\circ\text{C}$
$k_{SVS(fosc)}$	Supply voltage coefficient of oscillation frequency	$R_{BIAS} = 3.3\text{ k}\Omega$, VCO IN = 1.5 V , $V_{DD} = 2.85\text{ V}$ to 3.15 V		0.02		$\%/m\text{V}$
Jitter absolute (see Note 9)		$R_{BIAS} = 3.3\text{ k}\Omega$		100		ps

- NOTES: 8. The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.
9. The low-pass-filter (LPF) circuit is shown in Figure 28 with calculated values listed in Table 7. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully designed PCB with no device socket.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency		20			MHz
t_{PLZ}	PFD output disable time from low level	See Figures 4 and 5 and Table 4		21	50	ns
t_{PHZ}	PFD output disable time from high level			23	50	
t_{PZL}	PFD output enable time to low level			11	30	ns
t_{PZH}	PFD output enable time to high level			10	30	
t_r	Rise time	$C_L = 15\text{ pF}$, See Figure 4		2.3	10	ns
t_f	Fall time			2.1	10	ns



TLC29321

HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS097E – SEPTEMBER 1994 – REVISED MAY 1997

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2\text{ mA}$	4			V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.5	V
V_{IT}	Input threshold voltage at SELECT, VCO INHIBIT		1.5	2.5	3.5	V
I_I	Input current at SELECT, VCO INHIBIT	$V_I = V_{DD}$ or GND			± 1	μA
$Z_i(\text{VCO IN})$	Input impedance	VCO IN = $1/2 V_{DD}$		10		$\text{M}\Omega$
$I_{DD}(\text{INH})$	VCO supply current (inhibit)	See Note 4		0.01	1	μA
$I_{DD}(\text{VCO})$	VCO supply current	See Note 5		15	35	mA

NOTES: 4. Current into VCO V_{DD} , when VCO INHIBIT = V_{DD} , and PFD is inhibited.
 5. Current into VCO V_{DD} , when VCO IN = $1/2 V_{DD}$, $R_{BIAS} = 3.3\text{ k}\Omega$, VCO INHIBIT = GND, and PFD is inhibited.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = 2\text{ mA}$	4.5			V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.2	V
I_{OZ}	High-impedance-state output current	PFD INHIBIT = high, $V_I = V_{DD}$ or GND			± 1	μA
V_{IH}	High-level input voltage at FIN-A, FIN-B		4.5			V
V_{IL}	Low-level input voltage at FIN-A, FIN-B				1	V
V_{IT}	Input threshold voltage at PFD INHIBIT		1.5	2.5	3.5	V
C_i	Input capacitance at FIN-A, FIN-B			5		pF
Z_i	Input impedance at FIN-A, FIN-B			10		$\text{M}\Omega$
$I_{DD}(Z)$	High-impedance-state PFD supply current	See Note 6		0.01	1	μA
$I_{DD}(\text{PFD})$	PFD supply current	See Note 7		0.15	3	mA

NOTES: 6. Current into LOGIC V_{DD} , when FIN-A, FIN-B = GND, PFD INHIBIT = V_{DD} , no load, and VCO OUT is inhibited.
 7. Current into LOGIC V_{DD} , when FIN-A, FIN-B = 1 MHz ($V_{I(PP)} = 5\text{ V}$, rectangular wave), PFD INHIBIT = GND, no load, and VCO OUT is inhibited.



TLC2932I

HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS097E – SEPTEMBER 1994 – REVISED MAY 1997

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Operating oscillation frequency	$R_{BIAS} = 2.2\text{ k}\Omega$, VCO IN = $1/2 V_{DD}$	30	41	52	MHz
$t_{s(fosc)}$	Time to stable oscillation (see Note 8)	Measured from VCO INHIBIT↓			10	μs
t_r	Rise time	$C_L = 15\text{ pF}$, See Figure 3		5.5	10	ns
		$C_L = 50\text{ pF}$, See Figure 3		8		
t_f	Fall time	$C_L = 15\text{ pF}$, See Figure 3		5	10	ns
		$C_L = 50\text{ pF}$, See Figure 3		6		
Duty cycle at VCO OUT		$R_{BIAS} = 2.2\text{ k}\Omega$, VCO IN = $1/2 V_{DD}$	45%	50%	55%	
$\alpha(f_{osc})$	Temperature coefficient of oscillation frequency	$R_{BIAS} = 2.2\text{ k}\Omega$, VCO IN = $1/2 V_{DD}$, $T_A = -20^\circ\text{C}$ to 75°C		0.06		$\%/^\circ\text{C}$
$k_{SVS(fosc)}$	Supply voltage coefficient of oscillation frequency	$R_{BIAS} = 2.2\text{ k}\Omega$, VCO IN = 2.5 V , $V_{DD} = 4.75\text{ V}$ to 5.25 V		0.006		$\%/mV$
Jitter absolute (see Note 9)		$R_{BIAS} = 2.2\text{ k}\Omega$		100		ps

NOTES: 8. The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.
9. The LPF circuit is shown in Figure 28 with calculated values listed in Table 7. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully designed PCB with no device socket.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency		40			MHz
t_{PLZ}	PFD output disable time from low level	See Figures 4 and 5 and Table 4		21	40	ns
t_{PHZ}	PFD output disable time from high level			20	40	
t_{PZL}	PFD output enable time to low level			7.3	20	ns
t_{PZH}	PFD output enable time to high level			6.5	20	
t_r	Rise time	$C_L = 15\text{ pF}$, See Figure 4		2.3	10	ns
t_f	Fall time			1.7	10	ns



PARAMETER MEASUREMENT INFORMATION

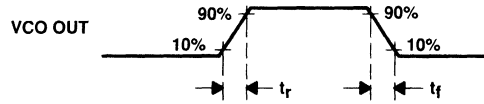
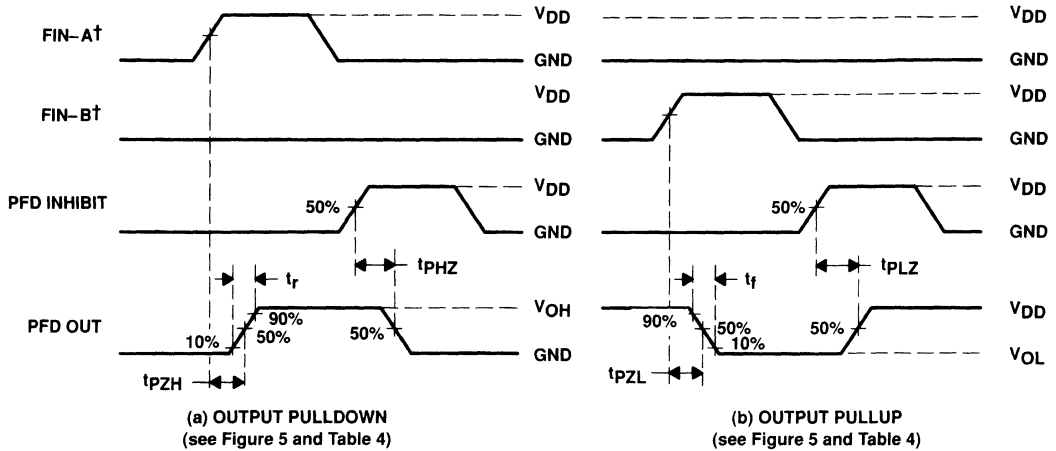


Figure 3. VCO Output Voltage Waveform



† FIN-A and FIN-B are for reference phase only, not for timing.

Figure 4. PFD Output Voltage Waveform

Table 4. PFD Output Test Conditions

PARAMETER	R_L	C_L	S ₁	S ₂
t_{PZH}	1 k Ω	15 pF	Open	Close
t_{PHZ}				
t_r				
t_{PZL}			Close	Open
t_{PLZ}				
t_f				

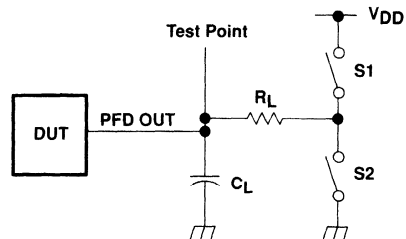


Figure 5. PFD Output Test Conditions

TLC2932I HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS097E – SEPTEMBER 1994 – REVISED MAY 1997

TYPICAL CHARACTERISTICS

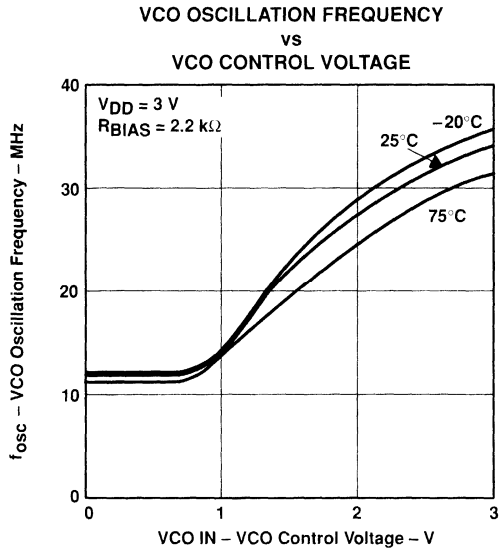


Figure 6

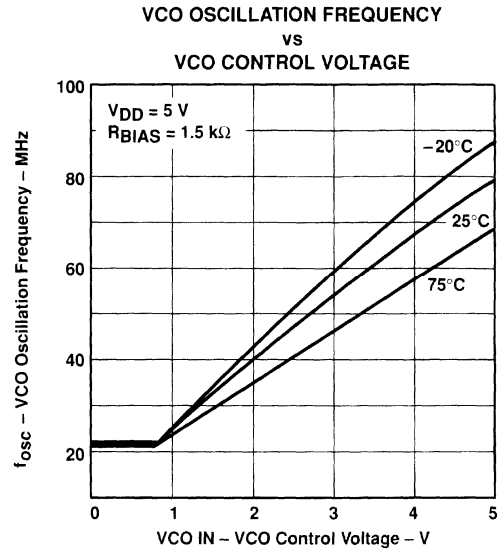


Figure 7

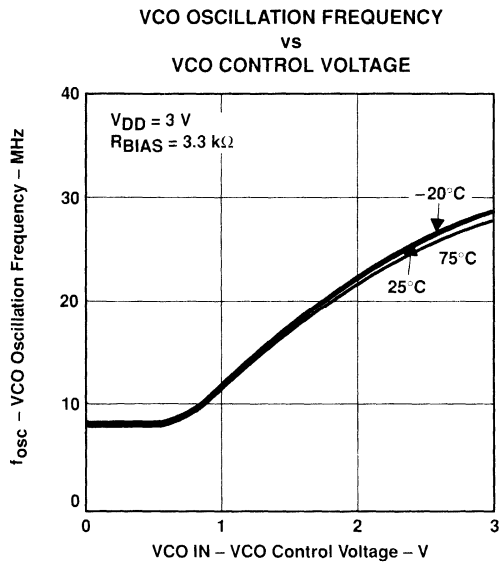


Figure 8

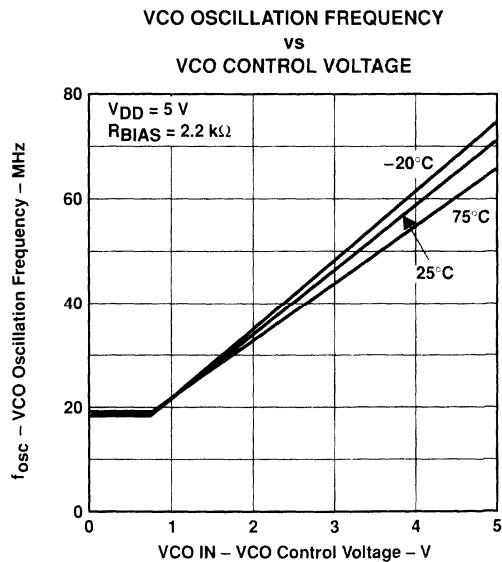


Figure 9



TYPICAL CHARACTERISTICS

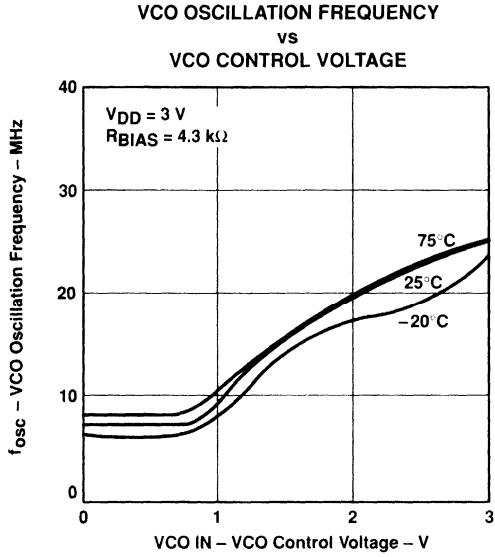


Figure 10

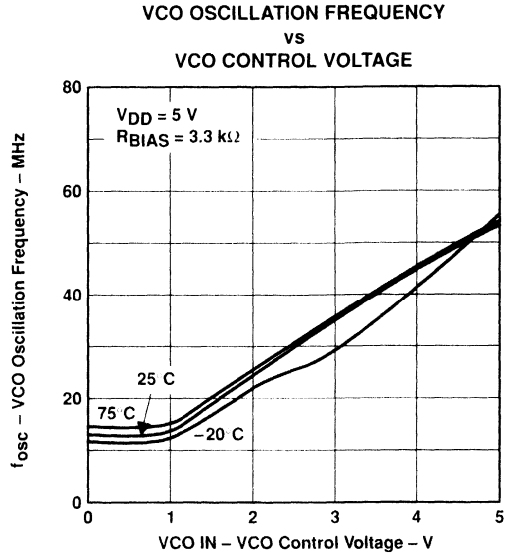


Figure 11

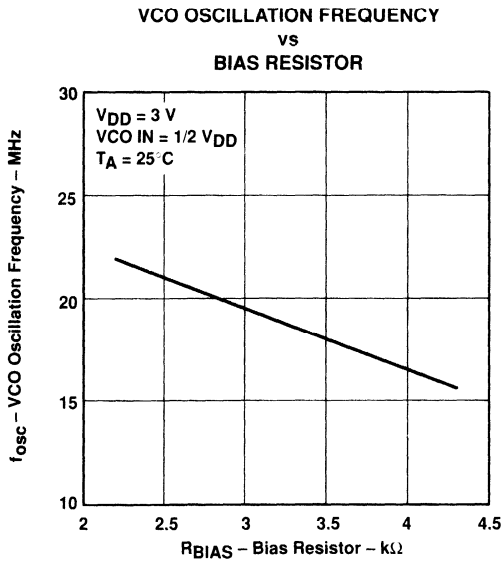


Figure 12

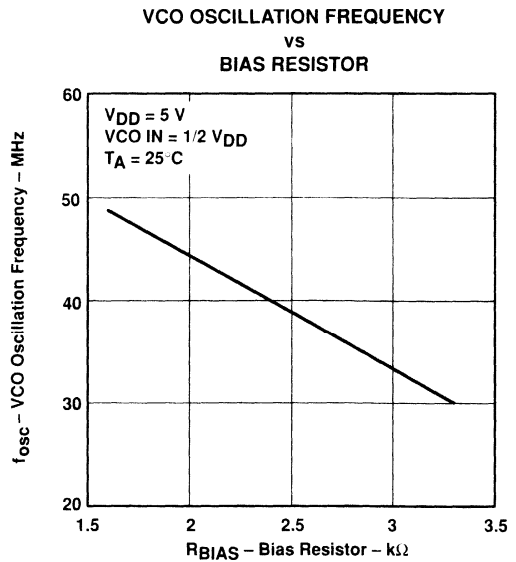


Figure 13

TLC2932I HIGH-PERFORMANCE PHASE-LOCKED LOOP

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TYPICAL CHARACTERISTICS

TEMPERATURE COEFFICIENT OF
OSCILLATION FREQUENCY
vs
BIAS RESISTOR

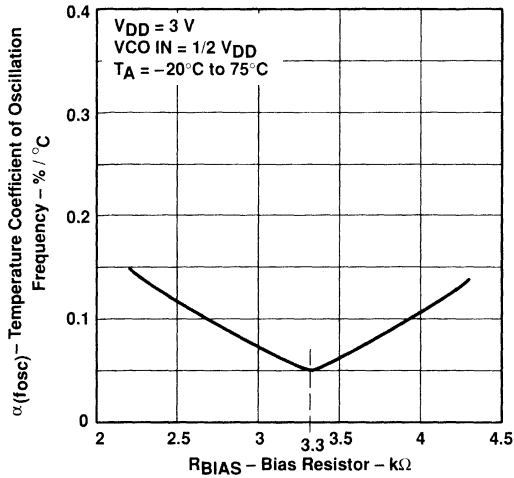


Figure 14

TEMPERATURE COEFFICIENT OF
OSCILLATION FREQUENCY
vs
BIAS RESISTOR

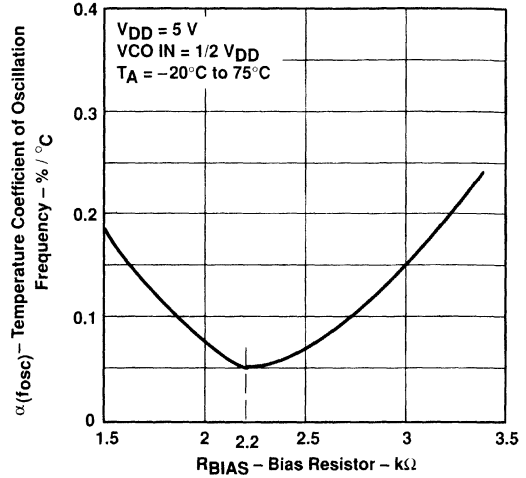


Figure 15

VCO OSCILLATION FREQUENCY
vs
VCO SUPPLY VOLTAGE

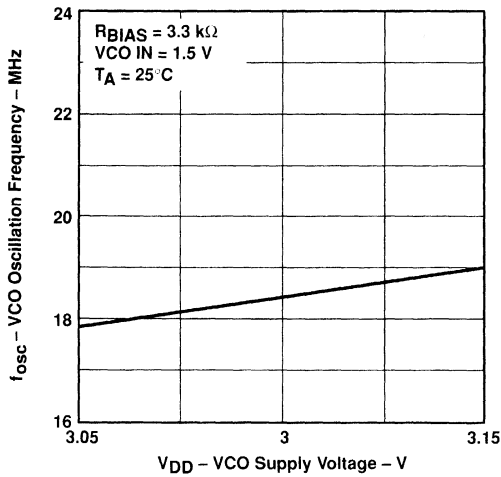


Figure 16

VCO OSCILLATION FREQUENCY
vs
VCO SUPPLY VOLTAGE

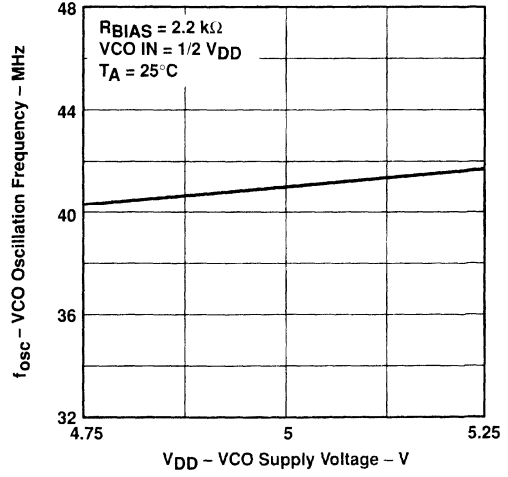


Figure 17



TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE COEFFICIENT OF VCO
OSCILLATION FREQUENCY
vs
BIAS RESISTOR

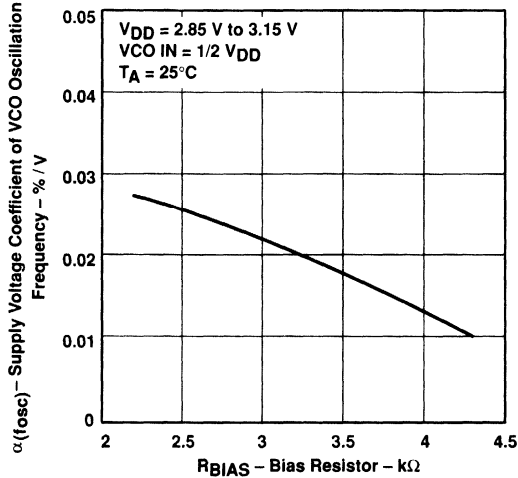


Figure 18

SUPPLY VOLTAGE COEFFICIENT OF VCO
OSCILLATION FREQUENCY
vs
BIAS RESISTOR

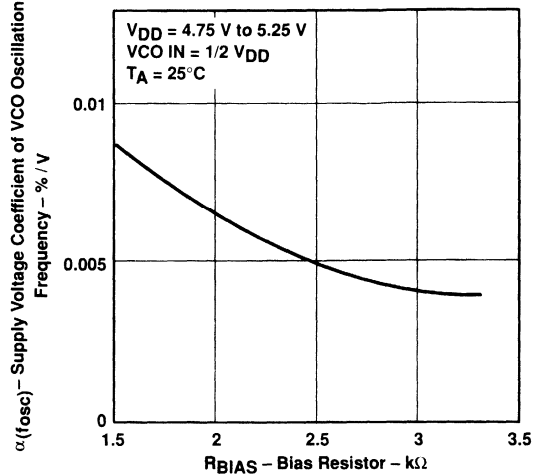


Figure 19

RECOMMENDED LOCK FREQUENCY
(×1 OUTPUT)
vs
BIAS RESISTOR

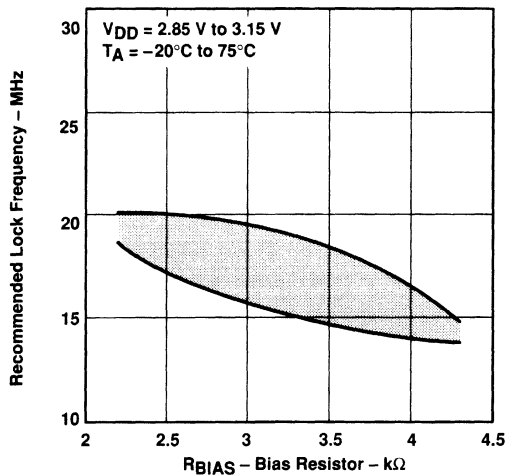


Figure 20

RECOMMENDED LOCK FREQUENCY
(×1 OUTPUT)
vs
BIAS RESISTOR

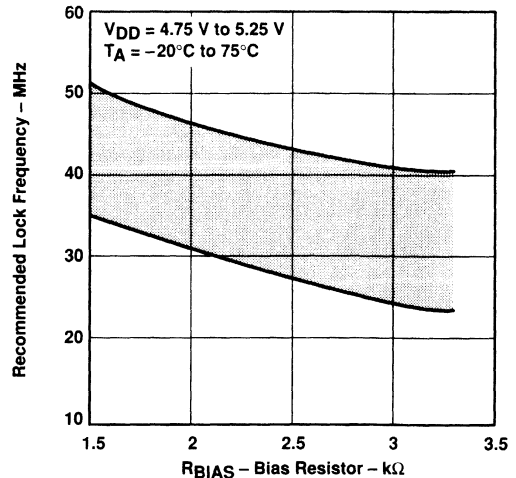
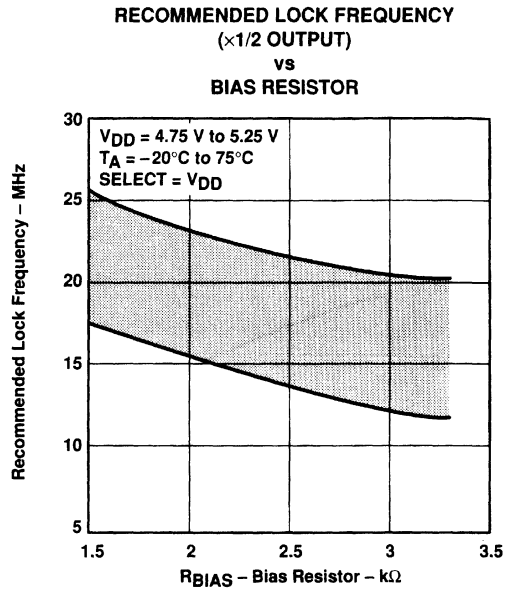
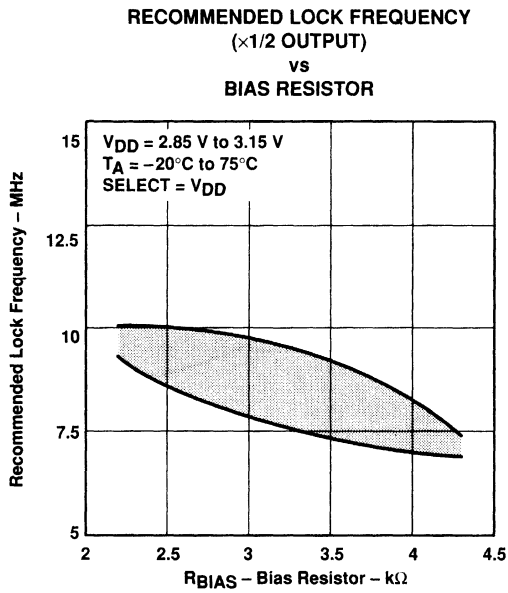


Figure 21

TLC2932I HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS097E – SEPTEMBER 1994 – REVISED MAY 1997

APPLICATION INFORMATION



APPLICATION INFORMATION

gain of VCO and PFD

Figure 24 is a block diagram of the PLL. The countdown N value depends on the input frequency and the desired VCO output frequency according to the system application requirements. The K_p and K_V values are obtained from the operating characteristics of the device as shown in Figure 24. K_p is defined from the phase detector V_{OL} and V_{OH} specifications and the equation shown in Figure 24(b). K_V is defined from Figures 8, 9, 10, and 11 as shown in Figure 24(c).

The parameters for the block diagram with the units are as follows:

- K_V : VCO gain (rad/s/V)
- K_p : PFD gain (V/rad)
- K_f : LPF gain (V/V)
- K_N : count down divider gain (1/N)

external counter

When a large N counter is required by the application, there is a possibility that the PLL response becomes slow due to the counter response delay time. In the case of a high frequency application, the counter delay time should be accounted for in the overall PLL design.

RBIAS

The external bias resistor sets the VCO center frequency with $1/2 V_{DD}$ applied to the VCO IN terminal. However, for optimum temperature performance, a resistor value of 3.3 kΩ with a 3-V supply and a resistor value of 2.5 kΩ for a 5-V supply is recommended. For the most accurate results, a metal-film resistor is the better choice but a carbon-composition resistor can be used with excellent results also. A 0.22 μF capacitor should be connected from the BIAS terminal to ground as close to the device terminals as possible.

hold-in range

From the technical literature, the maximum hold-in range for an input frequency step for the three types of filter configurations shown in Figure 25 is as follows:

$$\Delta\omega_H \approx 0.8 (K_p) (K_V) (K_f(\infty))$$

Where

$K_f(\infty)$ = the filter transfer function value at $\omega = \infty$

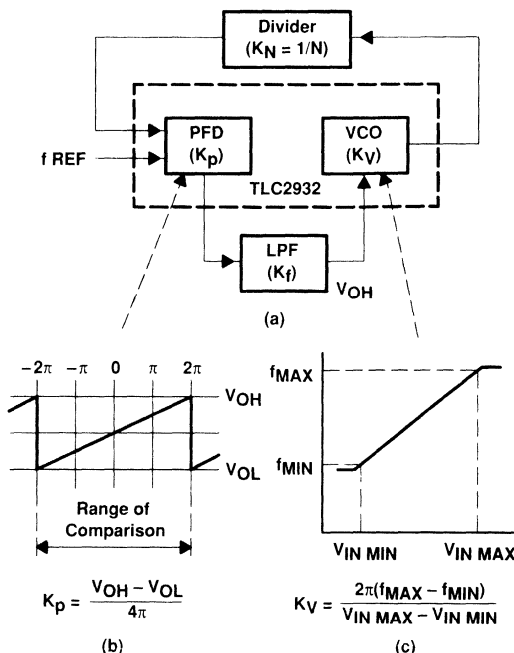


Figure 24. Example of a PLL Block Diagram

TLC2932I HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS097E – SEPTEMBER 1994 – REVISED MAY 1997

APPLICATION INFORMATION

low-pass-filter (LPF) configurations

Many excellent references are available that include detailed design information about LPFs and should be consulted for additional information. Lag-lead filters or active filters are often used. Examples of LPFs are shown in Figure 25. When the active filter of Figure 25(c) is used, the reference should be applied to FIN-B because of the amplifier inversion. Also, in practical filter implementations, C2 is used as additional filtering at the VCO input. The value of C2 should be equal to or less than one tenth the value of C1.

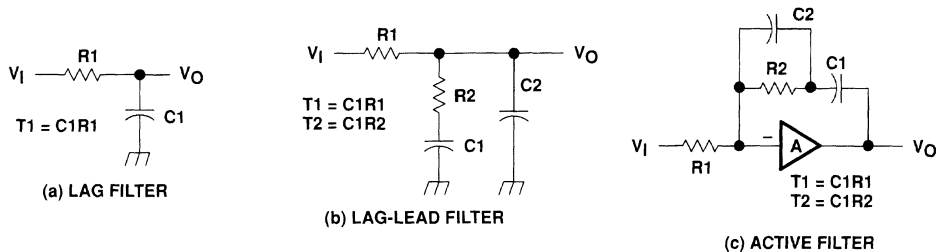


Figure 25. LPF Examples for PLL

the passive filter

The transfer function for the lag-lead filter shown in Figure 25(b) is;

$$\frac{V_O}{V_{IN}} = \frac{1 + s \cdot T_2}{1 + s \cdot (T_1 + T_2)}$$

Where

$$T_1 = R_1 \cdot C_1 \text{ and } T_2 = R_2 \cdot C_1$$

Using this filter makes the closed loop PLL system a second-order type 1 system. The response curves of this system to a unit step are shown in Figure 26.

the active filter

When using the active integrator shown in Figure 25(c), the phase detector inputs must be reversed since the integrator adds an additional inversion. Therefore, the input reference frequency should be applied to the FIN-B terminal and the output of the VCO divider should be applied to the input reference terminal, FIN-A.

The transfer function for the active filter shown in Figure 25(c) is:

$$F(s) = \frac{1 + s \cdot R_2 \cdot C_1}{s \cdot R_1 \cdot C_1}$$

Using this filter makes the closed loop PLL system a second-order type 2 system. The response curves of this system to a unit step are shown in Figure 27.

basic design example

The following design example presupposes that the input reference frequency and the required frequency of the VCO are within the respective ranges of the device.

APPLICATION INFORMATION

basic design example (continued)

Assume the loop has to have a 100 μs settling time (t_s) with a countdown $N = 8$. Using the Type 1, second order response curves of Figure 26, a value of 4.5 radians is selected for $\omega_n t_s$ with a damping factor of 0.7. This selection gives a good combination for settling time, accuracy, and loop gain margin. The initial parameters are summarized in Table 5. The loop constants, K_V and K_P , are calculated from the data sheet specifications and Table 6 shows these values.

The natural loop frequency is calculated as follows:

Since

$$\omega_n t_s = 4.5$$

Then

$$\omega_n = \frac{4.5}{100 \mu\text{s}} = 45 \text{ k-radians/sec}$$

Table 5. Design Parameters

PARAMETER	SYMBOL	VALUE	UNITS
Division factor	N	8	
Lockup time	t	100	μs
Radian value to selected lockup time	$\omega_n t$	4.5	rad
Damping factor	ζ	0.7	

Table 6. Device Specifications

PARAMETER	SYMBOL	VALUE	UNITS
VCO gain		76.6	Mrad/V/s
f _{MAX}	K_V	70	MHz
f _{MIN}		20	MHz
V _{IN MAX}		5	V
V _{IN MIN}		0.9	V
PFD gain	K_P	0.342357	V/rad

Table 7. Calculated Values

PARAMETER	SYMBOL	VALUE	UNITS
Natural angular frequency	ω_n	45000	rad/sec
$K = (K_V \cdot K_P)/N$		3.277	Mrad/sec
Lag-lead filter			
Calculated value	R1	15870	Ω
Nearest standard value		16000	
Calculated value	R2	308	Ω
Nearest standard value		300	
Selected value	C1	0.1	μF

TLC2932I HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS097E – SEPTEMBER 1994 – REVISED MAY 1997

APPLICATION INFORMATION

Using the low-pass filter in Figure 25(b) and divider ratio N, the transfer function for phase and frequency are shown in equations 1 and 2. Note that the transfer function for phase differs from the transfer function for frequency by only the divider value N. The difference arises from the fact that the feedback for phase is unity while the feedback for frequency is 1/N.

Hence, transfer function of Figure 24 (a) for phase is

$$\frac{\Phi_2(s)}{\Phi_1(s)} = \frac{K_p \cdot K_V}{N \cdot (T_1 + T_2)} \left[\frac{1 + s \cdot T_2}{s^2 + s \left[1 + \frac{K_p \cdot K_V \cdot T_2}{N \cdot (T_1 + T_2)} \right] + \frac{K_p \cdot K_V}{N \cdot (T_1 + T_2)}} \right] \quad (1)$$

and the transfer function for frequency is

$$\frac{F_{OUT}(s)}{F_{REF}(s)} = \frac{K_p \cdot K_V}{(T_1 + T_2)} \left[\frac{1 + s \cdot T_2}{s^2 + s \cdot \left[1 + \frac{K_p \cdot K_V \cdot T_2}{N \cdot (T_1 + T_2)} \right] + \frac{K_p \cdot K_V}{N \cdot (T_1 + T_2)}} \right] \quad (2)$$

The standard two-pole denominator is $D = s^2 + 2 \zeta \omega_n s + \omega_n^2$ and comparing the coefficients of the denominator of equation 1 and 2 with the standard two-pole denominator gives the following results.

$$\omega_n = \sqrt{\frac{K_p \cdot K_V}{N \cdot (T_1 + T_2)}}$$

Solving for $T_1 + T_2$

$$T_1 + T_2 = \frac{K_p \cdot K_V}{N \cdot \omega_n^2} \quad (3)$$

and by using this value for $T_1 + T_2$ in equation 3 the damping factor is

$$\zeta = \frac{\omega_n}{2} \cdot \left(T_2 + \frac{N}{K_p \cdot K_V} \right)$$

solving for T2

$$T_2 = \frac{2 \zeta}{\omega_n} - \frac{N}{K_p \cdot K_V}$$

then by substituting for T2 in equation 3

$$T_1 = \frac{K_V \cdot K_p}{N \cdot \omega_n^2} - \frac{2 \zeta}{\omega_n} + \frac{N}{K_p \cdot K_V}$$

APPLICATION INFORMATION

From the circuit constants and the initial design parameters then

$$R2 = \left[\frac{2 \zeta}{\omega_n} - \frac{N}{K_p \cdot K_V} \right] \frac{1}{C1}$$

$$R1 = \left[\frac{K_p \cdot K_V}{\omega_n^2 \cdot N} - \frac{2 \zeta}{\omega_n} + \frac{N}{K_p \cdot K_V} \right] \frac{1}{C1}$$

The capacitor, C1, is usually chosen between 1 μ F and 0.1 μ F to allow for reasonable resistor values and physical capacitor size. In this example, C1 is chosen to be 0.1 μ F and the corresponding R1 and R2 calculated values are listed in Table 7.

TLC2932I HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS097E – SEPTEMBER 1994 – REVISED MAY 1997

APPLICATION INFORMATION

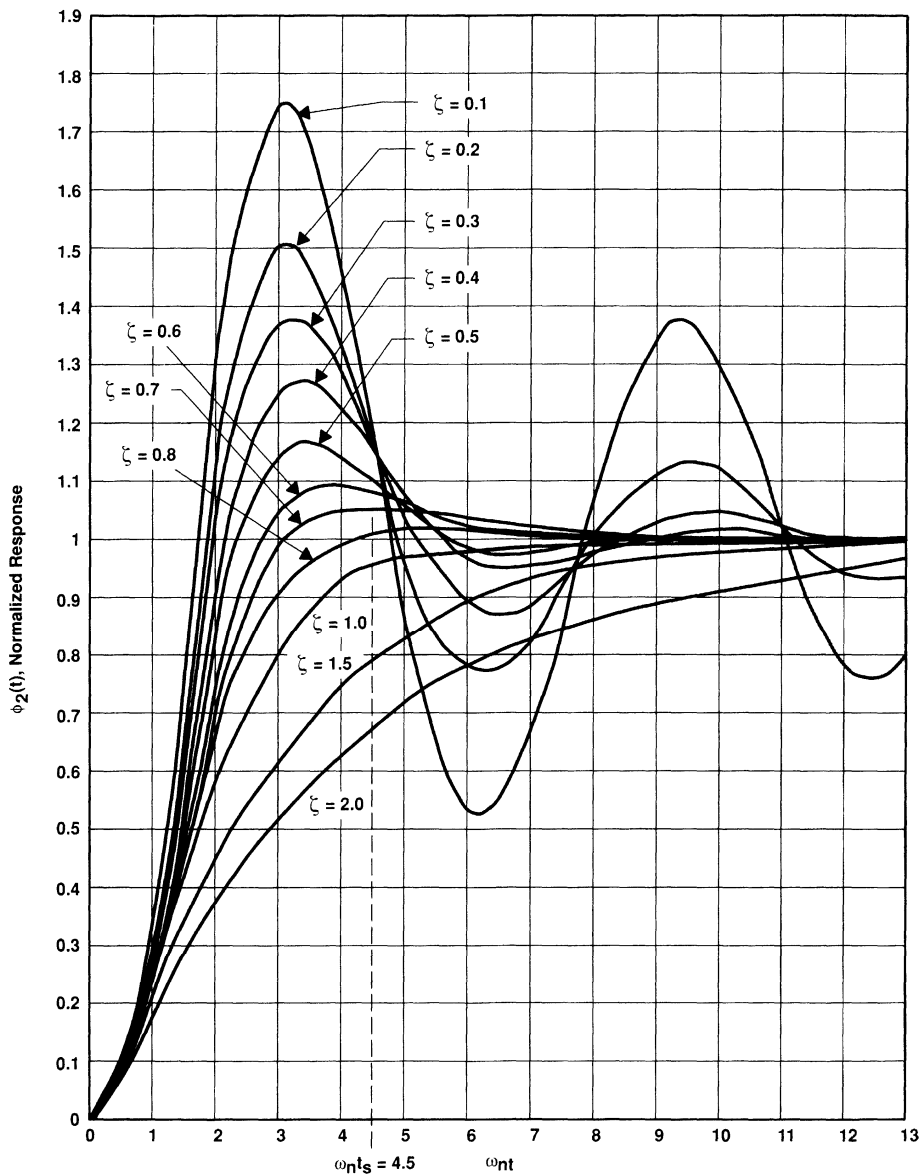


Figure 26. Type 1 Second-Order Step Response

APPLICATION INFORMATION

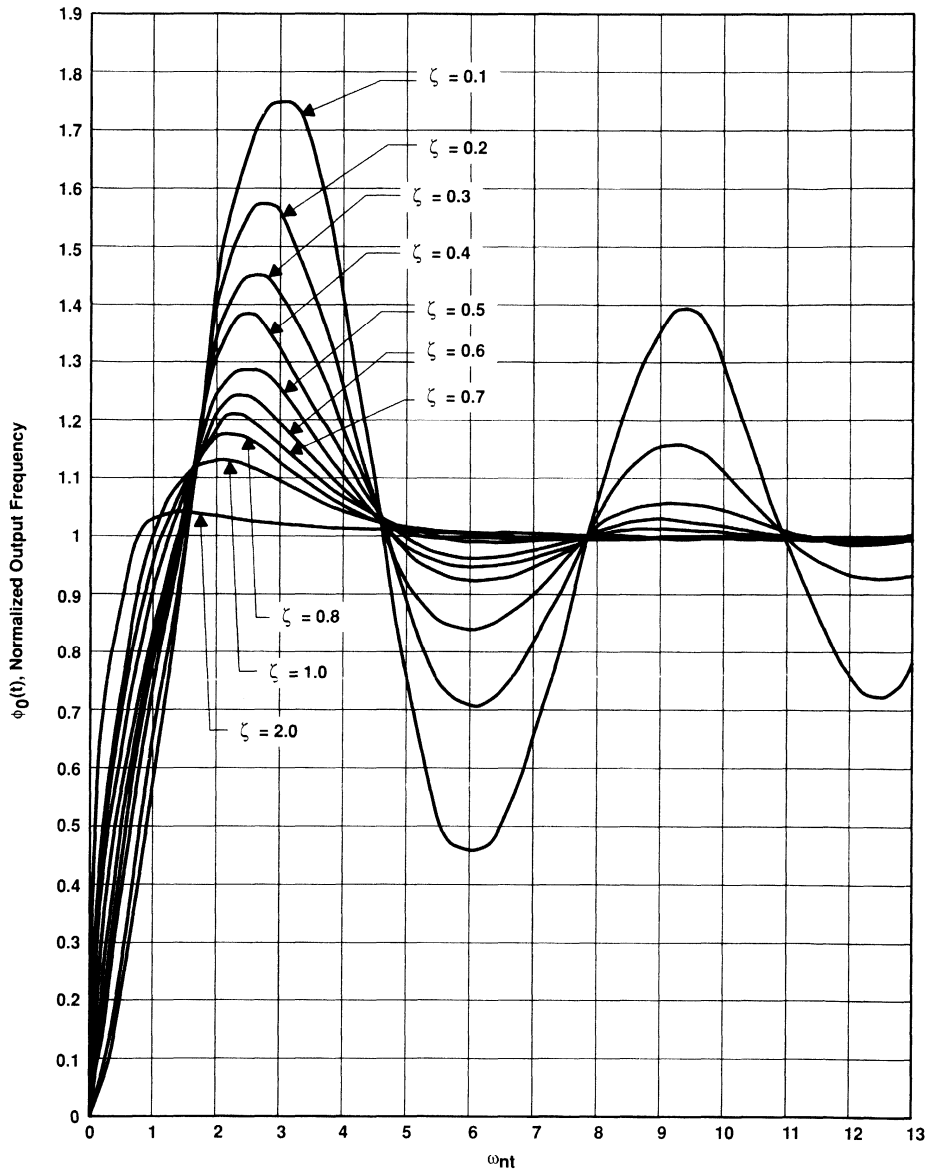


Figure 27. Type 2 Second-Order Step Response

TLC2932I HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS097E – SEPTEMBER 1994 – REVISED MAY 1997

APPLICATION INFORMATION

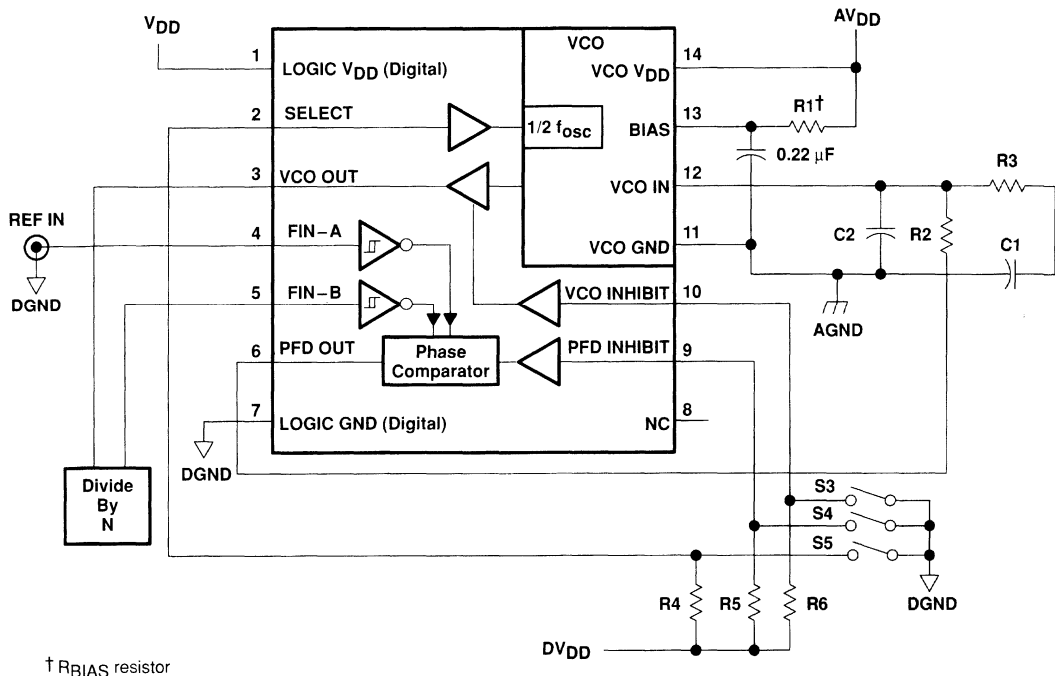


Figure 28. Evaluation and Operation Schematic

PCB layout considerations

The TLC2932I contains a high frequency analog oscillator; therefore, very careful breadboarding and printed-circuit-board (PCB) layout is required for evaluation.

The following design recommendations benefit the TLC2932I user:

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or RF PCB techniques should be used throughout the evaluation and production process.
- Wide ground leads or a ground plane should be used on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.
- LOGIC V_{DD} and VCO V_{DD} should be separate PCB traces and connected to the best filtered supply point available in the system to minimize supply cross-coupling.
- VCO V_{DD} to GND and LOGIC V_{DD} to GND should be decoupled with a 0.1-μF capacitor placed as close as possible to the appropriate device terminals.
- The no-connection (NC) terminal on the package should be connected to GND.

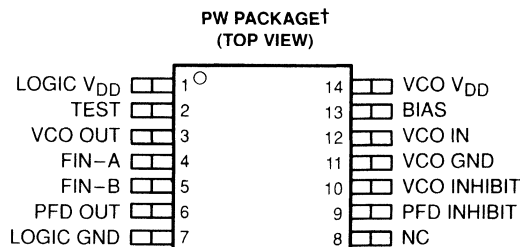


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TLC2933 HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS136A – APRIL 1996 – REVISED JUNE 1997

- **Voltage-Controlled Oscillator (VCO) Section:**
 - Ring Oscillator Using Only One External Bias Resistor (R_{BIAS})
 - Lock Frequency:
 - 43 MHz to 100 MHz ($V_{DD} = 5\text{ V} \pm 5\%$, $T_A = -20^\circ\text{C}$ to 75°C , $\times 1$ Output)
 - 37 MHz to 55 MHz ($V_{DD} = 3\text{ V} \pm 5\%$, $T_A = -20^\circ\text{C}$ to 75°C)
- **Phase-Frequency Detector (PFD) Section Includes a High-Speed Edge-Triggered Detector With Internal Charge Pump**
- **Independent VCO, PFD Power-Down Mode**
- **Thin Small-Outline Package (14 terminal)**
- **CMOS Technology**
- **Typical Applications:**
 - Frequency Synthesis
 - Modulation/Demodulation
 - Fractional Frequency Division
- **CMOS Input Logic Level**

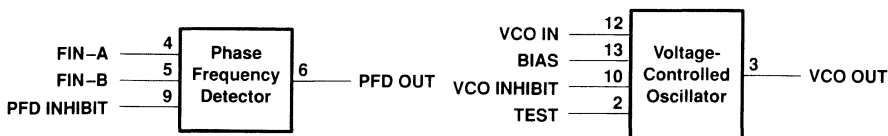


† Available in tape and reel only and ordered as the TLC2933PWLE.
NC – No internal connection

description

The TLC2933 is designed for phase-locked-loop (PLL) systems and is composed of a voltage-controlled oscillator (VCO) and an edge-triggered-type phase frequency detector (PFD). The oscillation frequency range of the VCO is set by an external bias resistor (R_{BIAS}). The high-speed PFD with internal charge pump detects the phase difference between the reference frequency input and signal frequency input from the external counter. Both the VCO and the PFD have inhibit functions that can be used as a power-down mode. With the high-speed and stable VCO characteristics, the TLC2933 is well suited for use in high-performance PLL systems.

functional block diagram



AVAILABLE OPTIONS

T _A	PACKAGE
	–20°C to 75°C

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TLC2933

HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS136A – APRIL 1996 – REVISED JUNE 1997

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
BIAS	13	I	Bias supply. An external resistor (R_{BIAS}) between VCO V_{DD} and BIAS supplies bias for adjusting the oscillation frequency range.
FIN-A	4	I	Input reference frequency $f_{(REF IN)}$ is applied to FIN-A.
FIN-B	5	I	Input for VCO external counter output frequency $f_{(FIN-B)}$. FIN-B is nominally provided from the external counter.
LOGIC GND	7		Ground for the internal logic.
LOGIC V_{DD}	1		Power supply for the internal logic. This power supply should be separate from VCO V_{DD} to reduce cross-coupling between supplies.
NC	8		No internal connection.
PFD INHIBIT	9	I	PFD inhibit control. When PFD INHIBIT is high, PFD OUT is in the high-impedance state, see Table 2.
PFD OUT	6	O	PFD output. When the PFD INHIBIT is high, PFD OUT is in the high-impedance state.
TEST	2	I	Test terminal. TEST connects to ground for normal operation.
VCO GND	11		Ground for VCO.
VCO IN	12	I	VCO control voltage input. Nominally the external loop filter output connects to VCO IN to control VCO oscillation frequency.
VCO INHIBIT	10	I	VCO inhibit control. When VCO INHIBIT is high, VCO OUT is low (see Table 1).
VCO OUT	3	O	VCO output. When VCO INHIBIT is high, VCO OUT is low.
VCO V_{DD}	14		Power supply for VCO. This power supply should be separated from LOGIC V_{DD} to reduce cross-coupling between supplies.

detailed description

VCO oscillation frequency

The VCO oscillation frequency is determined by an external resistor (R_{BIAS}) connected between the VCO V_{DD} and the BIAS terminals. The oscillation frequency and range depends on this resistor value. While all resistor values within the specified range result in excellent low temperature coefficients, the bias resistor value for the minimum temperature coefficient is nominally 2.2 k Ω with 3-V V_{DD} and nominally 2.4 k Ω with 5-V V_{DD} . For the lock frequency range refer to the recommended operating conditions. Figure 1 shows the typical frequency variation and VCO control voltage.

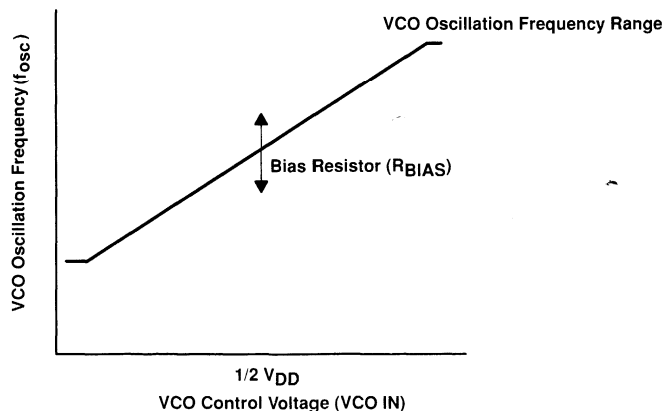


Figure 1. VCO Oscillation Frequency

VCO inhibit function

The VCO has an externally controlled inhibit function which inhibits the VCO output. A high level on the VCO INHIBIT terminal stops the VCO oscillation and powers down the VCO. The output maintains a low level during the power-down mode as shown in Table 1.

Table 1. VCO Inhibit Function

VCO INHIBIT	VCO OSCILLATOR	VCO OUT	I _{DD} (VCO)
Low	Active	Active	Normal
High	Stopped	Low level	Power Down

PFD operation

The PFD is a high-speed, edge-triggered detector with an internal charge pump. The PFD detects the phase difference between two frequency inputs supplied to FIN-A and FIN-B as shown in Figure 2. Nominally the reference is supplied to FIN-A, and the frequency from the external counter output is fed to FIN-B. For clock recovery PLL systems, other types of phase detectors should be used.

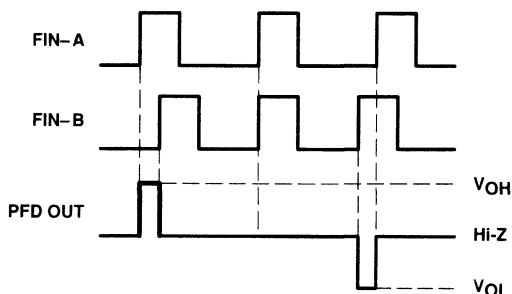


Figure 2. PFD Function Timing Chart

PFD inhibit control

A high level on the PFD INHIBIT terminal places PFD OUT in the high-impedance state and the PFD stops phase detection as shown in Table 2. A high level on the PFD INHIBIT terminal can also be used as the power-down mode for the PFD.

Table 2. VCO Output Control Function

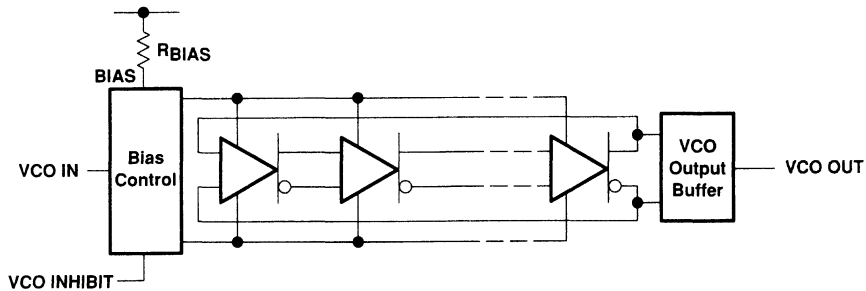
PFD INHIBIT	DETECTION	PFD OUT	I _{DD} (PFD)
Low	Active	Active	Normal
High	Stopped	Hi-Z	Power Down

TLC2933 HIGH-PERFORMANCE PHASE-LOCKED LOOP

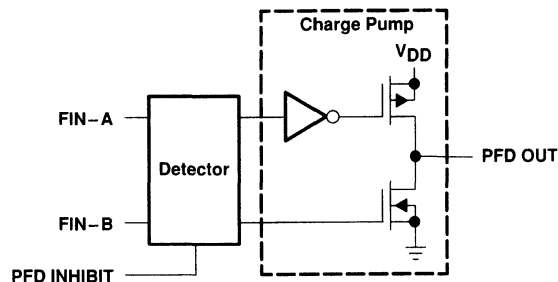
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schematics

VCO block schematic



PFD block schematic



absolute maximum ratings†

Supply voltage (each supply), V _{DD} (see Note 1)	7 V
Input voltage range (each input), V _I (see Note 1)	-0.3 V to V _{DD} + 0.3 V
Input current (each input), I _I	±20 mA
Output current (each output), I _O	±20 mA
Continuous total power dissipation at (or below) T _A = 25°C (see Note 2)	700 mW
Operating free-air temperature range, T _A	-20°C to 75°C
Storage temperature range, T _{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 5.6 mW/°C.

TLC2933 HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS136A – APRIL 1996 – REVISED JUNE 1997

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (each supply, see Note 3)	$V_{DD} = 3\text{ V}$	2.85	3	3.15	V
	$V_{DD} = 5\text{ V}$	4.75	5	5.25	
Input voltage, V_I (inputs except VCO IN)		0		V_{DD}	V
Output current, I_O (each output)		0		± 2	mA
VCO control voltage at VCO IN		1		V_{DD}	V
Lock frequency	$V_{DD} = 3\text{ V}$	37		55	MHz
	$V_{DD} = 5\text{ V}$	43		100	
Bias resistor, R_{BIAS}	$V_{DD} = 3\text{ V}$	1.8		2.7	k Ω
	$V_{DD} = 5\text{ V}$	2.2		3	

NOTE 3: It is recommended that the logic supply terminal (LOGIC V_{DD}) and the VCO supply terminal (VCO V_{DD}) be at the same voltage and separated from each other.

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

VCO section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	$I_{OH} = -2\text{ mA}$	2.4			V
V_{OL} Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.3	V
V_{IT+} Positive input threshold voltage at TEST, VCO INHIBIT		0.9	1.5	2.1	V
I_I Input current at TEST, VCO INHIBIT	$V_I = V_{DD}$ or ground			± 1	μA
$Z_i(\text{VCO IN})$ Input impedance at VCO IN	VCO IN = $1/2 V_{DD}$		10		M Ω
$I_{DD}(\text{INH})$ VCO supply current (inhibit)	See Note 4		0.01	1	μA
$I_{DD}(\text{VCO})$ VCO supply current	See Note 5		5.1	15	mA

NOTES: 4. The current into VCO V_{DD} and LOGIC V_{DD} when VCO INHIBIT = V_{DD} and PFD INHIBIT is high.

5. The current into VCO V_{DD} and LOGIC V_{DD} when VCO IN = $1/2 V_{DD}$, $R_{BIAS} = 2.4\text{ k}\Omega$, VCO INHIBIT = ground, and PFD INHIBIT is high.

PFD section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	$I_{OH} = -2\text{ mA}$	2.7			V
V_{OL} Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.2	V
I_{OZ} High-impedance-state output current	PFD INHIBIT = high, $V_I = V_{DD}$ or ground			± 1	μA
V_{IH} High-level input voltage at FIN-A, FIN-B		2.1			V
V_{IL} Low-level input voltage at FIN-A, FIN-B				0.9	V
V_{IT+} Positive input threshold voltage at PFD INHIBIT		0.9	1.5	2.1	V
C_i Input capacitance at FIN-A, FIN-B			5		pF
Z_i Input impedance at FIN-A, FIN-B			10		M Ω
$I_{DD}(Z)$ High-impedance-state PFD supply current	See Note 6		0.01	1	μA
$I_{DD}(\text{PFD})$ PFD supply current	See Note 7		0.7	4	mA

NOTES: 6. The current into LOGIC V_{DD} when FIN-A and FIN-B = ground, PFD INHIBIT = V_{DD} , PFD OUT open, and VCO OUT is inhibited.

7. The current into LOGIC V_{DD} when FIN-A and FIN-B = 30 MHz ($V_{I(PP)} = 3\text{ V}$, rectangular wave), PFD INHIBIT = GND, PFD OUT open, and VCO OUT is inhibited.



TLC2933

HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS136A – APRIL 1996 – REVISED JUNE 1997

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 3\text{ V}$
(unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Operating oscillation frequency	$R_{BIAS} = 2.4\text{ k}\Omega$, $VCO\ IN = 1/2\ V_{DD}$	38	48	55	MHz
$t_{s(fosc)}$	Time to stable oscillation (see Note 8)	Measured from $VCO\ INHIBIT\downarrow$			10	μs
t_r	Rise time, $VCO\ OUT\uparrow$	$C_L = 15\text{ pF}$, See Figure 3		3.3	10	ns
t_f	Fall time, $VCO\ OUT\downarrow$	$C_L = 15\text{ pF}$, See Figure 3		2	8	ns
	Duty cycle at $VCO\ OUT$	$R_{BIAS} = 2.4\text{ k}\Omega$, $VCO\ IN = 1/2\ V_{DD}$	45%	50%	55%	
$\alpha_{(fosc)}$	Temperature coefficient of oscillation frequency	$R_{BIAS} = 2.4\text{ k}\Omega$, $VCO\ IN = 1/2\ V_{DD}$, $T_A = -20^\circ\text{C}$ to 75°C		0.03		$\%/^\circ\text{C}$
$k_{SVS(fosc)}$	Supply voltage coefficient of oscillation frequency	$R_{BIAS} = 2.4\text{ k}\Omega$, $VCO\ IN = 1.5\text{ V}$, $V_{DD} = 2.85\text{ V}$ to 3.15 V		0.04		$\%/mV$
	Jitter absolute (see Note 9)	$R_{BIAS} = 2.4\text{ k}\Omega$		100		ps

NOTES: 8. The time period to stabilize the VCO oscillation frequency after the $VCO\ INHIBIT$ terminal is changed to a low level.

9. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully designed printed circuit board (PCB) with no device socket.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency		30			MHz
t_{PLZ}	Disable time, $PFD\ INHIBIT\uparrow$ to $PFD\ OUT\ Hi-Z$	See Figures 4 and 5 and Table 3		20	40	ns
t_{PHZ}	Disable time, $PFD\ INHIBIT\uparrow$ to $PFD\ OUT\ Hi-Z$			18	40	
t_{PZL}	Enable time, $PFD\ INHIBIT\downarrow$ to $PFD\ OUT\ low$			4.1	18	ns
t_{PZH}	Enable time, $PFD\ INHIBIT\downarrow$ to $PFD\ OUT\ high$			4.8	18	
t_r	Rise time, $PFD\ OUT\uparrow$	$C_L = 15\text{ pF}$, See Figure 4		3.1	9	ns
t_f	Fall time, $PFD\ OUT\downarrow$			1.5	9	ns



TLC2933

HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS136A – APRIL 1996 – REVISED JUNE 1997

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2\text{ mA}$	4.5			V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.5	V
V_{IT+}	Positive input threshold voltage at TEST, VCO INHIBIT		1.5	2.5	3.5	V
I_I	Input current at TEST, VCO INHIBIT	$V_I = V_{DD}$ or ground			± 1	μA
$Z_i(\text{VCO IN})$	Input impedance at VCO IN	VCO IN = $1/2 V_{DD}$		10		$\text{M}\Omega$
$I_{DD}(\text{INH})$	VCO supply current (inhibit)	See Note 4		0.01	1	μA
$I_{DD}(\text{VCO})$	VCO supply current	See Note 5		14	35	mA

NOTES: 4. The current into VCO V_{DD} and LOGIC V_{DD} when VCO INHIBIT = V_{DD} , and PFD INHIBIT high.

5. The current into VCO V_{DD} and LOGIC V_{DD} when VCO IN = $1/2 V_{DD}$, $R_{BIAS} = 2.4\text{ k}\Omega$, VCO INHIBIT = ground, and PFD INHIBIT high.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = 2\text{ mA}$	4.5			V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.2	V
I_{OZ}	High-impedance-state output current	PFD INHIBIT = high, $V_I = V_{DD}$ or ground			± 1	μA
V_{IH}	High-level input voltage at FIN-A, FIN-B		3.5			V
V_{IL}	Low-level input voltage at FIN-A, FIN-B				1.5	V
V_{IT+}	Positive input threshold voltage at PFD INHIBIT		1.5	2.5	3.5	V
C_i	Input capacitance at FIN-A, FIN-B			7		pF
Z_i	Input impedance at FIN-A, FIN-B			10		$\text{M}\Omega$
$I_{DD}(Z)$	High-impedance-state PFD supply current	See Note 6		0.01	1	μA
$I_{DD}(\text{PFD})$	PFD supply current	See Note 10		2.6	8	mA

NOTES: 6. The current into LOGIC V_{DD} when FIN-A and FIN-B = ground, PFD INHIBIT = V_{DD} , PFD OUT open, and VCO OUT is inhibited.

10. The current into LOGIC V_{DD} when FIN-A and FIN-B = 50 MHz ($V_{I(pp)} = 3\text{ V}$, rectangular wave), PFD INHIBIT = ground, PFD OUT open, and VCO OUT is inhibited.



TLC2933

HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS136A – APRIL 1996 – REVISED JUNE 1997

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Operating oscillation frequency	$R_{BIAS} = 2.4\text{ k}\Omega$, $V_{CO\ IN} = 1/2\ V_{DD}$	64	80	96	MHz
$t_{s(fosc)}$	Time to stable oscillation (see Note 8)	Measured from VCO INHIBIT↓			10	μs
t_r	Rise time, VCO OUT↑	$C_L = 15\text{ pF}$, See Figure 3		2.1	5	ns
t_f	Fall time, VCO OUT↓	$C_L = 15\text{ pF}$, See Figure 3		1.5	4	ns
	Duty cycle at VCO OUT	$R_{BIAS} = 2.4\text{ k}\Omega$, $V_{CO\ IN} = 1/2\ V_{DD}$	45%	50%	55%	
$\alpha_{(fosc)}$	Temperature coefficient of oscillation frequency	$R_{BIAS} = 2.4\text{ k}\Omega$, $V_{CO\ IN} = 1/2\ V_{DD}$, $T_A = -20^\circ\text{C}$ to 75°C		0.03		$\%/^\circ\text{C}$
$k_{SVS(fosc)}$	Supply voltage coefficient of oscillation frequency	$R_{BIAS} = 2.4\text{ k}\Omega$, $V_{CO\ IN} = 2.5\text{ V}$, $V_{DD} = 4.75\text{ V}$ to 5.25 V		0.02		$\%/mV$
	Jitter absolute (see Note 9)	$R_{BIAS} = 2.4\text{ k}\Omega$		100		ps

NOTES: 8: The time period to stabilize the VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.

9: Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully designed printed circuit board (PCB) with no device socket.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency		50			MHz
t_{pLZ}	Disable time, PFD INHIBIT↑ to PFD OUT Hi-Z	See Figures 4 and 5 and Table 3		20	40	ns
t_{pHZ}	Disable time, PFD INHIBIT↑ to PFD OUT Hi-Z			17	40	
t_{pZL}	Enable time, PFD INHIBIT↓ to PFD OUT low			3.7	10	ns
t_{pZH}	Enable time, PFD INHIBIT↓ to PFD OUT high			3.4	10	
t_r	Rise time, PFD OUT↑	$C_L = 15\text{ pF}$, See Figure 4		1.7	5	ns
t_f	Fall time, PFD OUT↓			1.3	5	ns



PARAMETER MEASUREMENT INFORMATION

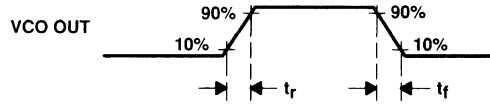
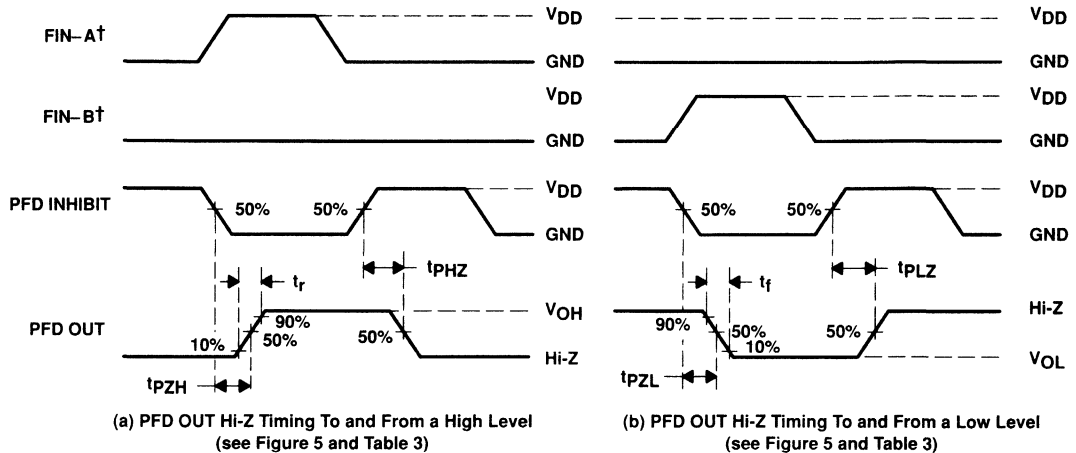


Figure 3. VCO Output Voltage Waveform



† FIN-A and FIN-B are for reference phase only, not for timing.

Figure 4. PFD Output Voltage Waveform

Table 3. PFD Output Test Conditions

PARAMETER	RL	CL	S1	S2
tpZH	1 kΩ	15 pF	Open	Closed
tpHZ				
tr			Closed	Open
tpZL				
tpLZ				
tf				

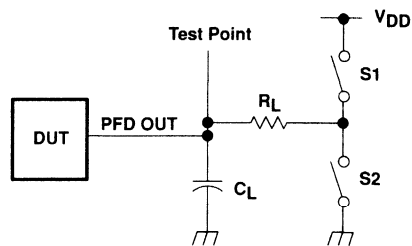


Figure 5. PFD Output Test Conditions

TLC2933 HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS136A – APRIL 1996 – REVISED JUNE 1997

TYPICAL CHARACTERISTICS

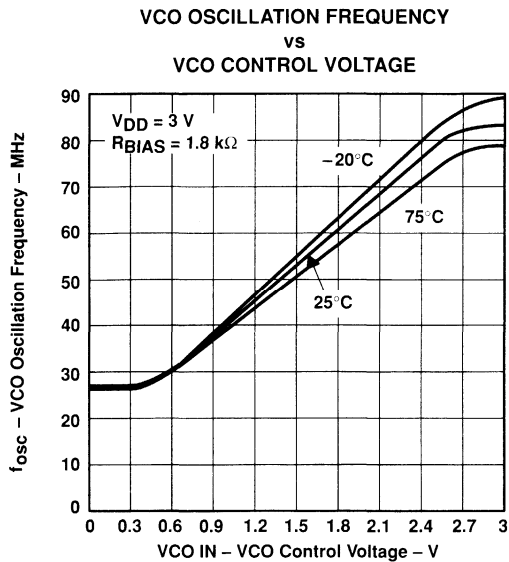


Figure 6

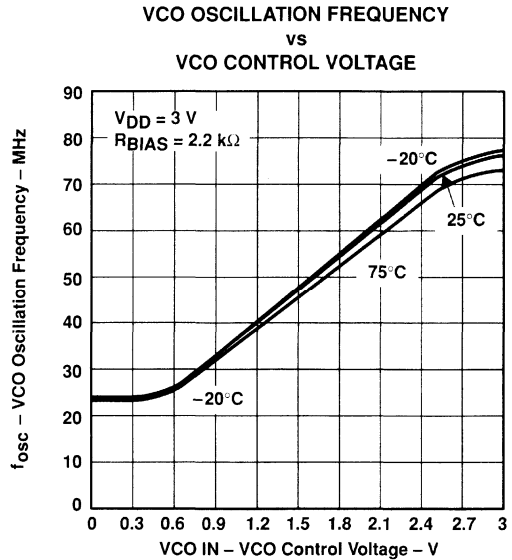


Figure 7

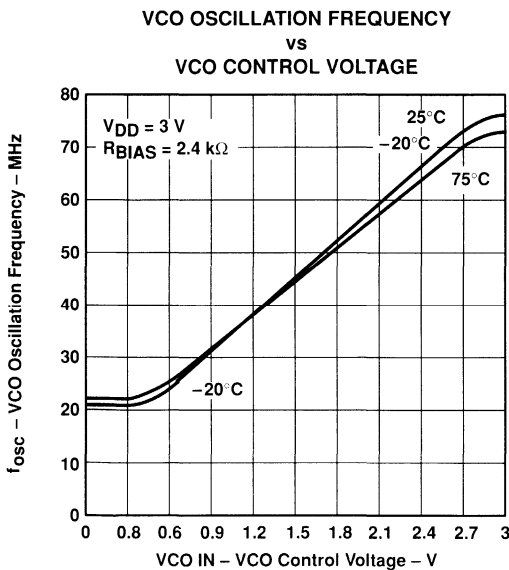


Figure 8

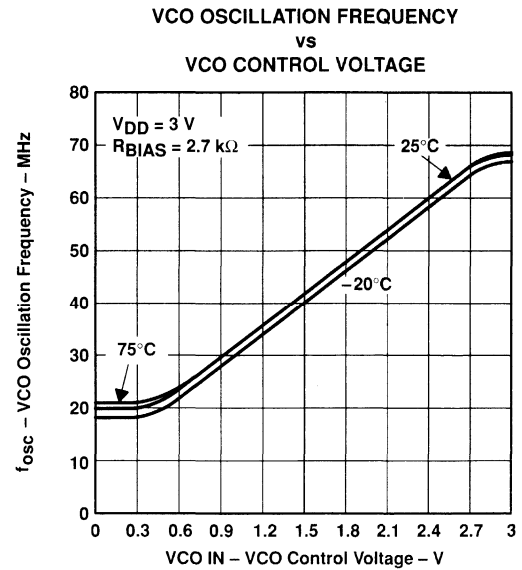


Figure 9



TYPICAL CHARACTERISTICS

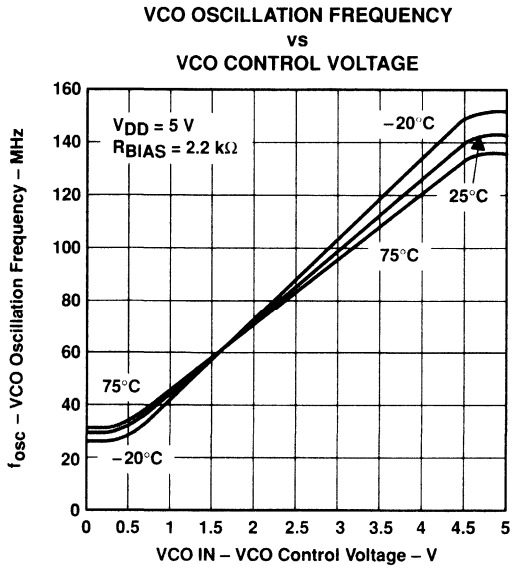


Figure 10

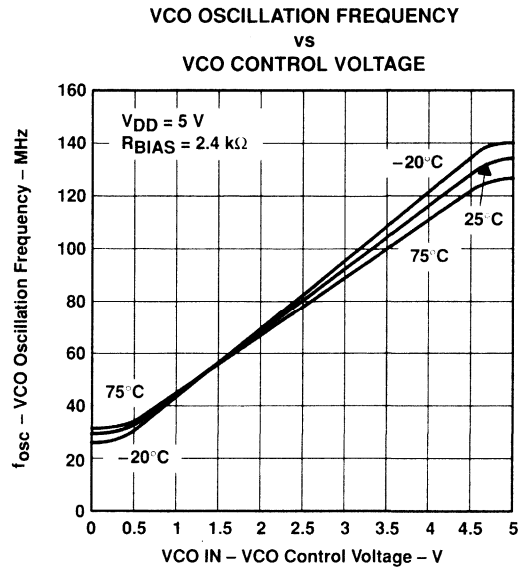


Figure 11

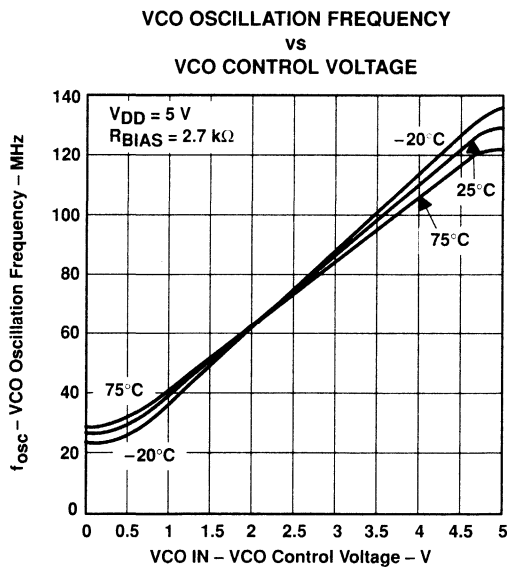


Figure 12

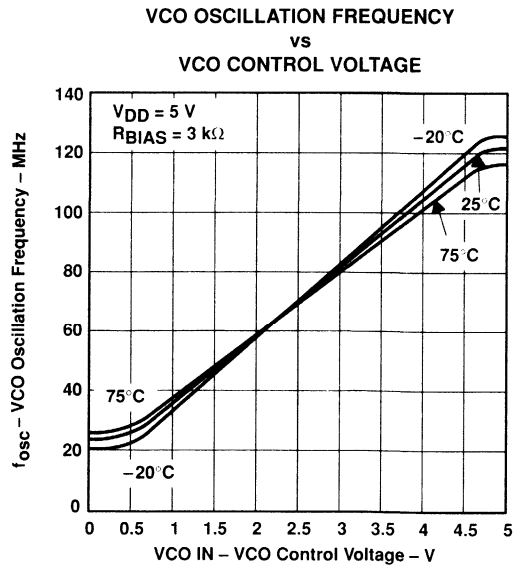


Figure 13

TLC2933 HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS136A – APRIL 1996 – REVISED JUNE 1997

TYPICAL CHARACTERISTICS

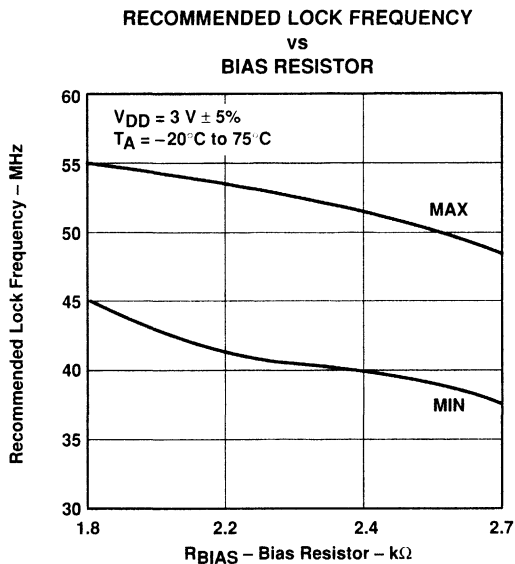


Figure 14

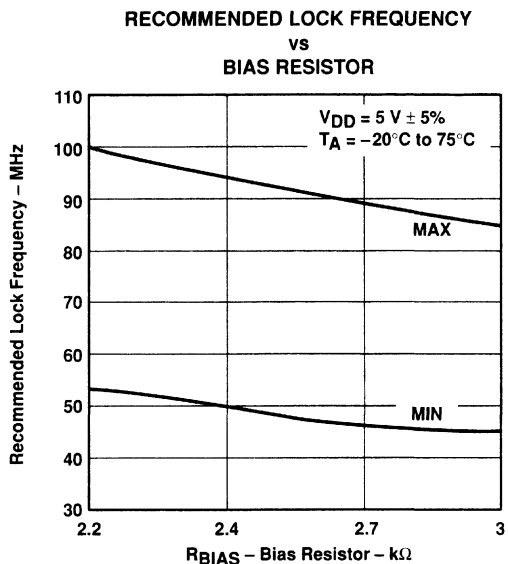


Figure 15

APPLICATION INFORMATION

gain of VCO and PFD

Figure 16 is a block diagram of the PLL. The divider N value depends on the input frequency and the desired VCO output frequency according to the system application requirements. The K_p and K_V values are obtained from the operating characteristics of the device as shown in Figure 16. K_p is defined from the phase detector V_{OL} and V_{OH} specifications and the equation shown in Figure 16(b). K_V is defined from Figures 8, 9, 10, and 11 as shown in Figure 16(c).

The parameters for the block diagram with the units are as follows:

- K_V : VCO gain (rad/s/V)
- K_p : PFD gain (V/rad)
- K_f : LPF gain (V/V)
- K_N : countdown divider gain (1/N)

external counter

When a large N counter is required by the application, there is a possibility that the PLL response becomes slow due to the counter response delay time. In the case of a high frequency application, the counter delay time should be accounted for in the overall PLL design.

R_{BIAS}

The external bias resistor sets the VCO center frequency with $1/2 V_{DD}$ applied to the VCO IN terminal. For the most accurate results, a metal-film resistor is the better choice but a carbon-composition resistor can also be used with excellent results. A 0.22 μ F capacitor should be connected from the BIAS terminal to ground as close to the device terminals as possible.

hold-in range

From the technical literature, the maximum hold-in range for an input frequency step for the three types of filter configurations shown in Figure 17 is as follows:

$$\Delta\omega_H = 0.8 (K_p) (K_V) (K_f (\infty)) \tag{1}$$

Where

$K_f (\infty)$ = the filter transfer function value at $\omega = \infty$

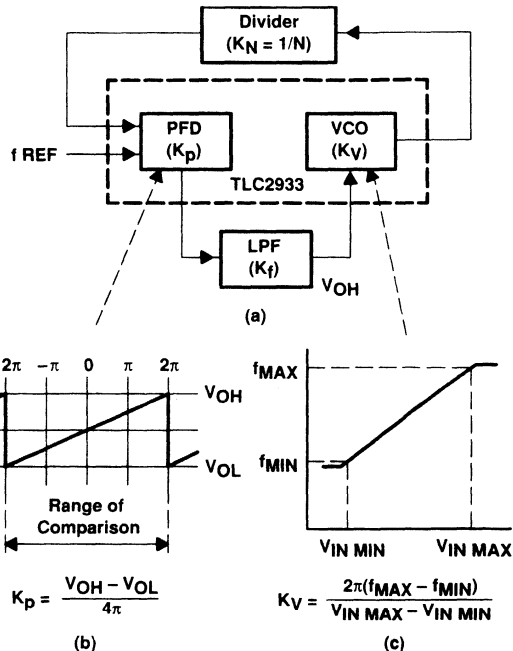


Figure 16. Example of a PLL Block Diagram

TLC2933 HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS136A – APRIL 1996 – REVISED JUNE 1997

APPLICATION INFORMATION

low-pass-filter (LPF) configurations

Many excellent references are available that include detailed design information about LPFs and should be consulted for additional information. Lag-lead filters or active filters are often used. Examples of LPFs are shown in Figure 17. When the active filter of Figure 17(c) is used, the reference should be applied to FIN-B because of the amplifier inversion. Also, in practical filter implementations, C2 is used as additional filtering at the VCO input. The value of C2 should be equal to or less than one tenth the value of C1.

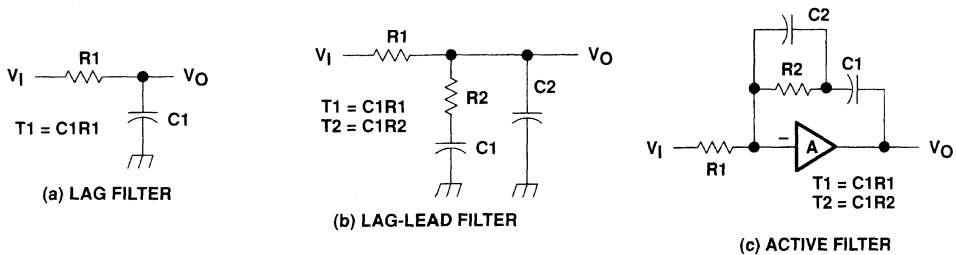


Figure 17. LPF Examples for PLL

the passive filter

The transfer function for the low-pass filter shown in Figure 17(b) is;

$$\frac{V_O}{V_{IN}} = \frac{1 + s \cdot T_2}{1 + s \cdot (T_1 + T_2)} \quad (2)$$

where

$$T_1 = R_1 \cdot C_1 \text{ and } T_2 = R_2 \cdot C_1$$

Using this filter makes the closed-loop PLL system a type 1 second-order system. The response curves of this system to a unit step are shown in Figure 18.

the active filter

When using the active filter shown in Figure 17(c), the phase detector inputs must be reversed since the filter adds an additional inversion. Therefore, the input reference frequency should be applied to the FIN-B terminal and the output of the VCO divider should be applied to the input reference terminal, FIN-A.

The transfer function for the active filter shown in Figure 17(c) is:

$$F(s) = \frac{1 + s \cdot R_2 \cdot C_1}{s \cdot R_1 \cdot C_1} \quad (3)$$

Using this filter makes the closed-loop PLL system a type 2 second-order system. The response curves of this system to a unit step are shown in Figure 19.

APPLICATION INFORMATION

Using the lag-lead filter in Figure 17(b) and divider N value, the transfer function for phase and frequency are shown in equations 4 and 5. Note that the transfer function for phase differs from the transfer function for frequency by only the divider N value. The difference arises from the fact that the feedback for phase is unity while the feedback for frequency is 1/N.

Hence, the transfer function of Figure 17(a) for phase is

$$\frac{\Phi_2(s)}{\Phi_1(s)} = \frac{K_p \cdot K_V}{N \cdot (T_1 + T_2)} \left[\frac{1 + s \cdot T_2}{s^2 + s \left[1 + \frac{K_p \cdot K_V \cdot T_2}{N \cdot (T_1 + T_2)} \right] + \frac{K_p \cdot K_V}{N \cdot (T_1 + T_2)}} \right] \quad (4)$$

and the transfer function for frequency is

$$\frac{F_{OUT}(s)}{F_{REF}(s)} = \frac{K_p \cdot K_V}{(T_1 + T_2)} \left[\frac{1 + s \cdot T_2}{s^2 + s \cdot \left[1 + \frac{K_p \cdot K_V \cdot T_2}{N \cdot (T_1 + T_2)} \right] + \frac{K_p \cdot K_V}{N \cdot (T_1 + T_2)}} \right] \quad (5)$$

The standard 2-pole denominator is $D = s^2 + 2 \zeta \omega_n s + \omega_n^2$ and comparing the coefficients of the denominator of equation (4) and (5) with the standard 2-pole denominator gives the following results.

$$\omega_n = \sqrt{\frac{K_p \cdot K_V}{N \cdot (T_1 + T_2)}} \quad (6)$$

Solving for $T_1 + T_2$

$$T_1 + T_2 = \frac{K_p \cdot K_V}{N \cdot \omega_n^2}$$

and by using this value for $T_1 + T_2$ in equation (6) the damping factor is

$$\zeta = \frac{\omega_n}{2} \cdot \left(T_2 + \frac{N}{K_p \cdot K_V} \right) \quad (7)$$

solving for T_2

$$T_2 = \frac{2 \zeta}{\omega_n} - \frac{N}{K_p \cdot K_V} \quad (8)$$

then by substituting for T_2 in equation (6)

$$T_1 = \frac{K_V \cdot K_p}{N \cdot \omega_n^2} - \frac{2 \zeta}{\omega_n} + \frac{N}{K_p \cdot K_V} \quad (9)$$

TLC2933 HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS136A – APRIL 1996 – REVISED JUNE 1997

APPLICATION INFORMATION

From the circuit constants and the initial design parameters then

$$R2 = \left[\frac{2 \zeta}{\omega_n} - \frac{N}{K_p \cdot K_V} \right] \frac{1}{C1} \quad (10)$$

$$R1 = \left[\frac{K_p \cdot K_V}{\omega_n^2 \cdot N} - \frac{2 \zeta}{\omega_n} + \frac{N}{K_p \cdot K_V} \right] \frac{1}{C1} \quad (11)$$

The capacitor, C1, is usually chosen between 1 μ F and 0.1 μ F to allow for reasonable resistor values and physical capacitor size.

APPLICATION INFORMATION

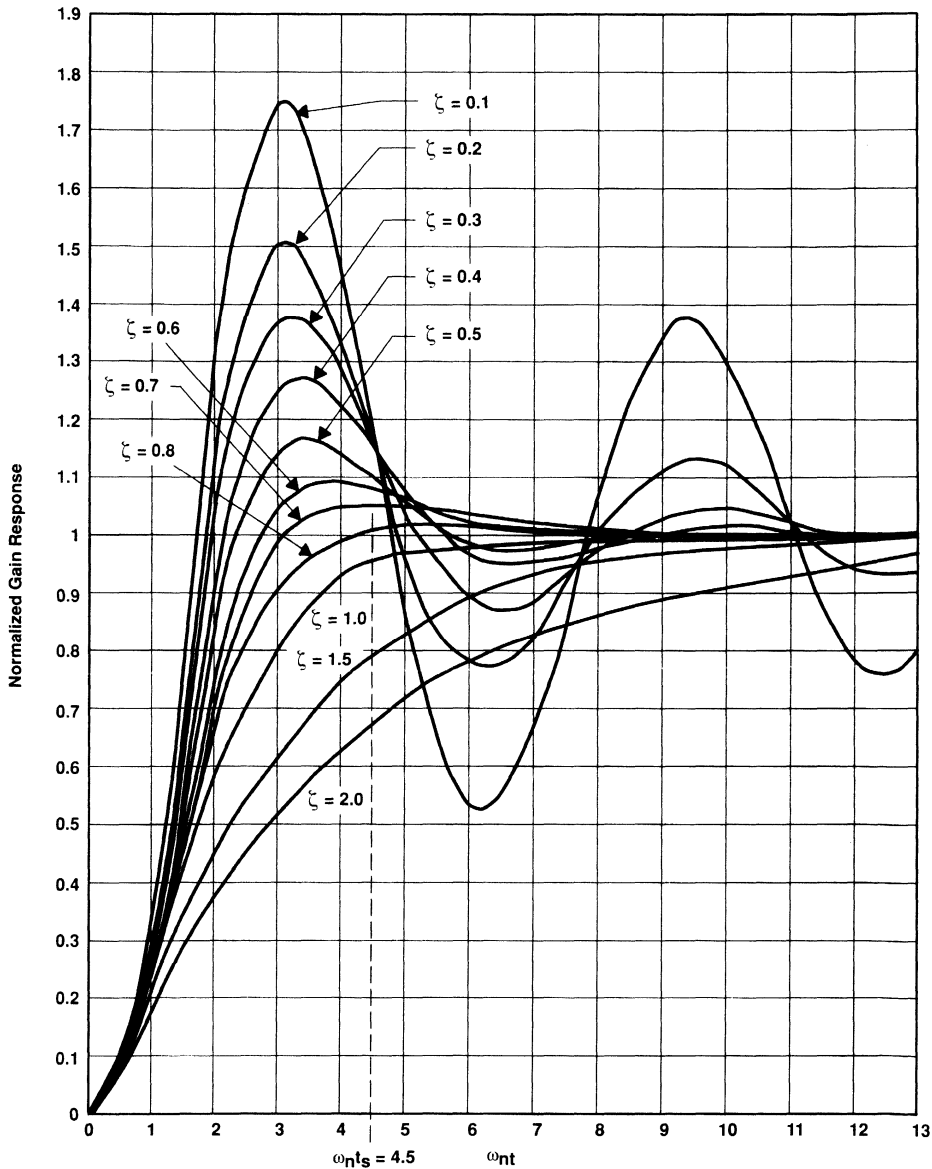


Figure 18. Type 1 Second-Order Step Response

TLC2933 HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS136A – APRIL 1996 – REVISED JUNE 1997

APPLICATION INFORMATION

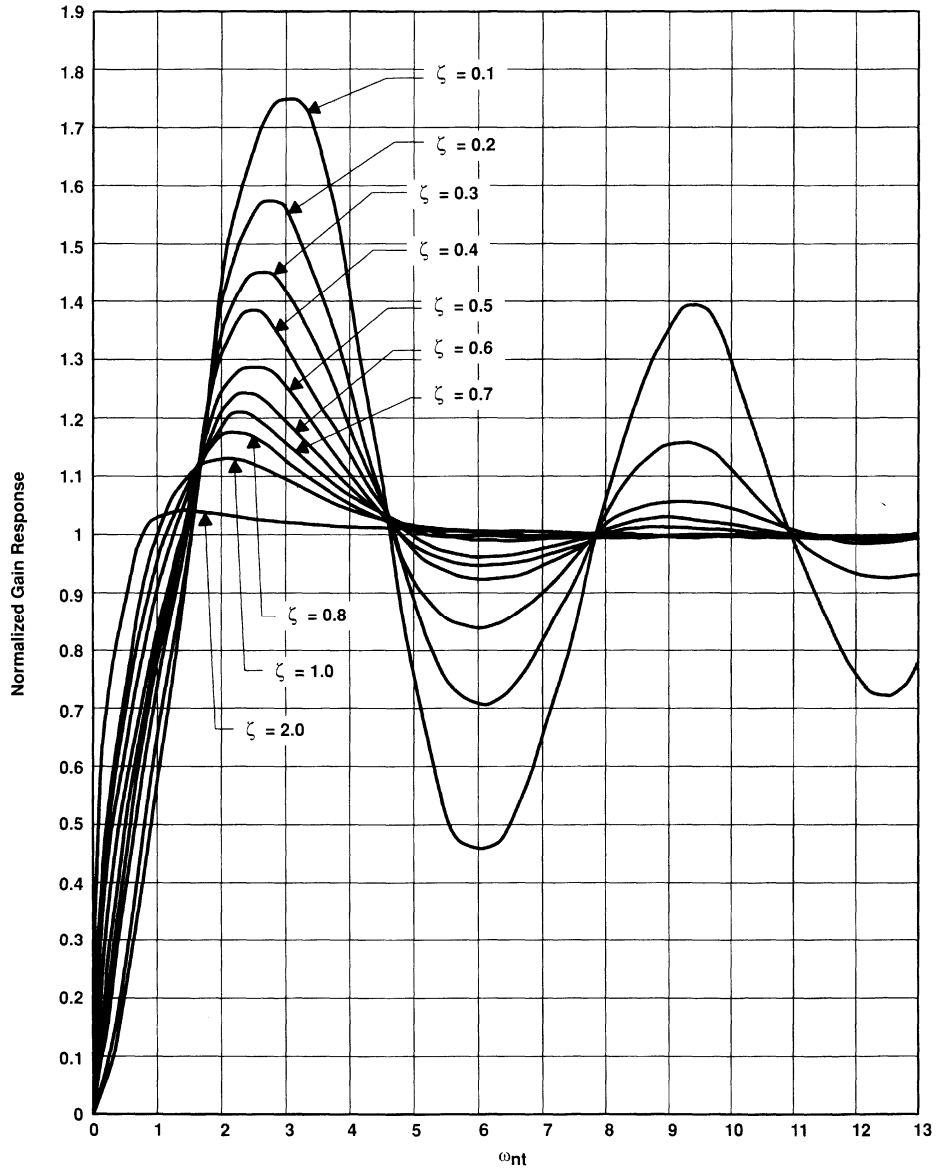
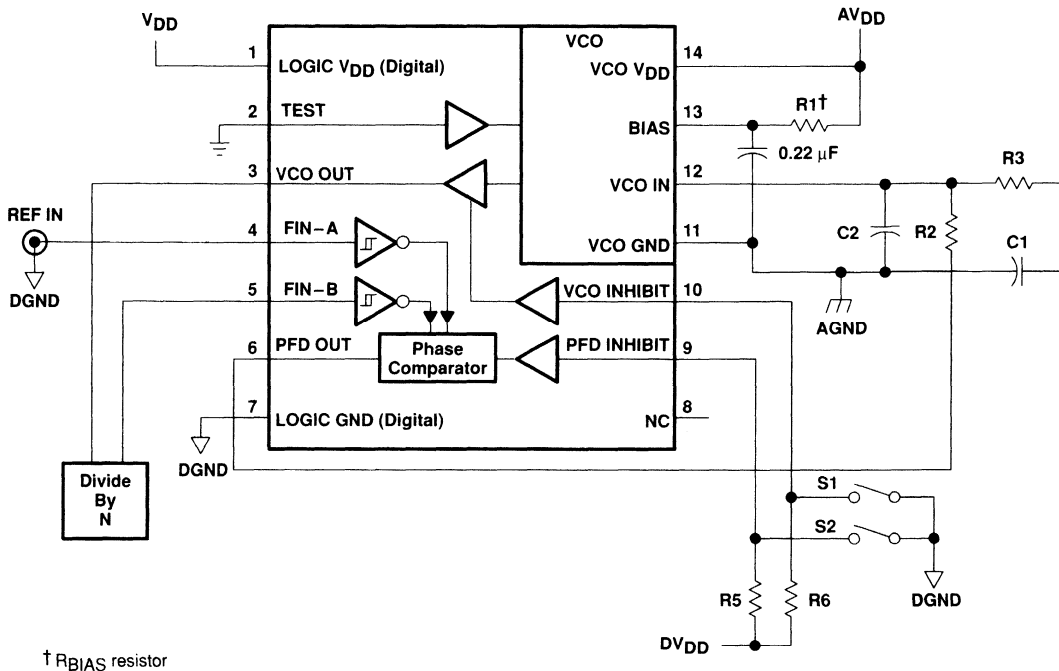


Figure 19. Type 2 Second-Order Step Response

TLC2933 HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS136A – APRIL 1996 – REVISED JUNE 1997

APPLICATION INFORMATION



† R_{BIAS} resistor

Figure 20. Evaluation and Operation Schematic

PCB layout considerations

The TLC2933 contains a high frequency oscillator; therefore, very careful breadboarding and PCB layout is required for evaluation.

The following design recommendations benefit the TLC2933 user:

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- Radio frequency (RF) breadboarding or RF PCB techniques should be used throughout the evaluation and production process.
- Wide ground leads or a ground plane should be used on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.
- LOGIC V_{DD} and VCO V_{DD} should be separate PCB traces and connected to the best filtered supply point available in the system to minimize supply cross-coupling.
- VCO V_{DD} to ground and LOGIC V_{DD} to ground should be decoupled with a 0.1-μF capacitor placed as close as possible to the appropriate device terminals.
- The no-connection (NC) terminal on the package should be connected to ground to prevent stray pickup.

TL32088 DIFFERENTIAL ANALOG BUFFER AMPLIFIER FOR THE TLC320AD58

SLAS123B – MARCH 1995 – REVISED NOVEMBER 1995

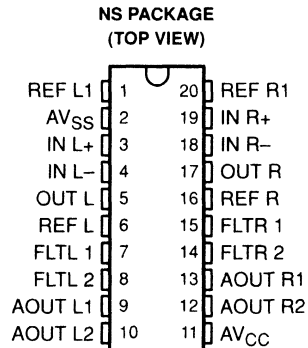
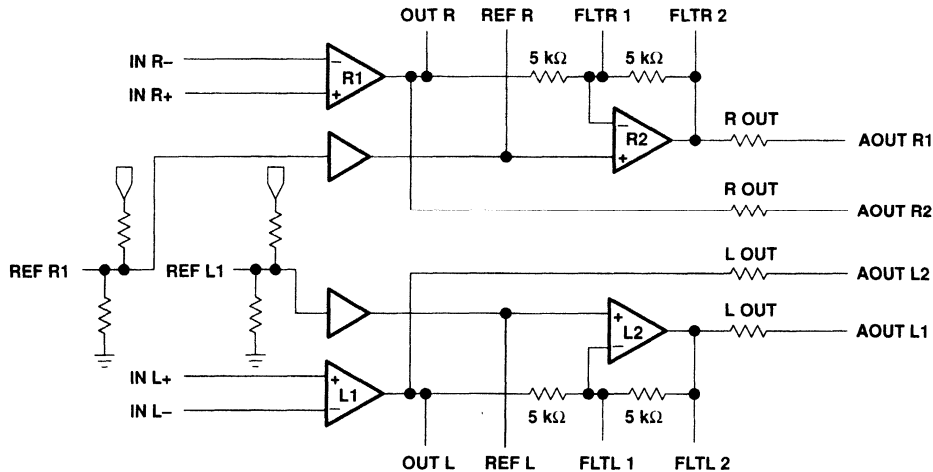
- **Analog Front-End Integrated Circuit for the 18-Bit Stereo Audio Sigma-Delta Analog-to-Digital Converter TLC320AD58C**
- **Low Distortion, Low Noise**
 - THD+N . . . 0.00056% Typ
 - SNR . . . 108-dB Typ
- **Adjustable Signal Gain**
- **5-V Single Supply Operation**
- **Internal Voltage Reference**
- **Operating Temperature . . . 0°C to 70°C**

description

The TL32088 is an analog signal conditioning integrated circuit built using a proprietary Texas Instruments bipolar process. This device is used for the analog signal input stage for the 18-bit, stereo audio, sigma-delta, analog-to-digital converter (ADC) TLC320AD58C exclusively. The TL32088 can convert input signals from single-ended to differential and differential to single-ended. The TL32088 also implements a single-ended to single-ended and differential to differential amplifier buffer. The differential output can be connected to the TLC320AD58C directly. The TLC32088 is composed of high performance amplifiers that offer wide output swing with low distortion and low noise. The reference voltage for the internal amplifier circuit is provided from an internal voltage reference circuit.

The TL32088 provides a wide output swing while maintaining 0.00056% THD+N and 108-dB SNR and, therefore, is ideally suited for high-end audio systems.

functional block diagram



AVAILABLE OPTIONS	
T _A	PACKAGE
	SMALL OUTLINE (NS)
0°C to 70°C	TL32088CNS

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



TL32088

DIFFERENTIAL ANALOG BUFFER AMPLIFIER

FOR THE TLC320AD58

SLAS123B – MARCH 1995 – REVISED NOVEMBER 1995

absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage, AV_{CC} (see Note 1)	7 V
Differential input voltage, V_{ID} (see Note 2)	AV_{CC}
Input voltage range, V_I (any input) (see Notes 1 and 3)	-0.3 to AV_{CC}
Output voltage, V_O	-0.3 to AV_{CC}
Output current, I_O	20 mA
Duration of short-circuit current at or below 25°C (output shorted to GND)	unlimited
Continuous total power dissipation, P_D ($T_A \leq 25^\circ\text{C}$) (see Note 4)	625 mW
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltage, are with respect to GND.
 2. Differential voltage is at the noninverting input with respect to the inverting input.
 3. All input voltage values must not exceed V_{CC} .
 4. Derating factor above $T_A = 25^\circ\text{C}$ is 10 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, AV_{CC}	4.75	5	5.25	V
Input voltage range, V_I (see Note 5)	1.1		3.9	V
Operating free-air temperature, T_A	0		70	°C

NOTE 5: The output voltage is undetermined when the input voltage exceeds recommended input voltage range.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 2.5\text{ V}$, $V_O = 2.5\text{ V}$ (AMP L1, R1)	$T_A = 25^\circ\text{C}$		1	6	mV
			$T_A = 0^\circ\text{C}$ to 70°C			7.5	
I_{IO}	Input offset current	$V_{IC} = 2.5\text{ V}$, $V_O = 2.5\text{ V}$ (AMP L1, R1)	$T_A = 25^\circ\text{C}$		5	100	nA
			$T_A = 0^\circ\text{C}$ to 70°C			150	
I_{IB}	Input bias current	$V_{IC} = 2.5\text{ V}$, $V_O = 2.5\text{ V}$ (AMP L1, R1)	$T_A = 25^\circ\text{C}$		20	150	nA
			$T_A = 0^\circ\text{C}$ to 70°C			250	
V_{IC}	Common-mode input voltage	$V_O \leq 7.5\text{ mV}$ (AMP L1, R1)	$T_A = 25^\circ\text{C}$		0.9	4.1	V
			$T_A = 0^\circ\text{C}$ to 70°C		1.1	3.9	
V_{OM+}	Maximum positive-peak output voltage			4.4			V
V_{OM-}	Maximum negative-peak output voltage					0.6	V
A_{vd}	Differential voltage amplification	$V_O = 2.5\text{ V} \pm 1\text{ V}$ (AMP L1, R1)	$T_A = 25^\circ\text{C}$		60		dB
CMRR	Common-mode rejection ratio	$V_O = 2.5\text{ V} \pm 1\text{ V}$ (AMP L1, R1)	$T_A = 25^\circ\text{C}$		85		dB
V_{ref}	Reference voltage			2.4	2.5	2.6	V
E_G	Gain error	See Note 6				$\pm 3\%$	
r_o	Output resistance		$T_A = 25^\circ\text{C}$		50		Ω
I_{CC}	Supply current (both channels)	$V_O = 2.5\text{ V}$, No load	$T_A = 25^\circ\text{C}$		17	20	mA
			$T_A = 0^\circ\text{C}$ to 70°C			25	

NOTE 6: Gain error is between OUT L and FLTL 1, OUT R and FLTR 1.



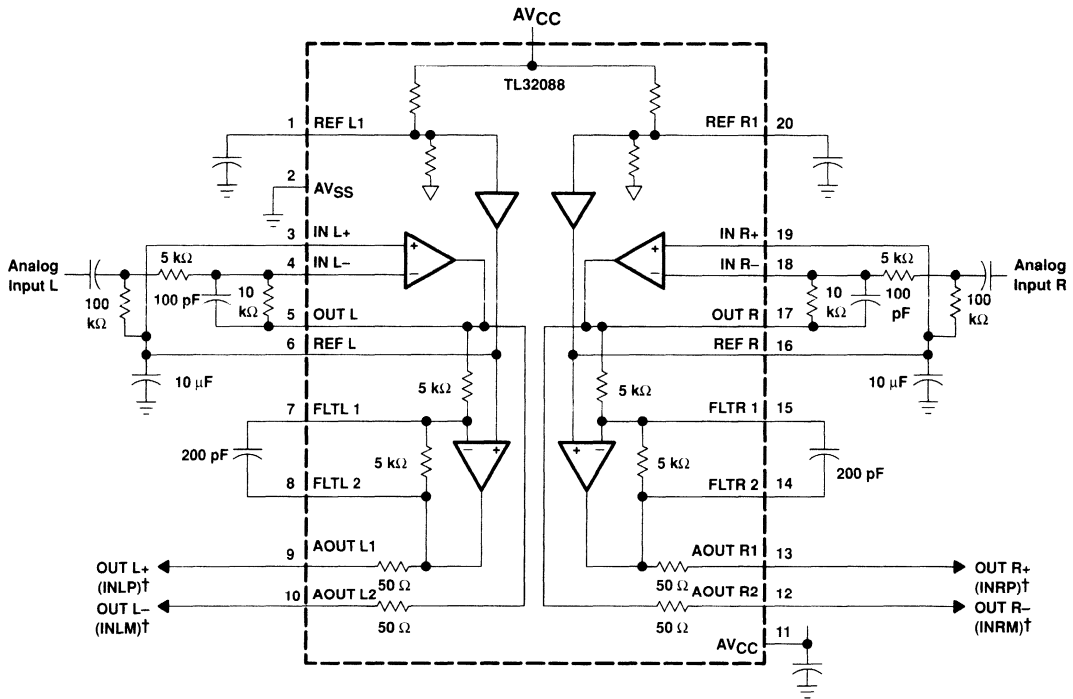
TL32088 DIFFERENTIAL ANALOG BUFFER AMPLIFIER FOR THE TLC320AD58

SLAS123B – MARCH 1995 – REVISED NOVEMBER 1995

operating characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate	$A_V = 1$, $V_I = 2.5\text{ V} + 0.5\text{ V (AMP L1, R1)}$		3		$\text{V}/\mu\text{s}$
B_1	Unity-gain bandwidth	AMP L1, R1		7		MHz
SNR	Signal-to-noise ratio (EIAJ)	A-Weighted test circuit (see Figure 2)	104	108		dB
THD+N	Total harmonic distortion plus noise	$V_{O(PP)} = 3.2\text{ V}$ $f = 1\text{ kHz}$, BW = 10 Hz to 20 kHz test circuit		0.00056%	0.001%	
	Crosstalk	$V_{O(PP)} = 3.2\text{ V}$, $f = 20\text{ kHz}$		-125		dB

APPLICATION INFORMATION



† TLC320AD58C input terminals.

Figure 1. TL32088 to TLC320AD58C Connections

TL32088
DIFFERENTIAL ANALOG BUFFER AMPLIFIER
FOR THE TLC320AD58

SLAS123B – MARCH 1995 – REVISED NOVEMBER 1995

APPLICATION INFORMATION

Table 1. A-Weighted Data

FREQUENCY	A WEIGHTING (dB)	FREQUENCY	A WEIGHTING (dB)
25	-44.6 ± 2	800	-0.1 ± 1
31.5	-39.2 ± 2	1000	0 ± 0
40	-34.5 ± 2	1250	0.6 ± 1
50	-30.2 ± 2	1600	1.0 ± 1
63	-26.1 ± 2	2000	1.2 ± 1
80	-22.3 ± 2	2500	1.2 ± 1
100	-19.1 ± 1	3150	1.2 ± 1
125	-16.1 ± 1	4000	1.0 ± 1
160	-13.2 ± 1	5000	0.5 ± 1
200	-10.8 ± 1	6300	-0.1 ± 1
250	-8.6 ± 1	8000	-1.1 ± 1
315	-6.5 ± 1	10000	-2.4 ± 1
400	-4.8 ± 1	12500	-4.2 ± 2
500	-3.2 ± 1	16000	-6.5 ± 2
630	-1.9 ± 1	—	—

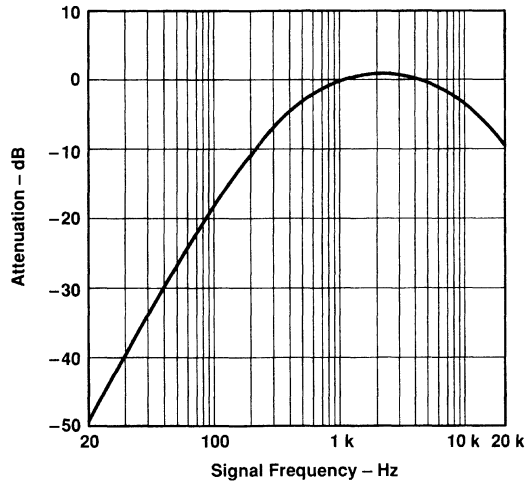


Figure 2. A-Weighted Function

General Information	1
General purpose ADCs	2
General Purpose DACs	3
DSP AICs and CODECs	4
Special Functions	5
Video Interface Palettes	6
Digital Imaging Sensor Products	7
Mechanical Information	8

Contents

	Page
TVP3026 :	6-3
TVP3030 :	6-7
TVP3033 :	6-11
TVP3409 :	6-13
TVP3703 :	6-15

9

Video Interface Palettes

- Supports System Resolutions up to 1600 × 1280 at 76-Hz Refresh Rate
- Supports Color Depths of 4-, 8-, 16-, 24-, and 32-Bit/Pixel
- Versatile Direct-Color Modes:
 - 24-Bit/Pixel with 8-Bit Overlay (O, R, G, B)
 - 24-Bit/Pixel (R, G, B)
 - 16-Bit/Pixel (5, 6, 5) XGA™ Configuration
 - 16-Bit/Pixel (6, 6, 4) Configuration
 - 15-Bit/Pixel With 1-Bit Overlay (1, 5, 5, 5) TARGA™ Configuration
 - 12-Bit/Pixel With 4-Bit Overlay (4, 4, 4, 4)
 - True-Color Gamma Correction
- Supports Packed Pixel Formats for 24-Bit/Pixel Using a 32- or 64-Bit/Pixel Bus
- 50% Duty Cycle Reference Clock for Higher Screen Refresh Rates in Packed-24 Modes
- Programmable Frequency Synthesis Phase-Locked Loops (PLL) for Dot Clock and Memory Clock
- Loop Clock PLL Compensates for System Delay and Ensures Reliable Data Latching
- Versatile Pixel Bus Interface Supports Little- and Big-Endian Data Formats
- 135-, 175-, 220-, 230-, 250-, and 270-MHz Versions
- On-Chip Hardware Cursor, 64 × 64 × 2 Cursor (XGA and X-Window™ Functionally Compatible)
- Direct Interfacing to Video RAM
- Supports Overscan For Creation of Custom Screen Borders
- Color-Keyed Switching of Direct Color and True Color or Overlay
- Hardware Port Select Switching Between Direct Color and True Color or Overlay
- Triple 8-Bit D/A Converters
- Analog-Output Comparators for Monitor Detection
- RS-343A-Compatible Outputs
- Direct VGA Pass-Through Capability
- Palette-Page Register
- Horizontal Zooming Capability
- Data Manual Available†

description

The TVP3026 is an advanced video interface palette (VIP) from Texas Instruments implemented in EPIC™ 0.8-micron CMOS process. The TVP3026 is a 64-bit VIP that supports packed-24 modes enabling 24-bit true color and high resolution at the same time without excessive amounts of frame buffer memory. For example, a 24-bit true color display with 1280 × 1024 resolution may be packed into 4 megabytes of VRAM. A PLL-generated, 50% duty cycle reference clock is output in the packed-24 modes, maximizing VRAM cycle time and screen refresh rate.

The TVP3026 supports all of the pixel formats of the TVP3020 VIP. Data can be split into 4- or 8-bit planes for pseudo-color mode or split into 12-, 16- or 24-bit true-color and direct-color modes. For the 24-bit direct color modes, an 8-bit overlay plane is available. The 16-bit direct- and true-color modes can be configured to IBM™ XGA (5, 6, 5), TARGA (1, 5, 5, 5), or (6, 6, 4) as another existing format. An additional 12-bit mode (4, 4, 4, 4) is supported with 4 bits for each color and overlay. All color modes support selection of little- or big-endian data format for the pixel bus. Additionally, the device is also software compatible with the IM5G176/8 and Bt476/8 color palettes.

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).

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EPIC is a trademark of Texas Instruments Incorporated.

XGA is a trademark of IBM.

TARGA is a trademark of Truevision Incorporated.

X-Windows is a trademark of Massachusetts Institute of Technology.

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TVP3026

VIDEO INTERFACE PALETTE

XLAS098B – MAY 1995 – REVISED NOVEMBER 1997

description (continued)

Two fully programmable PLLs for pixel clock and memory clock functions are provided, as well as a simple frequency doubler for dramatic improvements in graphics system cost and integration. A third loop clock PLL is incorporated, making pixel data latch timing much simpler than with other existing color palettes. In addition, four digital clock inputs (two TTL- and two ECL/TTL-compatible) can be used and are software selectable. The video clock provides a software-selected divide ratio of the chosen pixel clock. The shift clock output can be used directly as the VRAM shift clock. The reference clock output is driven by the loop clock PLL and provides a timing reference to the graphics accelerator.

Like the TVP3020, the TVP3026 also integrates a complete, IBM XGA-compatible hardware cursor on chip, making significant graphics performance enhancements possible. Additionally, hardware port select and color-keyed switching functions allow the user several options for producing graphical overlays on direct-color backgrounds.

The TVP3026 has three 256-by-8 color lookup tables with triple, 8-bit video, digital-to-analog converters (DACs) capable of directly driving a doubly terminated, 75-Ω line. The lookup tables are designed with a dual-port RAM architecture that enables ultra-high speed operation. Sync generation is incorporated on the green output channel. Horizontal sync (HSYNC) and vertical sync (VSYNC) are pipeline delayed through the device and optionally inverted to indicate screen resolution to the monitor. A palette-page register is available to select from multiple color maps in RAM when 4 bit planes are used. This allows the screen colors to be changed with only one microprocessor write cycle.

The device features a separate VGA bus that supports the integrated VGA modes in graphics accelerator applications, allowing efficient support for VGA graphics and text modes. The separate bus also is useful for accepting data from the feature connector of most VGA-supported personal computers, without the need for external data multiplexing.

The TVP3026 is highly system integrated. It can be connected to the serial port of VRAM devices without external buffer logic and connected to many graphics engines directly. It also supports the split shift-register transfer function, which is common to many industry standard VRAM devices.

The system-integration concept is even carried further to manufacturing test and field diagnosis. To support these, several highly integrated test functions have been designed to enable simplified testing of the palette and the entire graphics system.

AVAILABLE OPTIONS

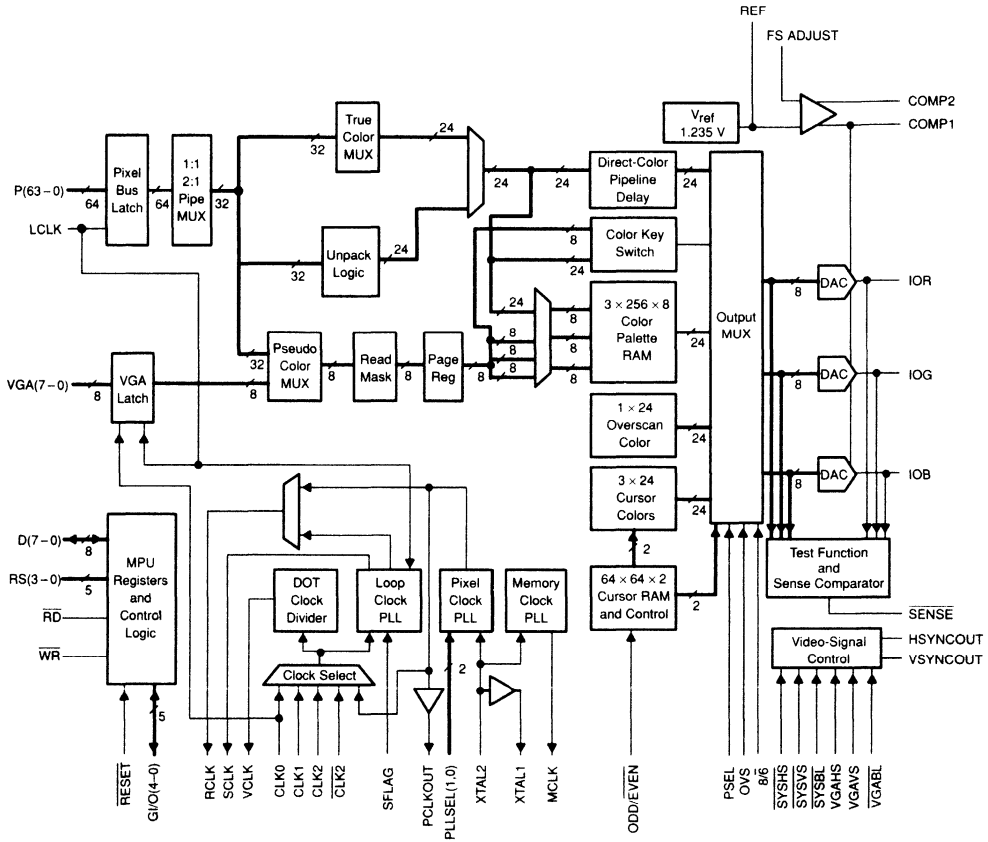
T _A	SPEED	DAC RESOLUTION	PACKAGE		
			CERAMIC FLAT PACK (HFG)	METAL QUAD FLAT PACK (MDN)	PLASTIC QUAD FLAT PACK (PCE)
0°C to 70°C	135 MHz	8 Bits	—	—	TVP3026–135PCE
	175 MHz	8 Bits	—	—	TVP3026–175PCE
	220 MHz	8 Bits	—	—	TVP3026–220PCE
	230 MHz	8 Bits	—	—	TVP3026–230PCE
	250 MHz	8 Bits	—	—	TVP3026–250PCE
	270 MHz	8 Bits	—	TVP3026–270MDN	—
–55°C to 125°C	175 MHz	8 Bits	TVP3026–175MHFG	—	—



TVP3026 VIDEO INTERFACE PALETTE

XLAS098B – MAY 1995 – REVISED NOVEMBER 1997

functional block diagram



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- Supports System Resolutions up to 1600 × 1280 at 86-Hz Refresh Rate
- Supports Color Depths of 4, 8, 16, 24, and 32 Bit/Pixel, All at Maximum Resolution
- 128-Bit-Wide Pixel Bus
- Versatile Direct-Color Modes:
 - 24-Bit/Pixel with 8-Bit Overlay (O, R, G, B)
 - 24-Bit/Pixel Packed-24 (R, G, B)
 - 16-Bit/Pixel (5, 6, 5) XGA Configuration
 - 16-Bit/Pixel (6, 6, 4) Configuration
 - 15-Bit/Pixel With 1-Bit Overlay (1, 5, 5, 5) TARGA Configuration
 - 12-Bit/Pixel With 4-Bit Overlay (4, 4, 4, 4)
- True-Color Gamma Correction
- Supports Packed Pixel Formats for 24 Bit/Pixel Using a 32-, 64-, or 128-Bit/Pixel Bus
- 50% Duty Cycle Reference Clock for Higher Screen Refresh Rates in Packed-24 Modes
- Programmable Frequency Synthesis PLLs for Dot Clock and Memory Clock
- Loop Clock PLL Compensates for System Delay and Ensures Reliable Data Latching
- Versatile Pixel Bus Interface Supports Little-Endian and Big-Endian Data Formats
- 175-, 220- and 250-MHz Versions
- On-Chip Hardware Cursor, 64 × 64 × 2 Cursor (XGA and X-Windows Functionally Compatible)
- Byte Router Allows Use of R, G, or B Direct-Color Channels Individually
- Direct Interfacing to Video RAM
- Overscan for Creation of Custom Screen Borders
- Color-Keyed Switching of Direct Color and True Color or Overlay
- Triple 8-Bit Digital-to-Analog (D/A) Converters
- Analog Output Comparators for Monitor Detection
- RS-343A Compatible Outputs
- Direct VGA Pass-Through Capability
- Palette-Page Register
- Horizontal Zooming Capability
- EPIC 0.8- μ m CMOS Process
- Data Manual Available†

description

The TVP3030 is an advanced video interface palette (VIP) from Texas Instruments implemented in EPIC™ 0.8-micron CMOS process. The TVP3030 is a 128-bit VIP that provides virtually all features of the 64-bit TVP3026. The TVP3030 doubles the pixel bus bandwidth, enabling 24-bit/pixel displays at resolutions up to 1600 × 1280 at a 76-Hz refresh rate. Also, 24-bit/pixel graphics at 1280 × 1024 resolution may be implemented at higher refresh rates with or without the use of pixel packing.

With the wider pixel bus comes additional 24-bit/pixel multiplexing modes: 4:1 (128-bit bus width for overlay and red-green-blue (RGB)) and 5:1 (120-bit bus width for RGB). The byte router function allows pseudo-color or monochrome image data to be taken from the red, green, or blue color channels. This enables high performance 24-bit/pixel architectures organized as red, green, and blue memory banks to provide 8-bit/pixel modes as well.

The TVP3030 extends the packed-24 modes to include 16:3 (pixels:load clocks) using a 128-bit pixel bus width. For example, this enables 24-bit/pixel graphics at 220 MHz pixel rate with only a 40 MHz VRAM serial output. With the 8:3 packed-24 mode (64-bit pixel bus width), a 24-bit/pixel display with 1280 × 1024 resolution may be packed into 4 megabytes of VRAM. A PLL-generated, 50% duty cycle reference clock is output in the packed-24 modes, maximizing VRAM cycle time.

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).

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XGA is a trademark of International Business Machines Corporation.

TARGA is a trademark of Truevision Incorporated.

TVP3030 VIDEO INTERFACE PALETTE

XLAS111A – MAY 1995 – REVISED NOVEMBER 1997

description (continued)

The TVP3030 supports all of the pixel formats of the TVP3026 VIP. Data can be split into 4-bit or 8-bit planes for pseudo-color mode or split into 12-, 16- or 24-bit true-color and direct-color modes. For the 24-bit direct color modes, an 8-bit overlay plane is available. The 16-bit direct- and true-color modes can be configured to IBM XGA® (5, 6, 5), TARGA® (5, 5, 5, 1), or as another (6, 6, 4) existing format. An additional 12-bit mode (4, 4, 4, 4) is supported with 4 bits for each color and overlay. All color modes support selection of little-endian or big-endian data format for the pixel bus. Additionally, the device is also software compatible with the INMOS™ IMSG176/8 and Brooktree™ Bt476/8 color palettes.

Two fully programmable phase-locked loops (PLLs) for pixel clock and memory clock functions are provided for dramatic improvements in graphics system cost and integration. A third loop clock PLL is incorporated making pixel data latch timing much simpler than with other existing color palettes. In addition, an external digital clock input is provided for VGA modes. The reference clock output is driven by the loop clock PLL and provides a timing reference to the graphics accelerator. The shift clock output may be used directly as the VRAM shift clock.

Like the TVP3026, the TVP3030 also integrates a complete, IBM XGA-compatible hardware cursor on chip, making significant graphics performance enhancements possible. Additionally, color-keyed switching is provided, giving the user an efficient means of combining graphic overlays and direct-color images on screen.

The TVP3030 has three 256 × 8 color look-up tables with triple 8-bit video digital-to-analog converters (DACs) capable of directly driving a doubly terminated 75-Ω line. The look-up tables are designed with a dual-ported RAM architecture that enables ultra-high speed operation.

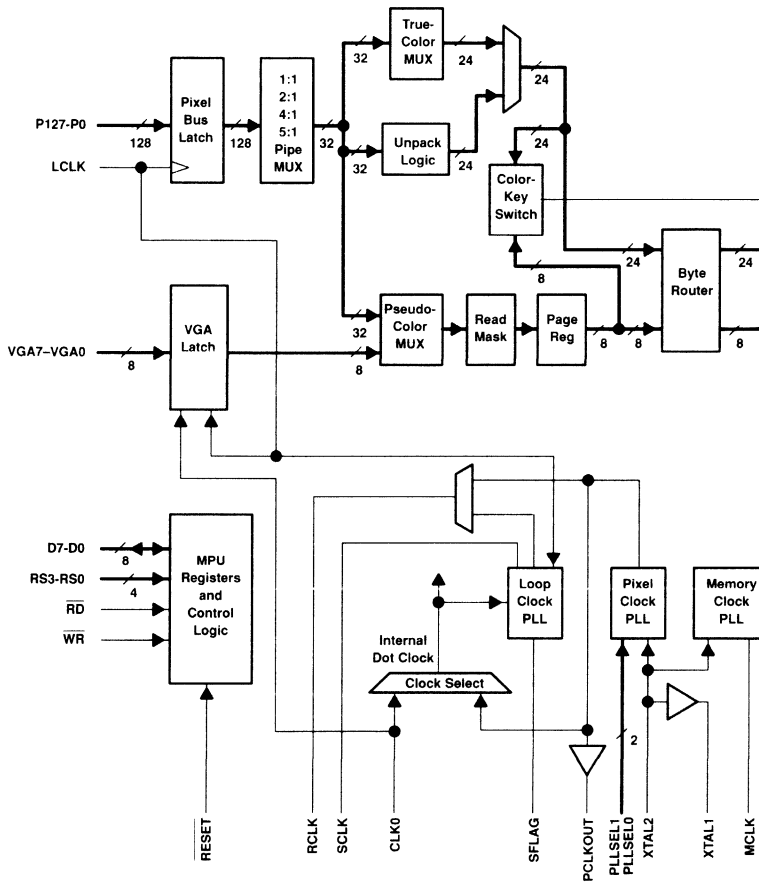
The device features a separate VGA bus that supports the integrated VGA modes in graphics accelerator applications, allowing efficient support for VGA graphics and text modes. The separate bus is also useful for accepting data from the feature connector of most VGA-supported personal computers, without the need for external data multiplexing.

The TVP3030 is a highly integrated system. It can be connected to the serial port of VRAM devices without external buffering and connected to many graphics engines directly. It also supports the split-shift register transfer operation, which is common to many industry standard VRAM devices. To aid in manufacturing test and field diagnosis, several highly integrated test functions have been designed to enable simplified testing of the palette and the entire graphics subsystem.

AVAILABLE OPTIONS

T _A	SPEED	DAC RESOLUTION	PACKAGE	
			FLAT PACK (PPA)	FLAT PACK (MEP)
0°C to 70°C	175 MHz	8 Bits	TVP3030-175PPA	–
	220 MHz	8 Bits	TVP3030-220PPA	–
	250 MHz	8 Bits	–	TVP3030-250MEP

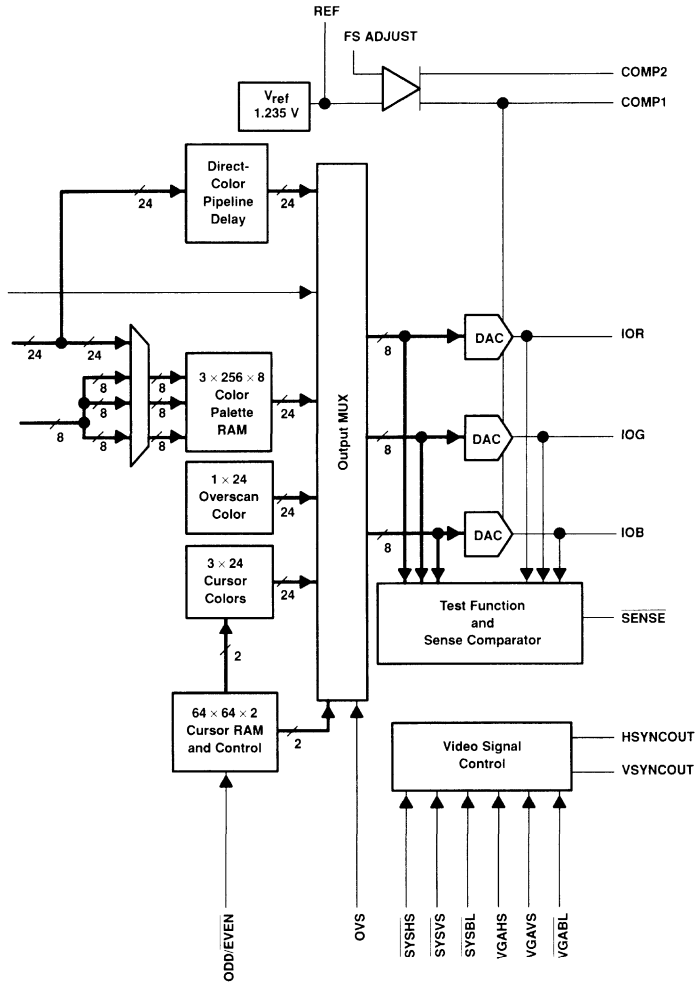
functional block diagram



TVP3030 VIDEO INTERFACE PALETTE

XLAS111A – MAY 1995 – REVISED NOVEMBER 1997

functional block diagram (continued)



- Supports System Resolutions up to 1600 x 1280 at 86-Hz Refresh Rate
- RGB Color Depths of 8, 16, 24, and 32 Bits/Pixel, All At Maximum Resolution
- Programmable Color Space Conversion
- Supports Interpolation for VGA Modes
- Supports RGB, YUV, and Mixed Modes
- 128-Bit Pixel Bus for Shared Frame Buffer Applications
- Supports Dual, Independent 64- or 32-Bit Pixel Ports for Separate Frame Buffer Applications
- RGB modes:
 - 24-Bit/Pixel With 8-Bit Overlay
 - 24-Bit/Pixel Packed-24
 - 16-Bit/Pixel XGA Configuration (5–6–5)
 - 15-Bit/Pixel With 1-Bit Overlay (1–5–5–5)
 - 15-Bit/Pixel Double Buffered (5–5–5)
 - 12-Bit/Pixel Double Buffered (4–4–4)
- YUV Modes:
 - 24-Bit/Pixel 4:4:4 Format
 - 16-Bit/Pixel 4:2:2 Format
- Mixed Modes:
 - 24-Bit YUV 4:4:4 and 8-Bit Overlay
 - 12-Bit YUV 4:1:1 and 4-Bit Overlay
 - 24-Bit Tagged YUV/RGB
 - 15-Bit Tagged YUV/RGB
 - 16-Bit YUV and 8-Bit Overlay + Luma-Key
- Gamma Correction for RGB or YUV Modes
- Hardware Cursor
- Programmable Window Output Controls Pixel Data Flow From Second Frame Buffer
- Supports WRAM Applications
- 175-, 220-, and 250-MHz Versions
- Power-Saving 3.3-V Supply Operation With 5-V Tolerant I/O
- Programmable Frequency Synthesis PLLs for Dot Clock and Memory Clock
- Two Sync PLLs to Compensate for System Delay and Ensure Reliable Data Latching
- Color and Luminance Keying
 - 64 x 64 x 2 Cursor RAM
 - XGA and X-Windows Functional Compatible
- Versatile Pixel Bus Interface Supports Little- and Big-Endian Data Formats
- Triple 8-Bit Monotonic D/A Converters
- Analog Output Comparators for Monitor Detection
- RS-343A Compatible Outputs
- Direct VGA Pass-Through Capability
- Palette Page Register
- Horizontal Zooming Capability
- EPIC 0.72 mm CMOS Process

description

The TLV3033 128-bit RAMDAC is a performance-enhanced version of the TVP3026 64-bit RAMDAC. By operating at high frequencies and integrating a wider pixel bus, the TVP3033 provides more colors at higher resolutions. Intended for 4M-byte to 8M-byte, VRAM-based high-end PC graphics systems, the TVP3033 supports speeds of 175-MHz, 220-MHz, and 250-MHz, enabling 24-bit true color (16.7 million colors) at 1600 × 1280 resolution at 86-Hz refresh rate. The TVP3033 is highly integrated with high-speed triple 8-bit DACs, three 256-x-8 color lookup tables, a 64 × 64 × 2 hardware cursor, and a programmable pixel multiplexing interface. The TVP is available in a 208-pin QFP package and is characterized from T_A = 0°C to 70°C.

† For the complete data manual (SLAS149), contact your local TI sales office.

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XGA is a trademark of IBM.

X-Window is a trademark of the Massachusetts Institute of Technology

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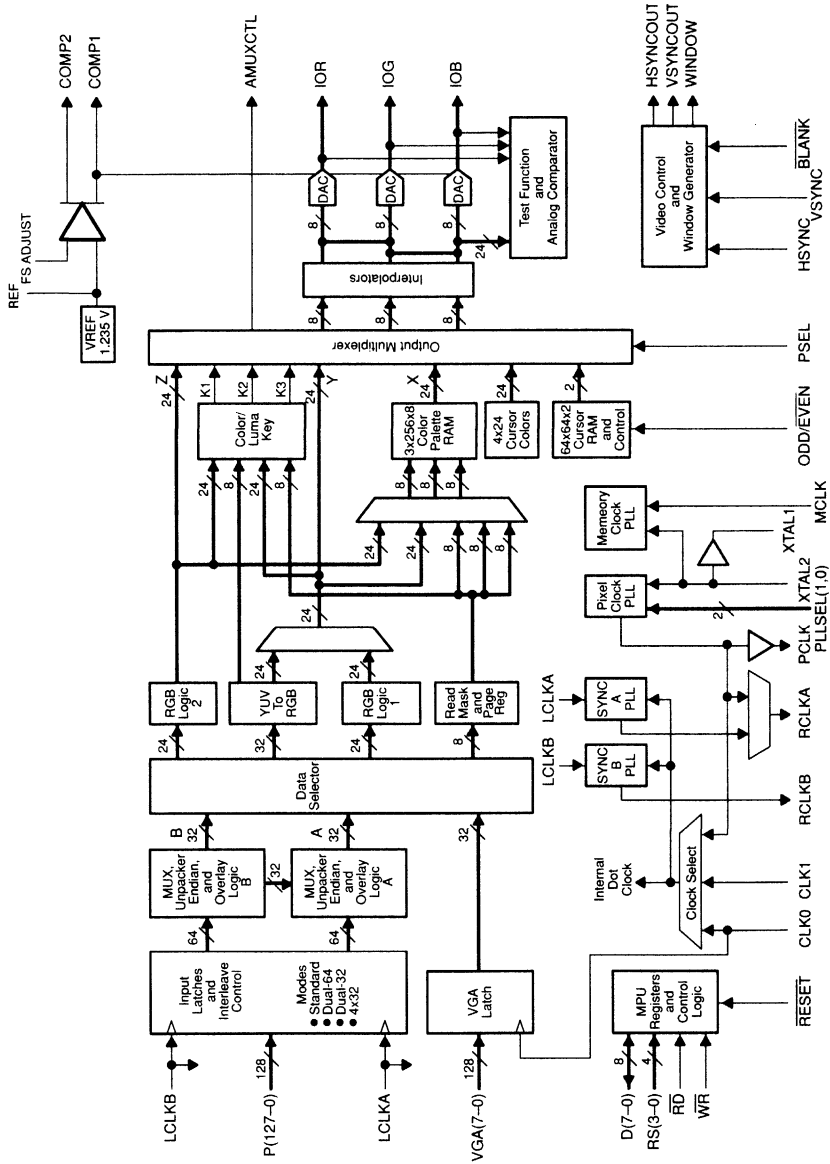
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TVP3033 VIDEO INTERFACE PALETTE

XLAS149 – NOVEMBER 1997

functional block diagram



TVP3409

VIDEO INTERFACE PALETTE TRUE-COLOR CMOS RAMDAC

XLAS092A – MAY 1995 – REVISED NOVEMBER 1997

features

- **Functionally Interchangeable With ATT20C409**
- **170/135 MHz (0.8 μ m CMOS)**
 - 170 MHz 2:1 Multiplex 8-Bit Pseudocolor
 - 73 MHz True-Color
- **16-Bit Pixel Port, Usable as an 8-Bit Port**
 - Compatible With ATT20C490 Using P(7-0)
 - Compatible With ATT20C498 Using P(15-0)
- **9 Software-Selectable Color Modes**
 - 24-Bit Packed Pixels
 - 24-Bit True Color
 - 8-Bit Pseudocolor
- **2:1 and 1:1 Pixel Multiplexing**
- **Power Dissipation of 1.19 W at 135 MHz Typ**
- **Dual Programmable Clock Synthesizers**
 - Pixel Clock and Memory Clock
 - Reset to 28.322-MHz and 25.175 MHz VGA Frequencies
 - Strobe Input Latches Frequency Select Lines

- **On-Chip PLL Clock Doubler**
 - 85 MHz Input
 - 170 MHz Pixel Output
- **256 \times 24 Color RAM**
- **Software Compatible With the AT&T ATT20C498/499/409**
- **68-Terminal Plastic Leaded Chip Carrier (PLCC) Package**
- **Data Manual Available†**

applications

- **Screen Resolutions (noninterlaced)**
 - 1600 \times 1280, 8-Bit/Pixel, 60 Hz
 - 1280 \times 1024, 16-Bit/Pixel, 60 Hz
 - 1024 \times 768, 16-Bit/Pixel, 100 Hz
 - 1024 \times 768, 24-Bit/Pixel, Packed, 67 Hz
 - 800 \times 600, 24-Bit/Pixel, Unpacked, 75 Hz
 - 800 \times 600, 24-Bit/Pixel, Packed, 110 Hz
- **True-Color Desktop, PC Add-in Card**
- **X-Windows Terminals**
- **Green PCs**

description

The TVP3409 is intended to be a direct replacement for the ATT20C409 RAM digital-to-analog converter (RAMDAC). The TVP3409 RAMDAC supports 8-bit multiplexed operation that can be input on 16 pixel terminals. The TVP3409 retains register compatibility with the ATT20C498 and ATT20C499 devices. The TVP3409 features 24-bit packed pixel modes that provide 24-bit graphics at up to 1024 x 768 screen resolution. Dual clock synthesizers offer two programmable and two fixed frequencies in phase-locked-loop A (PLLA) and one programmable and three fixed frequencies in phase-locked-loop B (PLLB). After reset, the frequencies are:

PLLA: 25.175, 28.322, 50, and 75 MHz

PLLB: 30, 40, 50, and 60 MHz

Easy identification of the RAMDAC allows the video BIOS to determine if a requested mode is available on the hardware being used.

AVAILABLE OPTIONS

T _A	SPEED	DAC RESOLUTION	PACKAGE
			CHIP CARRIER (FN)
0°C to 70°C	135 MHz	8 Bits	TVP3409–135CFN
	170 MHz	8 Bits	TVP3409–170CFN

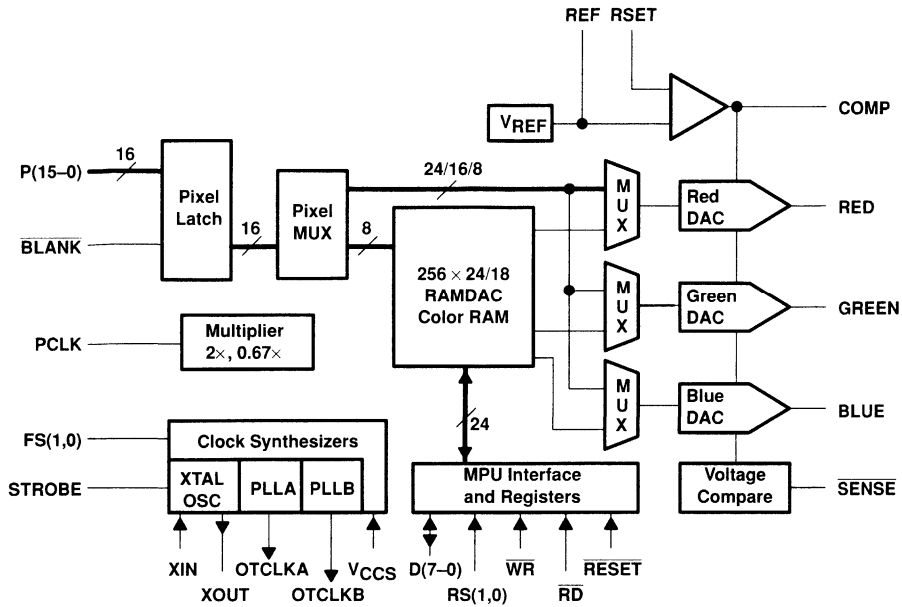
† For the complete data manual (SLAS092), contact the local TI sales office.

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TVP3409 VIDEO INTERFACE PALETTE TRUE-COLOR CMOS RAMDAC

XLAS092A - MAY 1995 - REVISED NOVEMBER 1997

functional block diagram



TVP3703
VIDEO INTERFACE PALETTE
TRUE-COLOR CMOS RAMDAC

XLAS100A – FEBRUARY 1995 – REVISED NOVEMBER 1997

- Fully Integrated Dual Clock Synthesizer and 16-Bit Pixel Port True-Color RAMDAC
- Two Phase-Locked-Loop (PLL) Synthesizers Provide Independently Controlled Video and Memory Clock Outputs
- Functionally Interchangeable with STG1703
- On-Chip PLL Clock Reference Requires Single External Crystal
- 16-Bit Pixel Port Supports VGA High-Color and True-Color Standards Up to 170 MHz
- Programmable Power-Down Features
- On-Chip Cyclic Redundancy Check (CRC) Test
- Data Sheet Available†

applications

- Screen Resolutions (Noninterlaced)
 - 1600 × 1280, 8-bit/pixel, 60 Hz
 - 1280 × 1024, 16-bit/pixel, 60 Hz
 - 1024 × 768, 16-bit/pixel, 85 Hz
 - 1024 × 768, 24-bit/pixel, packed, 70 Hz
 - 800 × 600, 24-bit/pixel, unpacked, 72 Hz
- True-Color Desktop, PC Add-In Cards

description

The TVP3703 is a super video graphics array (SVGA) compatible, true-color CMOS RAMDAC with integrated clock synthesizers that can provide the memory and pixel clock signals for a PC graphics subsystem. The video clock can be one of two VGA base frequencies or fourteen Video Electronics Standards Association (VESA) standard frequencies which can also be reprogrammed through the standard micro port interface.

The memory clock output is also user programmable at frequencies up to 80 MHz. The pixel modes supported by the TVP3703 include:

- Serializing 16-bit pixel port providing 170 MHz, 8-bit and 73 MHz, 24-bit packed pixel modes using an internal PLL
- 16-bit pixel port providing faster, high-color/true-color operation up to the 110 MHz sampling rate
- 8-bit pixel port providing standard SVGA and high-color/true-color modes up to the 110 MHz sampling rate

The 68 terminal FN package is designed to be interchangeable with the STG1703.

AVAILABLE OPTIONS

T _A	SPEED	DAC RESOLUTION	PACKAGE
			CHIP CARRIER (FN)
0°C to 70°C	135 MHz	8 Bits	TVP3703-135CFN
	170 MHz	8 Bits	TVP3703-170CFN

† For the complete data sheet (SLAS100), contact the local TI sales office.

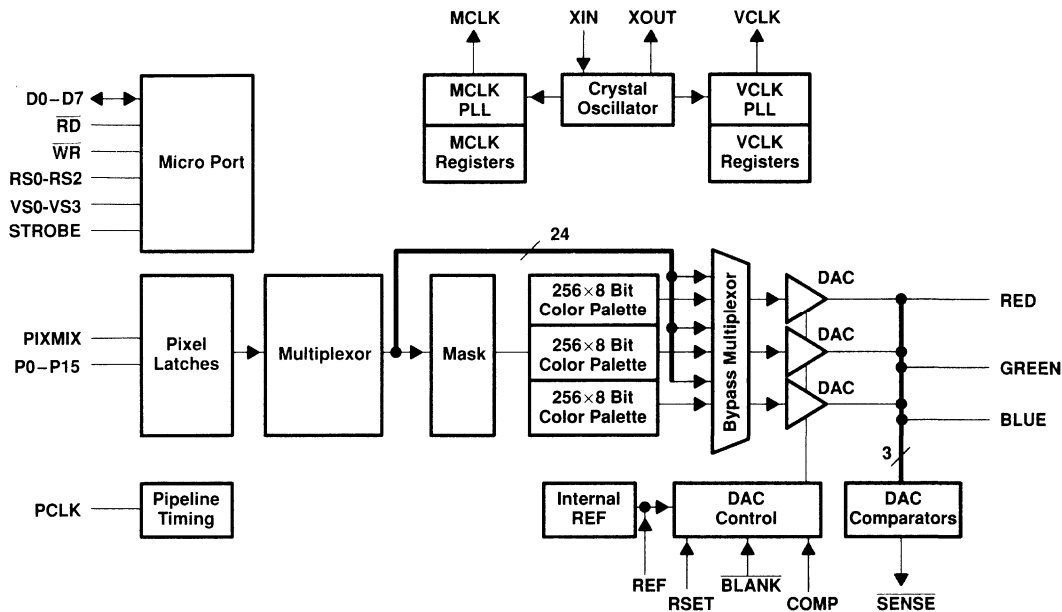
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TVP3703
VIDEO INTERFACE PALETTE
TRUE-COLOR CMOS RAMDAC

XLAS100A – FEBRUARY 1995 – REVISED NOVEMBER 1997

functional block diagram



General Information	1
General Purpose ADCs	2
General Purpose DACs	3
DSP AICs and CODECs	4
Special Functions	5
Video Interface Palettes	6
Digital Imaging Sensor Products	7
Mechanical Information	8

Contents

	Page
TLC8044 :	7-3
TLC8144 :	7-33
TLC8188 :	7-61

TLC8044

**12-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS**

SLAS128 – JUNE 1997

- Color or Gray Scale Operation
- Signals Processed in the Digital Domain
- Differential RGB Input Multiplexer
- Three 8-bit DACs for CCD Offset Level Shifting With Bipolar Correction Range
- Two Sampling Modes:
 - DAC Referenced
 - Correlated Double Sampling (CDS)
- 12-Bit ADC with 6 MSPS Operation
- Digital dc Restoration
- Pixel-By-Pixel Offset and Shading (Gain) Compensation
- Global Gain Adjust for Each Color (Channel)
- Compatible with 600 dpi CCD Image Sensors
- Global Offset Adjust for Each Color (Channel)
- Output Word Length Programmable to 8, 10, 12, or 16 Bits
- Programmable Threshold Detector for Each Color (Channel)
- Dual Internal Default Registers for Even/Odd Pixel Offset Correction
- 68-Terminal PLCC Package

applications

- Handy Scanners
- Flatbed Scanners

description

The TLC8044 is a 12-bit analog-to-digital interface subsystem for charge-coupled device (CCD) image sensors and scanners. An input multiplexer allows color operation with a single on-chip 12-bit ADC. The TLC8044 uses DSP circuits to correct for nonideal CCD image sensor and scanning system characteristics. Cost effective gray scale operation is obtained using a single multiplexer input. The TLC8044 three-channel input multiplexer and sampling function has two basic modes of operation: normal sampling and correlated double sampling. The internal sample and hold allows all three channels to be sampled simultaneously in color operation. Three DACs (8 bits + sign) are provided to allow bipolar adjustment of the dc level of the signal at the ADC input. Digital dc restoration is provided following the ADC. Variations in offset and luminance across a scan are dynamically corrected on a pixel-by-pixel basis, using calibration data provided by an external data store. Provisions are made for global adjustments of gain, contrast and color balance, and offset for brightness. The output word length can be programmed to 8, 10, 12, or 16 bits, and a programmable threshold detector is provided for use during calibration and OCR applications. The TLC8044 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T _A	PACKAGE
	CHIP CARRIER (FN)
0°C to 70°C	TLC8044FN

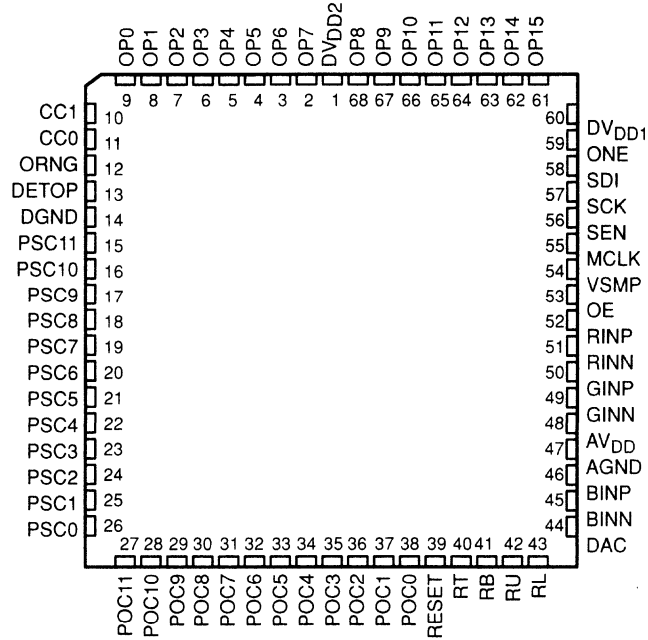
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



TLC8044
12-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS

SLAS128 - JUNE 1997

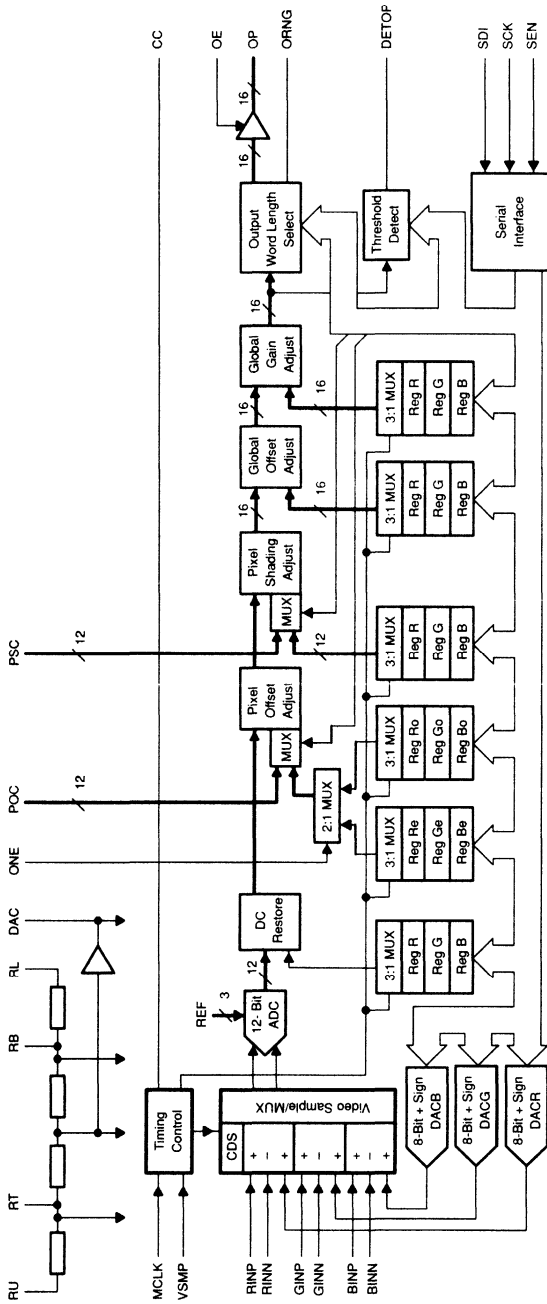
FN PACKAGE
(TOP VIEW)



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TLC8044
12-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
 SLAS128 - JUNE 1997

functional block diagram



TLC8044
12-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
 SLAS128 – JUNE 1997

Terminal Functions

TERMINAL NAME	NO.	TYPE	I/O	DESCRIPTION
AGND	47	Analog	I	Analog ground (0 V)
AVDD	48	Analog	I	Positive analog supply (5 V)
BINN	45	Analog	I	Negative blue channel input video
BINP	46	Analog	I	Positive blue channel input video
CC1,0	10, 11	Digital	O	Color code outputs. CC0 and CC1 indicate which channel the current output sample was taken from (R = 00, G = 01, B = 10).
DAC	44	Analog	O	Buffered midpoint of ADC reference string. DAC is used internally to set DAC reference voltages.
DETOP	13	Digital	O	Threshold detector output (active high). DETOP indicates that the current output pixel has exceeded the internally programmed threshold for that channel.
DGND	14	Digital	I	Digital ground (0 V)
DVDD1,2	60, 1	Digital	I	Positive digital supply (5 V)
GINN	49	Analog	I	Negative green channel input video
GINP	50	Analog	I	Positive green channel input video
MCLK	55	Digital	I	Master clock. MCLK is applied at either six times or twice the input pixel rate for color and monochrome operation, respectively. MCLK is divided by two internally to define the ADC sample rate and to provide the clock source for the DSP section.
OE	53	Digital	I	Output 3-state control. Outputs are enabled when OE = 0.
ONE	59	Digital	I	Odd not even. ONE defines the even and odd pixels when the internal pixel offset correction registers are in use (even = 0, odd = 1).
OP15–OP0	61-68, 2-9	Digital	O	Digital 16-bit output (3-state). In 8-, 10-, and 12-bit output modes, OP15 is used to indicate that the output pixel is negative; i.e., OP15 can be used as an under range indicator. OP15 is active high when indicating under range.
ORNG	12	Digital	O	Over range signal (active high). In 8-, 10-, and 12-bit output modes, this signal indicates that the current output pixel has exceeded the maximum achievable for the output word length in use.
POC11–POC0	27-38	Digital	I	Pixel offset coefficient input. The POC11–POC0 12-bit word is applied at the multiplexed pixel rate (i.e., three samples per pixel period in color mode) to correct offset errors in a pixel-by-pixel fashion.
PSC11–PSC0	15-26	Digital	I	Pixel shading coefficient input. The PSC11–PSC0 12-bit quantity is applied at the multiplexed pixel rate (i.e., three samples per pixel period in color mode) to correct shading effects in a pixel-by-pixel fashion.
RESET	39	Digital	I	Reset input (active high). RESET forces a reset of all internal registers in the TLC8044.
RINN	51	Analog	I	Negative red channel input video
RINP	52	Analog	I	Positive red channel input video
RU, RT, RB, RL	42, 40, 41, 43	Analog	I	ADC reference terminals. The voltage applied between RT (full scale) and RB (zero level), define the ADC reference range. RU and RL, upper and lower resistor terminals, are used to derive optimum reference voltages from an external 5-V reference.
SCK	57	Digital	I	Serial clock. Serial interface clock signal.
SDI	58	Digital	I	Serial data in. Serial interface input data signal.
SEN	56	Digital	I	Serial enable
VSMP	54	Digital	I	Video sample synchronization pulse. VSMP applied synchronously with MCLK specifies the point in time that the input is sampled. The timing of internal multiplexing between the R, G, and B channels is derived from this signal.

TLC8044
12-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
SLAS128 – JUNE 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD1} , V_{DD2} , V_{DD} , V_{DD} (see Note 1)	7 V
Digital inputs (see Note 1)	- 0.3 V to $V_{DD} + 0.3$ V
Analog inputs (see Note 1)	- 0.3 V to $V_{CC} + 0.3$ V
Digital outputs, maximum external voltage applied (see Note 1)	- 0.3 V to $V_{CC} + 0.3$ V
Reference input (see Note 1)	- 0.3 V to $V_{DD} + 0.3$ V
Operating temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	-50°C to 150°C
Lead temperature, soldering, 10 sec	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltages applied to V_{DD1} and V_{DD2} are measured with respect to the DGND terminal. V_{DD} is measured with respect to the AGND terminal. For the following specifications, unless otherwise noted, AGND and DGND are tied together (and represent 0 volts) and are referred to simply as GND. When the voltages applied to V_{DD1} , V_{DD2} , and V_{DD} are equal, they are referred to simply as V_{DD} , unless otherwise noted.

recommended operating conditions

total device

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75		5.25	V

digital inputs

	MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	0.9 V_{DD}			V
Low-level input voltage, V_{IL}			0.1 V_{DD}	V

input multiplexer

	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Setup time, input video before MCLK↑, $t_{su}(V)$		10			ns
Hold time, input video after MCLK↑, $t_h(V)$		25			ns
Setup time, reset video before MCLK↑, $t_{su}(R)$	CDS mode only	10			ns
Hold time, reset video after MCLK↑, $t_h(R)$	CDS mode only	25			ns

serial interface

	MIN	NOM	MAX	UNIT
Cycle time, MCLK, t_{cyc1}	83.3			ns
Pulse duration, MCLK high, $t_{w1}(MCLKH)$	37.5			ns
Pulse duration, MCLK low, $t_{w2}(MCLKL)$	37.5			ns
Setup time, VSMP↑ to MCLK↑, $t_{su}(D)$	10			ns
Hold time, MCLK↑ to VSMP↓, $t_h(D)$	10			ns
Setup time, POC/PCS to MCLK↓, $t_{su}(P)$	10			ns
Hold time, MCLK↓ to POC/PCS, $t_h(P)$	30			ns
Cycle time, SCK, t_{cyc2}	83.3			ns
Pulse duration, SCK high, $t_{w3}(SCKH)$	37.5			ns
Pulse duration, SCK low, $t_{w4}(SCKL)$	37.5			ns
Setup time, SDI to MCLK↑, $t_{su}(S)$	10			ns
Hold time, MCLK↑ to SDI change, $t_h(S)$	10			ns
Setup time, SCK↑ to SEN↑, $t_{su}(SCE)$	20			ns
Setup time, SEN↓ to SCK↑, $t_{su}(SEC)$	20			ns
Pulse duration, SEN high, $t_w(SEN)$	50			ns



TLC8044
12-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
 SLAS128 – JUNE 1997

electrical characteristics, $V_{DD} = 5\text{ V}$, $AGND = DGND = 0\text{ V}$, $T_A = \text{full range}$ (unless otherwise noted)

total device

PARAMETER		MIN	TYP	MAX	UNIT
I_{CC}	Supply current, active		80	130	mA
I_{CC}	Supply current, standby		8	10	mA

digital inputs

PARAMETER		MIN	TYP	MAX	UNIT
I_{IH}	High-level input current			1	μA
I_{IL}	Low-level input current			1	μA
C_i	Input capacitance		10		pF

digital outputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V_{OH}	High-level output voltage	$I_{OH} = -1\text{ mA}$			$V_{DD} - 0.75$	V
V_{OL}	Low-level output voltage	$I_{OL} = 1\text{ mA}$			0.75	V
I_{OZ}	High-impedance output current			1	μA	

input multiplexer

PARAMETER		MIN	TYP	MAX	UNIT
	Channel-to-channel gain matching		0.5%	5%	
V_{ICR}	Common mode input voltage	0.5		4.5	V

reference string

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z	Impedance, RT to RB	595	850	1105	Ω
Z	Impedance, RU to RL	1190	1700	2210	Ω
$V_{ref(RT)}$	Reference voltage, top	$V_{I(RU)} = 5\text{ V}$, $V_{I(RL)} = 0\text{ V}$		3.7875	V
$V_{ref(RB)}$	Reference voltage, bottom	$V_{I(RU)} = 5\text{ V}$, $V_{I(RL)} = 0\text{ V}$		1.2625	V
$V_{ref(DAC)}$	DAC reference voltage	$V_{I(RU)} = 5\text{ V}$, $V_{I(RL)} = 0\text{ V}$		2.525	V

8-bit DACs

PARAMETER	MIN	TYP	MAX	UNIT
Resolution	8			Bits
Zero-scale voltage	0		10	mV
Full-scale voltage	$V_{ref(DAC)} - 10$		$V_{ref(DAC)} + 10$	mV
Differential nonlinearity (DNL)		0.1	< 1	LSB
Integral nonlinearity (INL)		0.4	1	LSB



TLC8044
12-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS

SLAS128 – JUNE 1997

electrical characteristics, $V_{DD} = 5\text{ V}$, $AGND = DGND = 0\text{ V}$, $T_A = \text{full range}$ (unless otherwise noted)
(continued)

12-bit ADC

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		12			Bits
Sampling rate		6			MSPS
Full-scale transition error voltage at xINP (see Note 2)	Single-ended mode, $V_{I(xINN)} = 2.5\text{ V}$, DAC code = 000H	-100		100	mV
Zero-scale transition error voltage at xINP (see Note 3)	Single-ended mode, $V_{I(xINN)} = 2.5\text{ V}$, DAC code = 000H	-100		100	mV
Full-scale transition error voltage, $V_{I(xINP)} - V_{I(xINN)}$ (see Note 2)	Differential mode, DAC code = 000H	-25		25	mV
Zero-scale transition error voltage, $V_{I(xINP)} - V_{I(xINN)}$ (see Note 3)	Differential mode, DAC code = 000H	-25		25	mV
Differential nonlinearity (DNL) (see Note 4)				1.5	LSB
Maximum number of missing codes		0			CODES
Integral nonlinearity (INL) (see Note 5)			± 2	± 5	LSB

- NOTES:
2. The full-scale transition at xINP is the difference between the signal input voltage that causes the 4094 to 4095 transition and the measured reference voltage $V_{ref(RT)}$.
 3. The zero-scale transition at xINP is the difference between the signal input voltage that causes the 0 to 1 transition and the reference voltage $V_{ref(RB)}$.
 4. Differential nonlinearity (DNL) is the difference between the measured value between any two adjacent codes and the ideal 1 LSB value.
 5. Integral nonlinearity (INL) is the maximum deviation of the output from the ideal straight line between zero and the full-scale value.

switching characteristics

PARAMETER	MIN	TYP	MAX	UNIT
$t_{pd(D)}$ Propagation delay time, $MCLK\downarrow$ to output valid		50	75	ns
$t_{en(PZE)}$ Enable time, output, $OE\downarrow$ to data valid		70	75	ns
$t_{dis(PEZ)}$ Disable time, output, $OE\uparrow$ to high impedance		70	25	ns



TLC8044
12-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
 SLAS128 – JUNE 1997

PARAMETER MEASUREMENT INFORMATION

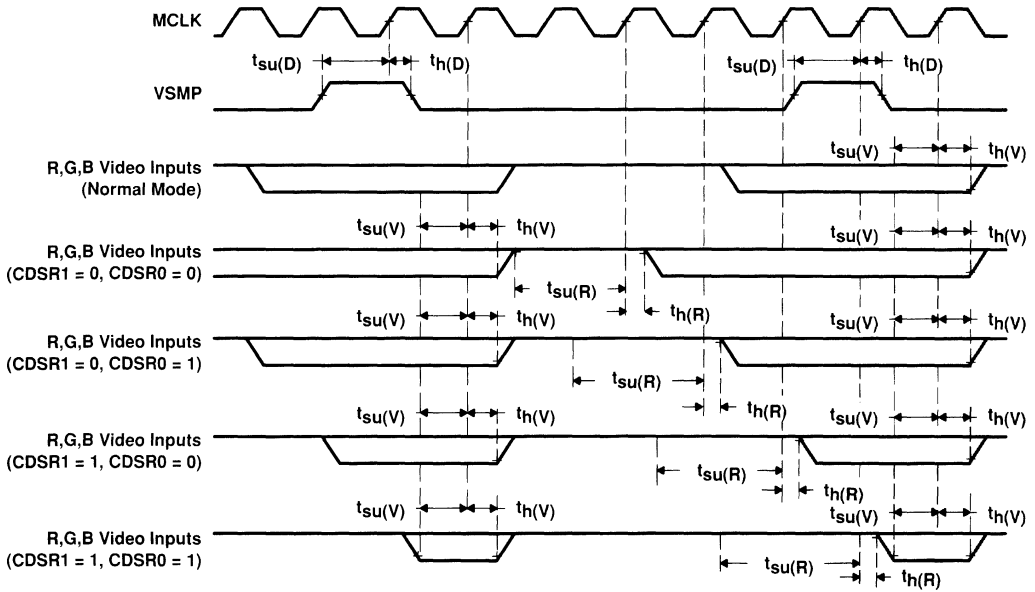


Figure 1. Detailed Video Input Timing – Color Mode

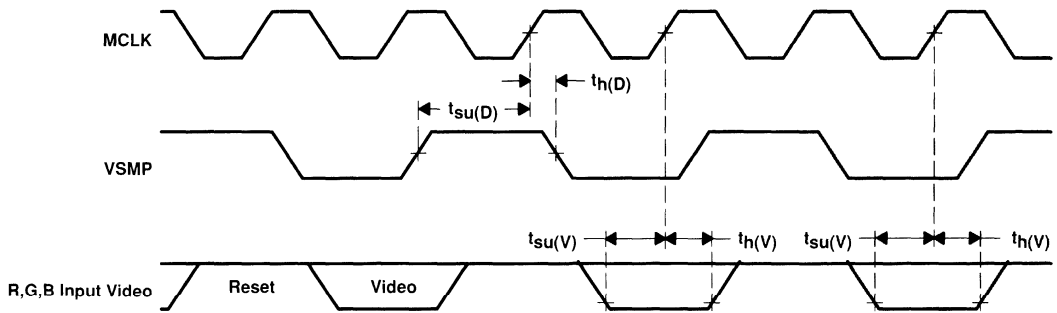


Figure 2. Detailed Video Input Timing – Monochrome Mode

PARAMETER MEASUREMENT INFORMATION

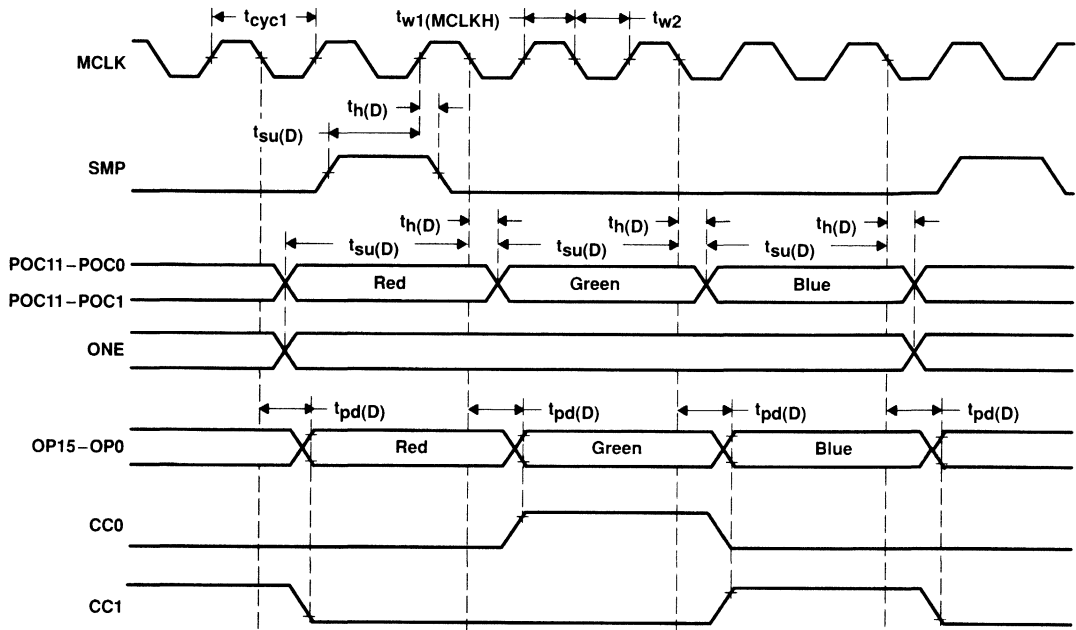


Figure 3. Detailed Digital Timing – Color Mode

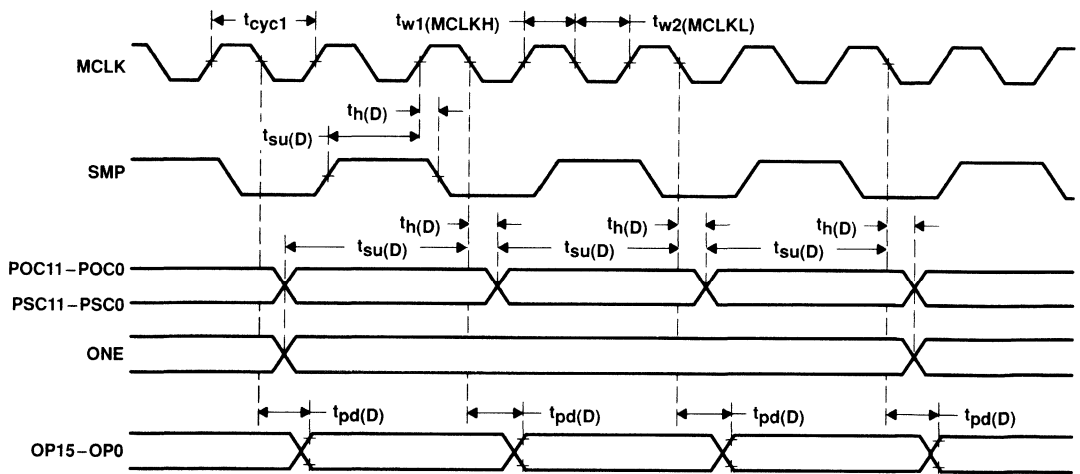


Figure 4. Detailed Digital Timing – Monochrome Mode

TLC8044
12-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
 SLAS128 – JUNE 1997

PARAMETER MEASUREMENT INFORMATION

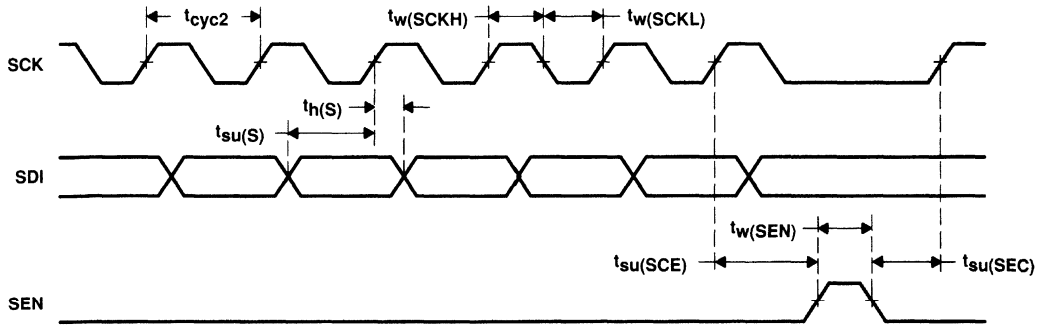


Figure 5. Detailed Digital Timing – Serial Interface

TYPICAL CHARACTERISTICS

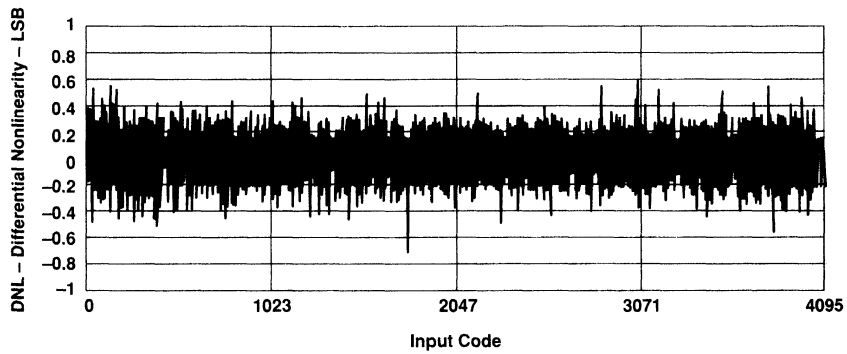


Figure 6. Differential Linearity With Code

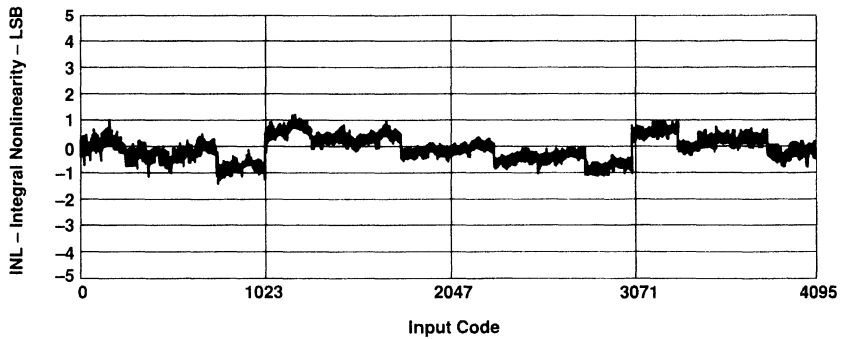


Figure 7. Integral Linearity With Code

PRINCIPLES OF OPERATION

general CCD system operation

CCD image sensor array output summary

Figure 8 shows a simplified CCD image sensor linear array system with typical CCD array inputs and outputs. The inputs for the shift gate (SH), reset, and two-phase clock drive the array. An electronic charge proportional to the light input is generated by a photo diode for each pixel of the array. The charge for each pixel is transferred in parallel into the analog CCD shift register using the shift gate input and then shifted out serially using a two-phase clock. At the CCD output (OS terminal), the array converts the charge for each pixel into a voltage using a capacitor and source follower MOS transistor. The charge on this capacitor is reset for each pixel by the reset pulse input. A typical output signal then includes a reset period, a dark period, and a period containing video output for each pixel, as shown in Figure 9. This signal sits on a varying dc offset of typically 5 V and is negative going for an increase in video output. An output (DOS terminal) also provides only the dc level from the CCD array.

TLC8044
12-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
 SLAS128 - JUNE 1997

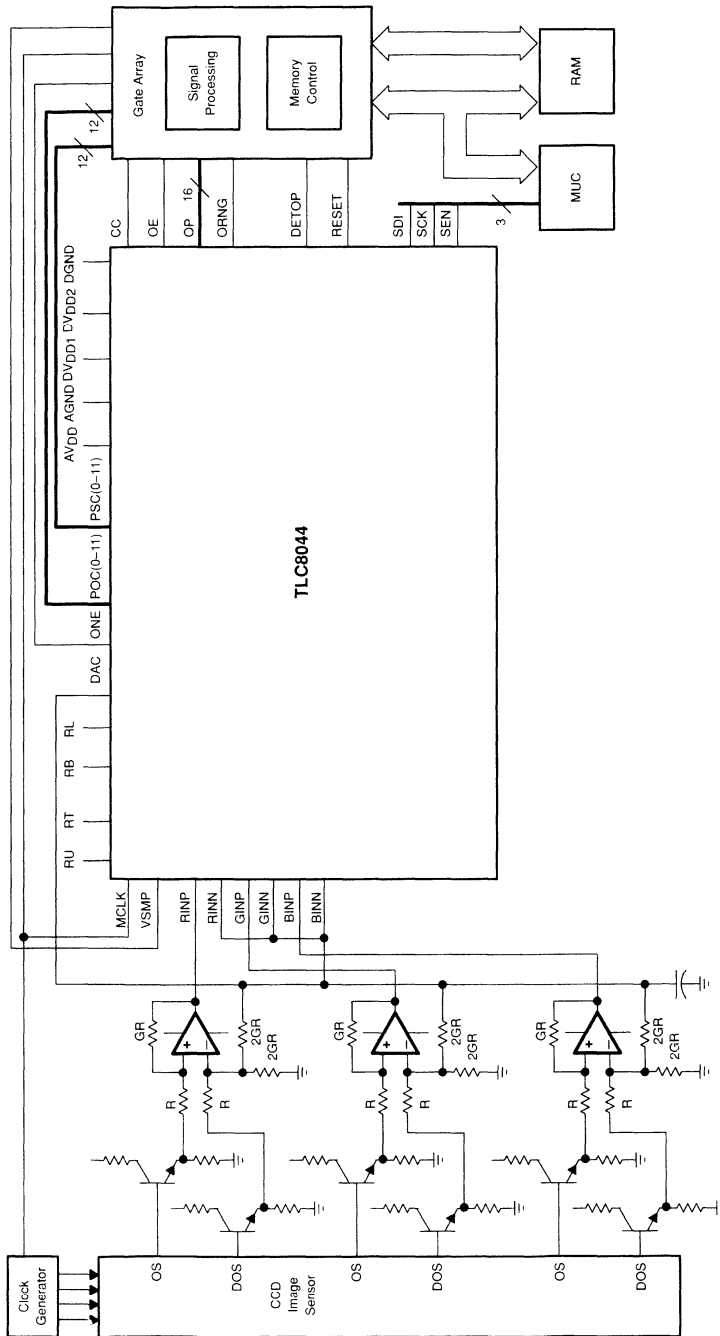


Figure 8. System Diagram

PRINCIPLES OF OPERATION

CCD image sensor array output summary (continued)

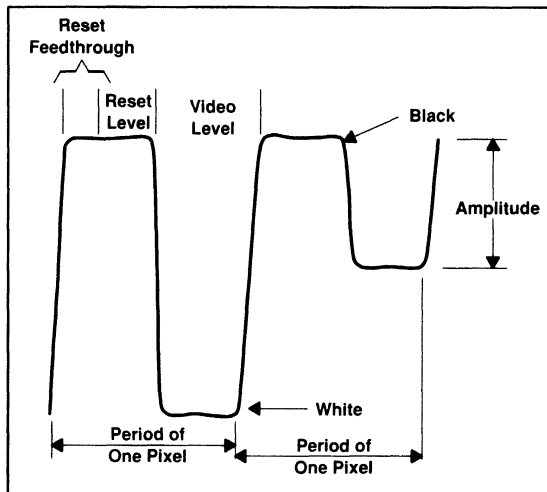


Figure 9. A Typical Charge-Coupled Display (CCD) Output Signal

CCD array analog-to-digital interface functions

The interface to the CCD array analog output and the conversion of the output into digital form involves the following functions:

1. The video output waveform first has to be removed from the varying dc level on which it sits and shifted in level to be compatible with an interface device running from a single 5-V supply rail.
2. Gain has to be applied to bring the signal up to the full-scale range of the analog-to-digital converter (ADC) and a means provided to adjust static gain to compensate for variations between devices or multiple outputs of color arrays. Once these static dc levels (offsets) and gain levels have been adjusted, dynamic corrections are needed on a pixel-by-pixel basis.
3. Dynamic gain adjustment is needed to compensate for the fall off in output from the center to the ends of the array when used in scanner applications (see Figure 10). Dynamic offset adjustments are required to compensate for the pixel-by-pixel variation in black dc levels obtained from different CCD array elements.
4. DC restoration may optionally be required. Global adjustments of gain and offset across a whole scan are respectively used to correct color balance and contrast and to change brightness.

PRINCIPLES OF OPERATION

CCD array analog-to-digital interface functions (continued)

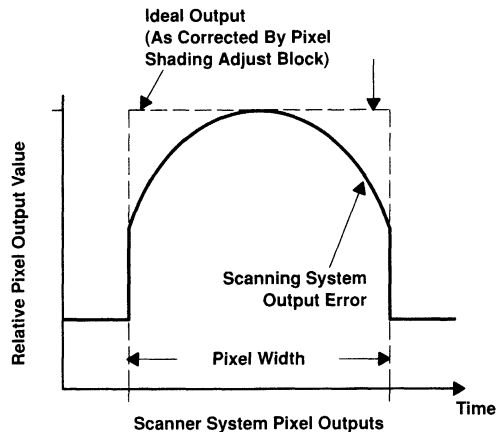


Figure 10. Scanner System Relative CCD Pixel Output

CCD scanner analog-to-digital interface subsystem

input dc level shift, output offset, and channel gain

The TLC8044 uses external operational amplifiers configured as differential amplifiers to remove the dc level present in the CCD outputs by using the common mode voltages from the OS and DOS outputs for each channel (see the functional block and system diagrams). DC bias is provided for the external differential amplifier from the TLC8044 DAC output as shown in the system diagram in Figure 8. Without any residual offset from the CCD, the differential amplifier minimum output is (DAC result)/2 and is unaffected by the external differential amplifier gain setting (G). The offset at the output of the external differential amplifiers, including residual offset from the CCD, should be low enough to ensure the CCD amplified signal is within the input common mode range of the TLC8044 and that the offset can be adjusted out by the TLC8044 internal DACs.

The external differential amplifiers also provide the system gain for each channel to ensure the output amplitude of each channel is greater than one half the ADC full-scale range. Variations between the RGB channels of the CCD can have a 10 to 1 ratio in output. To minimize the offset at the amplifier output with the highest gain, the external amplifiers should be configured for gains in the range 1/3 to 3 rather than 1 to 10 to compensate for this output variation. This is achieved by scaling the gain setting resistors shown in the system diagram by the gain factor (G) over this 1/3 to 3 range.

RGB channel multiplexer and sampler

For color CCD image sensor arrays, a combined three-input multiplexer and sampler is used enabling the use of a single fast 12-bit ADC and DSP channel.

The TLC8044 multiplexer has three differential inputs for each of the RGB channel outputs and a further internal input for each channel which is used to compensate for the residual offset in the input signal. This internal offset compensation is provided by the TLC8044 three 8-bit plus sign DACs, which provide bipolar offset correction with respect to the input reference levels. The DACs are updated through the serial interface.

PRINCIPLES OF OPERATION

RGB channel multiplexer and sampler (continued)

The input structure can be set up for use in single-ended or fully differential mode, under control of the serial interface data. The configuration shown in the system diagram is single ended, with the negative inputs tied to the DAC, which is the buffered midpoint of the ADC reference chain. Differential mode can be used when an amplifier with differential outputs is placed between the CCD image sensor and the TLC8044.

In color operation, the three-channel sampling system multiplexes the three channels to the ADC input in a sequence defined by the VSMP input synchronization pulse. In monochrome operation, channel synchronization between R, G, and B inputs is achieved through the serial interface.

analog-to-digital converter

The ADC is implemented using a 12-bit pipelined architecture which performs conversions at one half the MCLK clock rate. The ADC full-scale range is defined by the voltages applied to terminals RT and RB, which should be set to 3.75 V and 1.25 V respectively to give a full-scale range of 3.75 V - 1.25 V = 2.5 V.

The ADC internal input is differential with an input signal of 2.5 V corresponding to full scale (output code FFF hex) and -2.5 V corresponding to zero scale (output code 000 hex).

The RU and RL terminals are connected to extensions of the internal reference chain, which allow the 3.75-V and 1.25-V levels to be derived from a 5-V reference applied between RU and RL. All reference terminals should be capacitively decoupled externally.

The combination of the input multiplexer structure with the internal offset correction DACs accomodates a wide range of input voltages. The relationships between input voltage levels (at the positive and negative inputs INP and INN) and ADC full-scale and zero-scale results are shown in Tables 1 and 2 for a range of input offset voltages for both single-ended and differential input modes. The tables also show the DAC correction voltage and code required in each case.

The basic difference between single-ended and differential input modes is that a gain of 2 is applied to the input signal between INP and INN in the single-ended case. Thus an input differential of 1.25 V is converted to a full-scale ADC differential input of 2.5 V. Any residual offset present on the input signal is also gained by 2 in the single-ended mode, resulting in the required DAC values shown in Table 1.

Table 1. Single-Ended Mode Input Voltage Ranges

INPUT OFFSET VOLTAGE	FULL-SCALE INPUT VOLTAGE		ZERO-SCALE INPUT VOLTAGE		DAC VOLTAGE	DAC CODE (HEX)
	V _{I(INP)}	V _{I(INN)}	V _{I(INP)}	V _{I(INN)}		
0.625	4.375	2.5	1.875	2.5	-1.25	17F
0	3.75	2.5	1.25	2.5	0	000
-0.625	3.125	2.5	0.625	2.5	1.25	07F

Table 2. Differential Mode Input Voltage Ranges

DIFFERENTIAL INPUT OFFSET VOLTAGE	FULL-SCALE INPUT VOLTAGE		ZERO-SCALE INPUT VOLTAGE		DAC VOLTAGE	DAC CODE (HEX)
	V _{I(INP)}	V _{I(INN)}	V _{I(INP)}	V _{I(INN)}		
1.25	4.375	0.625	1.875	3.125	-1.25	17F
0	3.75	1.25	1.25	3.75	0	000
-1.25	3.125	1.875	0.625	4.375	1.25	07F

PRINCIPLES OF OPERATION

analog-to-digital converter (continued)

The examples in Tables 1 and 2 assume that the ADC reference terminals RT and RB are set to 3.75 V and 1.25 V, respectively. The signals shown in the tables cover the full-scale range of the ADC. In practice, a reduced range is used to allow some headroom, accommodating a wider range of input offset voltages. The ADC output code can be inverted under control of the serial interface. When not in use, the ADC can also be put into standby mode through the serial interface to reduce system power consumption.

sample modes

Two input sampling modes are provided, normal and correlated double sampling (CDS). Sampling mode selection is made through the serial interface. All video input timing and sampling is performed relative to the rising edge of the MCLK clock input signal. MCLK is applied to twice the required ADC conversion rate. Synchronization of sampling and channel multiplexing to the incoming video signals is performed by the VSMP input synchronization pulse. Table 3 is a summary of the device operating modes.

normal sampling mode

Figure 11(a) and Figure 11(b) show the timing of signals in normal sampling mode for both color and monochrome operation.

In color operation, all three input channels are sampled at the same instant on the first rising edge of MCLK after the VSMP pulse. An internal timing circuit then controls the multiplexing of the three channels to the ADC input in the R,G,B sequence. In this mode, VSMP is applied at the input pixel rate, and ADC conversions are performed at three times the input pixel rate.

For monochrome (single channel) operation, VSMP is again applied at the input pixel rate, however, for monochrome, the ADC is supplied with a continuous stream of samples from a single input channel. Input channel selection in this mode is achieved through the serial interface.

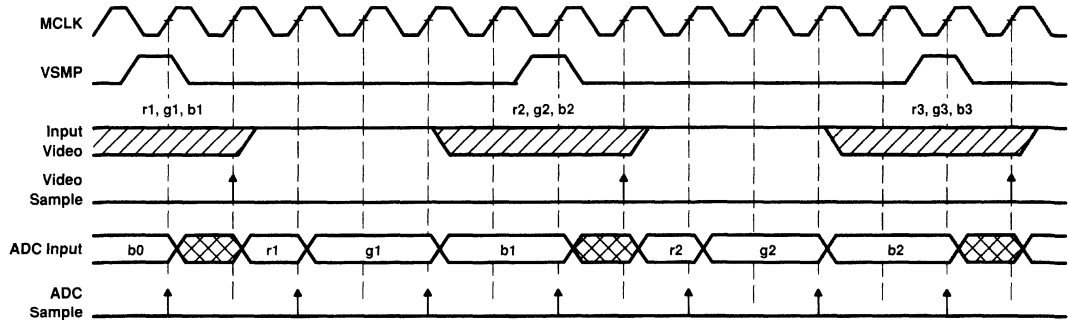
In both color and monochrome operation, a simple external delay circuit can be used to align the video data with the sampling instant, provided that the CCD clocks are generated from MCLK. Detailed timings for both cases are shown in Figures 3 and 4.

Table 3. Mode Summary

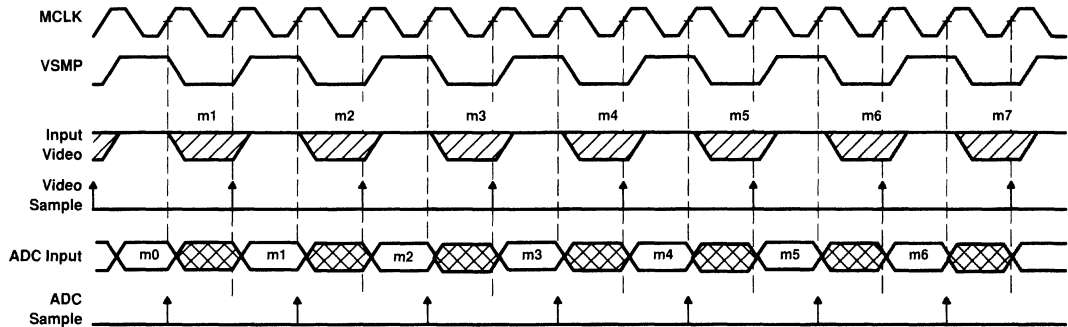
MODE	DESCRIPTION	CDS AVAILABLE	MAX SAMPLE RATE	SENSOR INTERFACE DESCRIPTION	TIMING REQUIREMENTS	REGISTER CONTENTS WITH CDS†	REGISTER CONTENTS WITHOUT CDS†
1	Color	Yes	2 MSPS	The three input channels (R, G, B) are sampled in parallel at 2 MSPS maximum. The sampled data is multiplexed into a single data stream before the internal ADC, giving an internal serial data rate of maximum 6 MSPS.	MCLK max: 12 Mhz MCLK: VSMP ratio is 6:1	Setup register 1: Word 1: 00h Word 2: 81h	Setup register 1: Word 1: 00h Word 2: 80h
2	Monochrome	Yes	2 MSPS	One input channel is continuously sampled. The internal multiplexer is held in one position under control of the user.	Identical to mode 1	Setup register 1: Word 1: 00h Word 2: 91h Setup register 2: Word 2: bits b(1,0) define which channel to be sampled	Setup register 1: Word 1: 00h Word 2: 90h Setup register 2: Word 2: bits b(1,0) define which channel to be sampled
3	Fast monochrome	Yes	4 MSPS	Identical to mode 2	MCLK max: 12 MHz MCLK: VSMP ratio is 3:1	Identical to mode 2 plus Setup register 2: Word 1: bits b(1,0) must be set to 00h	Identical to mode 2
4	Max speed monochrome	No	6 MSPS	Identical to mode 2	MCLK max: 12 MHz MCLK: VSMP ratio is 2:1	Not supported	Setup register 1: 5Dh Setup register 2: Word 2: bits b(1,0) define which channel to be sampled

† Only indicates relevant register bits.

PRINCIPLES OF OPERATION



(a) COLOR OPERATION



(b) MONOCHROME OPERATION

Figure 11. Normal Mode Input Timing

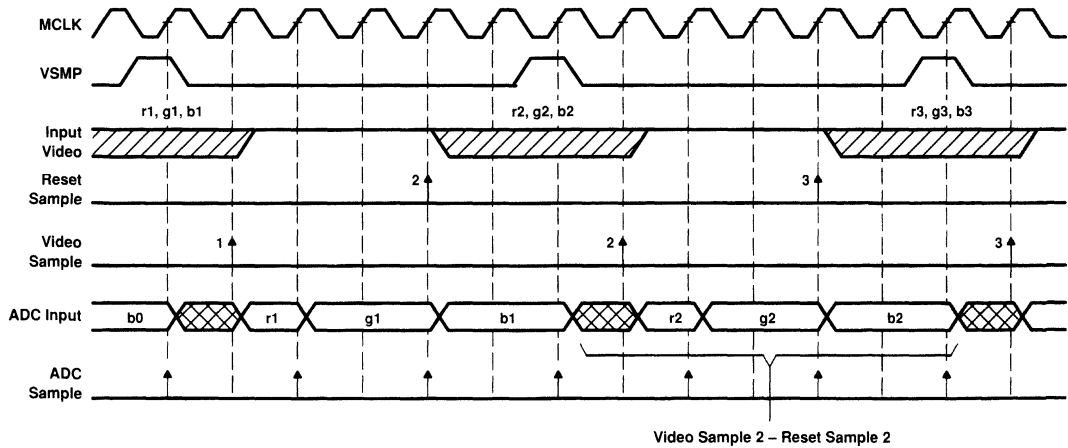


Figure 12. CDS Mode Input Timing

PRINCIPLES OF OPERATION

correlated double sampling

Correlated double sampling is a circuit technique for reducing any correlated noise between the reset (black) level and the video level of the CCD array. Referring to the block diagram shown in Figure 13(a), a sample of the CCD output is taken and held at the reset level and another sample is taken and held at the video level. These two levels are subtracted essentially nulling any common signal, and thereby minimizing the correlated noise that exists at both the reset level and the video level. Figure 13(b) shows relative timing.

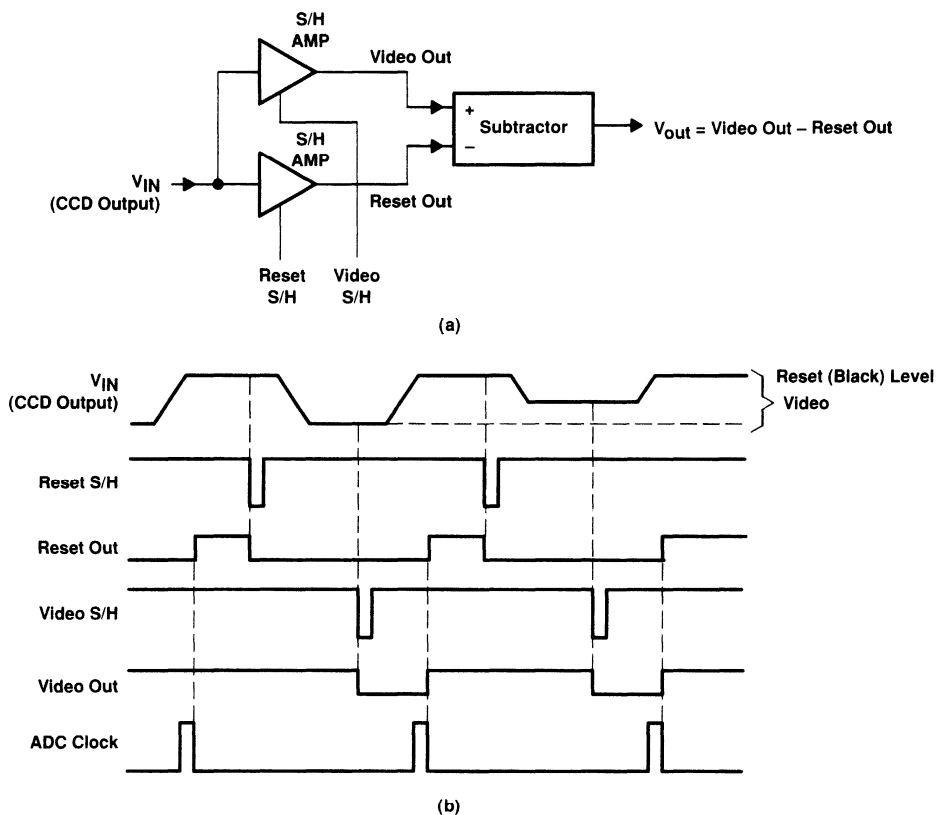


Figure 13. Simplified Correlated Double Sampling

correlated double sampling mode

In CDS mode, two samples are taken per channel within each pixel period. Figure 12 shows the timing diagram for this mode of operation. The video signal is sampled during the reset phase and during the video information with timing defined relative to the VSMP input. The difference between these two samples forms the input to the ADC. The relative timing of the reset and video samples shown in Figure 12 is the default (post-reset) condition. The timing of the reset sample relative to the video sample can be advanced by one or retarded by one or two MCLK periods under control of the serial interface. Figure 1 shows a detailed video input timing diagram with all four CDS timing options.

PRINCIPLES OF OPERATION***correlated double sampling mode (continued)***

To perform CDS input sampling, the device should be set up in single-ended mode with the differential inputs of each channel (xINP, xINN) connected together to the video input signal.

For positive going input signals, i.e., white signal level greater than the reset level, the offset DACs should be set to the maximum negative value (DAC code 1FF hex). This configuration sets the zero signal level (video input equal to the reset level) at the ADC zero-scale code transition. Increasing the DAC code towards zero moves the zero signal level up from the ADC zero-scale code transition. For negative-going input signals, i.e., white signal level less than the reset level, the DACs should be set to the maximum positive value (DAC code 0FF hex). This configuration sets the zero signal level at the ADC full-scale code transition. The polarity of the ADC output signal can be inverted under control of the serial interface data.

The multiplexing shown in Figure 12 refers to color operation, however the same overall timing scheme applies to monochrome CDS operation, in that a single input sample is applied to the ADC per VSMP period. Thus the maximum sampling rate in monochrome CDS mode is limited to one third of the maximum rate achievable in normal monochrome sampling mode.

digital image processing

The digital image processing functions following the ADC as shown in the functional block diagram include the following:

- DC restore: This allows fine adjustment of the dc video level at the ADC output with adjustment values being programmed through the serial interface.
- Pixel-by-pixel offset compensation: This uses offset coefficients that are either externally supplied at the multiplexed channel rate or supplied from internal default registers whose values are programmed through the serial interface.
- Compensation for pixel-by-pixel shading curve nonuniformity and photo response nonuniformity within the sensor: Coefficients are externally supplied at the multiplexed channel rate. Default registers are provided for use during calibration.
- Global offset adjust: Offset adjust over the whole scan for each channel to give brightness control. Values are programmed through the serial interface.
- Global gain adjust: Independent gain adjust over the whole scan for each channel to give contrast and color balance control. Gain values are programmed through the serial interface.
- Programmable output word length selection: The output word length can be programmed to 8, 10, 12, or 16 bits through the serial interface.
- Programmable threshold detector with independent thresholds for each channel.

Global adjustments are implemented after the pixel-by-pixel compensations allowing calibrations and modifications in operational use without having to recalibrate the pixel-by-pixel factors.

DC restore

The dc restore block is used for fine adjustment of the dc signal level at the ADC output by adding a value stored in an internal register. Separate level adjust registers are provided for each channel (color) with multiplexing between channels controlled internally. The level adjust registers are programmed through the serial interface as 12-bit 2s complement numbers with a range of ± 0.5 of the ADC full scale, allowing 1-bit resolution in adjustment of the ADC output. The dc adjustment registers are reset to zero.

PRINCIPLES OF OPERATION

pixel offset compensation

The output of the dc restore circuit is passed to an adder which performs pixel-by-pixel offset compensation. Compensation values can either be supplied externally at the multiplexed pixel rate, allowing different correction values for each pixel in the array, or supplied from internal default values programmed through the serial bus. Selection between the two sources is controlled through the serial bus. Two sets of internal default registers are provided to allow correction values to be stored internally for use on even and odd pixels with selection between the two sets under control of the ONE terminal (ONE low for even registers, ONE high for odd registers). This feature allows correction of differing dc offsets output on even and odd pixels, which occur in some CCD sensors, using internally stored data.

Pixel offset correction values are input or stored as 12-bit 2s complement numbers. Programmable internal scaling is provided which allows the offset correction factors to cover ± 0.5 , ± 0.25 , ± 0.125 , or ± 0.0625 of the ADC full-scale range. The internal pixel correction registers are reset to zero.

pixel shading compensation

This stage is implemented as a digital multiplier which corrects for nonuniform shading using externally supplied 12-bit unsigned values. The external correction factors are supplied at the multiplexed pixel rate. The external correction range is from 0 to 4, which allows shading nonuniformity of up to 75% (i.e., the minimum input signal is 25% of the peak) to be corrected without loss of resolution in the high gain pixels at the center of the scan. Internal default registers are provided to set the gain through this block during calibration. The internal registers default to a value of 1 (equivalent to decimal 1024 in this range) on reset.

global offset adjust

Global offset adjust is provided by an adder using three independent bipolar offset coefficients set through the serial interface. A range of ± 4 times the ADC full-scale range in steps of a half output LSB is provided. This range allows the output signal to be shifted across the entire range of the 16-bit output bus. The global offset coefficients are programmed as 16-bit 2s complement numbers, which default to zero on reset.

global gain adjust

Global gain adjust is provided by a multiplier using gain values set through the serial interface. Three independent 16-bit gain values with a range of 0 to 2 are stored (one for each channel). The default value of the global gain coefficients is 1 (equivalent to decimal 32768 in this range).

threshold detector

The threshold detector operates on the output signal from the global gain adjust stage, comparing the signal to individual threshold levels for each color channel, which are programmed through the serial interface. If the signal exceeds the threshold, the DETOP terminal is forced high. Two basic modes of operation can be programmed, either multiplexing between the three channels in sequence with the internal data, or operating continuously on one of the three channels. The input signals to the threshold detector are represented as 16-bit bipolar 2s complement numbers. Threshold values should be programmed as 15-bit unipolar numbers in the range 0 to 32767.

effect of image processing on ADC output

The combined effect of the image processing sections on the ADC output is summarized by the formula in the note following Table 4. All values are shown in decimal. Examples of the process are given in Table 4. Examples 1–8 show the results with no pixel offset scaling. Examples 9–11 show the added effect of pixel offset scaling. All examples use a half range ADC value (2048) for the ADC output (ADCOP).

If defaults are used throughout, then the output of the ADC is output directly on the OP0–OP11 bus as listed in Table 4, example 1.

PRINCIPLES OF OPERATION

effect of image processing on ADC output (continued)

In Table 4, example 2 shows how the half range ADCOP value (2048) is affected by adding dc restoration (value 128). This value is added directly to the ADCOP value. All other parameters are default, so this result passes directly to the OP0–OP11 output. Inserting the values in the formula gives:

$$OP0-OP11 = (((2048 + 128 + (0 \times 1)) \times 1) + (0.5 \times 0)) \times 1$$

In Table 4, example 9 shows the effect of internal scaling (POSCL) on the pixel offset compensation (POC). The value 01 on POSCL indicates a scaling factor of 0.5 (refer to Table 5, setup register 2). The POC value of 128 is multiplied by 0.5. The result is added to the ADC output. Defaults have been used on all other stages, so the resulting value of 2048 is directly output on OP0–OP11. Examples 10 and 11 show the effect of different scaling factors. Inserting the values in the formula gives:

$$OP0-OP11 = (((2048 + 0 + (128 \times 0.5)) \times 1) + (0.5 \times 0)) \times 1$$

Table 4. Examples of Image Processing on ADC Output

PARAMETER	ADCOP	DCREST	POC	POSCL	PCS	GLOBAL OFFSET	GLOBAL GAIN	OP0–OP11
Range	0 to 4095	-2048 to 2047	-2048 to 2047		0 to 4095	-32768 to 32767	0 to 65536	0 to 4095
Default		0	0	00	1024	0	32768	
Example 1	2048	0	0	00	1024	0	32768	2048
Example 2	2048	128	0	00	1024	0	32768	2176
Example 3	2048	0	-256	00	1024	0	32768	1792
Example 4	2048	0	0	00	512	0	32768	1024
Example 5	2048	-64	128	00	1536	0	32768	3168
Example 6	2048	0	0	00	1024	1024	32768	2560
Example 7	2048	0	0	00	1024	0	16384	1024
Example 8	2048	-64	128	00	512	1024	16384	784
Example 9	2048	0	128	01	1024	0	32768	2112
Example 10	2048	0	128	10	1024	0	32768	2080
Example 11	2048	0	128	11	1024	0	32768	2064

NOTE:

$$OP0-OP11 = (((ADCOP + DCREST + (POC \times POSCL)) \times PSC) + (0.5 \times \text{Global Offset})) \times \text{Global Gain}$$

where:

- ADCOP 12-bit output of the ADC
- DCREST 2s complement 12-bit number source directly from the DC restore registers
- POC 2s complement 12-bit number source directly from the POC bus or registers
- POSCL scaling factor as defined in Table 5 setup register 2
- PSC 12-bit unsigned number sourced from the PSC bus or register and divided by 1024
- Global Offset 16-bit 2s complement number sourced directly from the global offset adjust registers
- Global Gain 16-bit unsigned number sourced from the global gain register and divided by 32768
- OP0–OP11 12-bit result of the image processing that is output from the device on the bus OP0–OP15



PRINCIPLES OF OPERATION

output word length select

This block is used to define the output word length, which can be programmed to 8, 10, 12, or 16 bits through the serial interface. An internal clip function is provided that can be used in unipolar or bipolar fashion. For example, if an 8-bit output word length is selected, the output data on OP0 – OP15 is limited to the range 0 to 255 for unipolar clipping or – 128 to 127 for bipolar clipping. If the signal to this block exceeds the positive clip level, the ORNG signal is forced high. In 8-, 10-, and 12-bit output modes, the output data bit OP15 functions as an under range flag; i.e., it is driven high if the input signal is less than the negative clip level. OP15 also functions as an under range signal in 16-bit unipolar clipping mode.

serial interface

The serial interface data is used to configure the device operation and to program internal data registers. Figure 14 shows a timing diagram of a serial write operation. A serial data stream applied to the SDI terminal is clocked into the device on the rising edge of SCK. The data stream comprises 6 address bits and two 8-bit data words. When this data has is shifted into the device, a pulse applied to SEN transfers the data to the appropriate internal register.

Tables 5 and 6 define the internal register map for the device and control bit functionality, respectively. The first 4 addresses in Table 5 (address bit a5 = 0) are used to program setup registers and to provide a software reset feature. The remaining eight entries in Table 5 define the address locations of internal data registers, and three additional subaddresses are defined for the red, green, or blue registers. Address bits a1 and a0 select between the red, green, and blue registers, as defined in Table 5. When a1 and a0 are set to 1, all three registers are updated to the same date value, as specified in data words 1 and 2. Blank entries in Table 5 are taken as don't care values.

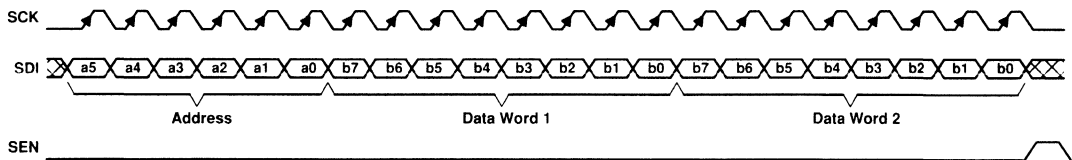


Figure 14. Serial Interface Timing

system timing

System timing diagrams that relate the timing between taking an input sample, applying the related pixel offset and shading coefficients, and the output of the digital video data are shown in Figures 1 and 2. These diagrams show the overall latency of the device in both color and monochrome operating modes. Detailed digital timing diagrams are shown in Figure 15, 16, and 17.

TLC8044
12-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS

SLAS128 – JUNE 1997

PRINCIPLES OF OPERATION

Table 5. Serial Interface Register Map

ADDRESS <a5...a0>	DESCRIPTION	DATA WORD	BIT							
			b7	b6	b5	b4	b3	b2	b1	b0
000000	Setup register 1	1 2	ENADC	BICLIP	ADCMX	MONO	DEFPG	DEFPO	DNS	INVADC CDS
000001	Setup register 2	1 2	POSCL1	POSCL0	WLSEL1	WLSEL0	THSEL1	THSEL0	CDSREF1 CHAN1	CDSREF0 CHAN0
000010	Reserved	1 2								
000011	Software reset	1 2								
1000xx	DAC values	1 2	D7	D6	D5	D4	D3	D2	D1	POL D0(LSB)
1001xx	DC restore values	1 2	D7	D6	D5	D4	D11(MSB) D3	D10 D2	D9 D1	D8 D0(LSB)
1010xx	Default even pixel offsets	1 2	D7	D6	D5	D4	D11(MSB) D3	D10 D2	D9 D1	D8 D0(LSB)
1011xx	Default odd pixel offsets	1 2	D7	D6	D5	D4	D11(MSB) D3	D10 D2	D9 D1	D8 D0(LSB)
1100xx	Default pixel gains	1 2	D7	D6	D5	D4	D11(MSB) D3	D10 D2	D9 D1	D8 D0(LSB)
1101xx	Global offsets	1 2	D15(MSB) D7	D14 D6	D13 D5	D12 D4	D11 D3	D10 D2	D9 D1	D8 D0(LSB)
1110xx	Global gains	1 2	D15(MSB) D7	D14 D6	D13 D5	D12 D4	D11 D3	D10 D2	D9 D1	D8 D0(LSB)
1111xx	Threshold values	1 2	D7	D14(MSB) D6	D13 D5	D12 D4	D11 D3	D10 D2	D9 D1	D8 D0(LSB)

xx		ADDRESS LSB DECODE†	DEFAULT PIXEL DECODE‡
a1	a0		
0	0	Red register	Blue register
0	1	Green register	Red register
1	0	Blue register	Green register
1	1	Red, green, and blue	Red, green, and blue

† Default address

‡ The address decoding is applicable for default pixel gain in monochrome mode.



TLC8044
12-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS

SLAS128 – JUNE 1997

PRINCIPLES OF OPERATION

Table 6. Control Bit Descriptions

REGISTER	BITS	DEFAULT	DESCRIPTION
Setup Register 1	ENADC	1	ADC standby control: 0 = standby 1 = active
	BICLIP	0	Bipolar clip enable: 0 = unipolar clip 1 = bipolar clip
	ADCMX	0	ADC MUX control: 0 = normal operation 1 = ADC output multiplexed to OP
	MONO	0	Mono/color select: 0 = color operation 1 = monochrome operation
	DEFPG	0	Select default pixel gain: 0 = external pixel gain 1 = default (internal)
	DEFPO	0	Select default pixel offsets: 0 = external pixel offsets 1 = default (internal)
	DNS	0	Select differential/single-ended mode: 0 = single ended 1 = differential
	INVADC	0	ADC output polarity: 0 = noninverted 1 = inverted
	CDS	0	Select correlated double sampling mode: 0 = normal sampling 1 = CDS mode
Setup Register 2	POSCL1, 0	00	Pixel offset scaling: 00 = $\pm 0.5 f_S$ 01 = $\pm 0.25 f_S$ 10 = $\pm 0.125 f_S$ 11 = $\pm 0.0625 f_S$
	WLSEL1, 0	10	Output word length select: 00 = 8 bits (OP0 - OP7 contains output word) 01 = 10 bits (OP0 - OP9 contains output word) 10 = 12 bits (OP0 - OP11 contains output word) 11 = 16 bits (OP0 - OP15 contains output word)
	THSEL1, 0	11	Threshold detector operating mode: 00 = Operating on red channel only 01 = Operating on green channel only 10 = Operating on blue channel only 11 = Three channel
	CDSREF1, 0	01	CDS mode reset timing adjust: 00 = Advance 1 MCLK period 01 = Normal 10 = Retard 1 MCLK period 11 = Retard 2 MCLK periods
	CHAN1, 0	00	Monochrome mode channel select: 00 = Red channel 01 = Green channel 10 = Blue channel 11 = Not used



TLC8044
12-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
 SLAS128 – JUNE 1997

PRINCIPLES OF OPERATION

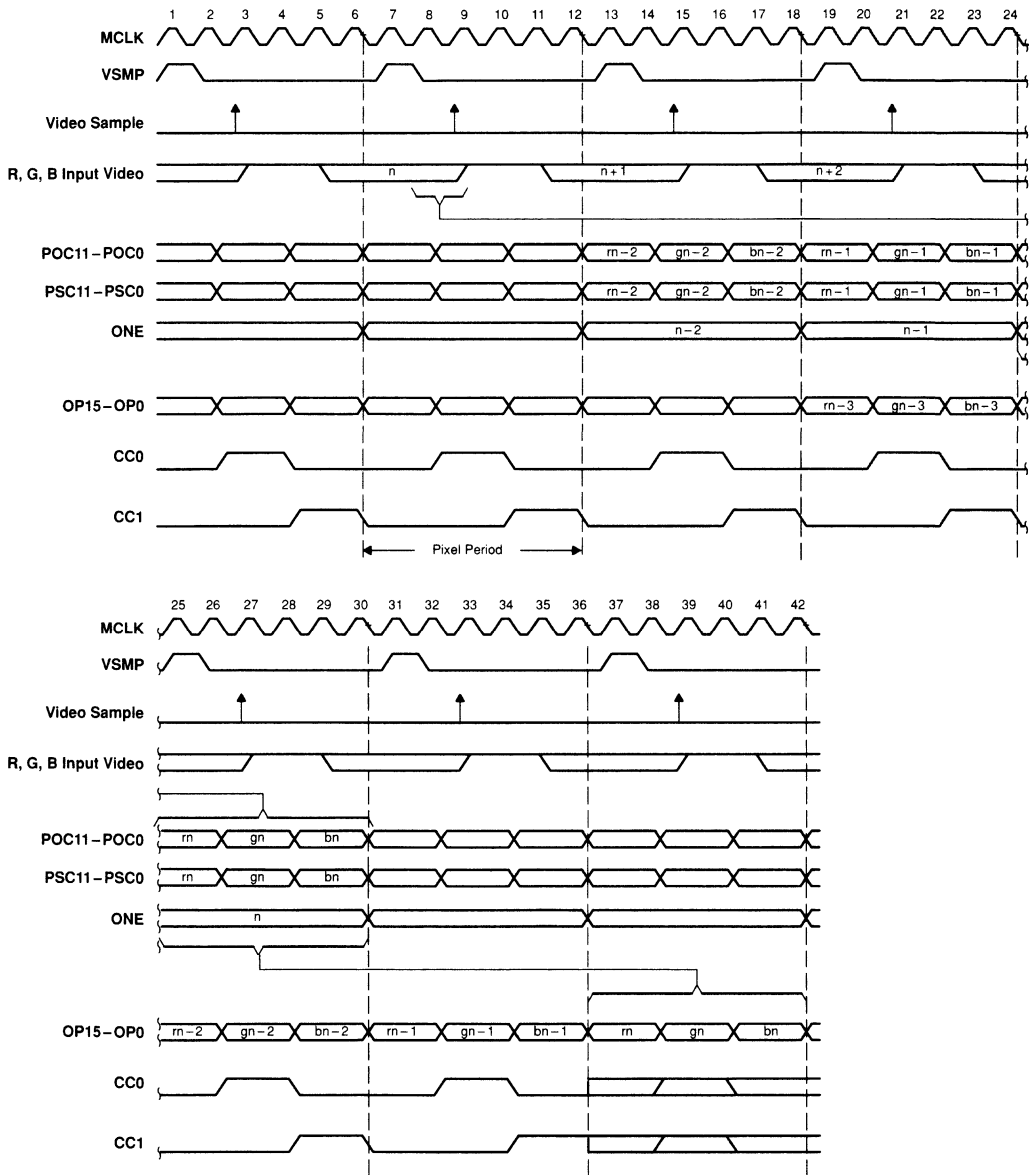
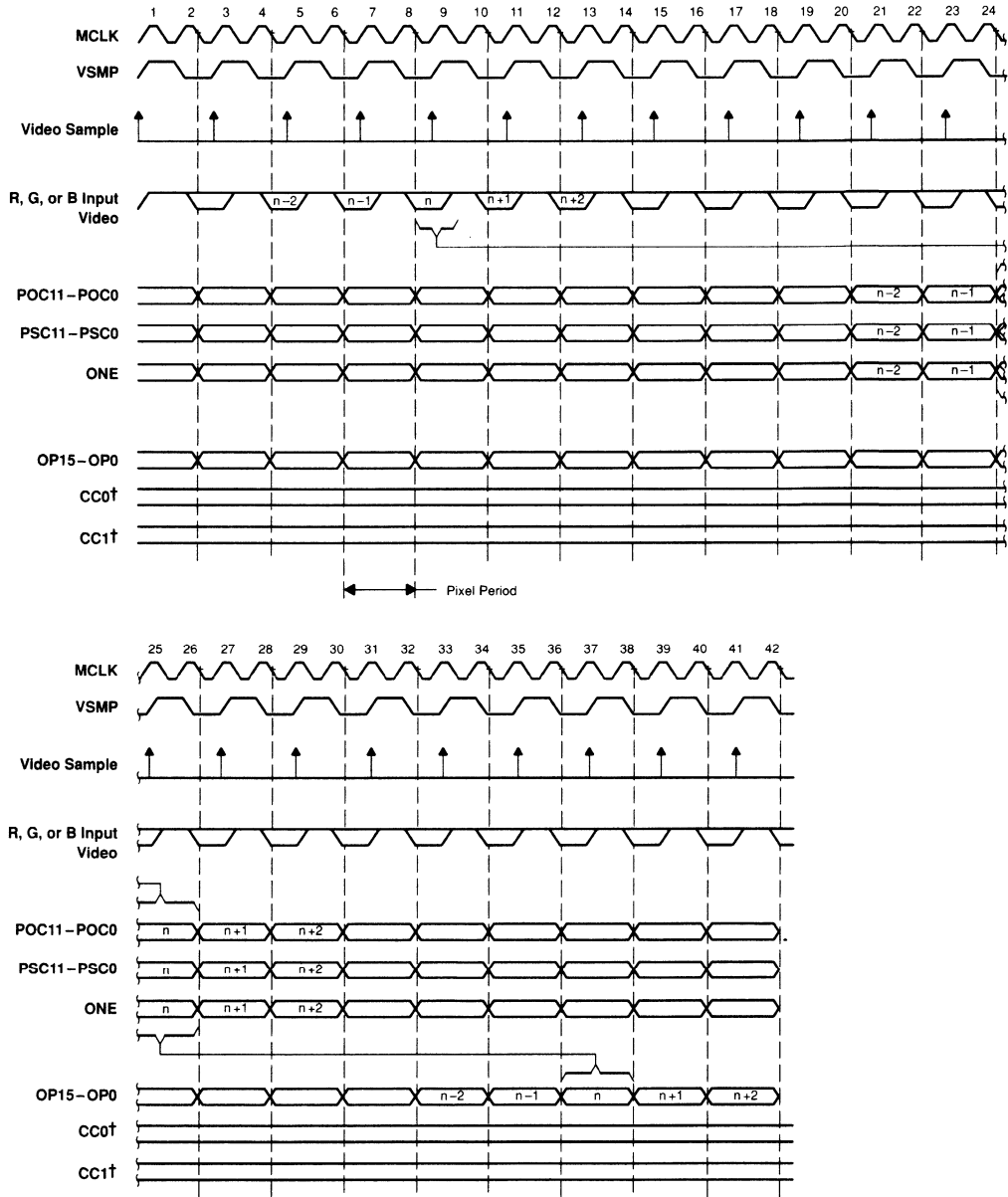


Figure 15. System Timing – Color Mode

TLC8044
12-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
SLAS128 – JUNE 1997

PRINCIPLES OF OPERATION



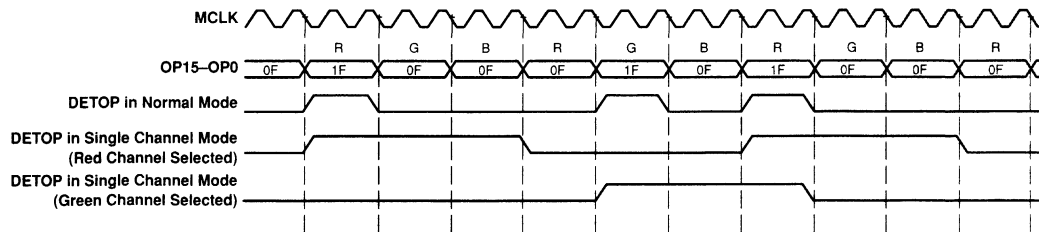
† The CC(10) output state is defined via the serial bus in monochrome mode.

Figure 16. System Timing – Monochrome Mode



TLC8044
12-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
 SLAS128 – JUNE 1997

PRINCIPLES OF OPERATION



NOTE A: All thresholds are set to 10 hex.

Figure 17. Timing of Threshold Detector Output DETOP

APPLICATION INFORMATION

running the TLC8044 at 4-megasamples/sec in CDS monochrome mode

The TLC8044 can be set up to provide a 4-megasample/sec throughput when in CDS monochrome mode; however, the VSMP input must run continuously at 4 MHz.

The following paragraphs describe operation of the TLC8044 in monochrome mode (sampling one channel only). The maximum sample rate in color CDS mode is 2-megasamples/channel/sec.

In CDS mode, the video signal is sampled both during the reset phase and when video information is present with timing defined to a VSMP input. The difference between these two samples forms the input to the ADC. In monochrome mode, all samples are taken from one input video channel. The device is set up as listed in Table 6. See Tables 4 and 5 for offset DAC values in CDS mode.

System timing is shown in Figure 18. MCLK clocks the device at 12 MHz (as normal). VSMP, which controls the sample rate, is run at 4 MHz. A reset sample is taken on the rising edge of MCLK after VSMP is asserted. The corresponding video sample is taken on the next MCLK rising edge. Compensation coefficients (pixel offset and pixel shading) are sampled on the falling edge of MCLK 26.5 periods after the initial reset sample. The processed digital outputs appear on OP0–OP15 41.5 MCLK periods after the initial reset sample.

In Figure 18 the system timing diagram shows a negative-going video sample. The polarity of the ADC output signal can be inverted under control of the serial interface. Setup and hold times are specified in the recommended operating conditions table.

Table 7. Relevant Register Settings

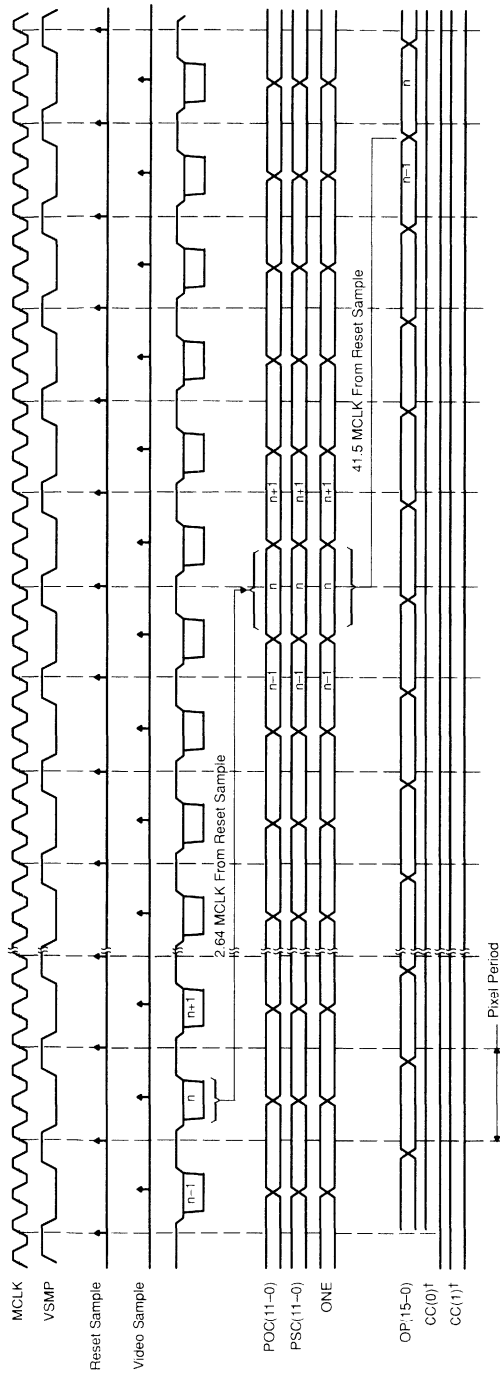
REGISTER	BITS	VALUE†	DESCRIPTION
Setup register 1	ENADC	U	ADC standby control
	BICLIP	U	Select unipolar clip
	ADCMX	0	ADC MUX control
	MONO	1	Monochrome operation
	DEFPG	U	Select default pixel gain
	DEFPO	U	Select default pixel offsets
	DNS	0	Select single-ended mode
	INVADC	U	ADC output polarity
Setup register 2	CDS	1	Select correlated double sampling mode
	POSCL1,0	UU	Pixel offset scaling
	WLSEL1,0	UU	Select 12-bit output word
	THSEL1,0	UU	Three channel
	CDSREF1,0	00	Advance one MCLK period
CHAN1,0	UU	Select channel to be sampled	

† U = User defined

TLC8044

12-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS

SLAS128 – JUNE 1997



† CC(1,0) Output state defined via serial bus in monochrome mode

Figure 18. System Timing – CDS Mode at 4-Megasamples/Sec

TLC8144

10-BIT ANALOG-TO-DIGITAL INTERFACE FOR CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS

SLAS158 – MAY 1997

features

- Reset Level Clamp
- Correlated Double Sampling (CDS)
- Fine Offset Level Shifting
- Programmable Gain Amplification
- 10-Bit ADC With Maximum 6 MSPS
- Digital Post-Processing for Pixel-By-Pixel Image
- Simple Clocking Scheme
- Control by Serial or Parallel Interface
- Hardware Compatible With Extended Parallel Port (EPP)
- 48-Pin QFP Package

applications

- Document Scanners
- CCD Sensor Interfaces
- Contact Image Sensor (CIS) Interfaces

description

The TLC8144 integrates the analog signal conditioning required by CCD sensors with a 10-bit ADC and optional pixel-by-pixel image compensation requiring minimal external circuitry and provides a cost effective, sensor-to-digital domain system solution.

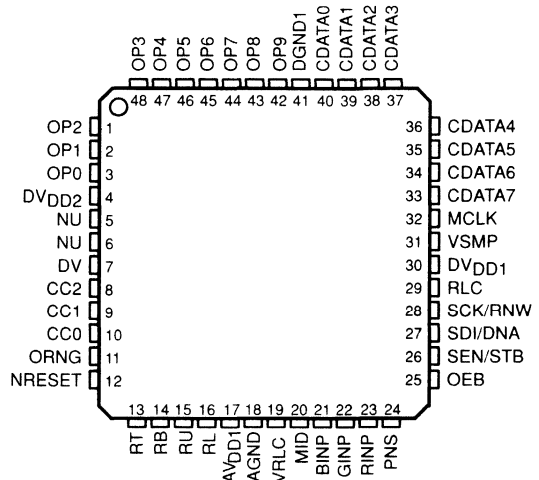
Each analog conditioning channel provides reset level clamp, CDS, fine offset level shifting, and gain amplification. The three channels are multiplexed into the ADC. Output from the ADC can either be direct or passed through a digital post-processing function. The post-processing provides compensation for variations in offset and luminance on a pixel-by-pixel basis.

The flexible output architecture allows 10-bit data to be accessed either on a 10-bit bus or a time-multiplexed 8-bit bus. The TLC8144 can be configured for pixel-by-pixel or line-by-line multiplexing operation. Reset level clamp and/or CDS features can be optionally bypassed. Device configuration is either by a simple serial or 8-bit parallel interface. The TLC8144 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T _A	PACKAGE
	0°C to 70°C

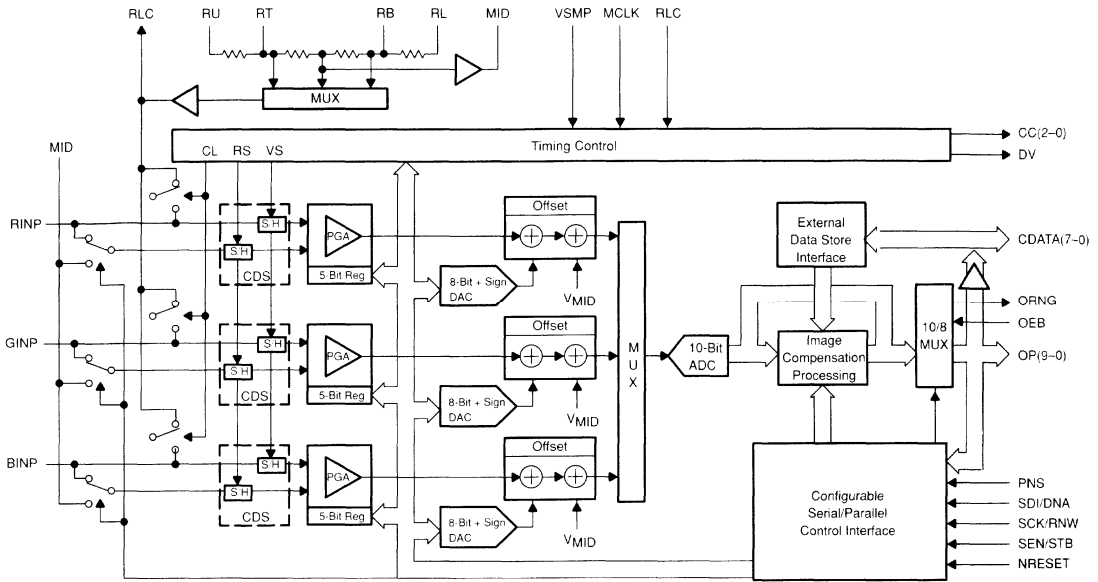
PT PACKAGE
(TOP VIEW)



NU – Make no external connection.

TLC8144
10-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
 SLAS158 – MAY 1997

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	18	I Analog supply	Analog ground (0 V)
AVDD1	17	I Analog supply	Positive analog supply (5 V)
BINP	21	I Analog	Blue channel input video
CC(2-0)	8, 9, 10	O Digital	Color code outputs. These outputs indicate from which channel the current output sample was taken. (R = 00X, G = 01X, B = 10X). Two codes are provided per channel.
CDATA(7-0)	33-40	I Digital	Image compensation data read/write at twice the ADC conversion rate
DGND1	41	I Digital supply	Digital ground (0 V)
DV	7	O Digital	Data valid output, active low
DVDD1, 2	30, 4	I Digital supply	Positive digital supply (5 V)
GINP	22	I Analog	Green channel input video

TLC8144
10-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
SLAS158 – MAY 1997

Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
MCLK	32	I Digital	Master clock. This clock is applied at either six, four, or two times the input pixel rate depending on the operational mode. MCLK is divided by two internally to define the ADC sample rate, and to provide the clock source for the digital logic.
MID	20	O Analog	Buffered midpoint of ADC reference string. Used internally to set DAC reference voltages.
NC	5, 6	Unused	These terminals must be left unconnected.
NRESET	12	I Digital	Reset input, active low. This signal forces a reset of all internal registers in the device.
OEB	25	I Digital	Output 3-state control. All outputs enabled when OEB = 0.
OP(9-0)	42-48, 1-3	I Digital I Digital	3-state digital 10-bit bidirection bus. There are four modes: 3-state: when OEB = 1 Output 10 bit: 10-bit data output from bus Output 8-bit multiplexed: data output on bits OP(9-2) at twice pixel rate Input 8 bit: control data input on bits OP(9-2)
ORNG	11	O Digital	Over-range signal, active high. This signal indicates that the current output pixel has exceeded the maximum or minimum achievable value somewhere within the pixel processing.
PNS	24	I Digital	Control interface select, parallel (high) or serial (low, default)
RINP	23	I Analog	Red channel input video
RLC	29	I Digital	Selects whether reset level clamp is applied on a pixel-by-pixel basis. If RLC is required on each pixel, then this terminal can be tied high.
RU, RT, RB, RL	15, 13, 14, 16	I Analog	ADC reference voltages. The ADC reference range is applied between V_{RT} (full scale) and V_{RB} (zero level). V_{RU} and V_{RL} can be used to derive optimum reference voltages from an external 5-V reference.
SCK/RNW	28	I Digital	Serial interface: serial interface clock signal Parallel interface: high = OP(9-2) is output, low = OP(9-2) is input bus
SDI/DNA	27	I Digital	Serial interface: serial interface input data signal Parallel interface: high = data, low = address
SEN/STB	26	I Digital	Serial interface: enable, active high Parallel interface: strobe, active low
VRLC	19	O Analog	Selectable analog output voltage for RLC
VSMP	31	I Digital	Video sample synchronization pulse. This signal is applied synchronously with MCLK to specify the point in time that the input is sampled. The timing of internal multiplexing between the R, G, and B channels is derived from this signal.



TLC8144
10-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
 SLAS158 – MAY 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, from DV _{DD1} , DV _{DD2} , and AV _{DD1} (see Note 1)	7 V
Digital inputs (see Note 1)	-0.3 V to V _{DD} + 0.3 V
Analog inputs (see Note 1)	-0.3 V to V _{CC} + 0.3 V
Digital outputs, maximum external voltage applied (see Note 1)	-0.3 V to V _{CC} + 0.3 V
Reference input (see Note 1)	-0.3 V to V _{DD} + 0.3 V
Operating temperature range, T _A	0°C to 70°C
Storage temperature range, T _{stg}	-50°C to 150°C
Lead temperature, soldering, 10 sec	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the corresponding DGND or AGND terminal.

recommended operating conditions

total device

	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	4.75		5.25	V

digital inputs

	MIN	NOM	MAX	UNIT
High-level input voltage, V _{IH}	0.8 V _{DD}			V
Low-level input voltage, V _{IL}			0.2 V _{DD}	V

timing requirements

input multiplexer

	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Setup time, input video before MCLK↑, t _{su(V)}		10			ns
Hold time, input video after MCLK↑, t _{h(V)}		25			ns
Setup time, reset video before MCLK↑, t _{su(R)}	CDS mode only	10			ns
Hold time, reset video after MCLK↑, t _{h(R)}	CDS mode only	25			ns

TLC8144
10-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
SLAS158 – MAY 1997

timing requirements (continued)

serial interface

	MIN	NOM	MAX	UNIT
Cycle time, MCLK, t_{cyc1}	83.3			ns
Pulse duration, MCLK high, $t_{w1}(MCLKH)$	37.5			ns
Pulse duration, MCLK low, $t_{w2}(MCLKL)$	37.5			ns
Setup time, CDATA to MCLK↓	10			ns
Hold time, MCLK↓ to CDATA	30			ns
Setup time, VSMP↑ to MCLK↑, $t_{su}(D)$	10			ns
Hold time, MCLK↑ to VSMP↓, $t_h(D)$	10			ns
Cycle time, SCK, t_{cyc2}	83.3			ns
Pulse duration, SCK high, $t_{w3}(SCKH)$	37.5			ns
Pulse duration, SCK low, $t_{w4}(SCKL)$	37.5			ns
Setup time, SDI to SCK↑, $t_{su}(S)$	10			ns
Hold time, SCK↑ to SDI change, $t_h(S)$	10			ns
Setup time, SCK↑ to SEN↑, $t_{su}(SCE)$	20			ns
Setup time, SEN↓ to SCK↑, $t_{su}(SEC)$	20			ns
Pulse duration, SEN high, $t_w(SEN)$	50			ns

electrical characteristics, $V_{DD} = 5\text{ V}$, $GND = 0\text{ V}$, $T_A = \text{full range}$ (unless otherwise noted)

total device

PARAMETER	MIN	TYP	MAX	UNIT
I_{CC} Supply current, active		110	140	mA
I_{CC} Supply current, standby		10	15	mA

digital inputs

PARAMETER	MIN	TYP	MAX	UNIT
I_{IH} High-level input current			1	μA
I_{IL} Low-level input current			1	μA
C_i Input capacitance		10		pF

digital outputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	$I_{OH} = -1\text{ mA}$	$V_{DD} - 0.75$			V
V_{OL} Low-level output voltage	$I_{OL} = 1\text{ mA}$			0.75	V
I_{OZ} High impedance output current				1	μA

input multiplexer

PARAMETER	MIN	TYP	MAX	UNIT
Channel-to-channel gain matching		0.5%	5%	
V_{ICR} Common mode input voltage	0.5		4.5	V



TLC8144
10-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS

SLAS158 – MAY 1997

electrical characteristics, $V_{DD} = 5\text{ V}$, $GND = 0\text{ V}$, $T_A = \text{full range}$ (unless otherwise noted) (continued)

reference string

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z	Impedance, RT to RB		595		1105	Ω
Z	Impedance, RU to RL		1190		2200	Ω
$V_{ref}(RT)$	Reference voltage, top	$V_{I(RU)} = 5\text{ V}$, $V_{I(RL)} = 0\text{ V}$	3.4	3.5	3.6	V
$V_{ref}(RB)$	Reference voltage, bottom	$V_{I(RU)} = 5\text{ V}$, $V_{I(RL)} = 0\text{ V}$	1.4	1.5	1.6	V
$V_{ref}(DAC)$	DAC reference voltage	$V_{I(RU)} = 5\text{ V}$, $V_{I(RL)} = 0\text{ V}$	2.475	2.5	2.525	V

8-bit DACs

PARAMETER		MIN	TYP	MAX	UNIT
Resolution		8			Bits
Zero-scale voltage		$V_{ref}(DAC) - 10$		$V_{ref}(DAC) + 10$	mV
Full-scale voltage error		0		10	mV
Differential nonlinearity (DNL)			0.1	< 1	LSB
Integral nonlinearity (INL)			0.4	1	LSB

10-bit ADC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			10			Bits
f_s	Sampling rate				6	MSPS
Full-scale transition voltage at xINP		Single-ended mode, $V_{I(xINN)} = 2.5\text{ V}$, DAC code = 000H		3.5		V
Zero-scale transition voltage at xINP		Single-ended mode, $V_{I(xINN)} = 2.5\text{ V}$, DAC code = 000H		1.5		V
Differential nonlinearity (DNL)			-1		1	LSB
Integral nonlinearity (INL)			-2		2	LSB

switching characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$t_{pd(D)}$	Propagation delay time, MCLK \downarrow to output valid		25	75	ns
$t_{en(PZE)}$	Enable time, output, OE \downarrow to data valid		25	75	ns
$t_{dis(PEZ)}$	Disable time, output, OE \uparrow to high impedance		10	25	ns

PARAMETER MEASUREMENT INFORMATION

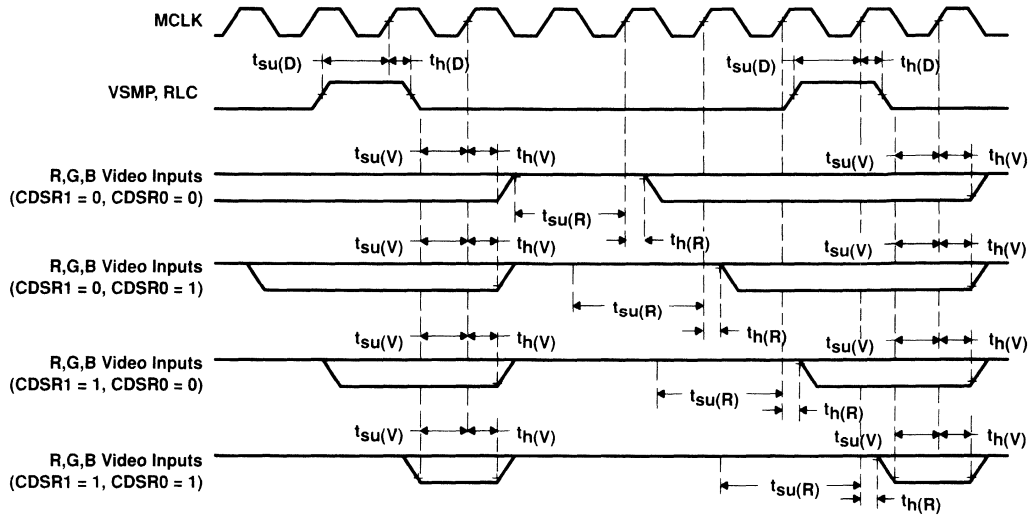


Figure 1. Detailed Video Input Timing – Modes 1 and 2

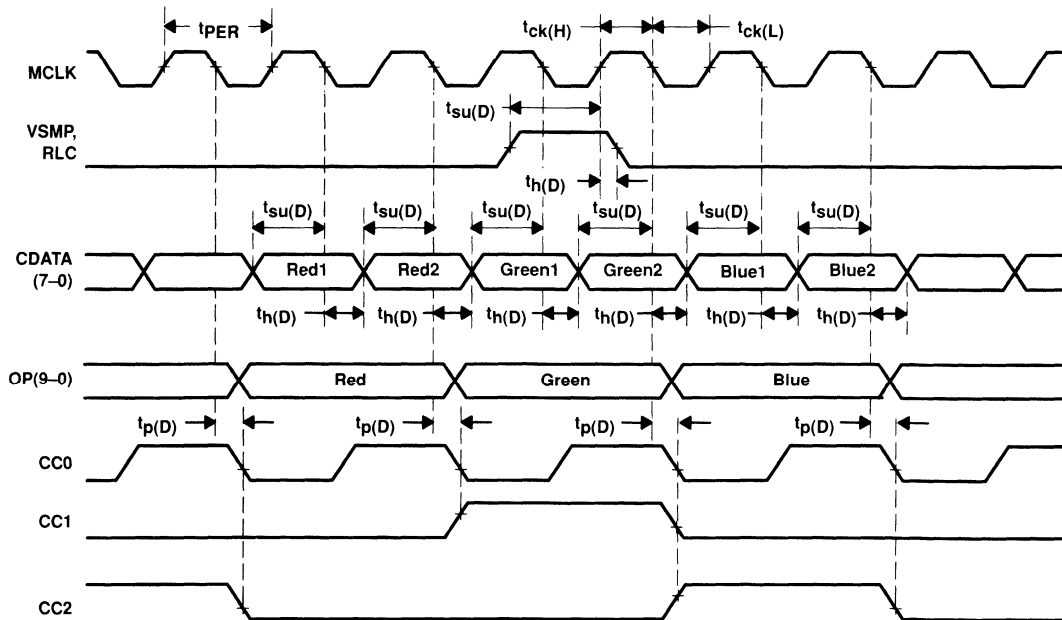


Figure 2. Detailed Digital Timing – Modes 1 and 2

TLC8144
10-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
 SLAS158 – MAY 1997

PARAMETER MEASUREMENT INFORMATION

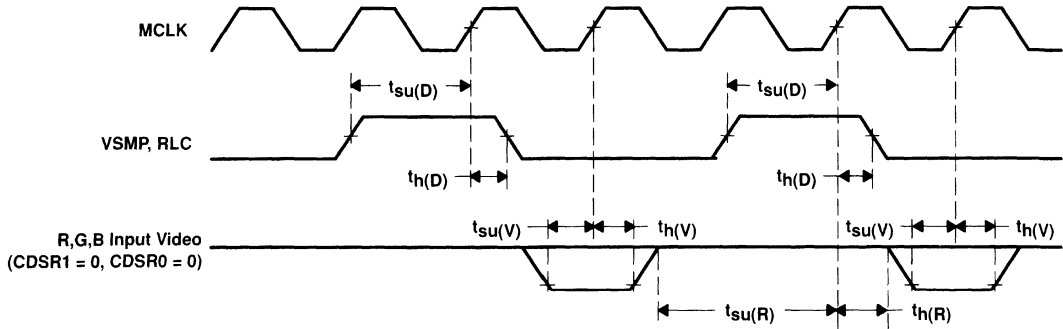


Figure 3. Detailed Video Input Timing – Mode 3

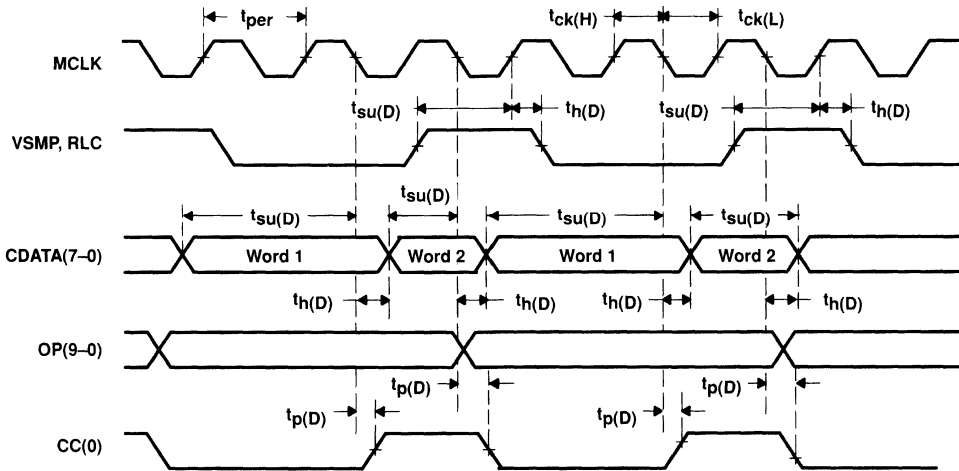


Figure 4. Detailed Digital Timing – Mode 3

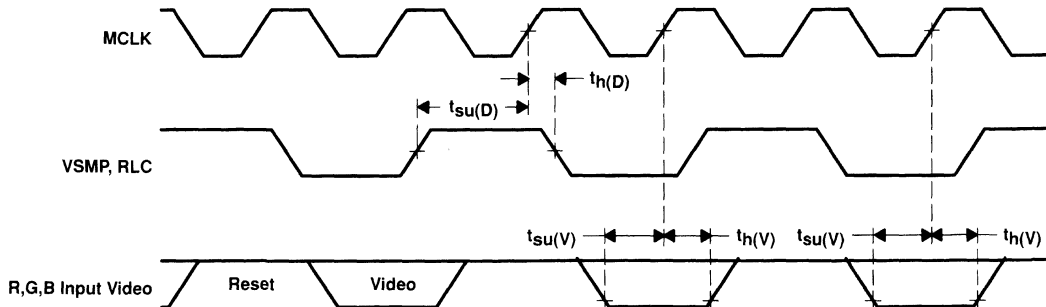


Figure 5. Detailed Video Input Timing – Mode 4

PARAMETER MEASUREMENT INFORMATION

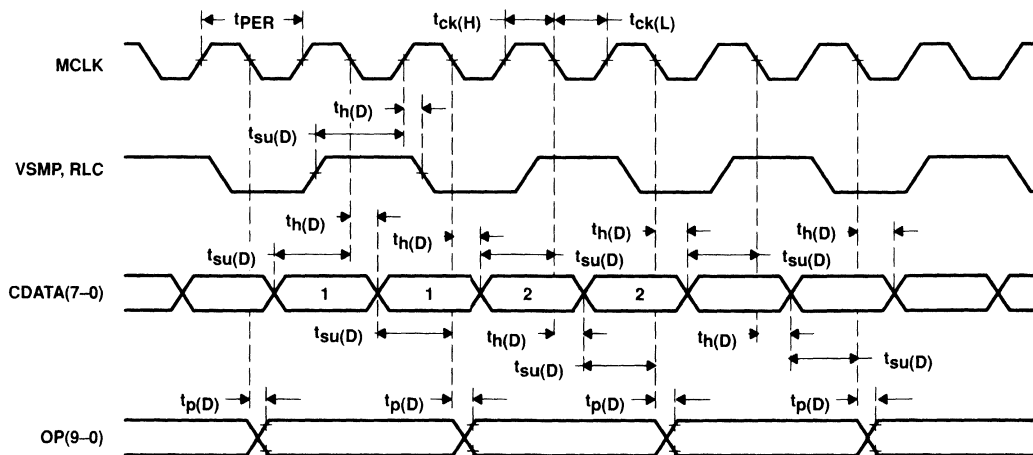


Figure 6. Detailed Digital Timing – Mode 4

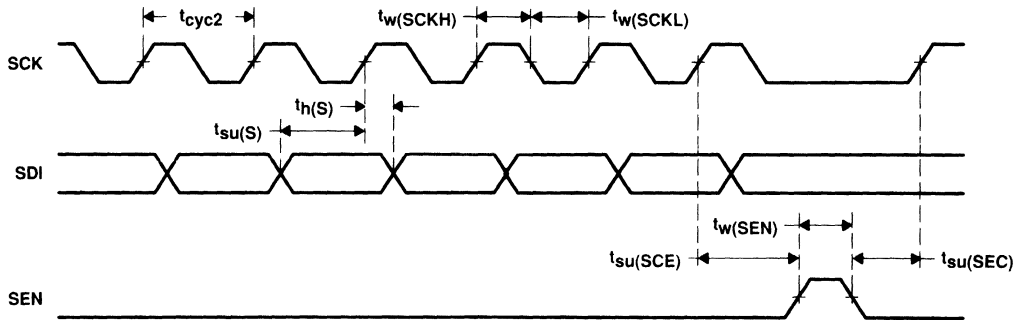


Figure 7. Detailed Timing for Serial Interface

PRINCIPLES OF OPERATION

sample and hold, offset DACs, and programmable gain amplifier

Each analog input (RINP, GINP, BINP) of the TLC8144 consists of a sample and hold (S/H), a programmable gain amplifier (PGA), and a dc offset correction block. The operation of the red input stage is summarized in Figure 8.

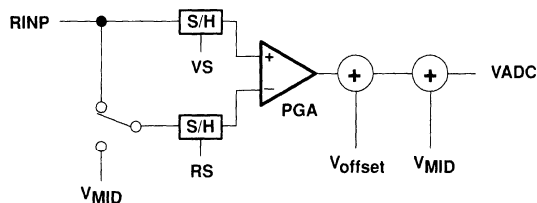


Figure 8. Sample and Hold Amplifier

The sample and hold block can operate in two modes of operation, CDS (correlated double sampling) or single ended. In CDS operation, the video signal processed is the difference between the voltage applied at the RINP input when the reset signal (RS) occurs, and the voltage at the RINP input when video signal (VS) occurs. This is summarized in Figure 9.

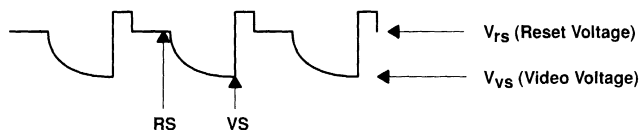


Figure 9. Reset and Video

When using CDS, the actual dc value of the input signal is not important, as long as the signal extremes are maintained within 0.5 volts of the chip power supplies. Since the signal processed is the difference between the two sample voltages, the common dc voltage is rejected.

In single-ended operation, the VS and RS control signals occur simultaneously, and the voltage applied to the reset switch is fixed at VMID. Therefore, the voltage processed is the difference between the voltage applied to RINP when VS/RS occurs, and VMID. When using single-ended operation, the dc content of the video signal is not rejected.

The programmable gain amplifier block multiplies the resulting input voltage by a value between 0.5 and 8.25 which can be programmed independently for each of the three input channels with the serial (or parallel) interface. Table 1 gives the programmed code versus gain level. The dc value of the gained signal can then be trimmed by the 8-bit plus sign DAC. The voltage output by this DAC is shown as Voffset in Figure 8. The range of the DAC is (VMID/2).

The output from the offset DAC stage is referenced to the VMID voltage which allows the input to the ADC to maximize the dynamic range, and is shown in Figure 8 by the final VMID addition.

PRINCIPLES OF OPERATION

Table 1. PGA Gain Coding

CODE	GAIN	CODE	GAIN	CODE	GAIN	CODE	GAIN
00000	0.5	01000	2.5	10000	4.5	11000	6.5
00001	0.75	01001	2.75	10001	4.75	11001	6.75
00010	1	01010	3	10010	5	11010	7
00011	1.25	01011	3.25	10011	5.25	11011	7.25
00100	1.5	01100	3.5	10100	5.5	11100	7.5
00101	1.75	01101	3.75	10101	5.75	11101	7.75
00110	2	01110	4	10110	6	11110	8
00111	2.25	01111	4.25	10111	6.25	11111	8.25

For the input stage, the final analog voltage applied to the ADC can be expressed as:

$$V_{ADC} = G(V_{VS} - V_{RS}) + \left[(1 - 2 \times \text{Sign}) \times \frac{\text{DAC_CODE}}{255} \times \frac{V_{MID}}{2} \right] + V_{MID} \quad (7)$$

where:

- V_{ADC} is the voltage applied to the ADC
- G is the programmed gain
- V_{VS} is the voltage of the video sample
- V_{RS} is the voltage of the reset sample
- Sign is the offset DAC sign bit
- DAC_CODE is the offset DAC input value
- V_{MID} is the TLC8144 generated V_{MID} voltage

clamping

The ADC has a lower reference of V_{RB} (typically 1.25 V) and an upper reference of V_{RT} (typically 3.75 V). When an ADC input voltage is applied to the ADC equal to V_{RB} , the resulting code is 000h. When an ADC input voltage is applied to the ADC equal to V_{RT} , the resulting code is 3FFh.

Both CDS and single-ended operation can be used with reset level clamping. A typical input configuration is shown in Figure 10.

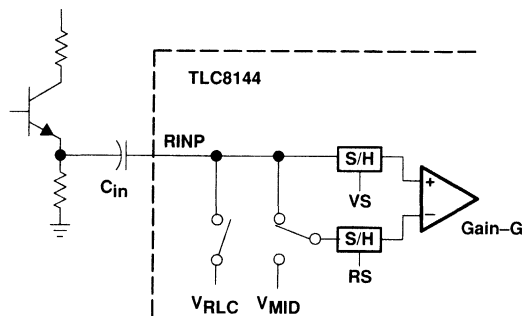


Figure 10. Video Input

TLC8144
10-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS

SLAS158 – MAY 1997

PRINCIPLES OF OPERATION

The position of the clamp relative to the video sample is programmable by CDSREF (0,1) (see Table 6). By default, the reset sample occurs on the fourth MCLK rising edge after VSMP. The relative timing between the reset sample (and CL) and video sample can be altered as shown in Figure 11.

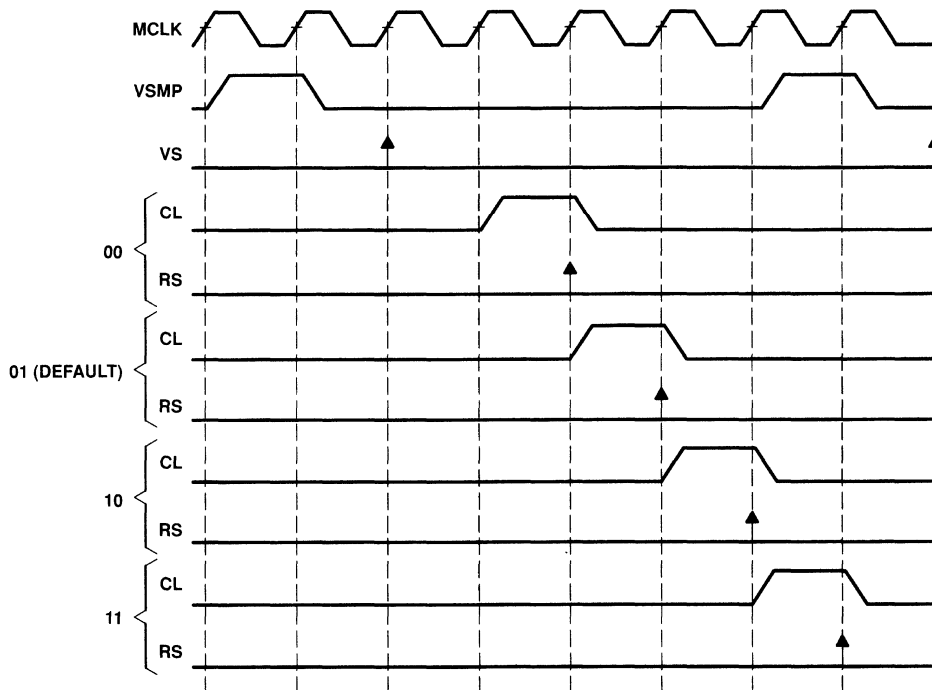


Figure 11. Reset Sample and Clamp Timing

When the clamp pulse is active, the voltage on the TLC8144 side of C_{in} , i.e. RINP, is forced to be equal to the V_{RLC} clamp voltage. The V_{RLC} clamp voltage is programmable to three different levels with the serial interface. The programming of the clamp voltage is dependent on the type of sampling selected and the polarity of the input video signal. For CDS operation, matching the clamp voltage to the amplitude and polarity of the video signal is very important, allowing complete use of the wide input common-mode range of the TLC8144. If the input video is positive going, it is advisable to clamp to V_{CL} (lower clamp voltage). If the video is negative going, it is advisable to clamp to V_{CU} (upper clamp voltage). Regardless of where the video is clamped, the offset DAC is programmed to move the ADC output corresponding to the reset level to an appropriate value to maximize the ADC dynamic range. For single-ended operation, it is recommended that the clamp voltage is set to V_{cm} (middle clamp voltage).

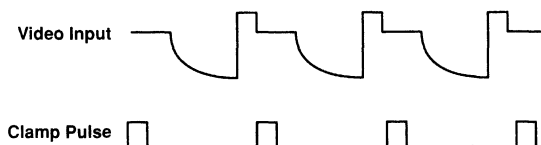


Figure 12. Video Input and Clamp



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PRINCIPLES OF OPERATION

A reset level clamp is activated when the RLC terminal is high on an MCLK rising edge (see Figure 14). By default, this initiates an internal clamp pulse three MCLK pulses later (see Figure 11; CL). The relationship between CL and RS is fixed; therefore, altering the RS position also alters the CL position (see Figure 11). Table 6 shows the three possible clamp voltages for the reset level.

EXAMPLE OF OPERATION

PARAMETERS	TEST CONDITIONS
Input video polarity	Positive
Input sampling	CDS
Input voltage amplitude ($V_{VS} - V_{RS}$)	2 V
Programmable gain	$\times 1$
Clamping	Yes, $V_{CL} = 1.5$ V

After the input capacitor, the input signal to the TLC8144 can be represented as shown in Figure 13.

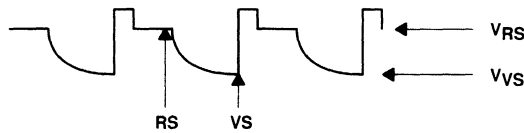


Figure 13. Video and Reset Sampling

Then for a black pixel:

$$V_{RS} = V_{CL}$$

$$V_{VS} = V_{CL}$$

Assuming that the offset DAC is set to 00 (decimal):

$$V_{ADC} = 1 \times (V_{CL} - V_{CL}) + \left[(1 - 2 \times 0) \times \frac{0}{255} V_{MID} \times \frac{V_{MID}}{2} \right] + V_{MID} \tag{8}$$

$$V_{ADC} = 0 + 0 + V_{MID} \tag{9}$$

$$V_{ADC} = V_{MID} \tag{10}$$

An input voltage of V_{MID} corresponds to a code of 512 (decimal) from the ADC.

To maximize the dynamic range of the ADC input, it is necessary to program the offset DAC code to move the ADC code corresponding to the black level toward code 000h.

Hence, set the offset DAC to 204 (decimal) with the sign bit set.

$$V_{ADC} = 1 \times (V_{CL} - V_{CL}) + \left[(1 - 2 \times 1) \times \frac{204}{255} V_{MID} \times \frac{V_{MID}}{2} \right] + V_{MID} \tag{11}$$

$$V_{ADC} = 0 - \frac{102}{255} V_{MID} + V_{MID} \tag{12}$$

$$V_{ADC} = \frac{153}{255} V_{MID} \tag{13}$$

When the V_{MID} is 2.5 V, the ADC input voltage is 1.5 volts, which results in an ADC code of 102 (decimal).

TLC8144
10-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
 SLAS158 – MAY 1997

PRINCIPLES OF OPERATION

For a white pixel:

$$V_{RS} = V_{CL}$$

$$V_{VS} = V_{CL} + 2$$

For a white pixel, using the same offset DAC value, the ADC input can be expressed as:

$$V_{ADC} = 1 \times (V_{CL} + 2 - V_{CL}) + \left[(1 - 2 \times 0) \times \frac{204}{255} V_{MID} \times \frac{V_{MID}}{2} \right] + V_{MID} \quad (14)$$

$$V_{ADC} = 2 - \frac{102}{255} V_{MID} + V_{MID} \quad (15)$$

$$V_{ADC} = 2 + \frac{153}{255} V_{MID} \quad (16)$$

When the V_{MID} is 2.5 V, the ADC input voltage is 3.5 volts, which results in a code of 921 (decimal).

Therefore, the output codes from the ADC are between 102 (decimal) and 921 (decimal), which implies that the ADC input has been set up to maximize the dynamic range available.

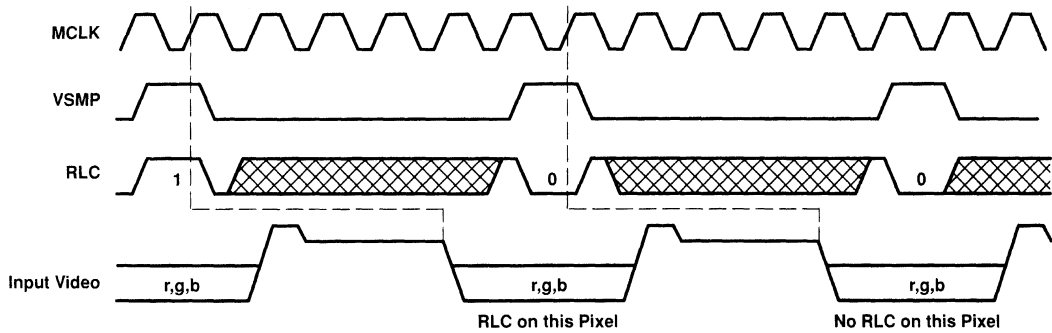


Figure 14. RLC Timing

PRINCIPLES OF OPERATION

video sampling options

TLC8144 can interface to CCD sensors using four basic modes of operation (summarized in Table 3). Mode configurations are controlled by a combination of control bits and timing applied to the MCLK and VSMP terminals. The default operational mode is color with CDS enabled (mode 1).

color mode definition (mode 1)

Figure 15 summarizes the timing relationships within the color mode. MCLK is applied at twice the required ADC conversion rate. Synchronization of sampling and channel multiplexing to the incoming video signal is performed by the VSMP pulse (active high). The three input channels (R, G, B) are sampled in parallel on the rising edge of MCLK following a VSMP pulse. The sampled data is multiplexed into a single data stream at three times the VSMP rate and passes through the internal pipeline and emerges on the OP(9–0) bus 20.5 MCLK periods later.

When the digital post-processing stage is activated, compensation data is clocked into the device at twice the ADC conversion rate (e.g., two reads per red pixel). The first of the two bytes is required on the CDATA bus 15.5 MCLK periods after the corresponding VSMP pulse. CC(2–0) can be used to control the three lower address lines of an external RAM. Both correlated double sampling (CDS) and single sample modes of operation are available.

monochrome mode definitions

One input channel is continuously sampled on the rising edge of MCLK following a VSMP pulse. The user can specify which input channel (R, G, B) to be sampled by writing to TLC8144 internal control registers. There are three separate monochrome modes with different maximum sample rates and CDS availability.

details of monochrome mode timing (mode 2)

Figure 16 summarizes the timing relationships. The timing in this mode is identical to mode 1 except for the CC(2–0) outputs. One input channel is sampled three times (due to the multiplexer being held in one position) and passes through the device as three separate samples. Two of the samples can be ignored at the output. The CC(1,2) output terminals reflect the input channel selected (R, G, or B).

details of fast monochrome mode timing (mode 3)

Figure 17 summarizes the timing relationships. This mode allows the maximum sample rate to be increased to 4 MSPS. This is achieved by altering the MCLK:VSMP ratio to 3:1. In this mode, the timing of RS and CL must be fixed (see Clamping section).

The sampled video data pass through the internal pipeline and emerge on the OP(9–0) bus 29.5 MCLK periods later.

If the digital post-processing stage is activated, compensation data are clocked into the device at twice the internal pixel rate (e.g., two reads per red pixel). The first of the two bytes is required on the CDATA bus 22.5 MCLK periods after the corresponding VSMP pulse.

details of maximum speed monochrome mode (mode 4)

Figure 18 summarizes the timing relationships. This mode allows the maximum sample rate to be increased to 6 MSPS. This is achieved by altering the MCLK:VSMP ratio to 2:1. The latency through the device is identical to modes 1 and 2. CDS is not available in this mode.

TLC8144
10-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS

SLAS158 – MAY 1997

Table 2. Mode Summary

MODE	DESCRIPTION	CDS AVAILABLE	MAX SAMPLE RATE	SENSOR INTERFACE DESCRIPTION	TIMING REQUIREMENTS	REGISTER CONTENTS WITH CDS†	REGISTER CONTENTS WITHOUT CDS†
1	Color	Yes	2 MSPS	The three input channels (R, G, B) are sampled in parallel at 2 MSPS maximum. The sampled data is multiplexed into a single data stream before the internal ADC, giving an internal serial data rate of maximum 6 MSPS.	MCLK max. 12 Mhz. MCLK:VSMP ratio is 6:1.	Setup register 1: 1Bh	Setup register 1: 19h
2	Monochrome	Yes	2 MSPS	One input channel is continuously sampled. The internal multiplexer is held in one position under control of the user.	Identical to mode 1	Setup register 1: 1Fh Setup register 3: bits b(7-6) define which channel to be sampled	Setup register 1: 1Dh Setup register 3: bits b(7-6) define which channel to be sampled
3	Fast monochrome	Yes	4 MSPS	Identical to mode 2	MCLK max. 12 MHz. MCLK:VSMP ratio is 3:1.	Identical to mode 2 plus Setup register 3: bits b(5-4) must be set to 00h	Identical to mode 2
4	Max Speed monochrome	No	6 MSPS	Identical to mode 2	MCLK max. 12 MHz. MCLK:VSMP ratio is 2:1.	Not applicable	Setup register 1: 5Dh Setup register 3: bits b(7-6) define which channel to be sampled

† Only indicates relevant register bits.



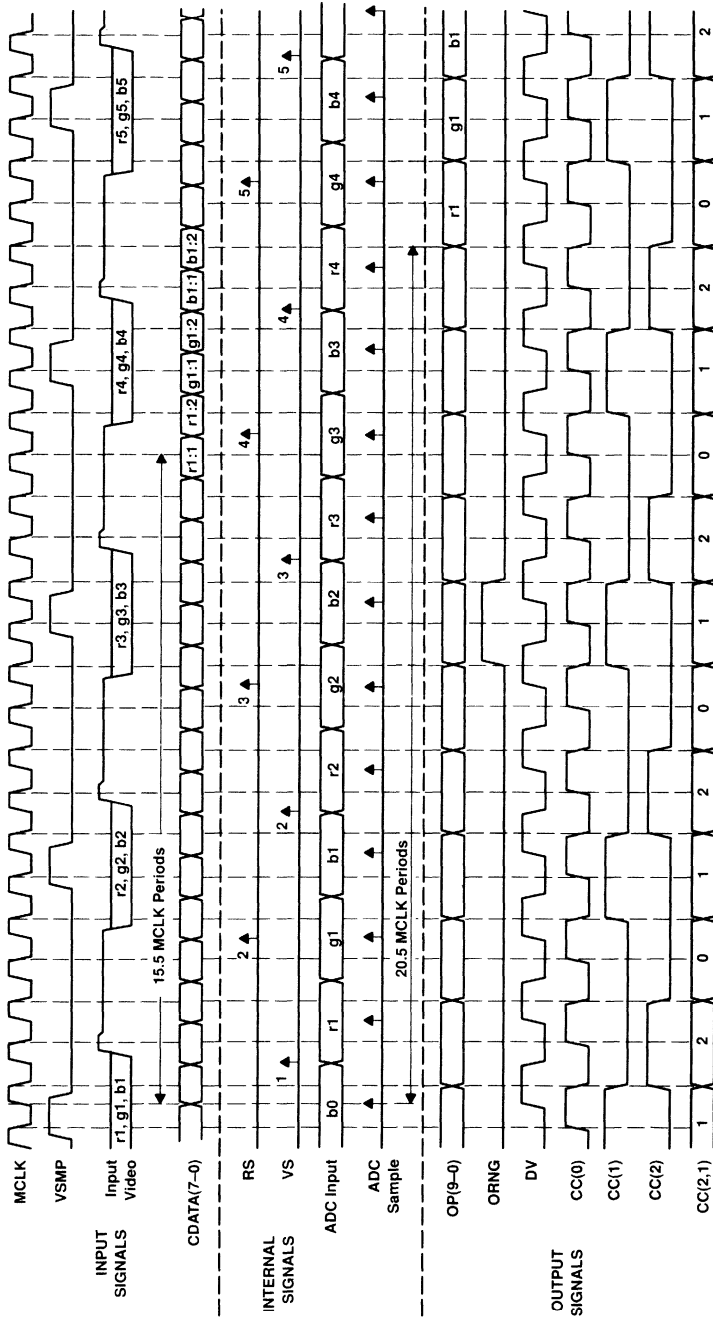
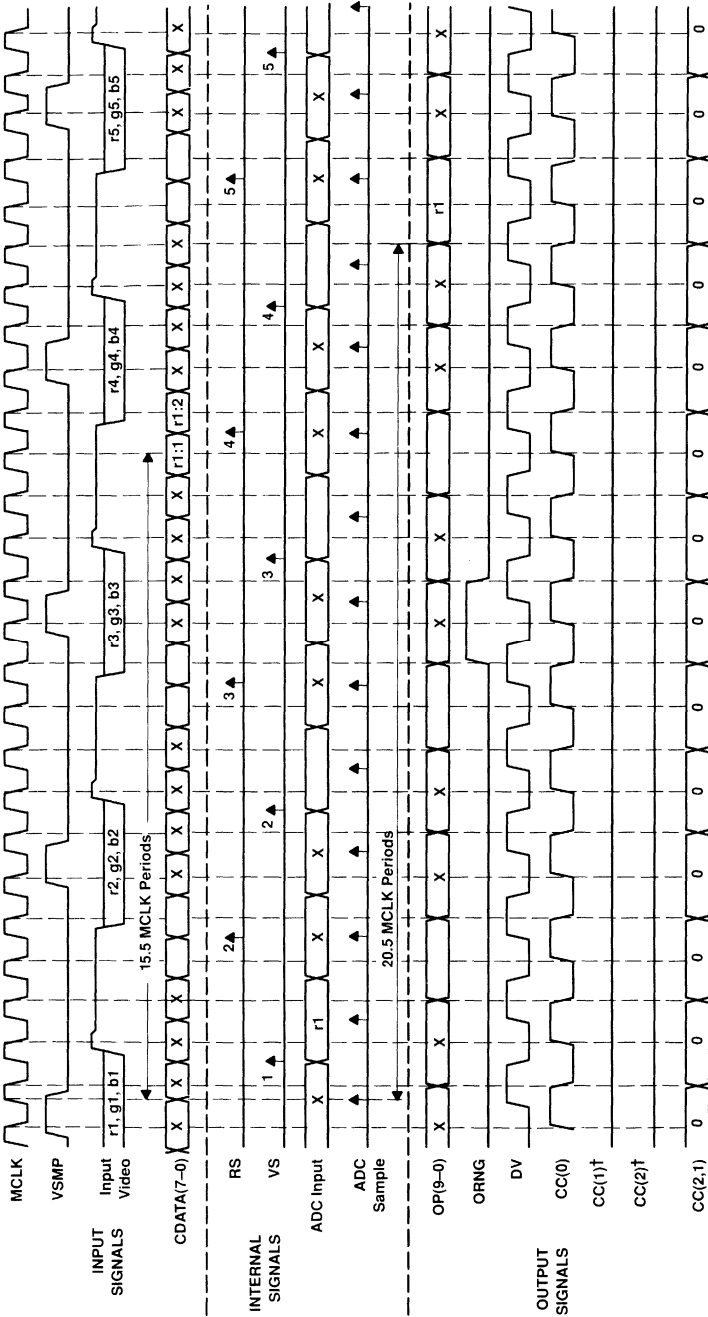


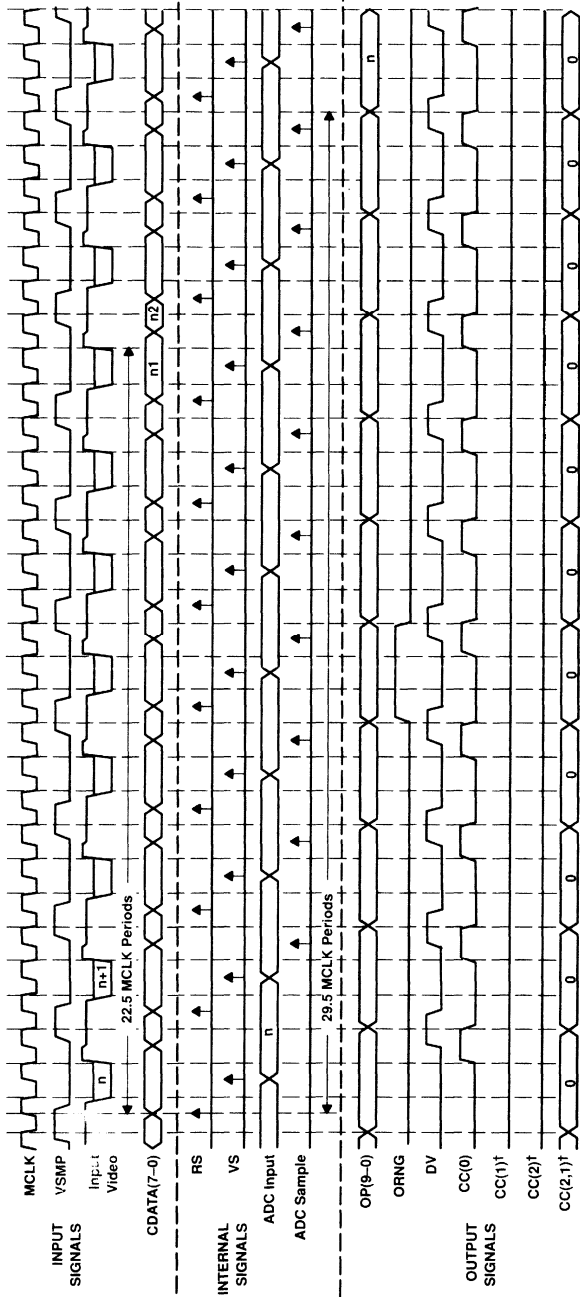
Figure 15. Default Timing in CDS Color Mode

TLC8144
10-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
 SLAS158 - MAY 1997



† This example shows function when red channel selected. CC(1) and CC(2) indicate the selected channel (R, G, or B). 'X' indicates don't care.

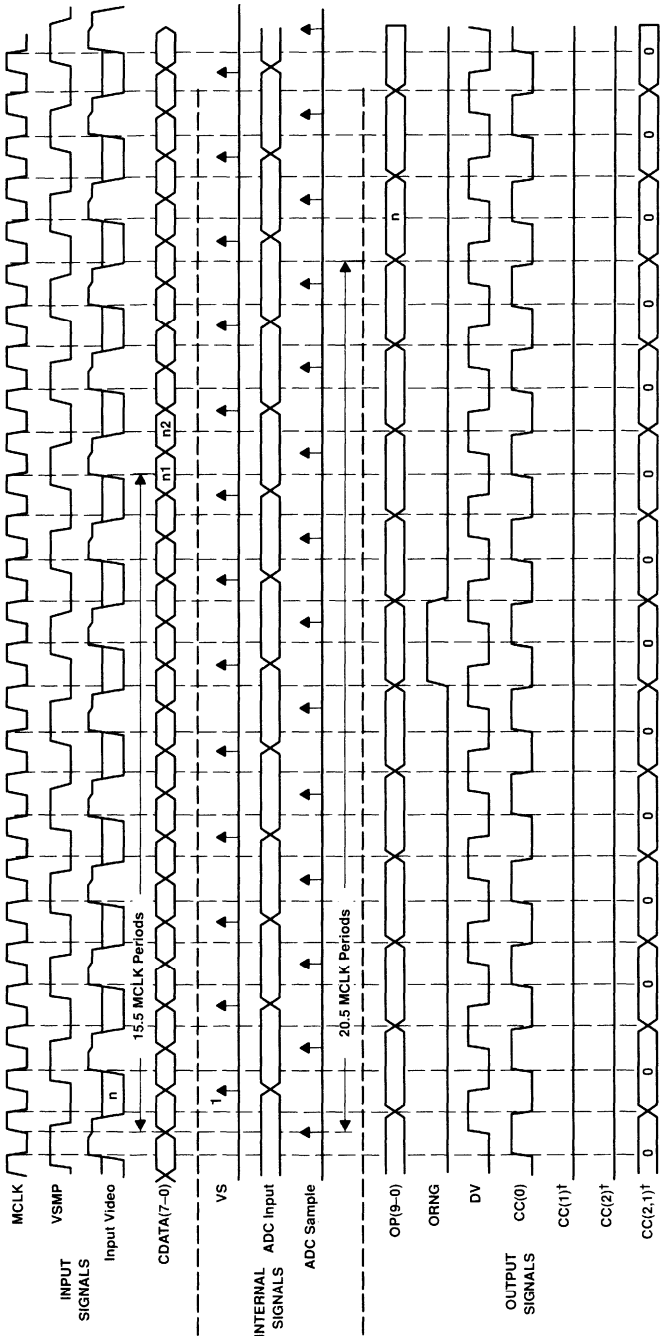
Figure 16. Default Timing in CDS Monochrome Mode



† This example shows function when red channel selected. CC(1) and CC(2) indicate the selected channel (R, G, or B).

Figure 17. Default Timing in Fast CDS Color Mode

TLC8144
10-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
 SLAS158 – MAY 1997



† This example shows function when red channel selected. CC(1) and CC(2) indicate the selected channel (R, G, or B).

Figure 18. Default Timing in Maximum Speed Non-CDS Monochrome Mode

PRINCIPLES OF OPERATION

digital signal processing

The default operation of the TLC8144 bypasses the digital compensation block. This enables the output from the ADC to be output directly on the OP(9–0) terminals. If selected, the pixel data from the ADC is processed by the digital compensation block in Figure 19. This section describes the subblocks of the digital compensation block.

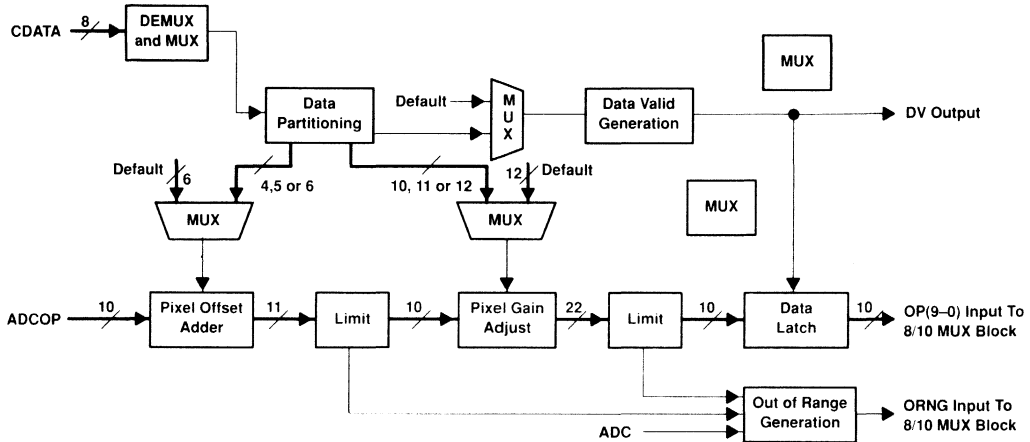


Figure 19. Digital Signal Processing Block Diagram

CDATA, DEMUX, and MUX

The input to this block is coefficient data presented to the CDATA(7–0) terminals at twice the pixel rate, i.e., two 8-bit words are input for each pixel of video data.

data partitioning

The 16 bits of data per pixel from the CDATA demultiplexer is partitioned into pixel offset, pixel gain, and pixel valid bits (see Table 3). Table 4 details the resulting range and resolution options.

Table 3. Bit Allocation Assignment

DVMODE	PWP1	PWP0	CDATA WORD 1								CDATA WORD 2							
			B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	O3	O2	O1	O0
0	0	1	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	O4	O3	O2	O1	O0
0	1	0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	O5	O4	O3	O2	O1	O0
1	0	0	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	DV	O3	O2	O1	O0
1	0	1	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	DV	O4	O3	O2	O1	O0

PRINCIPLES OF OPERATION

Table 4. Bit Range and Resolution Options

DVMODE	PWP1	PWP0	NO. OF OFF-SET BITS	OFFSET RANGE	NO. OF GAIN BITS	GAIN RANGE	GAIN RESOLUTION (LSB STEPS)	DV BITS
0	0	0	4	-8 to 7	12	0:2	0.25	0
0	0	1	5	-16 to 15	11	0:2	0.5	0
0	1	0	6	-32 to 31	10	0:2	1	0
1	0	0	4	-8 to 7	11	0:2	0.5	1
1	0	1	5	-16 to 15	10	0:2	1	1

pixel offset adder

The pixel offset adder uses the offset coefficients that are either supplied externally through the CDATA interface or from the internal default registers. The object of this block is to correct for the small offsets that can occur from the CCD on a pixel-by-pixel basis. The output from the pixel offset adder is limited to be between 0 and 1023 (decimal).

pixel gain adjust

The pixel gain adjust block corrects for the pixel-by-pixel shading curve non-uniformity and photo response non-uniformity within the CCD sensor. This block has a gain range of 0 to 2. The output word from the pixel gain adjust is limited to be between 0 and 1023 (decimal).

effect of digital compensation on ADC output

The combined effect of the digital compensation sections on the ADC output is summarized by the formula:

$$OP(9-0) = (ADCOP + POC) \times PSCF \tag{17}$$

where:

all values are decimal

OP(9-0) is the 10-bit result output from the TLC8144

ADCOP is the 10-bit output of the ADC

POC is a number sourced from the internal registers or derived from the CDATA bus input

PSCF is a number depending on bit range and resolution options (see Table 4)

data valid generation

The DV terminal state determines whether a DV pulse is generated for a particular pixel. For example, if red pixels only are required, the DV pulse can be generated as shown in Figure 20.

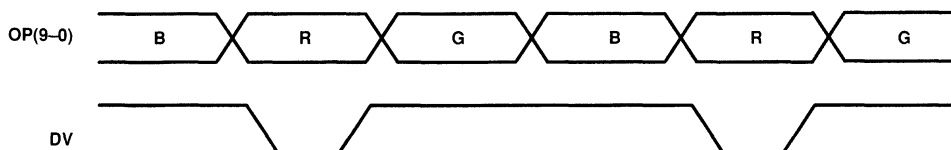


Figure 20. Data Valid Timing

PRINCIPLES OF OPERATION

data latch

Under control of the LATCHOP bit, the output data bus can be prevented from clamping until the next data valid pulse. Figure 21 shows the resulting signal relationships.

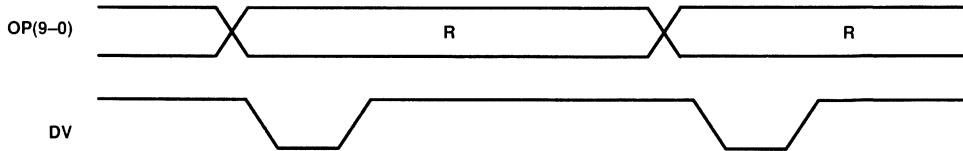


Figure 21. Data Valid Timing With LATCHOP Bit

output data interface

By default, data is output from the device as a 10-bit wide word on OP(9-0). Optionally, data can be output in an 8-bit word format. Figure 22 shows this function. Data is presented on OP(9-2) at twice the pixel rate.

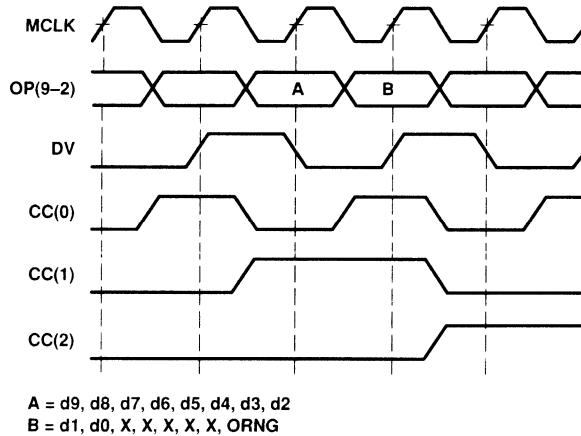


Figure 22. 8-Bit Multiplexed Bus Output

TLC8144
10-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
 SLAS158 - MAY1997

PRINCIPLES OF OPERATION

controlling the TLC8144

The TLC8144 can be configured through a serial interface or a parallel interface. Selection of the interface type is by the PNS terminal which must be tied high (parallel) or low (serial).

serial interface

The serial interface consists of three terminals (see Figure 23). A 6-bit address is clocked in MSB first followed by an 8-bit data word, also MSB first. Each bit is latched on the rising edge of SCK, which can operate at up to 12 MHz. Once the data has been shifted into the device, a pulse is applied to SEN to transfer the data to the appropriate internal register.

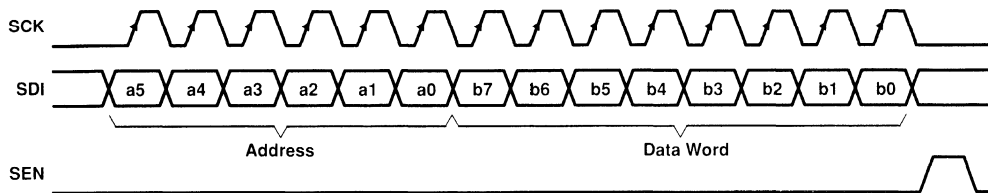


Figure 23. Serial Interface Timing

parallel interface

The parallel interface uses bits (9–2) of the OP bus as well as the STB, DNA, and RNW terminals (see Figure 24). Terminal RNW must be low during a write operation. The DNA terminal level defines whether the data byte is address (low) or data (high). The data bus OP(9–2) is latched in during the low period of STB. This interface is compatible with the extended parallel port interface.

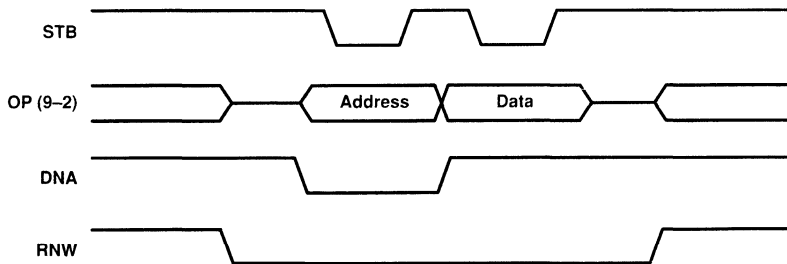


Figure 24. Parallel Interface Timing

TLC8144
10-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS
SLAS158 – MAY1997

PRINCIPLES OF OPERATION

internal register definition

Table 5 summarizes the internal register content. The first four addresses in the table are used to program setup registers and to provide a software reset feature (00h is not used). The remaining seven entries in the table define the address locations of internal data registers. In each case, three sub-addresses are defined for the red, green, and blue registers. Selection between the red, green, and blue registers is performed by address bits a1 and a0, as defined in Table 5. Setting both a1 and a0 equal to 1 forces all three registers to be updated to the same data value.

Table 5. Register Map Contents

ADDRESS <a5-a0>	DESCRIPTION	DEFAULT (HEX)	BIT								
			b7	b6	b5	b4	b3	b2	b1	b0	
000000	Not used										
000001	Setup register 1	1B	DVMODE	VSMP6M	DEFDV	DEFPO	DEFPG	MONO	CDS	ENADC	
000010	Setup register 2	00			CDATOUT	BYPASS	LATCHOP	INVOP		MUXOP	
000011	Setup register 3	11	CHAN[1]	CHAN[0]	CDSREF[1]	CDSREF[0]	PWP[1]	PWP[0]	RLC[1]	RLC[0]	
000100	Software reset	00									
000101	Reserved	00									
1000xx	DAC values	00	DAC[7]	DAC[6]	DAC[5]	DAC[4]	DAC[3]	DAC[2]	DAC[1]	DAC[0]	
1001xx	DAC signs	00									DSIGN
1010xx	PGA gains	00				PGA[4]	PGA[3]	PGA[2]	PGA[1]	PGA[0]	
1011xx	Pixel offsets	00			OFF[5]	OFF[4]	OFF[3]	OFF[2]	OFF[1]	OFF[0]	
1100xx	Pixel gain MSB	80	GAIN[11]	GAIN[10]	GAIN[9]	GAIN[8]	GAIN[7]	GAIN[6]	GAIN[5]	GAIN[4]	
1101xx	Pixel gain LSB	00					GAIN[3]	GAIN[2]	GAIN[1]	GAIN[0]	
1110xx	Data valid	01									DV

NOTE 2: Blank entries can be taken as don't care values.

xx		ADDRESS LSB DECODE
a1	a0	
0	0	Red register
0	1	Green register
1	0	Blue register
1	1	Red, green, and blue registers



TLC8144
10-BIT ANALOG-TO-DIGITAL INTERFACE FOR
CHARGE-COUPLED DEVICE IMAGE SENSORS FOR SCANNERS

SLAS158 – MAY1997

PRINCIPLES OF OPERATION

Table 6. Register Definitions

REGISTER	BIT NO.	BIT NAMES	DEFAULT	DESCRIPTION
Setup register 1	0	ENADC	1	ADC standby control: 0 = standby, 1 = active
	1	CDS	1	Select correlated double sampling mode: 0 = normal sampling, 1 = CDS mode
	2	MONO	0	Mono/color select: 0 = color, 1 = monochrome operation
	3	DEFPG	1	Select default pixel gain: 0 = external pixel gain, 1 = internal
	4	DEFPO	1	Select default pixel offsets: 0 = external pixel offsets, 1 = internal
	5	DEFDV	0	Select default internal data valid: 0 = external DV, 1 = internal
	6	VSMP6M	0	Required when VSMP at 6 MSPS: 0 = other mode, 1 = VSMP at 6 MSPS
Setup register 2	7	DVMODE	0	External data valid control (see Table 3)
	0	MUXOP	0	8-bit output mode: 0 = 10-bit, 1 = 8-bit multiplexed
	1			
	2	INVOP	0	Inverts ADC output: 0 = non-inverting, 1 = inverting
	3	LATCHOP	0	OP bus updated on DV pulse; OP bus updated each sample, 1 = update only on DV pulse
	4	BYPASS	0	Bypass digital post-processing: 0 = bypass, 1 = no bypass
	5	CDATOUT	0	Data on OP terminals available on CDAT terminals: 0 = no, 1 = yes
Setup register 3	6			
	7			
	1,0	RLCL(1,0)	01	Reset level clamp voltage 00 = 1.5 V 01 = 2.5 V 10 = 3.5 V 11 = Not used
	3,2	PWP(1,0)	00	Parallel word partitioning (see Table 3)
5,4	CDSREF(1,0)	01	CDS mode reset timing adjust 00 = Red channel 01 = Green channel 10 = Blue channel 11 = Not used	
7,6	CHAN(1,0)	00	Monochrome mode channel select 00 = Red channel 01 = Green channel 10 = Blue channel 11 = Not used	

APPLICATION INFORMATION

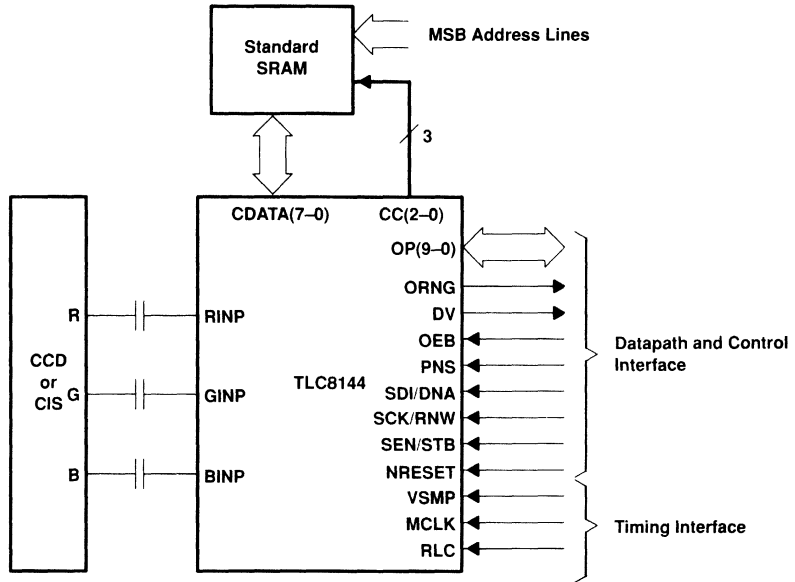


Figure 25. System Diagram

TLC8188 10-BIT, 4MSPS, CIS/LINEAR CCD SENSOR PROCESSOR

SLAS177 - DECEMBER 1997

- Supports Both CIS and CCD Sensors
- 10-bit, 4MSPS, A/D Converter
- Differential Nonlinearity Error: ± 0.5 LSB Typ
- Integral Nonlinearity Error: ± 1 LSB Typ
- 8-bit Offset Correction DAC
- PGA With 6-bit Gain Resolution
- Auto-cycling Gain and Offset Control
- Single 5 V Supply Operation
- Very Low Power: 155 mW Typical
- Control by Parallel and Serial Interface
- Internal Reference Voltages
- 32-pin TSSOP Package

description

The TLC8188 is a highly-integrated monolithic analog signal processor/digitizer designed to interface the contact image sensor (CIS) and linear charge-coupled device (CCD) image sensors in scanner applications. The input of the TLC8188 allows direct connection to the CIS and direct ac coupling of the linear CCD. The TLC8188 performs all the analog processing functions necessary to maximize the dynamic range, correct various errors associated with the CIS and the linear CCD sensors, and then digitize the results with an on-chip analog-to-digital converter (ADC). The key components of the TLC8188 include: input clamp circuitry and a correlated double sampler (CDS), a programmable gain amplifier (PGA) with auto-cycling gain control, a programmable offset correction controlled by a digital-to-analog converter (DAC), a 10-bit, 4 MSPS pipeline ADC, a bidirectional parallel bus and a three-wire serial port for easy microprocessor interface, and internal reference voltages.

Designed in advanced CMOS process, the TLC8188 operates from a single 5-V power supply and its digital interface is 3 V compatible. The normal power consumption of the TLC8188 is just 155 mW.

Fully integrated analog processing circuitry, high throughput rate, single supply operation and low cost make the TLC8188 an ideal CIS/linear CCD sensor interfacing solution for imaging applications such as scanners and multifunctional office equipment (printer/scanner/facsimile/copier).

The part is available in a 32-pin TSSOP package and is specified over 0°C to 70°C operating temperature range.

AVAILABLE OPTIONS

T _A	PACKAGED DEVICES
	SMALL OUTLINE (DA)
0°C to 70°C	TLC8188CDA

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



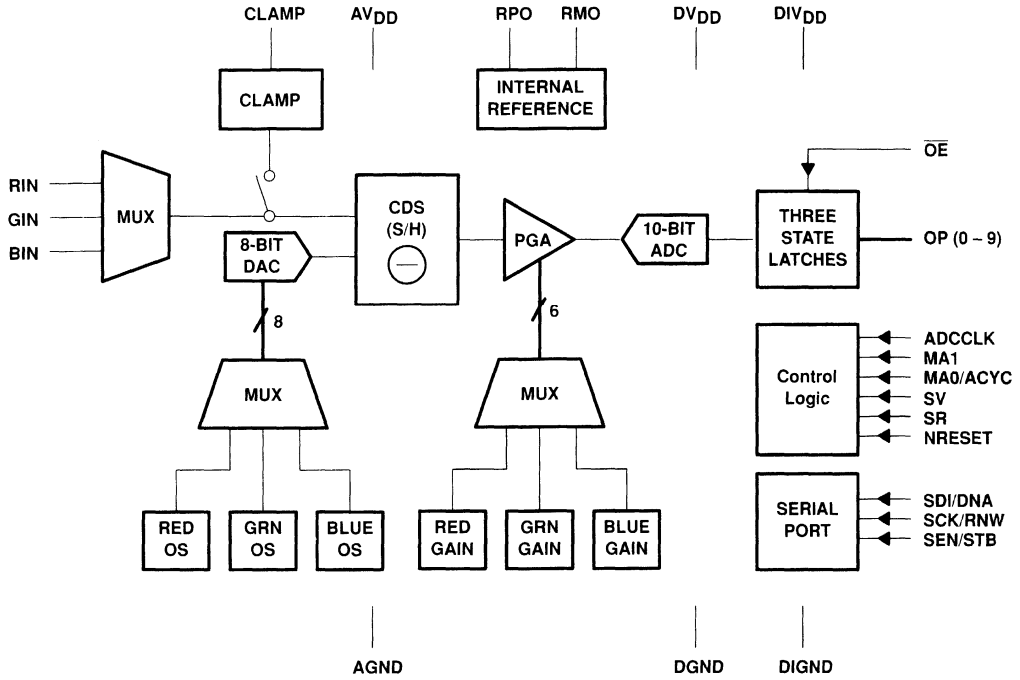
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TLC8188
10-BIT, 4MSPS, CIS/LINEAR CCD SENSOR PROCESSOR

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functional block diagram



PRODUCT PREVIEW



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TLC8188
10-BIT, 4MSPS, CIS/LINEAR CCD SENSOR PROCESSOR

SLAS177 – DECEMBER 1997

Terminal Functions

TERMINAL NAME		NO.	I/O	DESCRIPTION
OP[0:4]	1 – 5	O		Three-state bi-directional data bus, OP0 and OP1 are output only.
DIVDD	6			Digital interface circuit supply voltage, +3 V to +5 V
DIGND	7			Digital interface circuit ground
OP[5:9]	8 – 12	O		Three-state bi-directional data bus.
NRESET	13	I		Power-on reset and Interface mode control. If SEN/STB is logic "1" when NRESET goes high then device is in parallel configuration data input mode. If SEN/STB is logic "0" when NRESET goes high then device is in serial data input mode.
SDI/DNA	14	I		Serial interface: serial interface input data Parallel interface: 1 – data, 0 – address
DGND	15			Digital ground
DVDD	16			Digital supply voltage, +5 V
SCK/RNW	17	I		Serial interface: serial clock Parallel interface: 1 – OP[9:2] is output bus, 0 – OP[9:2] is input bus
ADCCLK	18	I		ADC conversion clock input.
OE	19	I		Three-state output enable, active low
SEN/STB	20	I		Serial interface: serial data transfer enable, active high. Parallel interface: strobe, active low.
SV	21	I		CCD signal level sample pulse input
SR	22	I		CCD reset level sample pulse input, CIS sample pulse input
CLAMP	23	I		CCD input clamp signal
MA1, MA0/ACYC	24, 25	I		MA1 and MA0 select the color to which all internal MUX (input, gain, offset) will point. When in auto cycling mode, the input mux and internal registers are auto cycled by the ACYC. The ACYC is a control signal such as a line start pulse that defines the start of a current scanning line.
AGND	26			Analog ground
AVDD	27			Analog supply voltage, +5 V
BIN	28	I		Blue channel input
GIN	29	I		Green channel input
RIN	30	I		Red channel input
RMO	31	O		Ref– output for external decoupling
RPO	32	O		Ref+ output for external decoupling

PRODUCT PREVIEW



General Information	1
General Purpose ADCs	2
General Purpose DACs	3
DSP AICs and CODECS	4
Special Functions	5
Video Interface Palettes	6
Digital Imaging Sensor Products	7
Mechanical Information	8

Contents

	Page
Mechanical Information :	8-3



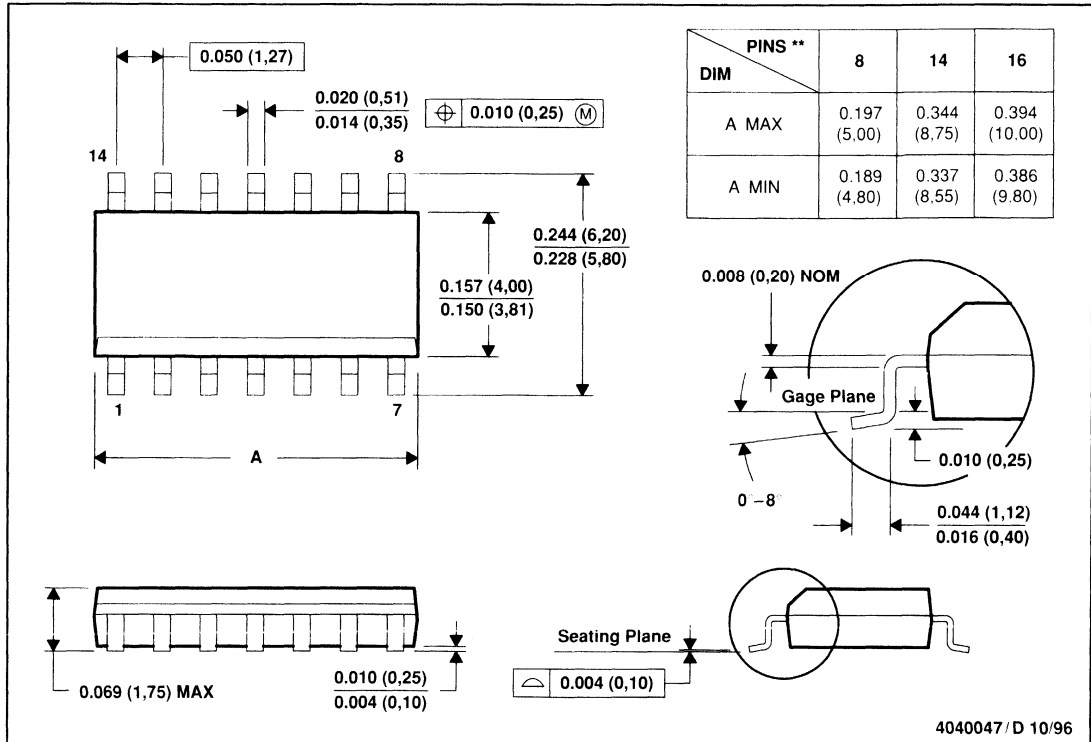
MECHANICAL INFORMATION

MECHANICAL DATA

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

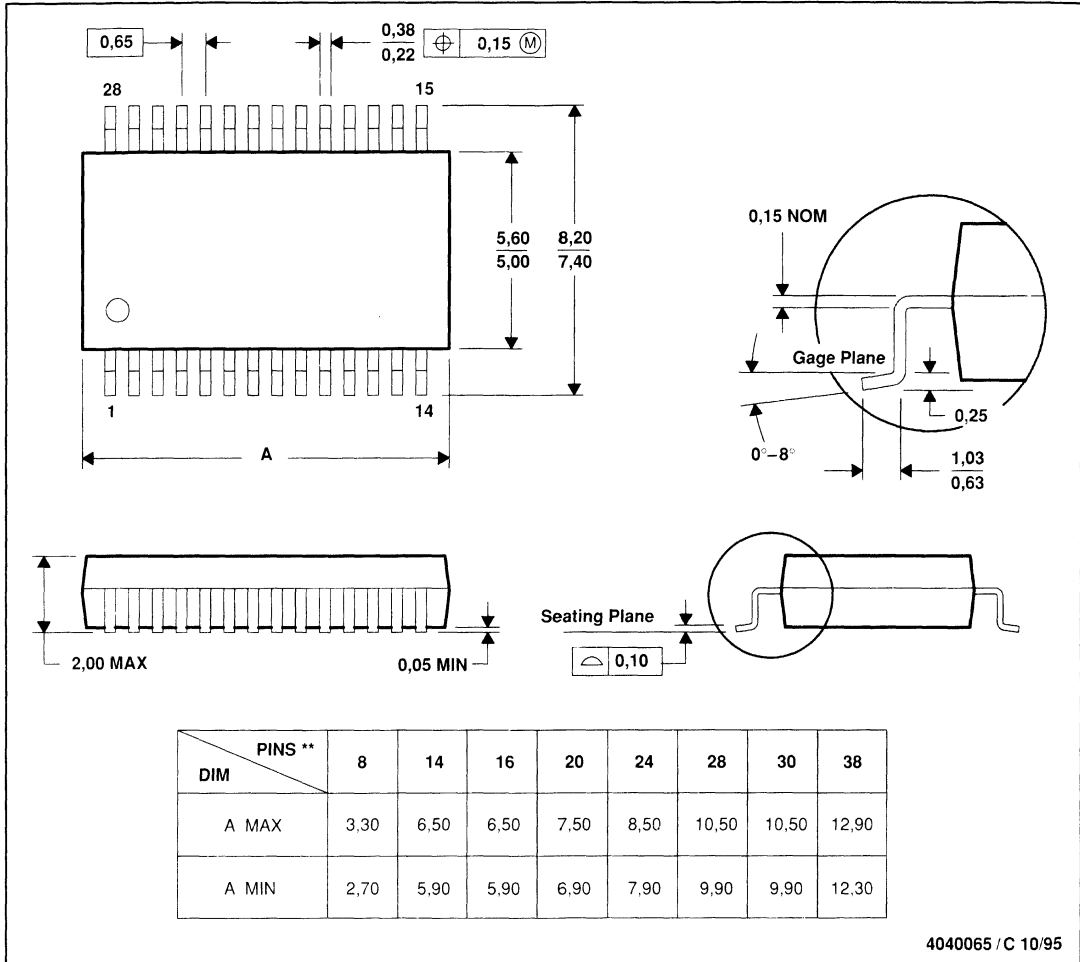
MECHANICAL INFORMATION

MECHANICAL DATA

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

28 PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150



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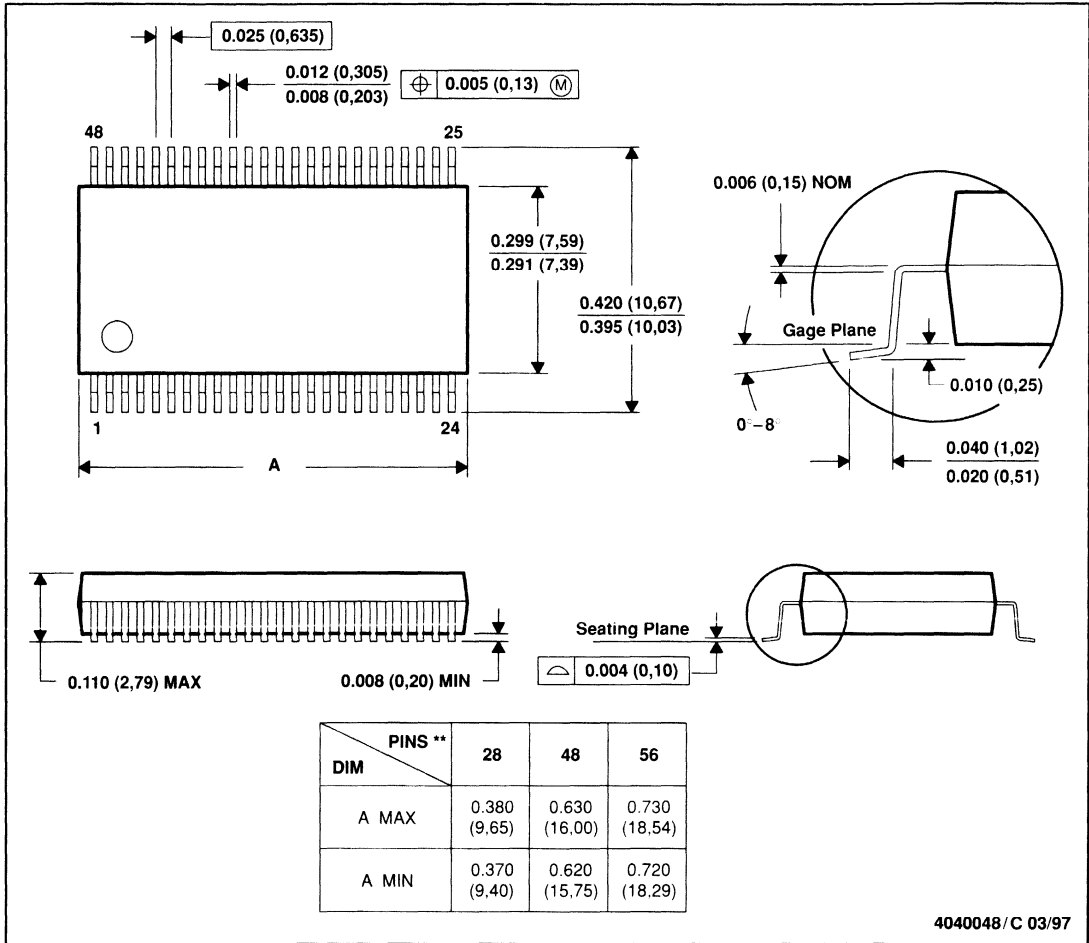
MECHANICAL INFORMATION

MECHANICAL DATA

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

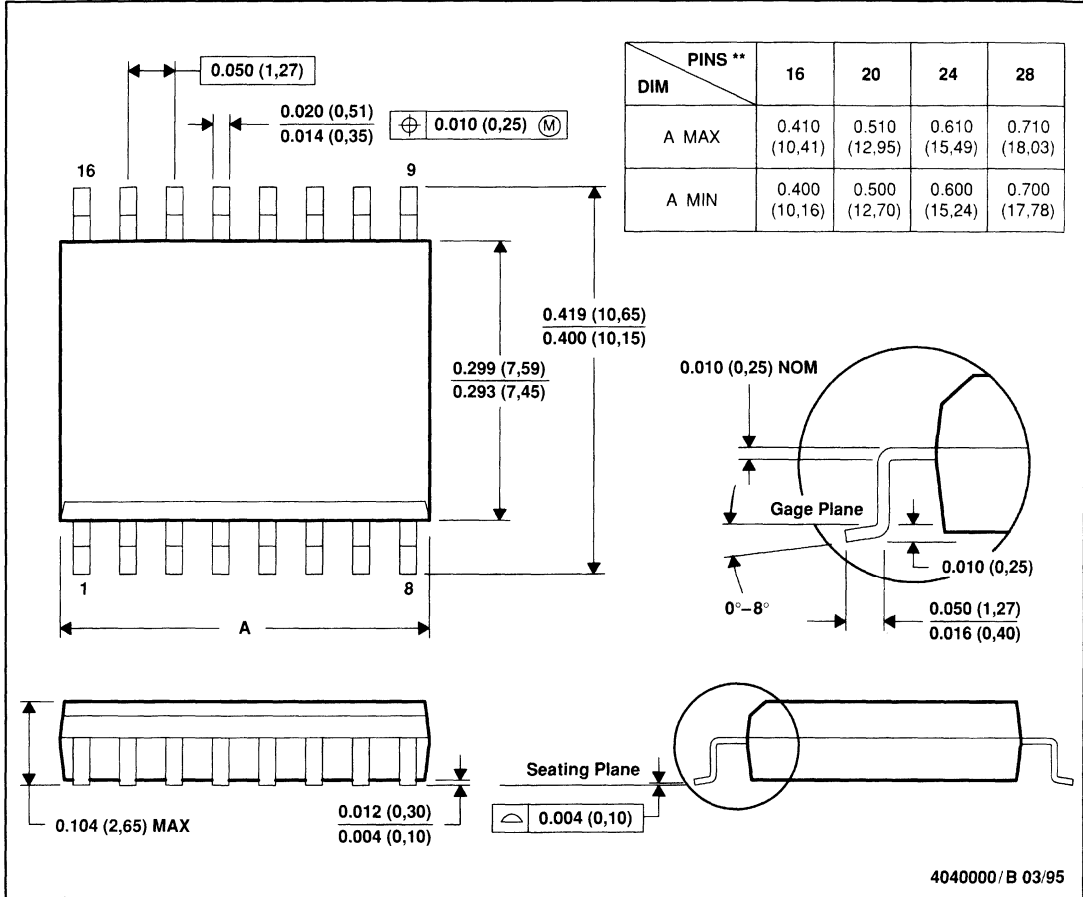
MECHANICAL INFORMATION

MECHANICAL DATA

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN

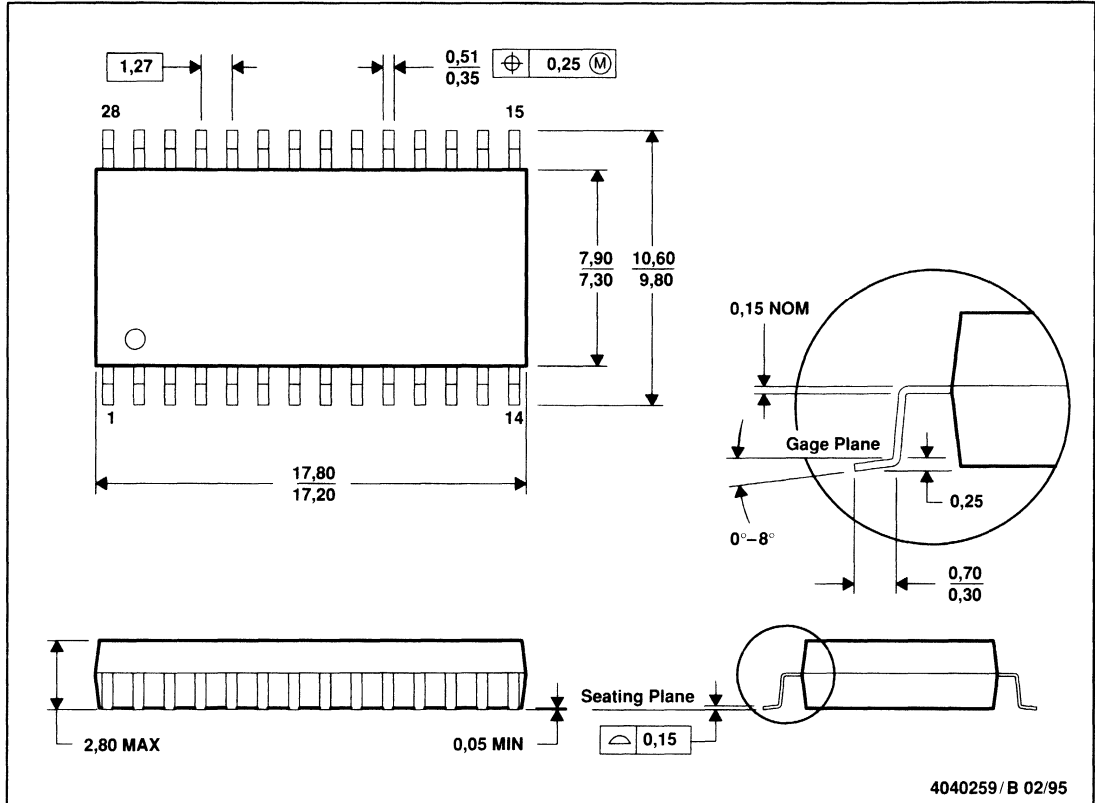


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013

MECHANICAL DATA

DWB (R-PDSO-G28)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions include mold flash or protrusion.

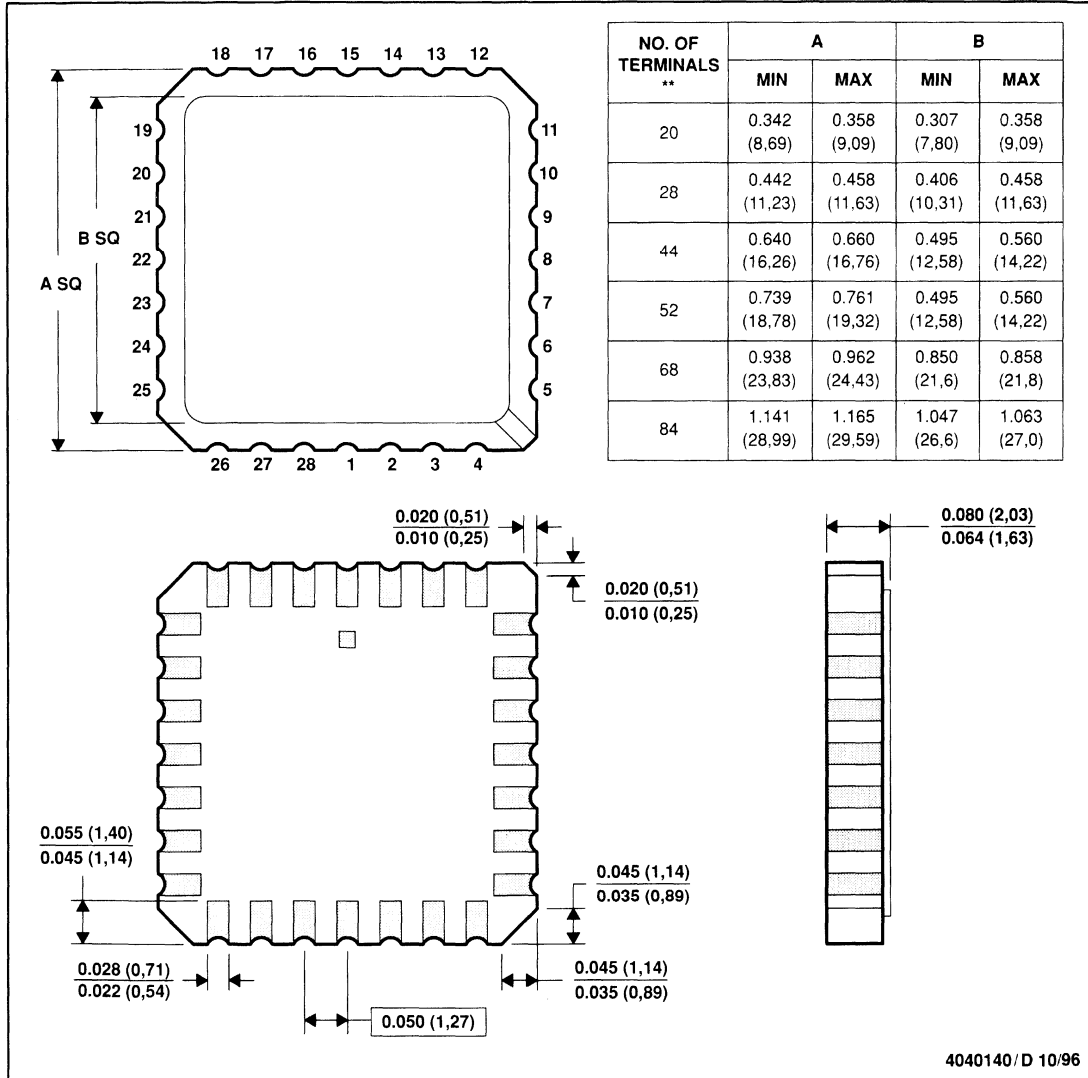
MECHANICAL INFORMATION

MECHANICAL DATA

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a metal lid.
 D. The terminals are gold plated.
 E. Falls within JEDEC MS-004

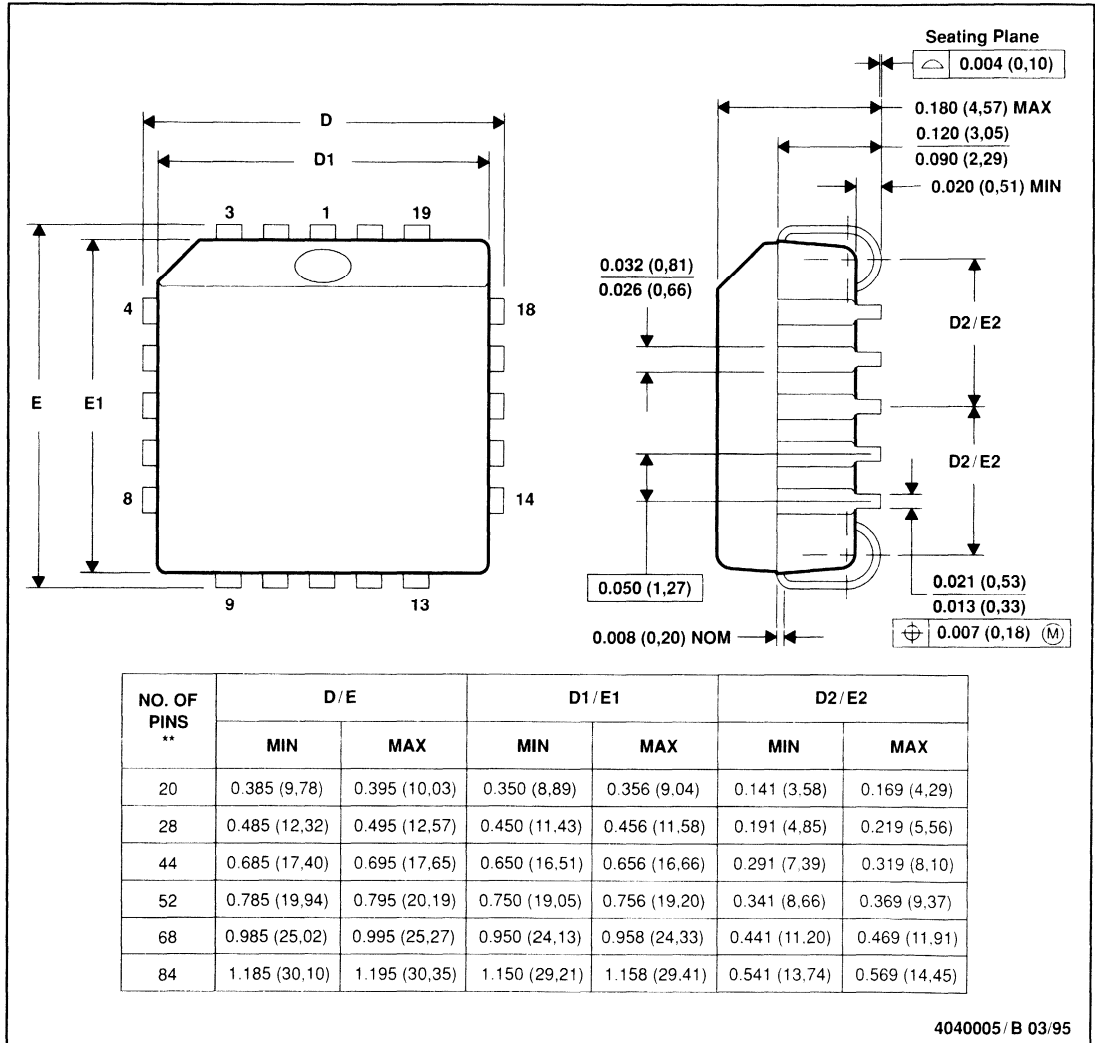
MECHANICAL INFORMATION

MECHANICAL DATA

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



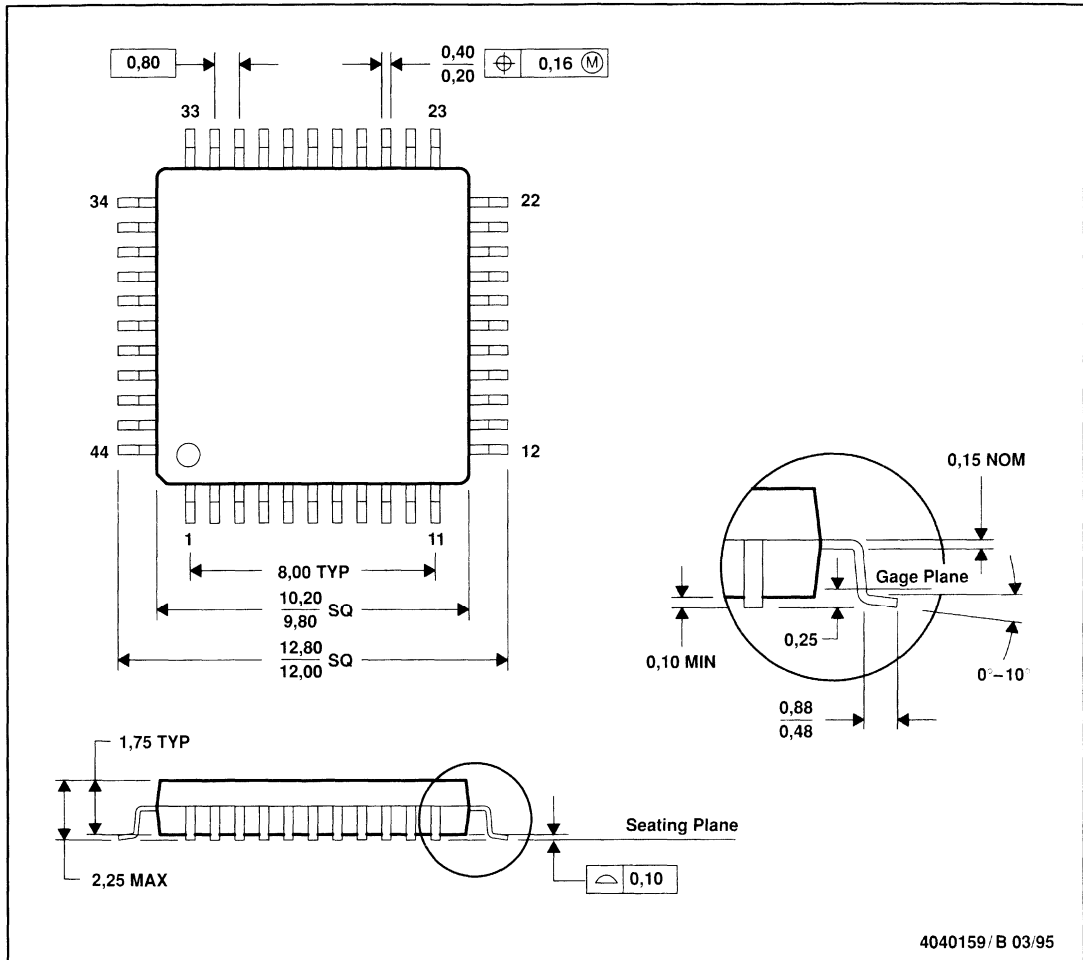
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

MECHANICAL INFORMATION

MECHANICAL DATA

FR (S-PDFP-G44)

PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.



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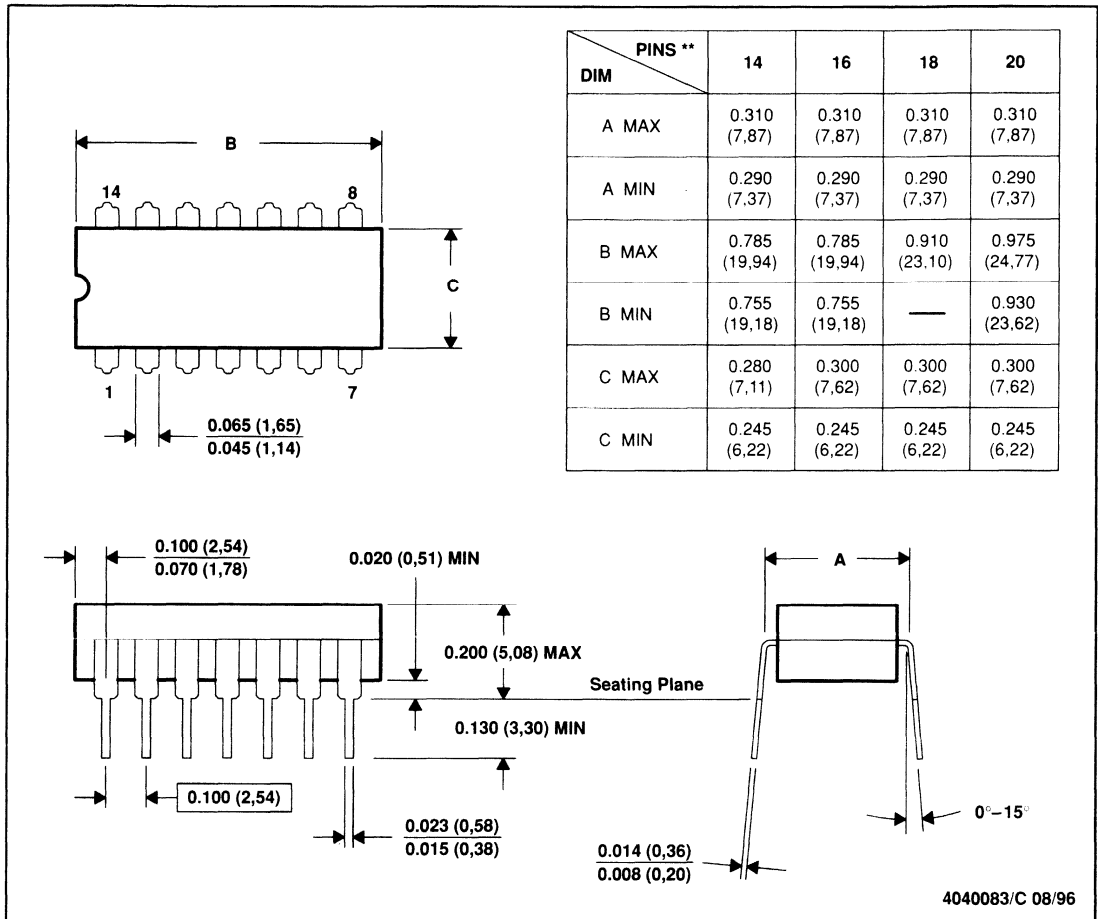
MECHANICAL INFORMATION

MECHANICAL DATA

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 E. Falls within MIL-STD-1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, and GDIP1-T20

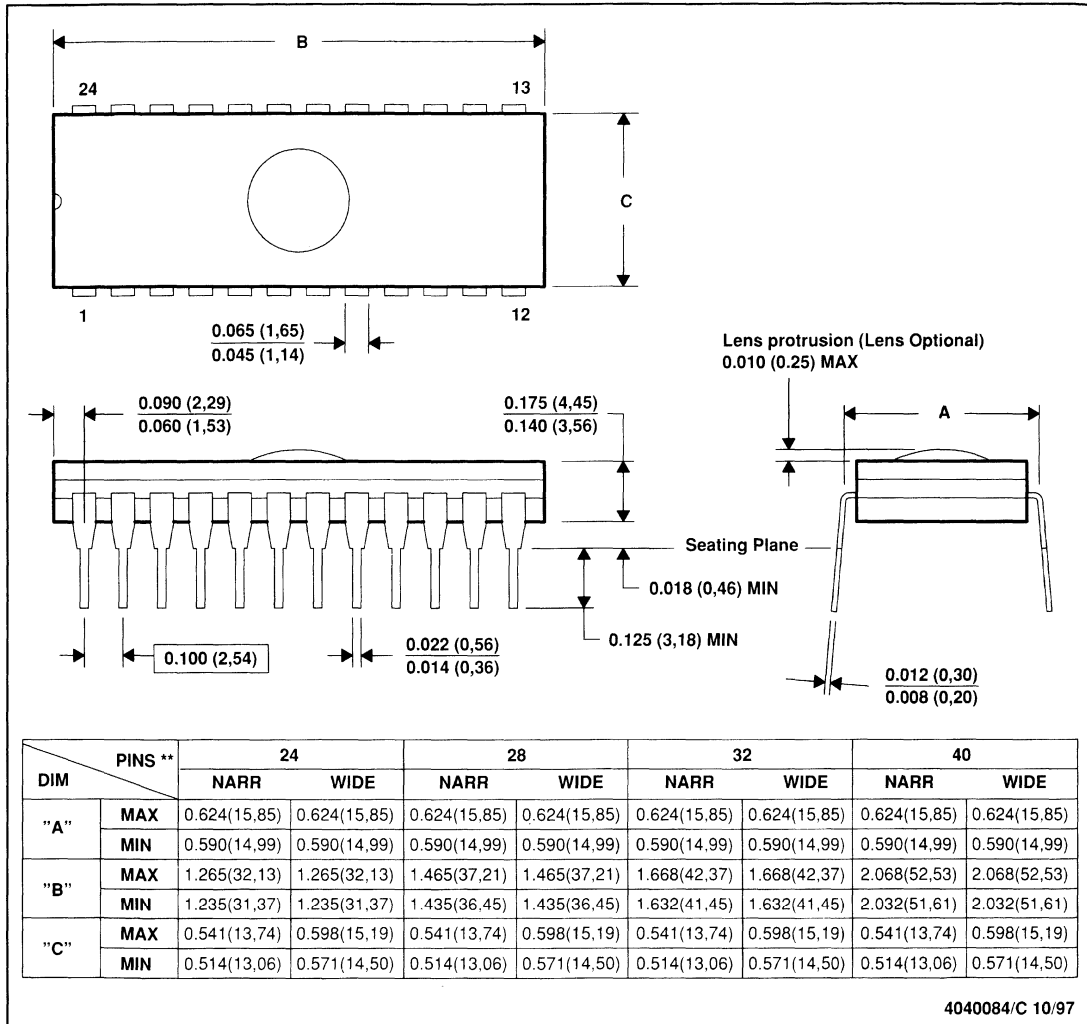
MECHANICAL INFORMATION

MECHANICAL DATA

J (R-CDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN

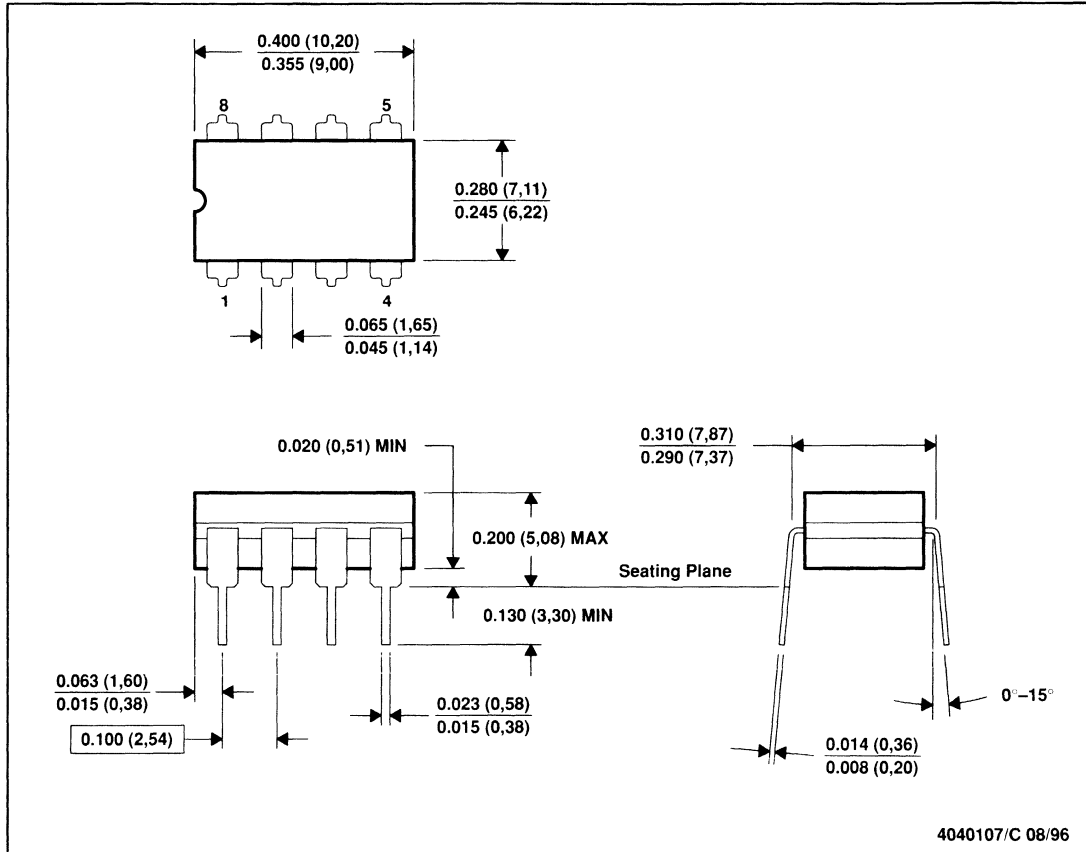


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Window (lens) added to this group of packages (24,28,32,40 pin).
 D. This package can be hermetically sealed with a ceramic lid using glass frit.
 E. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.

MECHANICAL DATA

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 E. Falls within MIL-STD-1835 GDIP1-T8

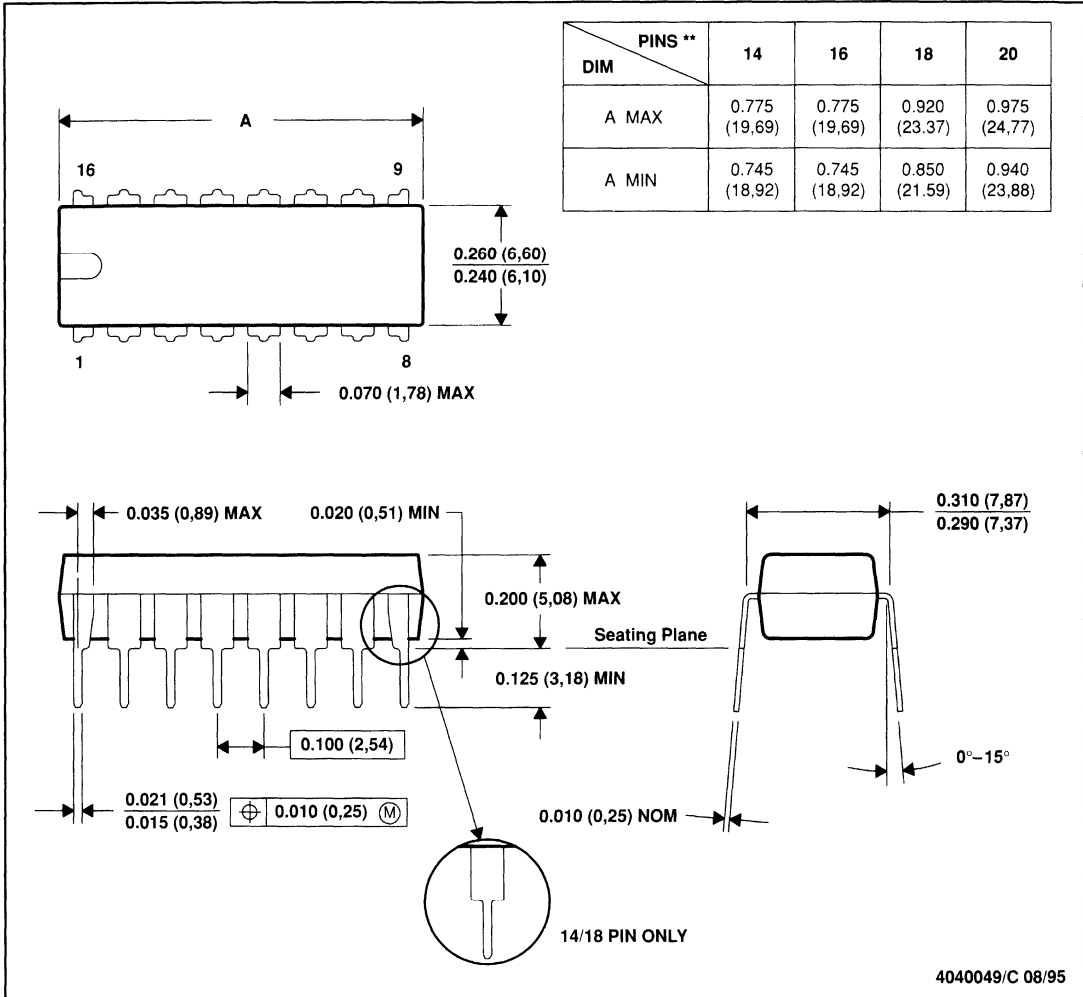
MECHANICAL INFORMATION

MECHANICAL DATA

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

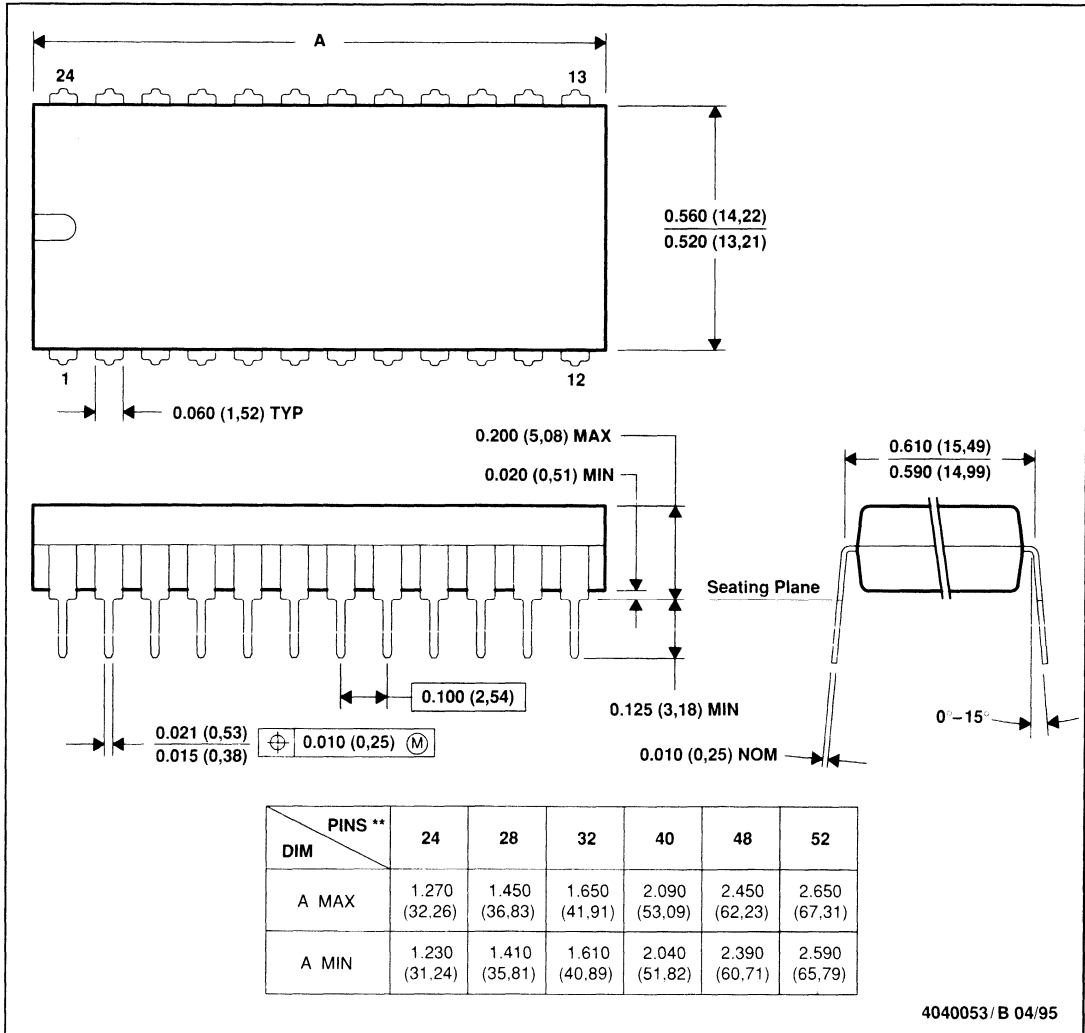
MECHANICAL INFORMATION

MECHANICAL DATA

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-011
 D. Falls within JEDEC MS-015 (32 pin only)



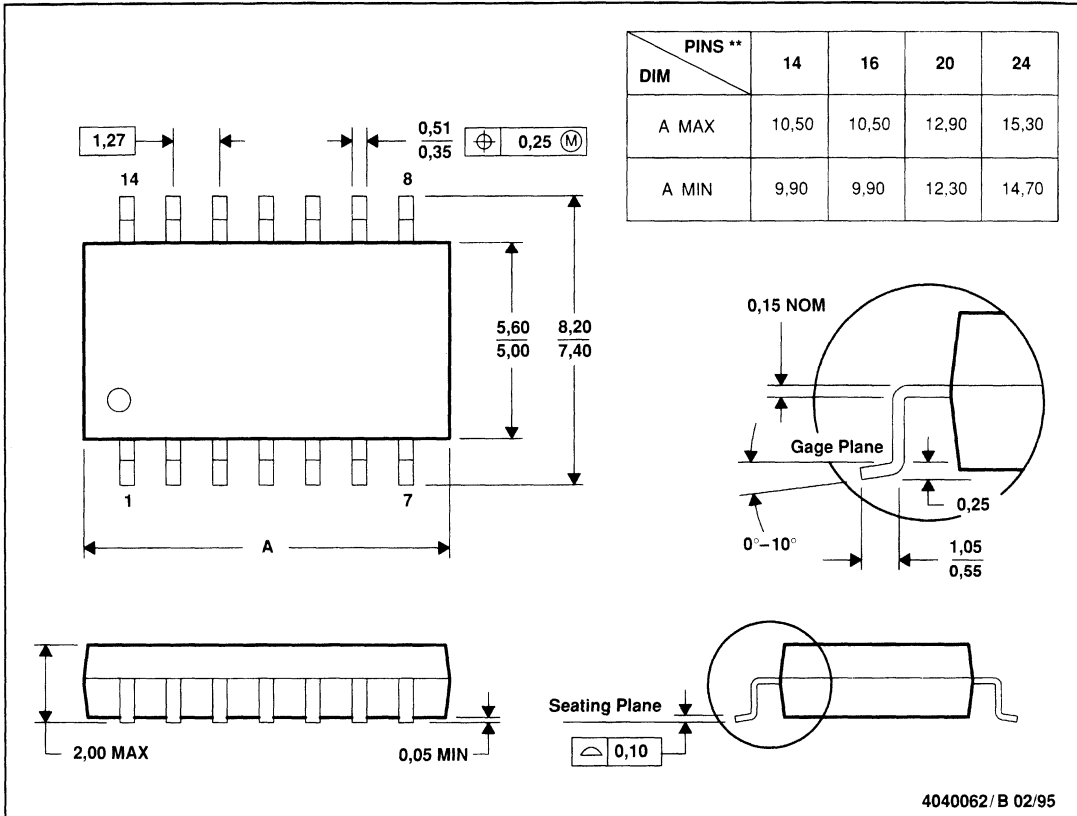
MECHANICAL INFORMATION

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

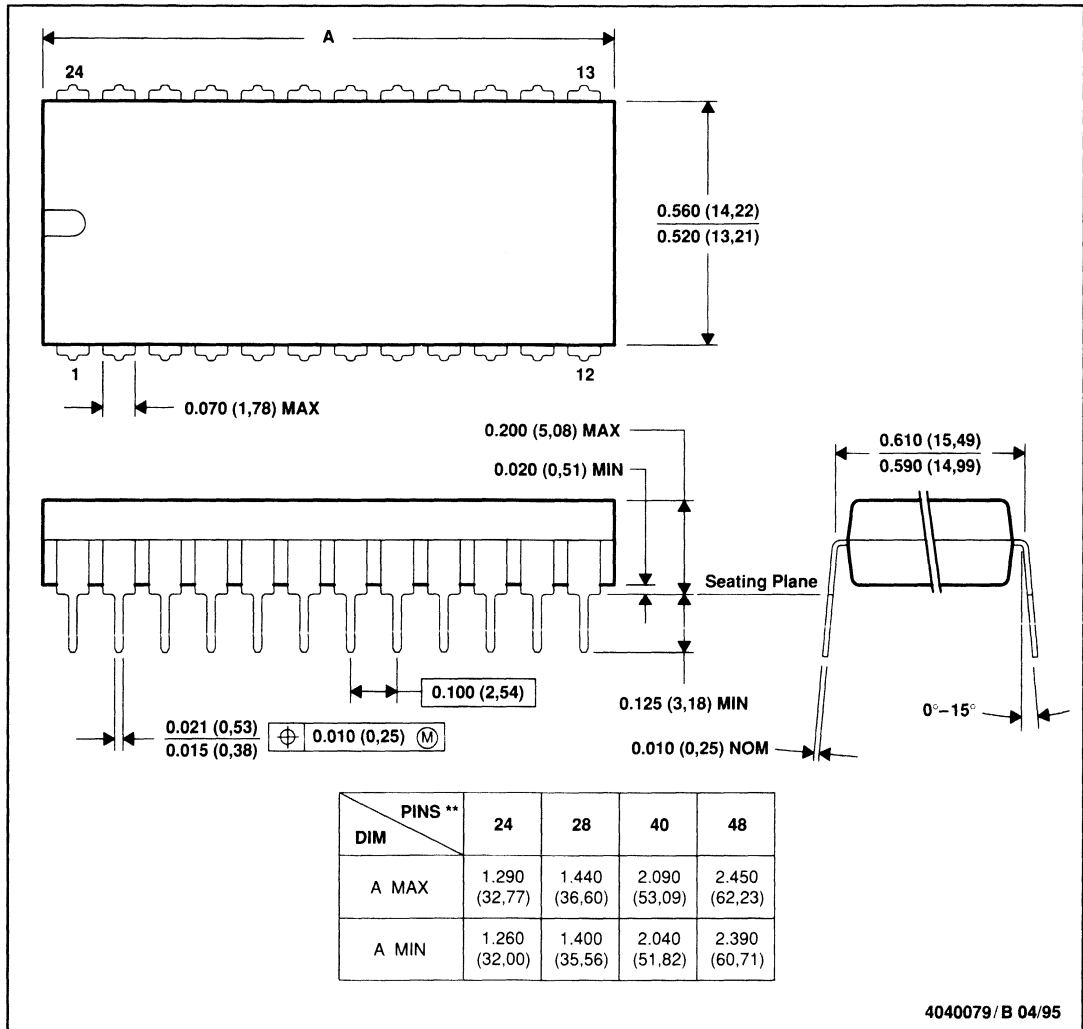
MECHANICAL INFORMATION

MECHANICAL DATA

NW (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-011

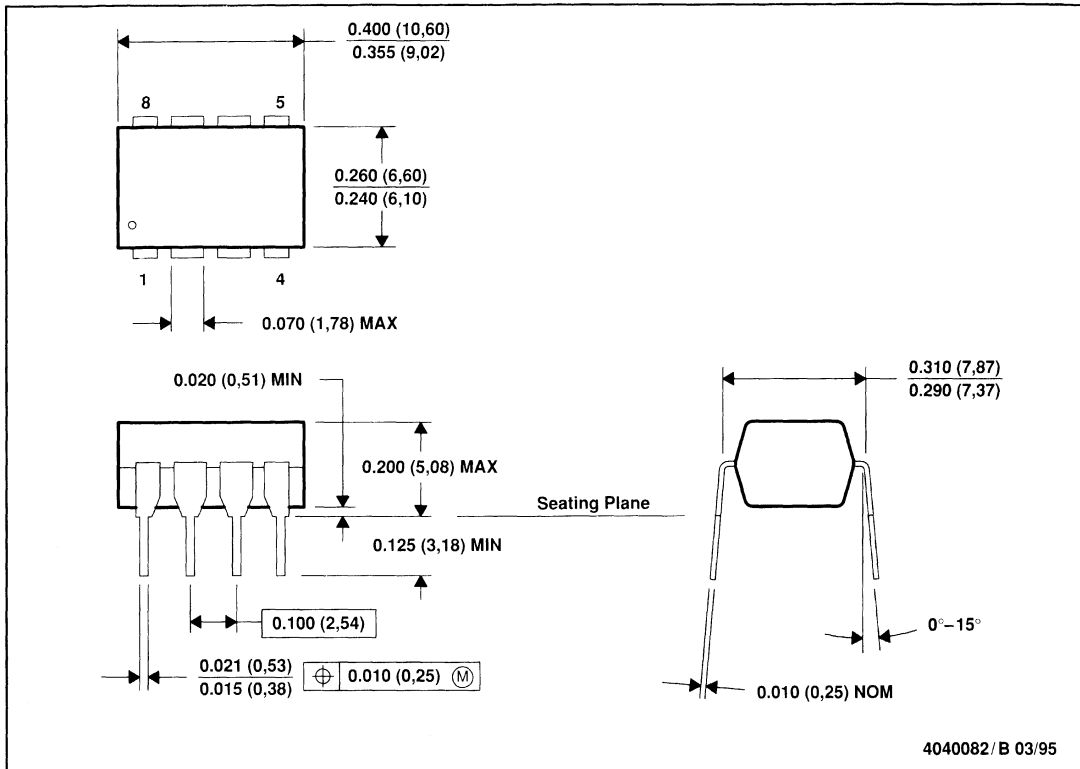


MECHANICAL INFORMATION

MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



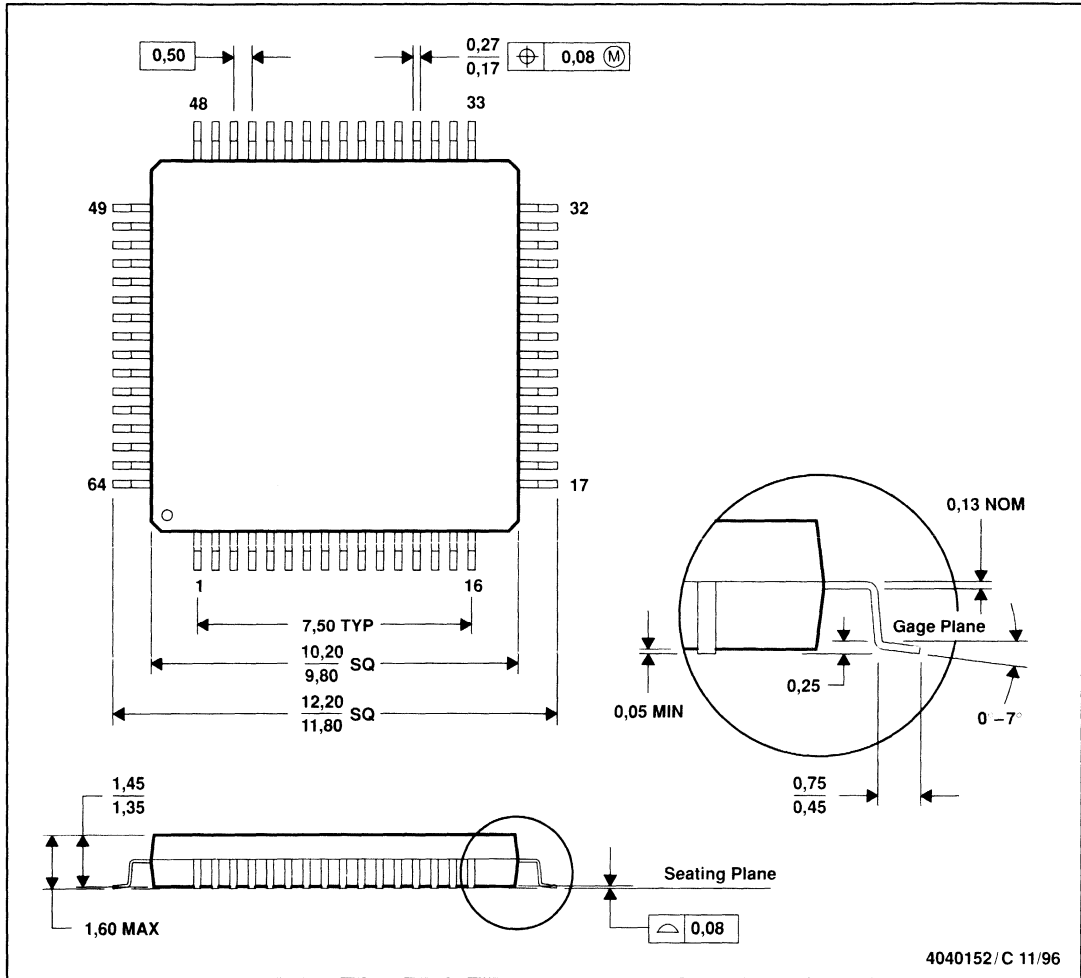
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

MECHANICAL INFORMATION

MECHANICAL DATA

PM (S-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-026
 - D. May also be thermally enhanced plastic with leads connected to the die pads.

 **TEXAS
INSTRUMENTS**

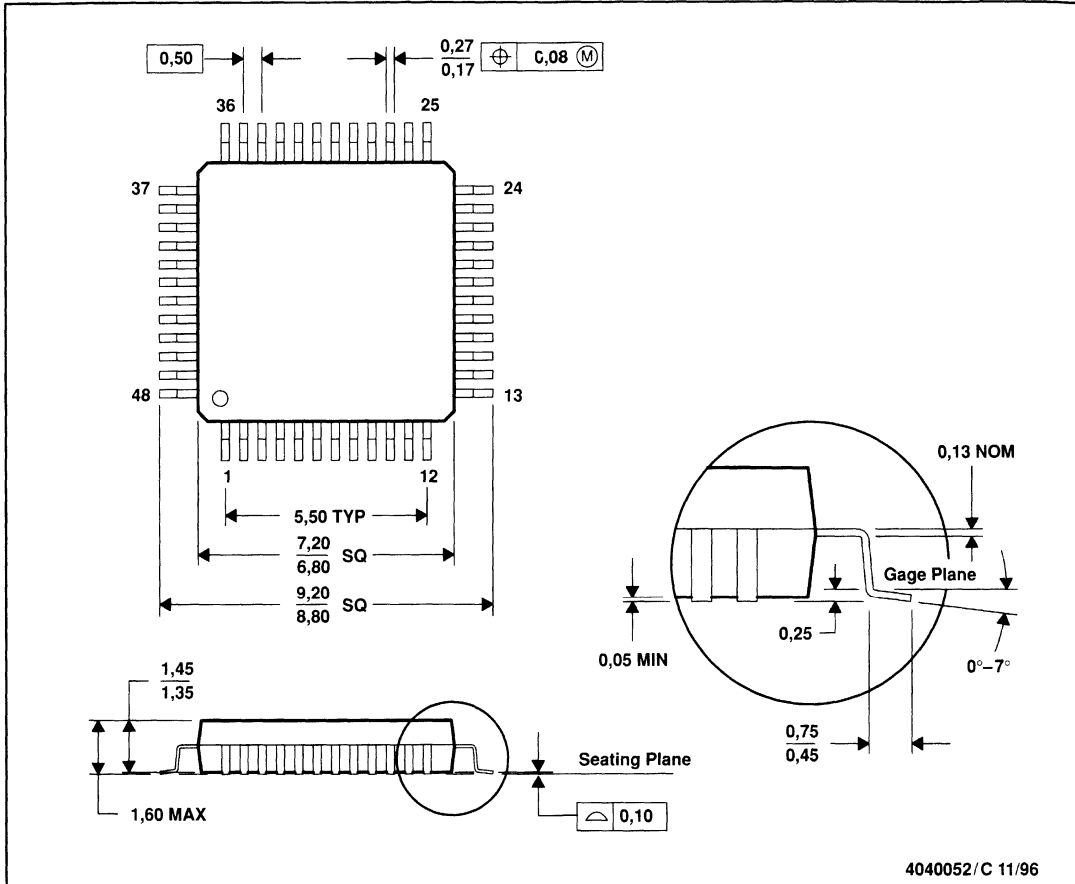
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MECHANICAL INFORMATION

MECHANICAL DATA

PT (S-PQFP-G48)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-026
 - D. This may also be a thermally enhanced plastic package with leads connected to the die pads.

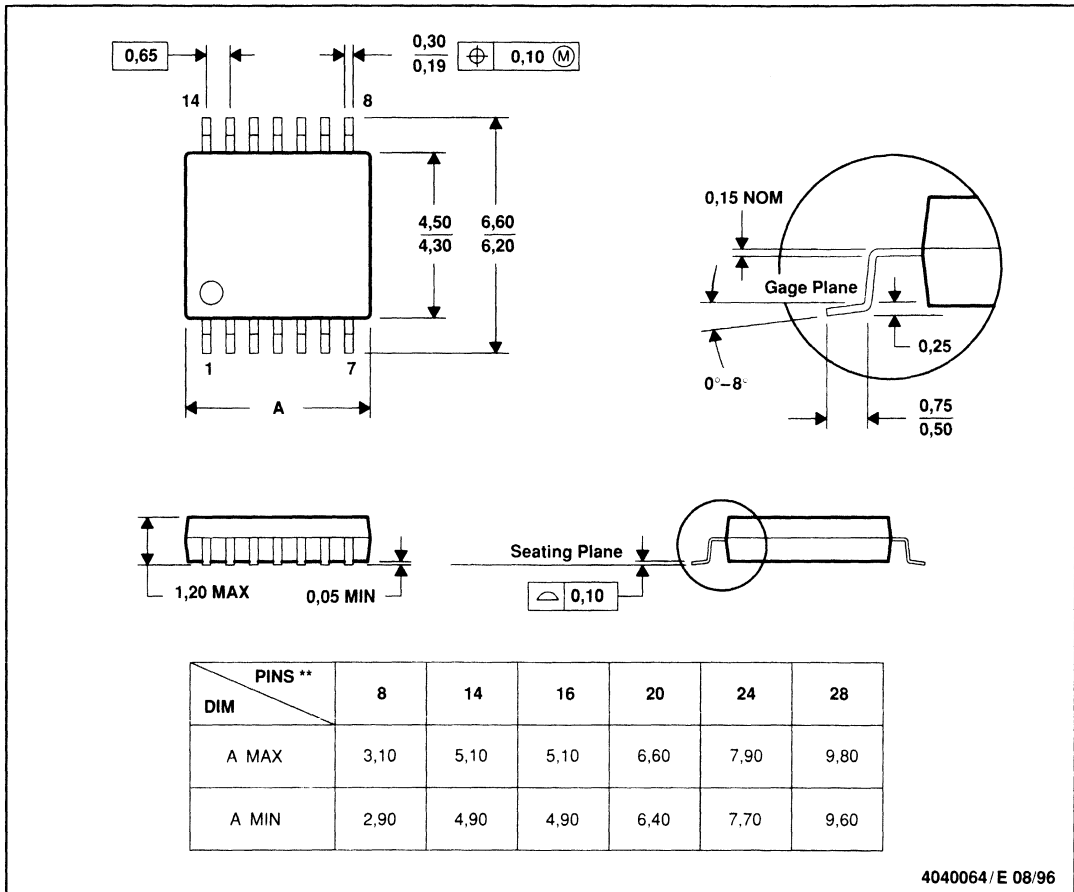
MECHANICAL INFORMATION

MECHANICAL DATA

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

NOTES

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